EVAL6565N, 30W AC-DC ADAPTER WITH THE L6565 QUASI-RESONANT PWM CONTROLLER

by Claudio Adragna

This note describes the evaluation board of the Quasi-resonant (QR) PWM controller L6565 (order code: EVAL6565N) and presents the results of its bench evaluation. The board implements a 30W, single-output (15V/2A), wide-range mains input, QR converter that can be used as a reference design for an AC-DC adapter, where good performance is to be achieved at low cost.
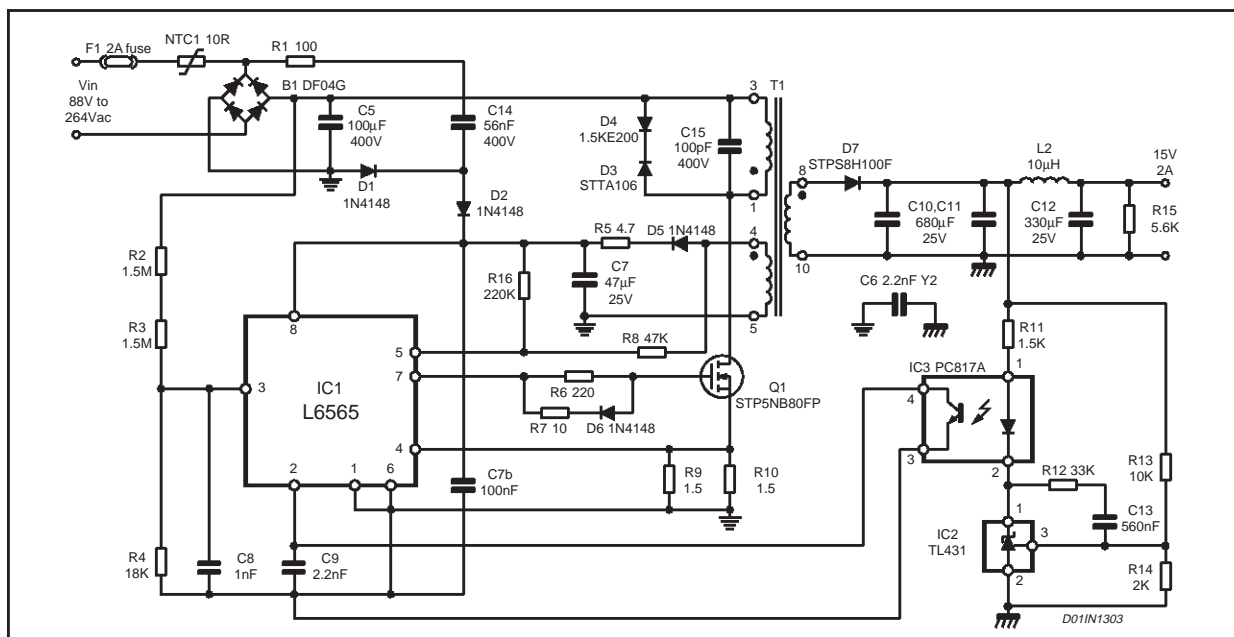
Design Specification

Table 1 summarizes the electrical specification of the application, table 2 provides the BOM and table 3 lists transformer's spec. The electrical schematic is shown in figure 1 and the PCB layout in figure 2.

Table 1. EVAL6565N evaluation board: electrical specification

Input Voltage Range (V_{in})	88 to 264 Vac
Mains Frequency (f_L)	50/60 Hz
Maximum Output Power (P_{out})	30 W
Output	V_{out} = 15 V $\pm$ 3% I_{out} = 0 to 2 A $V_{ripple} \leq$ 1%
Minimum Switching Frequency (@ 100 V_{DC} input voltage)	60 kHz
Target Efficiency (@ P_{out} = 30 W, V_{in} = 88÷264 Vac)	η > 80%
Maximum No-load Input Power	< 0.75 W [*]
Note: (*) compliant with European Code of Conduct on Efficiency of External Power Supplies, phase 2, 01.01.2003	

Figure 1. EVAL6565N evaluation board: electrical schematic

The electrical specification is typical of an AC-DC adapter for consumer equipment, usually realized as an external unit. As such, it falls within the scope of the European "Code of Conduct on Efficiency of External Power Supplies" and is required to be "efficient" under no-load conditions as specified in table 4. The design target is to fulfill the phase 2 requirements, so as to be up-to-date until the year 2005, when phase 3 will set even more stringent limits. Some hints to upgrade the design according to this further step will be given in a following section.

Table 2. EVAL6565N evaluation board: Bill Of Material

Symbol	Value	Note
R1	100 Ω	5%
R2, R3	1.5 MΩ	
R4	18 kΩ	
R5	4.7 Ω	
R6	220 Ω	
R7	10 Ω	
R8	47 kΩ	
R9, R10	1.5 Ω	Metallic film
R11	1.5 kΩ	
R12	33 kΩ	
R13	10 kΩ	
R14	2 kΩ	
R15	5.6 kΩ	
R16	220 kΩ	
C5	100 µF	400V, Rubycon, MXR series or equivalent
C6	2.2 nF	Y1 class
C7	47 µF	25V electrolytic
C7b	100 nF	Plastic film or ceramic
C8, C9	2.2 nF	Plastic film or ceramic
C10, C11	680 µF	25V Rubycon, ZL series or equivalent
C12	330 µF	25V Sanyo, CG series or equivalent
C13	560 nF	Plastic film or ceramic
C14	56 nF	400V, polyester
C15	100 pF	1kV, Y5P, Panasonic or equivalent
L2	10 µH	ELC08D100E, R=44 mΩ, Panasonic or equivalent
T1	558179	See spec on table 3. Supplied by Albe s.r.l. (Tel. +39 363 61493)
B1	DF06G	1A / 600V bridge, DIP4, GI or equivalent
D1, D2, D5, D6	1N4148	0.3A / 75V, glass case, Vishay or equivalent
D3	STTA106	1A / 600V Turboswitch, F126, ST
D4	1.5KE200	200V Transil, CB429, ST
D7	STPS8H100F	8A / 100 V Schottky, ISOWATT220AB, ST
IC1	L6565	QR PWM controller, DIP8, ST [1]
IC2	TL431CZ	Shunt regulator, TO92, ST
IC3	PC817A	Optocoupler, Sharp or equivalent
Q1	STP5NB80FI	1.8 Ω / 800V, TO220FP, ST
NTC1	SSN550	NTC 10 Ω, Vishay or equivalent
F1	T2A250V	2A, 250V ELU
PCB	---	FR-4, Cu single layer 35µm, 95.8 x 64.7 mm
Notes: if not otherwise specified, all resistors are 1%, 1/4 W		
Q1 and D7 are both provided with a 40 °C/W heatsink SK95/25/SA from Fischer Elektronik		

Table 3. EVAL6565N: transformer specification (Part number 558179, supplied by Albe s.r.l.)

Core	E25/13/7, N67 Material or 3C85 or equivalent				
Bobbin	Vertical mounting, 10 pins				
Air gap	≈ 1 mm for an inductance 1-3 of 740 µH				
Leakage inductance	< 20 µH (@ 60 kHz) pins 1-3 with 4,5,7,8,9,10 shorted				
Windings Spec & Build	Pin Start/End	Winding	Wire	Turns	Notes
	1/2	Pri1	AWG26	40	Innermost winding
	7/9	Sec1	2xAWG23	8	Pins 7-8 will be shorted on the PCB
	8/10	Sec2	2xAWG23	8	Pins 9-10 will be shorted on the PCB
	2/3	Pri2	AWG26	40	Pin2 will be cut for safety
	4/5	Aux	AWG32	8	Evenly spaced

Figure 2. EVAL6565N: PCB layout, silk + bottom layer (top view); 1:1 scale
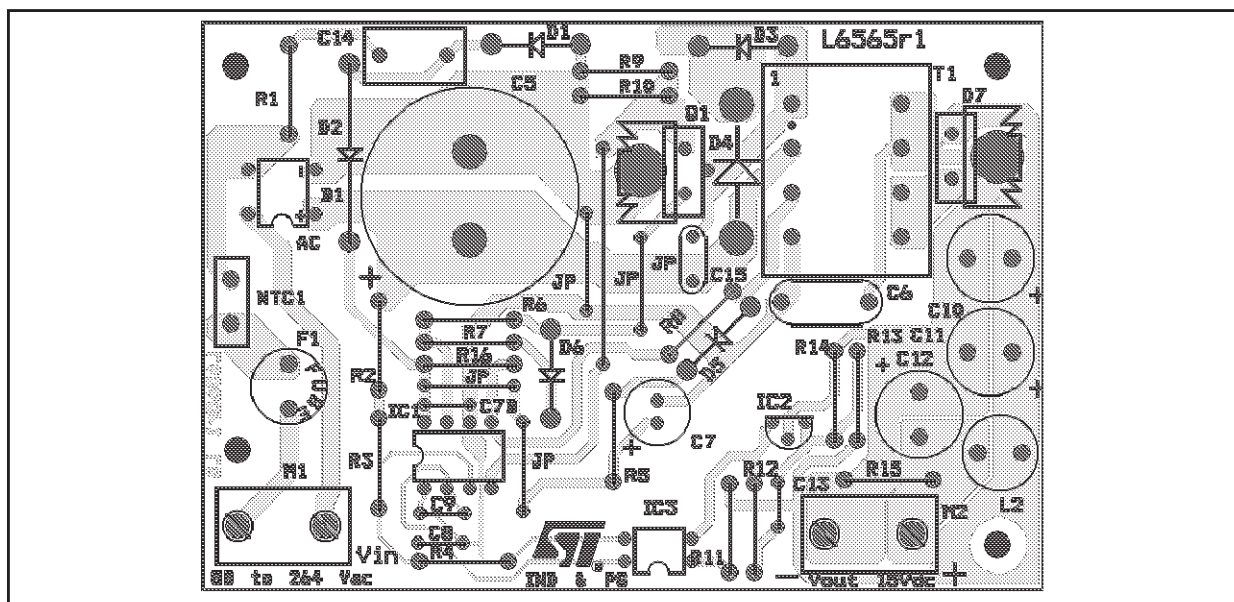

Table 4. Limits envisaged by European Code of Conduct on Efficiency of External Power Supplies

Rated Input Power	No-load Power Consumption		
	Phase 1 01.01.2001	Phase 2 01.01.2003	Phase 3 01.01.2005
≥ 0.3 W and < 15 W	1.0 W	0.75 W	0.30 W
≥ 15 W and < 50 W	1.0 W	0.75 W	0.50 W
≥ 50 W and < 75 W	1.0 W	0.75 W	0.75 W

Evaluation board functionality

The minimum switching frequency (60 kHz @ V_{in} = 100 VDC) has been chosen trading off transformer's size against frequency-related losses. The reflected voltage has been chosen equal to 150V, then ZVS will be achieved only when the converter operates from the 110V mains; however, this value seems to provide a good compromise between capacitive and switching losses at 220V mains. To provide room for the leakage inductance spike an 800V MOSFET (STP5NB80FI) will be used.

To get 150V reflected voltage, the primary-to-secondary turn ratio is made 1:10, which originates relatively low reverse voltages at the secondary side and allows the use of a schottky rectifier as the secondary diode (D7). An STPS8H100F has been selected.

Two design choices have been done to meet the no-load consumption target. First, the converter is started up with a charge pump made up by D1, D2, C14 and R1 instead of the usual dropping resistor. This circuit, usable thanks to the extremely low start-up current of the L6565, provides a typical wake-up time going from 2.2s @ 88 Vac to 0.7s @ 264 Vac, while dissipating less than 50 mW @ 264 Vac, i.e. saving about 200 mW as compared to a start-up circuit made with a dropping resistor that gives the same wake-up time. Second, the leakage inductance spikes are handled by a Transil clamp (D4, with the addition of D3 to prevent direct conduction during MOSFET's ON-time), instead of an RCD clamp, thus saving about 200 mW more.

R2+R3 and R4 compensate for the power capability change vs. the input voltage (Voltage Feedforward). Their ratio has been found simply by fixing the high side one (using a high resistance value to keep the losses low) and varying the low side resistance until the converter loses output voltage regulation with the same load @ 88 and 264 Vac. A 1nF film capacitor bypasses any noise on pin #3 to ground.

To stay within ±3% tolerance, the output voltage regulation is done with secondary feedback, using a typical arrangement TL431+optocoupler. R12, C13 and C9 (on the primary side) compensate the voltage loop for stability. Typically, the crossover frequency is 5 kHz with 70° phase margin.

A 100 pF low-loss capacitor (C15) has been added across the primary winding to optimize MOSFET's losses at maximum load by a small snubbing effect on the drain voltage rate of rise. The delay between transformer' s demagnetization and MOSFET's turn-on is adjusted by means of R8. The final value of 47 kW has been experimentally determined so as to achieve the optimum turn-on point (after the addition of C15).

The converter is fully protected against short circuit: under this conditions it operates at the frequency of the internal starter (2.5 kHz) and the reflected voltage on the auxiliary winding drops, hence the supply voltage of the L6565 cannot be maintained. This results in intermittent operation ("hiccup" mode) with low power throughput (< 1W @ 264 Vac). R10 prevents improper MOSFET's turn-on, due to signal bouncing on the pin, by pulling up the ZCD pin that would be completely floating otherwise. Additionally, thanks to the 2nd overcurrent level on the L6565's current sense pin, also a short circuit directly across the secondary winding - or D7 failing short - will cause an intermittent operation with an even lower level of power throughput.

Board evaluation: getting started

The AC voltage, generated by an AC source ranging from 88 Vac to 264 Vac, will be applied to connector M1 (at the bottom left-hand corner). Should one want to use a high-voltage DC source, remember that the start-up charge pump would not work and a dropping resistor would be needed to let the L6565 start.

The 15 VDC output (connector M2) is located close to the bottom right-hand corner and will be connected to the load. If an electronic load is going to be used in CC mode, make sure that the voltage which the load starts sinking current at is > 1 V or use CR mode if this cannot be set, otherwise the board may not start up at maximum load. This happens because Vout needs to build up a little in order for the ZCD signal to be large enough to trigger QR operation [2]. Before that, the converter runs at the frequency of the internal starter, with a much lower power capability that may be easily exceeded if the load starts sinking the maximum current as Vout is just above zero. In this case V_{out} gets clamped at a low value, the ZCD signal cannot reach the minimum amplitude required, QR operation cannot take place and the system cannot start up.

Like in any offline circuit, extreme caution must be used when working with the application board because it contains dangerous and lethal potentials. The application must be tested with an isolation transformer connected between the AC mains and the input of the board to avoid any risk of electrical shock.

Board evaluation: bench results and significant waveforms

In the following tables the results of some bench evaluations are summarized. A number of waveforms under different load and line conditions are shown for user's reference.

Table 5. EVAL6565N: typical performance

Parameter	Value	Unit
Regulated Output Voltage (@ V_{in} = 220 V_{ac}, I_{out} = 2A)	14.924	V
Minimum Operating Frequency (@ V_{in} = 88 V_{ac}, I_{out} = 2A)	60	kHz
Maximum Operating Frequency (@ V_{in} = 264 V_{ac}, I_{out} = 1.1 A)	214	kHz
Line Regulation (V_{in} = 88 to 264 V_{ac}, I_{out} = 2 A)	1	mV
Load Regulation (V_{in} = 88 V_{ac}, I_{out} = 0 to 2 A)	55	mV
High-frequency Output Voltage Ripple (@ V_{in} = 88 V_{ac}, I_{out} = 2A)	10	mV
Line-frequency Output Voltage Ripple (@ V_{in} = 88 V_{ac}, fL = 60 Hz, I_{out} = 2A)	< 5	mV
Maximum Full-load Efficiency (@ V_{in} = 176 V_{ac}, I_{out} = 2)	85	%
Maximum No-load Input Power (@ V_{in} = 264 V_{ac})	0.6	W

Table 6. EVAL6565N: Line/load regulation and Efficiency

Vac [V]		88	110	132	176	220	264
Iout [A]	2.0	Vout = 14.925V η = 82.6 %	Vout = 14.924V η = 84.0 %	Vout = 14.924V η = 84.5 %	Vout = 14.924V η = 85.0 %	Vout = 14.924V η = 84.5 %	Vout = 14.924V η = 83.1 %
	1.5	Vout = 14.938V η = 83.3 %	Vout = 14.938V η = 84.6 %	Vout = 14.938V η = 84.9 %	Vout = 14.938V η = 84.9 %	Vout = 14.938V η = 83.6 %	Vout = 14.938V η = 81.8 %
	1.0	Vout = 14.952V η = 84.0 %	Vout = 14.952V η = 85.0 %	Vout = 14.952V η = 85.0 %	Vout = 14.952V η = 84.0 %	Vout = 14.952V η = 81.7 %	Vout = 14.952V η = 78.7 %
	0.5	Vout = 14.966V η = 83.1 %	Vout = 14.966V η = 83.1 %	Vout = 14.966V η = 83.1 %	Vout = 14.966V η = 81.3 %	Vout = 14.966V η = 77.1 %	Vout = 14.966V η = 72.6 %
	0.2	Vout = 14.974V η = 78.8 %	Vout = 14.974V η = 78.8 %	Vout = 14.974V η = 76.8 %	Vout = 14.974V η = 73.0 %	Vout = 14.974V η = 66.5 %	Vout = 14.974V η = 58.7 %

Table 7. EVAL6565N: Light-load Input Power (@ Pout = 0.5 W)

VAC [V]	88	110	132	176	220	264
Pin [W]	0.9	1.0	1.1	1.2	1.5	1.6

Table 8. EVAL6565N: No-load Input Power

VAC [V]	88	110	132	176	220	264
Pin [W]	0.4	0.4	0.45	0.5	0.55	0.60

Table 9. EVAL6565N: Maximum Power Capability(measured at 0.95·Vout)

VAC [V]	88	110	132	176	220	264
Pinmax [W]	52.5	57.1	59.5	60.2	57.4	52.3

Table 10. EVAL6565N: Typical Wake-up Time

VAC [V]	88	110	132	176	220	264
TWAKE [s]	2.21	1.65	1.34	1.16	0.91	0.75

Figure 3. Full load, Vin = 100 VDC (left), Vin = 380 VDC (right)

Ch2: Q1 drain voltage
Ch1: current sense pin
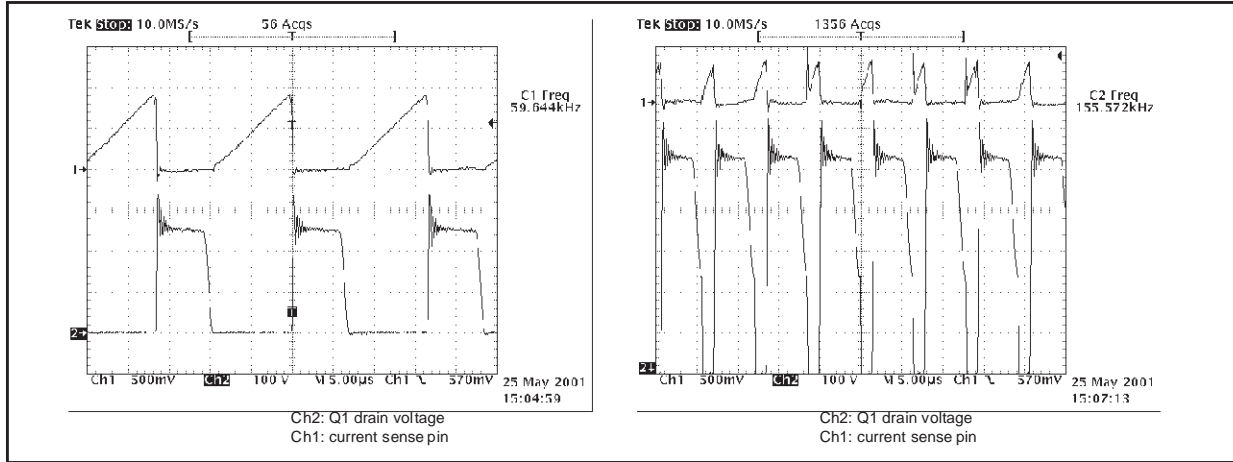
Figure 4. EVAL6565N: Half load, Vin = 100 VDC (left), Vin = 380 VDC (right, note uneven skipping)

Ch2: Q1 drain voltage
Ch1: current sense pin
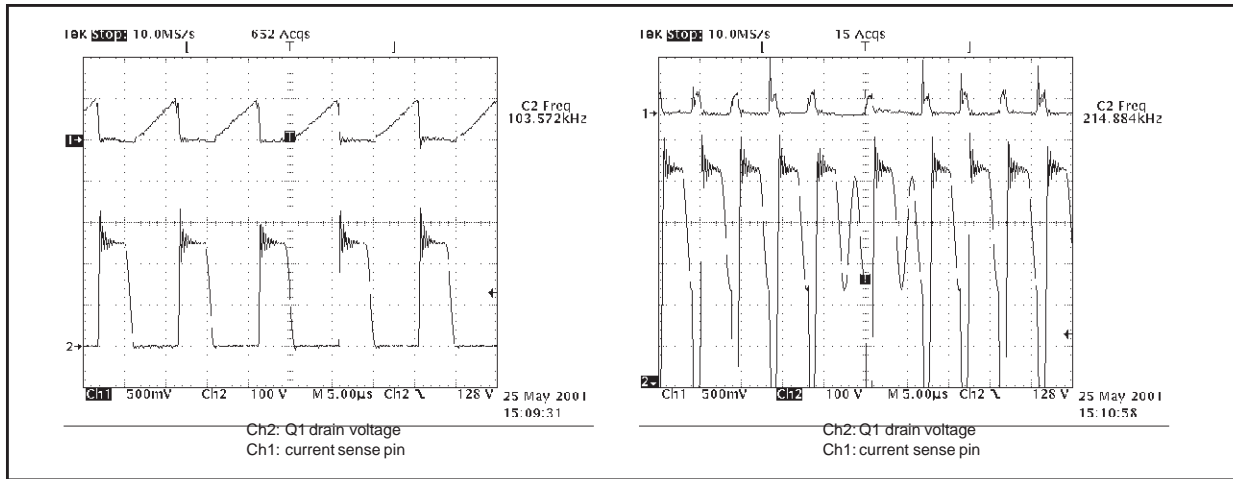
Figure 5. EVAL6565N: No load, Vin = 100 VDC (left), Vin = 380 VDC (right, burst-mode)

Ch2: Q1 drain voltage
Ch1: current sense pin
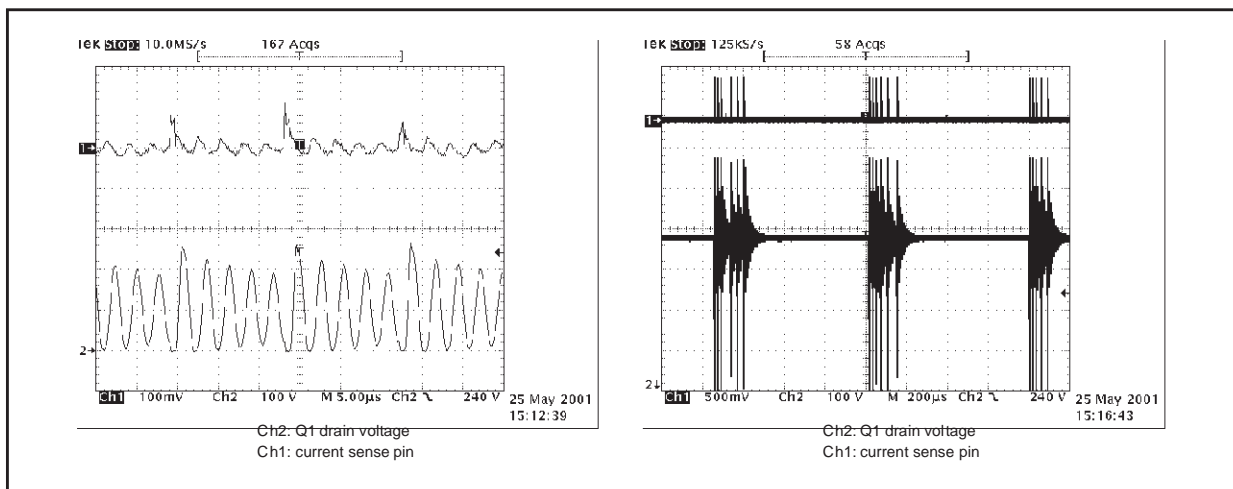
Figure 6. EVAL6565N Full-load Output Ripple @ Vin = 110 Vac: high freq. (left), line freq. (right)
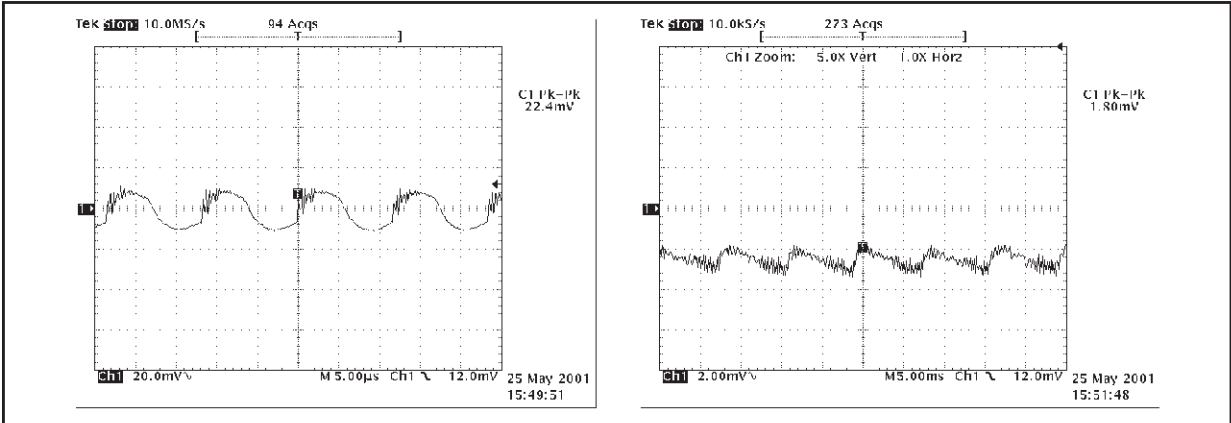
Figure 7. EVAL6565N behavior upon short circuit on: the output (left), D7 (right). Vin = 220 Vac

Ch1: Q1 drain voltage
Ch2: L6565 supply voltage

Ch1: Q1 drain voltage
Ch2: L6565 supply voltage
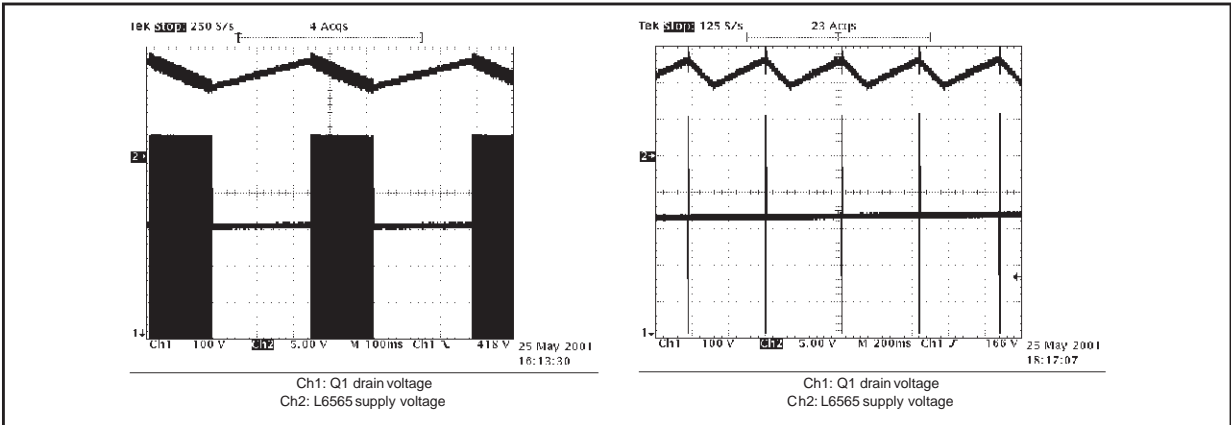
Figure 8. EVAL6565N: Load Transient (@ Vin = 220 Vac: Iout = 0.5 to 2.5 A)

Ch2: Output voltage
Ax1:Load current
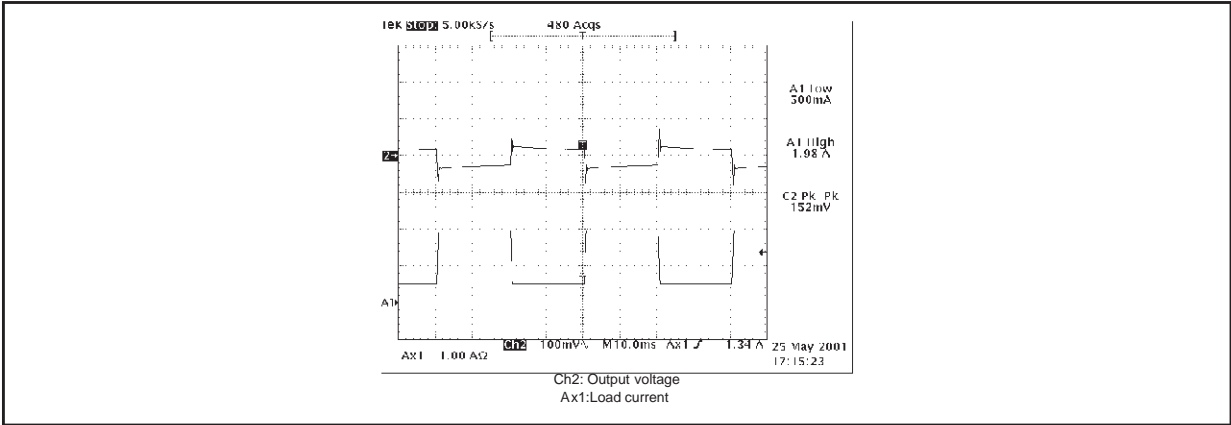
Evaluation board optimization for minimum no-load consumption

Some more optimization steps need to be taken in order for the EVAL6565N to fulfill the limits envisaged by the 3rd phase of the European Code of Conduct on Efficiency of External Power Supplies, which will be active starting from 01.01.2005. According to this, the no-load consumption must be less than 0.5 W at rated input voltage (220 Vac for European mains, the 110 Vac of the US mains is not a concern). To have some margin, it is a

common design target to fulfill the spec even at maximum input voltage (264 Vac).

The optimization steps are basically three:

1) Eliminate C15. This will slightly hurt efficiency at heavy and moderate load but save about 100 mW of no-load input consumption at maximum mains.

2) Replace the start-up charge pump with a more efficient high-voltage active start-up circuit, like the one shown in figure 9. This will save about 40 mW input consumption.

3) The feedback network topology at the primary side should be changed as shown in figure 10. The feedback topology used in the EVAL6565N is such that under no-load conditions the optocoupler draws about 3mA out of pin COMP, which adds up to the quiescent current of the IC. This additional load causes the Vcc voltage to drop so that a small dummy load (R15) is required at the secondary side. With the circuit in figure 10, the operating current of optocoupler is reduced at 1 mA and also the dummy load can be reduced, just the 10 kΩ resistor used to provide adequate bias current to the TL431. The input consumption will be reduced by about 100 mW.
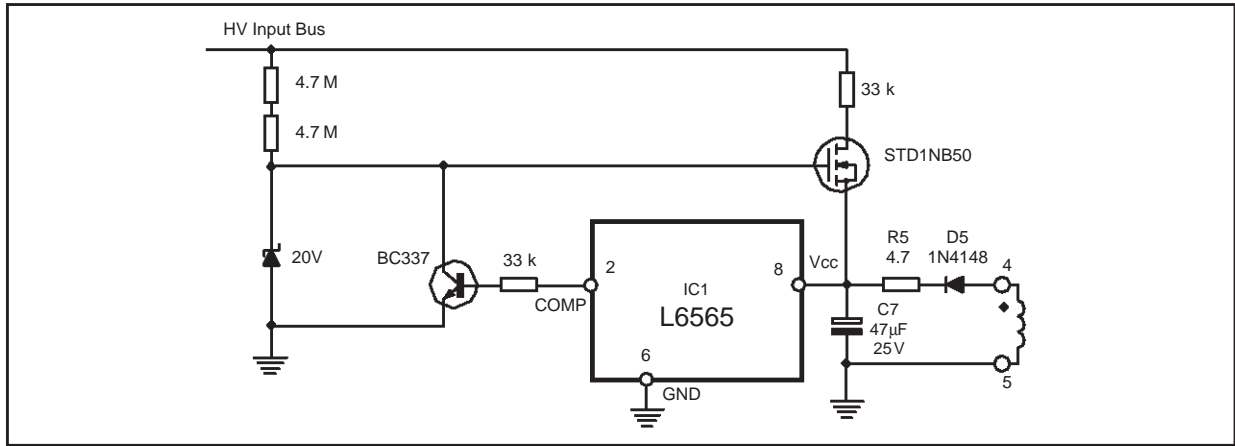
Figure 9. High-voltage active start-up circuit

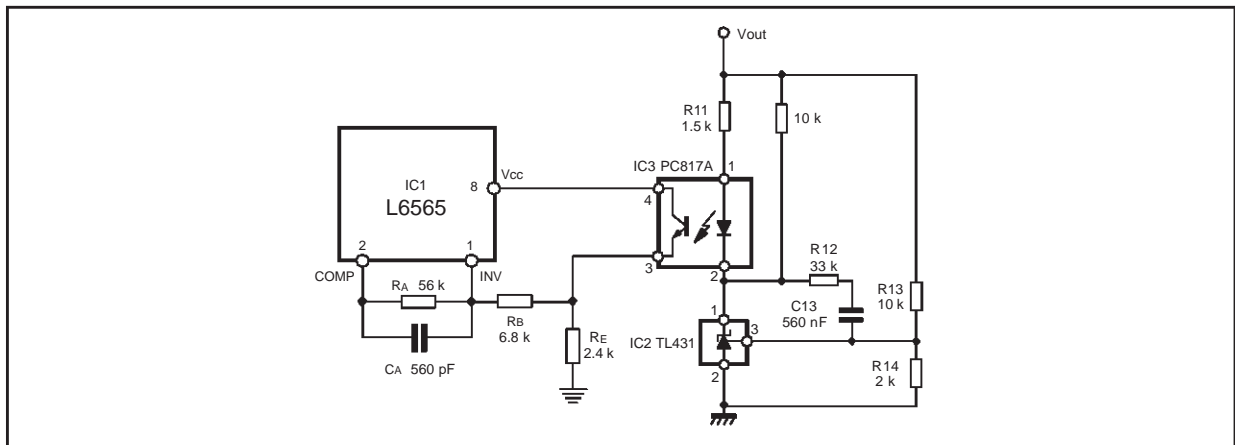**Figure 10. Low-consumption feedback network**

Table 11. EVAL6565N modified as per optimization steps 1 to 3: no-load input power measurements

VAC [V]	88	110	132	176	220	264
Pin [W]	0.3	0.3	0.3	0.35	0.4	0.4

To gain more design margin the following tips could be considered:

a) Increase R2, R3 and R4: by using 4.7MΩ for R2 and R3 and 56 kΩ for R4, the input consumption will be reduced by 30 mW.

b) Reduce the parasitic capacitance of the drain node by using a smaller or lower voltage rating MOS-FET. The price to pay is more dissipation at full load and a larger heatsink. For example, with the next smaller size (STP4NB80), the C_{oss} is reduced by 30%, with an estimated power saving of about 15 mW under no-load conditions. The full load losses, however, will be increased by 2/3 and a 24 $°$C/W heatsink (instead of 40 $°$C/W) will be needed. It might be worth designing with a lower reflected voltage, so that a lower voltage MOSFET can be used. For example the 600V-rated MOSFET with the same $R_{ds(on)}$ as the STP5NB80, the STP4NC60, has a C_{oss} which is only 53%, which allows saving about 20 mW. The full-load losses will be slightly increased but not so much.

c) Another way to reduce the drain parasitic capacitance is to minimize the parasitic capacitance of the primary winding. To achieve a low capacitance, split the primary winding (this goes in favor of a low leakage inductance too) and wind first the half whose end is to be connected to the drain of the MOS-FET. In case of multiple layer winding, which exhibits higher capacitance, it is useful to embed one layer of isolation in between. This, however, tends to increase leakage inductance and therefore should be done with care. Slotted bobbins are also very effective to this end but they tend to increase leakage inductance too.

REFERENCES

[1] "L6565 Quasi-Resonant SMPS Controller" Datasheet

[2] "L6565 Quasi-Resonant Controller" (AN1326)