FAIRCHILD SEMICONDUCTOR®

October 2008

# SG6741
# Highly Integrated Green-Mode PWM Controller

## Features

- High-Voltage Startup
- Low Operating Current: 4mA
- Linearly Decreasing PWM Frequency to 22kHz
- Frequency Hopping to Reduce EMI Emission
- Peak-Current-Mode Control
- Cycle-by-Cycle Current Limiting
- Leading-Edge Blanking
- Synchronized Slope Compensation
- Gate Output Maximum Voltage Clamp: 18V
- $V_{DD}$ Over-Voltage Protection (Auto Restart)
- $V_{DD}$ Under-Voltage Lockout (UVLO)
- Internal Open-Loop Protection
- Constant Power Limit (Full AC Input Range)

## Applications

General-purpose switch-mode power supplies and flyback power converters, including:

- Power Adapters
- Open-Frame SMPS

## Description

The highly integrated SG6741 PWM controller provides several features to enhance the performance of flyback converters.

The highly integrated SG6741 series of PWM controllers provides several features to enhance the performance of flyback converters.

To minimize standby power consumption, a proprietary green-mode function provides off-time modulation to linearly decrease the switching frequency at light-load conditions. To avoid acoustic-noise problems, the minimum PWM frequency is set above 22KHz. This green-mode function enables the power supply to meet international power conservation requirements. With the internal high-voltage startup circuitry, the power loss due to bleeding resistors is also eliminated. To further reduce power consumption, SG6741 is manufactured using the BiCMOS process, which allows an operating current of only 4mA.

SG6741 integrates a frequency-hopping function that helps reduce EMI emission of a power supply with minimum line filters. Its built-in synchronized slope compensation achieves stable peak-current-mode control. The proprietary internal line compensation ensures constant output power limit over a wide range of AC input voltages, from $90V_{AC}$ to $264V_{AC}$.

SG6741 provides many protection functions. In addition to cycle-by-cycle current limiting, the internal open-loop protection circuit ensures safety when an open-loop or output short-circuit failure occurs. PWM output is disabled until $V_{DD}$ drops below the UVLO lower limit; then the controller starts again. As long as $V_{DD}$ exceeds about 26V, the internal OVP circuit is triggered.

SG6741 is available in an 8-pin SOP package.

## Ordering Information

| Part Number | Operating Temperature Range | Package | Eco Status | Packing Method |
|---|---|---|---|---|
| SG6741SZ | -40 to +105°C | 8-Lead Small Outline Package (SOP) | Green | Tape & Reel |
| SG6741SY | -40 to +105°C | 8-Lead Small Outline Package (SOP) | Green | Tape & Reel |

*For Fairchild's definition of "green" Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.*

## Application Diagram

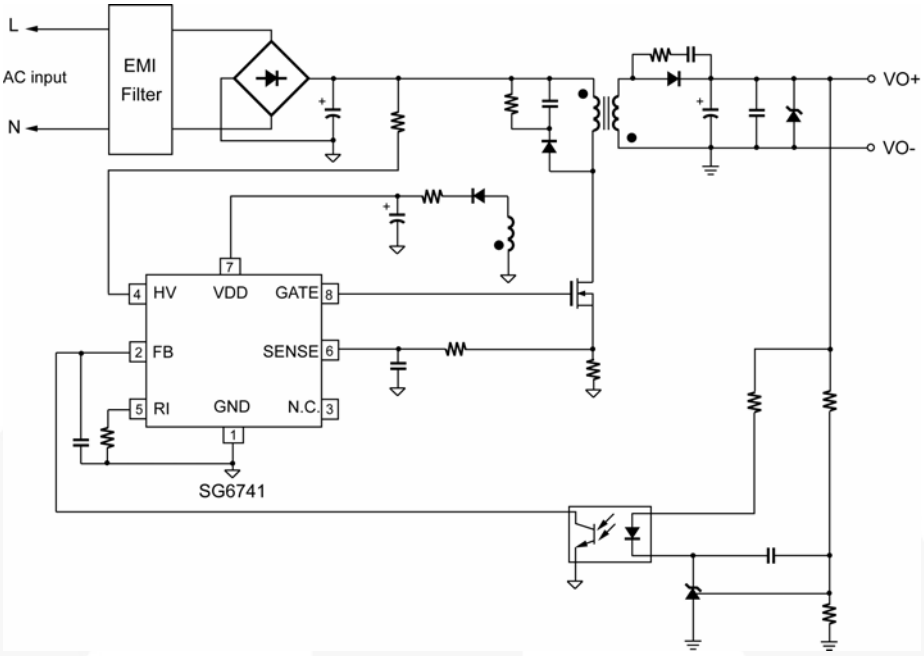



**Figure 1. Typical Application**

## Internal Block Diagram

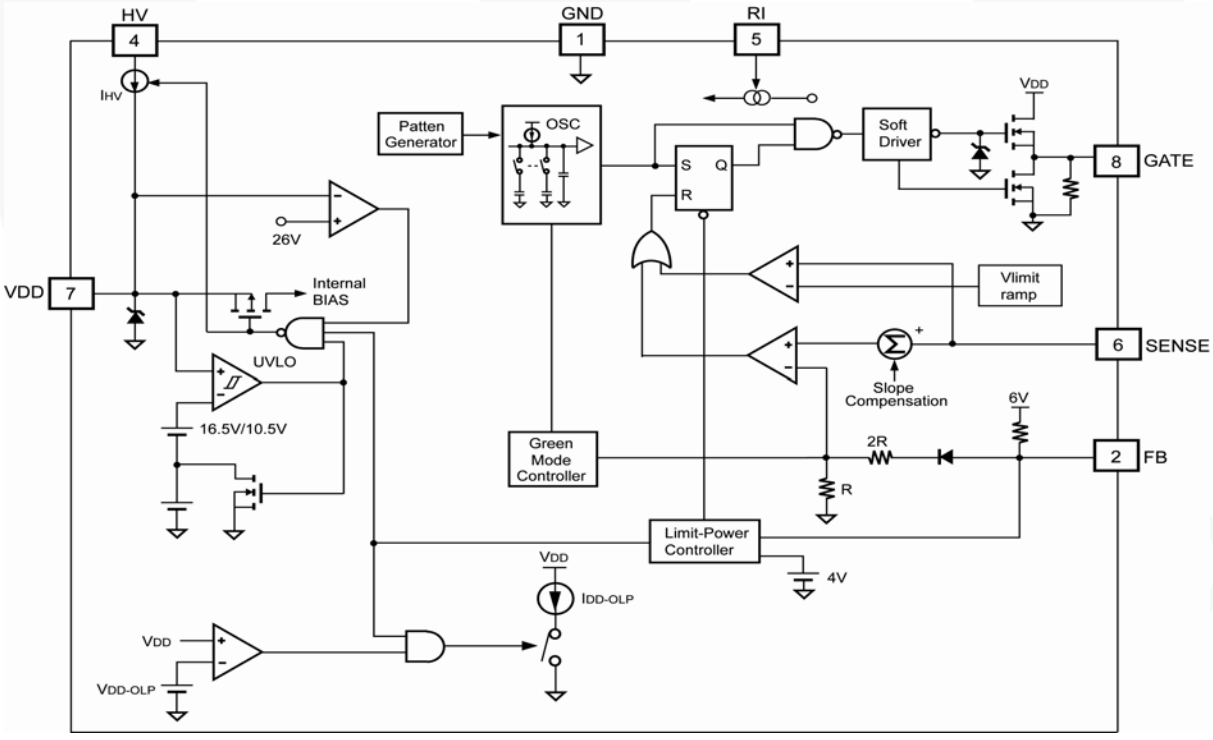
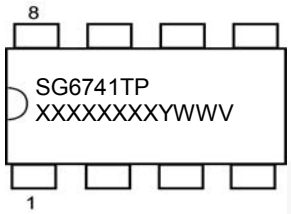


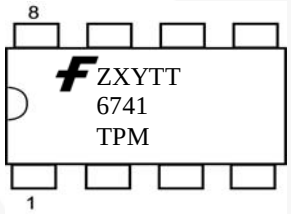

**Figure 2. Functional Block Diagram**

## Marking Information




T: S = SOP
P: Z =Lead Free
Null=regular package
XXXXXXXX: Wafer Lot
Y: Year; WW: Week
V: Assembly Location

Marking for SG6741SZ




F: Fairchild logo
Z: Plant code
X: 1 digit year code
Y: 1 digit week code
TT: 2 digits die run code
T: Package type (S = SOP)
P: Y=Green package
M: Manufacture flow code

Marking for SG6741SY

**Figure 3. Top Mark**

## Pin Configuration

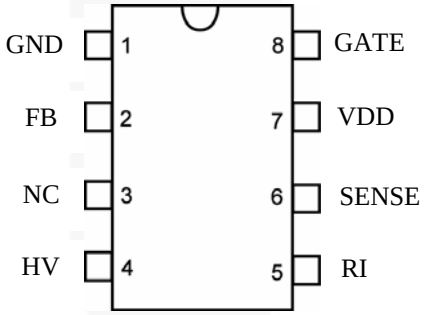



**Figure 4. Pin Configuration (Top View)**

## Pin Definitions

| Pin # | Name | Description |
|---|---|---|
| 1 | GND | Ground. |
| 2 | FB | The signal from the external compensation circuit is fed into this pin. The PWM duty cycle is determined in response to the signal on this pin and the current-sense signal on the SENSE pin. |
| 3 | NC | No connection. |
| 4 | HV | For startup, this pin is pulled high to the line input or bulk capacitor via resistors. |
| 5 | RI | A resistor connected from the RI pin to GND pin provides the SG6741 with a constant current source. This determines the center PWM frequency. Increasing the resistance reduces PWM frequency. Using a 26KΩ resistor ($R_I$) results in a 65kHz center PWM frequency. |
| 6 | SENSE | Current sense. The sensed voltage is used for peak-current-mode control and cycle-by-cycle current limiting. |
| 7 | VDD | Power supply. The internal protection circuit disables PWM output as long as $V_{DD}$ exceeds the OVP trigger point. |
| 8 | GATE | The totem-pole output driver. Soft driving waveform is implemented for improved EMI. |

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. All voltage values, except differential voltages, are given with respect to the ground pin.

| Symbol | Parameter | | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{VDD}$ | DC Supply Voltage[1, 2] | | | 30 | V |
| $V_{FB}$ | FB Pin Input Voltage | | -0.3 | 7.0 | V |
| $V_{SENSE}$ | SENSE Pin Input Voltage | | -0.3 | 7.0 | V |
| $V_{RI}$ | RI Pin Input Voltage | | -0.3 | 7.0 | V |
| $V_{HV}$ | HV Pin Input Voltage | | | 500 | V |
| $P_D$ | Power Dissipation ($T_A < 50°C$) | | | 400 | mW |
| $\Theta_{JA}$ | Thermal Resistance (Junction-to-Air) | | | 141 | °C/W |
| $T_J$ | Operating Junction Temperature | | -40 | +125 | °C |
| $T_{STG}$ | Storage Temperature Range | | -55 | +150 | °C |
| $T_L$ | Lead Temperature (Wave Soldering or IR, 10 Seconds) | | | +260 | °C |
| ESD | Electrostatic Discharge Capability, Human Body Model, JESD22-A114 | All Pins Except HV Pin | | 4 | kV |
| | Electrostatic Discharge Capability, Machine Model, JESD22-A115 | All Pins Except HV Pin | | 200 | V |

**Notes**:
1. All voltage values, except differential voltages, are given with respect to the network ground terminal.
2. Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device.

## Electrical Characteristics

$V_{DD}$=15V, $T_A$=25°C, unless otherwise noted.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| **$V_{DD}$ Section** | | | | | | |
| $V_{OP}$ | Continuously Operating Voltage | | | | 22 | V |
| $V_{DD-ON}$ | Start Threshold Voltage | | 15.5 | 16.5 | 17.5 | V |
| $V_{DD-OFF}$ | Minimum Operating Voltage | | 9.5 | 10.5 | 11.5 | V |
| $I_{DD-ST}$ | Startup Current | $V_{DD-ON}$ – 0.16V | | | 30 | µA |
| $I_{DD-OP}$ | Operating Supply Current | $V_{DD}$=15V, GATE Open | | 4 | 5 | mA |
| $I_{DD-OLP}$ | Internal Sink Current | $V_{DD-OLP}$ +0.1V | 50 | 70 | 90 | µA |
| $V_{TH-OLP}$ | $I_{DD-OLP}$ off Voltage | | 6.5 | 7.5 | 8.0 | V |
| $V_{DD-OVP}$ | $V_{DD}$ Over-Voltage Protection | | 25 | 26 | 27 | V |
| $t_{D-VDDOVP}$ | $V_{DD}$ Over-Voltage Protection Debounce Time | | 100 | 180 | 260 | µs |
| **HV Section** | | | | | | |
| $I_{HV}$ | Supply Current from HV Pin | $V_{AC}$=90V ($V_{DC}$=120V), $V_{DD}$=10µF | | 2.0 | | mA |
| $I_{HV-LC}$ | Leakage Current After Startup | HV=500V, $V_{DD}$=$V_{DD-OFF}$+1V | | 1 | 20 | µA |
| **Oscillator Section** | | | | | | |
| $f_{OSC}$ | Frequency in Nominal Mode | Center Frequency | 62 | 65 | 68 | KHz |
| | | Hopping Range | ±3.7 | ±4.2 | ±4.7 | |
| $t_{HOP}$ | Hopping Period | | | 4.4 | | ms |
| $f_{OSC-G}$ | Green-Mode Frequency | | 16 | 18 | 21 | KHz |
| $f_{DV}$ | Frequency Variation vs. $V_{DD}$ Deviation | $V_{DD}$=11V to 22V | | | 5 | % |
| $f_{DT}$ | Frequency Variation vs. Temperature Deviation | $T_A$=-40 to 105°C | | | 5 | % |

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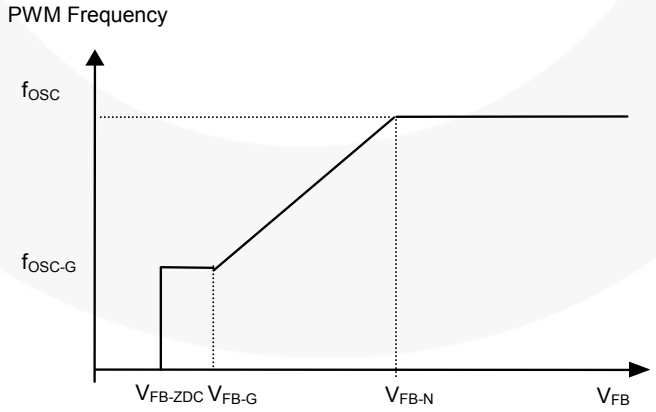


**Figure 5. $V_{FB}$ vs. PWM Frequency**

## Electrical Characteristics (Continued)

$V_{DD}$=15V, $T_A$=25°C, unless otherwise noted.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| **Feedback Input Section** | | | | | | |
| $A_V$ | Input Voltage to Current-Sense Attenuation | | 1/3.75 | 1/3.20 | 1/2.75 | V/V |
| $Z_{FB}$ | Input Impedance | | 4 | | 7 | kΩ |
| $V_{FB-OPEN}$ | Output High Voltage | FB Pin Open | 5.5 | | | V |
| $V_{FB-OLP}$ | FB Open-Loop Trigger Level | | 3.7 | 4.0 | 4.3 | V |
| $t_{D-OLP}$ | Delay Time of FB Pin Open-Loop Protection | $R_I$=26kΩ | 50 | 56 | 62 | ms |
| $V_{FB-N}$ | Green-Mode Entry FB Voltage | | 1.9 | 2.1 | 2.3 | V |
| $V_{FB-G}$ | Green-Mode Ending FB Voltage | | | $V_{FB-N}$-0.5 | | V |
| $V_{FB-ZDC}$ | Zero Duty-Cycle Input Voltage | | $V_{FB-G}$ - 0.25 | $V_{FB-G}$ - 0.20 | $V_{FB-G}$ - 0.10 | V |
| **Current-Sense Section** | | | | | | |
| $Z_{SENSE}$ | Input Impedance | | | 12 | | KΩ |
| $V_{STHFL}$ | Current Limit Flatten Threshold Voltage | | 0.87 | 0.90 | 0.93 | V |
| $V_{STHVA}$ | Current Limit Valley Threshold Voltage | $V_{STHFL}$–$V_{STHVA}$ | 0.30 | 0.34 | 0.38 | V |
| $t_{PD}$ | Delay to Output | | | 100 | 200 | ns |
| $t_{LEB}$ | Leading-Edge Blanking Time | | 275 | 350 | 425 | ns |
| $V_{S-SCP}$ | Threshold Voltage for SENSE Short-Circuit Protection | | | 0.15 | | V |
| $t_{D-SSCP}$ | Delay Time for SENSE Short-Circuit Protection | $V_{SENSE}$<0.15V, $R_I$=26kΩ | | 180 | | µs |
| **GATE Section** | | | | | | |
| $DCY_{MAX}$ | Maximum Duty Cycle | | 70 | 75 | 80 | % |
| $V_{GATE-L}$ | Gate Low Voltage | $V_{DD}$=15V, $I_O$=50mA | | | 1.5 | V |
| $V_{GATE-H}$ | Gate High Voltage | $V_{DD}$=12.5V, $I_O$=50mA | 8 | | | V |
| $t_r$ | Gate Rising Time | $V_{DD}$=15V, $C_L$=1nF | 150 | 250 | 350 | ns |
| $t_f$ | Gate Falling Time | $V_{DD}$=15V, $C_L$=1nF | 30 | 50 | 90 | ns |
| $I_{GATE-SOURCE}$ | Gate Source Current | $V_{DD}$=15V, GATE=6V | 250 | | | mA |
| $V_{GATE-CLAMP}$ | Gate Output Clamping Voltage | $V_{DD}$=22V | | | 18 | V |

**Notes**:

3. When activated, the output is disabled and the latch is turned off.
4. The threshold temperature for enabling the output again and resetting the latch after OTP has been activated.

## Typical Performance Characteristics

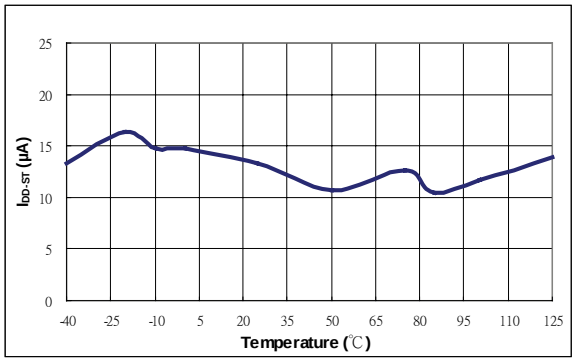


**Figure 6. Startup Current ($I_{DD-ST}$) vs. Temperature**

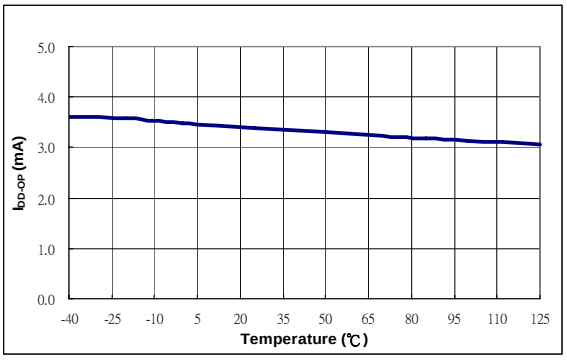


**Figure 7. Operation Supply Current ($I_{DD-OP}$) vs. Temperature**

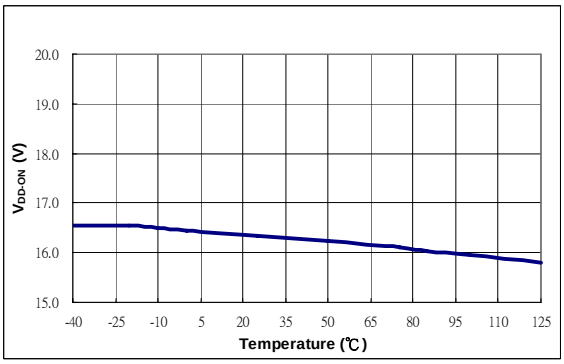


**Figure 8. Start Threshold Voltage ($V_{DD-ON}$) vs. Temperature**

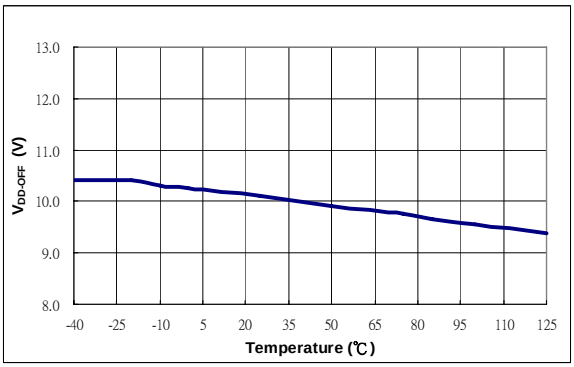


**Figure 9. Minimum Operating Voltage ($V_{DD-OFF}$) vs. Temperature**

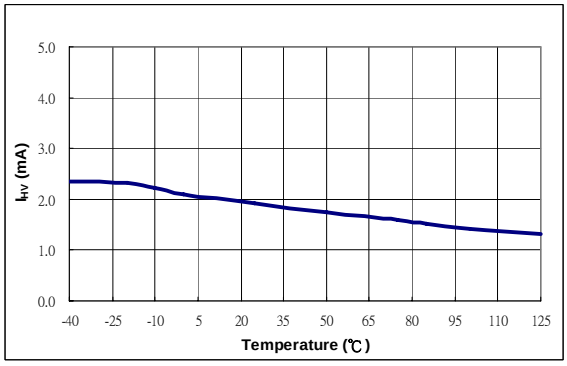


**Figure 10. Supply Current Drawn from HV Pin ($I_{HV}$) vs. Temperature**

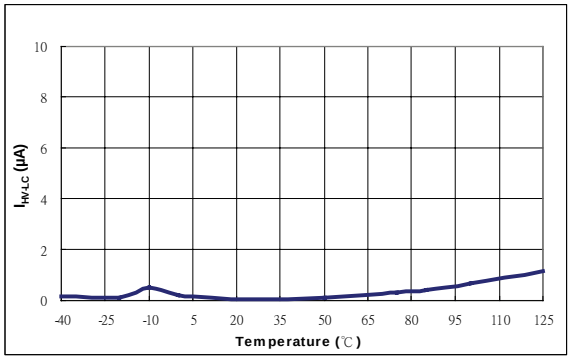


**Figure 11. HV Pin Leakage Current After Startup ($I_{HV-LC}$) vs. Temperature**

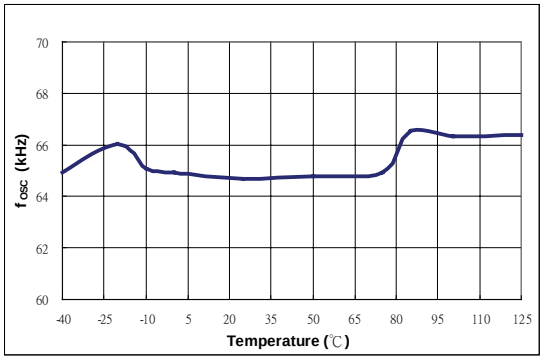


**Figure 12. Frequency in Nominal Mode ($f_{OSC}$) vs. Temperature**

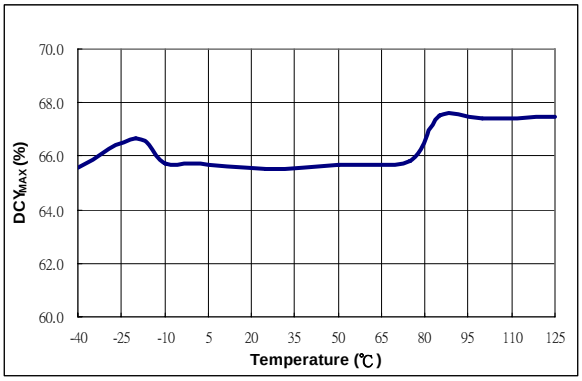


**Figure 13. Maximum Duty Cycle ($DCY_{MAX}$) vs. Temperature**

## Functional Description

### Startup Current

For startup, the HV pin is connected to the line input or bulk capacitor through an external resistor, $R_{HV}$, which is recommended as 100KΩ. Typical startup current drawn from pin HV is 2mA and it charges the hold-up capacitor through the resistor $R_{HV}$. When the $V_{DD}$ capacitor level reaches $V_{DD-ON}$, the startup current switches off. At that moment, the $V_{DD}$ capacitor only supplies the SG6741 to maintain the $V_{DD}$ before the auxiliary winding of the main transformer to carry on provide the operating current.

### Operating Current

Operating current is around 4mA. The low operating current enables better efficiency and reduces the requirement of $V_{DD}$ hold-up capacitance.

### Green-Mode Operation

The patented green-mode function provides an off-time modulation to reduce switching frequency in light-load and no-load conditions. The on time is limited for better abnormal or brownout protection. $V_{FB}$, which is derived from the voltage feedback loop, is used as the reference. Once $V_{FB}$ is lower than the threshold voltage, switching frequency is continuously decreased to the minimum green-mode frequency, around 22KHz ($R_I$=26KΩ).

### Oscillator Operation

A resistor connected from the RI pin to the GND pin generates a constant current source for the controller. This current is used to determine the center PWM frequency. Increasing the resistance reduces PWM frequency. Using a 26KΩ resistor $R_I$ results in a corresponding 65KHz PWM frequency. The relationship between $R_I$ and the switching frequency is:

$$f_{PWM} = \frac{1690}{R_I\ (K\Omega)} (KHz) \quad (1)$$

The range of the PWM oscillation frequency is designed as 47kHz ~ 109kHz.

### Current Sensing / PWM Current Limiting

Peak-current-mode control is utilized in SG6741 to regulate output voltage and provide pulse-by-pulse current limiting. The switch current is detected by a sense resistor into the SENSE pin. The PWM duty cycle is determined by this current-sense signal and $V_{FB}$, the feedback voltage. When the voltage on the SENSE pin reaches around $V_{COMP}$ = ($V_{FB}$–1.2)/3.2, the switch cycle is terminated immediately. $V_{COMP}$ is internally clamped to a variable voltage around 0.85V for output power limit.

### Leading-Edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike occurs on the sense-resistor. To avoid premature termination of the switching pulse, a leading-edge blanking time is built in. During this blanking period, the current-limit comparator is disabled and cannot switch off the gate driver.

### Under-Voltage Lockout (UVLO)

The turn-on and turn-off thresholds are fixed internally at 16.5V/10.5V. During startup, the hold-up capacitor must be charged to 16.5V through the startup resistor so that IC is enabled. The hold-up capacitor continues to supply $V_{DD}$ before the energy can be delivered from auxiliary winding of the main transformer. $V_{DD}$ must not drop below 10.5V during this startup process. This UVLO hysteresis window ensures that hold-up capacitor is adequate to supply $V_{DD}$ during startup.

### Gate Output / Soft Driving

The SG6741 BiCMOS output stage is a fast totem pole gate driver. Cross conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability. The output driver is clamped by an internal 18V Zener diode to protect power MOSFET transistors against undesirable gate over-voltage. A soft driving waveform is implemented to minimize EMI.

### Built-in Slope Compensation

The sensed voltage across the current-sense resistor is used for peak-current-mode control and pulse-by-pulse current limiting. Built-in slope compensation improves stability and prevents sub-harmonic oscillation. SG6741 inserts a synchronized positive-going ramp at every switching cycle.

### Constant Output Power Limit

When the SENSE voltage, across the sense resistor $R_S$, reaches the threshold voltage around 0.9V, the output GATE drive is turned off after a small delay, $t_{PD}$. This delay introduces an additional current, proportional to $t_{PD} \cdot V_{IN} / L_P$. The delay is nearly constant, regardless of the input voltage $V_{IN}$. Higher input voltage results in a larger additional current and the output power limit is also higher than that under low input line voltage. To compensate this variation for wide AC input range, a sawtooth power-limiter is designed to solve the unequal power-limit problem. The power limiter is designed as a positive ramp signal and is fed to the inverting input of the OCP comparator. This results in a lower current limit at high-line inputs than at low-line inputs.

## Functional Description (Continued)

### $V_{DD}$ Over-Voltage Protection (OVP)

$V_{DD}$ over-voltage protection has been built in to prevent damage due to abnormal conditions. Once the $V_{DD}$ voltage is over the $V_{DD}$ over-voltage protection voltage ($V_{DD-OVP}$), and lasts for $t_{D-VDDOVP}$, the PWM pulses is disabled until the $V_{DD}$ voltage drops below the UVLO, then starts up again. Over-voltage conditions are usually caused by open feedback loops.

### Limited Power Control

The FB voltage increases every time the output of the power supply is shorted or overloaded. If the FB voltage remains higher than a built-in threshold for longer than $t_{D-OLP}$, PWM output is turned off. As PWM output is turned off, the supply voltage $V_{DD}$ begins decreasing.

When $V_{DD}$ goes below the turn-off threshold (eg, 10.5V) the controller totally shuts down. $V_{DD}$ is charged up to the turn-on threshold voltage of 16V through the startup resistor until PWM output is restarted. This protection is activated as long as the overloading condition persists. This prevents the power supply from overheating.

### Noise Immunity

Noise on the current sense or control signal may cause significant pulse width jitter, particularly in the continuous-conduction mode. Slope compensation helps alleviate this problem. Good placement and layout practices should be followed. Avoiding long PCB traces and component leads, locating compensation and filter components near to the SG6741, and increasing the power MO gate resistance improves performance.

## Applications Information

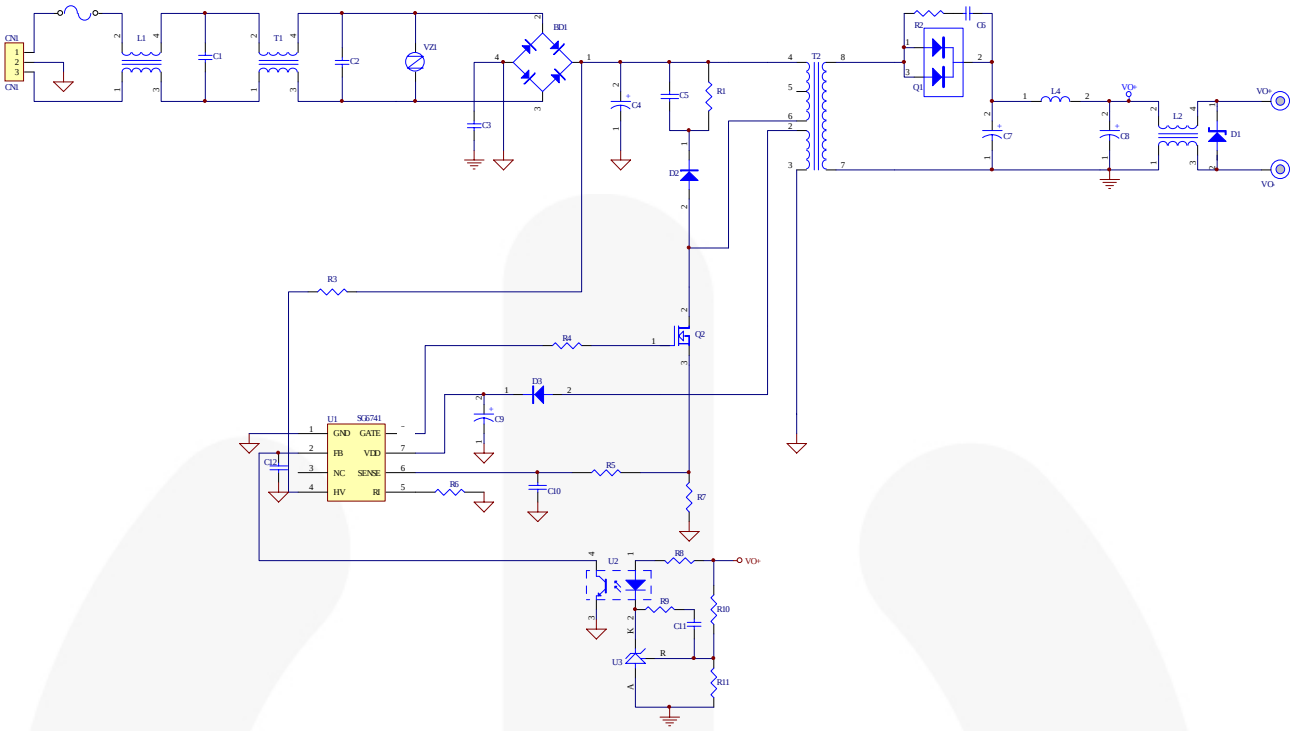


**Figure 14. 60W Flyback 12V/5A Application Circuit**

## BOM

| Designator | Part Type | Designator | Part Type |
|---|---|---|---|
| BD1 | BD 4A/600V | Q2 | MOS 7A/600V |
| C1 | XC 0.68μF/300V | R1 | R 100KΩ 1/2W |
| C2 | XC 0.1μF/300V | R2 | R 47Ω 1/4W |
| C3 | YC 2200pF/Y1 | R3 | R 100KΩ 1/2W |
| C4 | EC 120μF/400V | R4 | R 20Ω 1/8W |
| C5 | CC 0.01μF/500V | R5 | R 100Ω 1/8W |
| C6 | CC 1000pF/100V | R6 | R 33KΩ 1/8W |
| C7 | EC 1000μF/25V | R7 | R 0.3Ω 2W |
| C8 | EC 470μF/25V | R8 | R 680Ω 1/8W |
| C9 | EC 22μF/50V | R9 | R 4.7KΩ 1/8W |
| C10 | CC 470pF/50V | R10 | R 150KΩ 1/8W |
| C11 | CC 2200pF/50V | R11 | R 39KΩ 1/8W |
| C12 | CC 0.01μF/50V | THER1 | Thermistor TTC104 |
| D1 | Zener Diode 15V 1/2W (option) | T1 | 10mH |
| D2 | BYV95C | T2 | 600μH(PQ2620) |
| D3 | FR103 | U1 | IC SG6741 |
| F1 | FUSE 4A/250V | U2 | IC PC817 |
| L1 | Inductor (900μH) | U3 | IC TL431 |
| Q1 | STP20-100CT | VZ1 | VZ 9G |

## Physical Dimensions

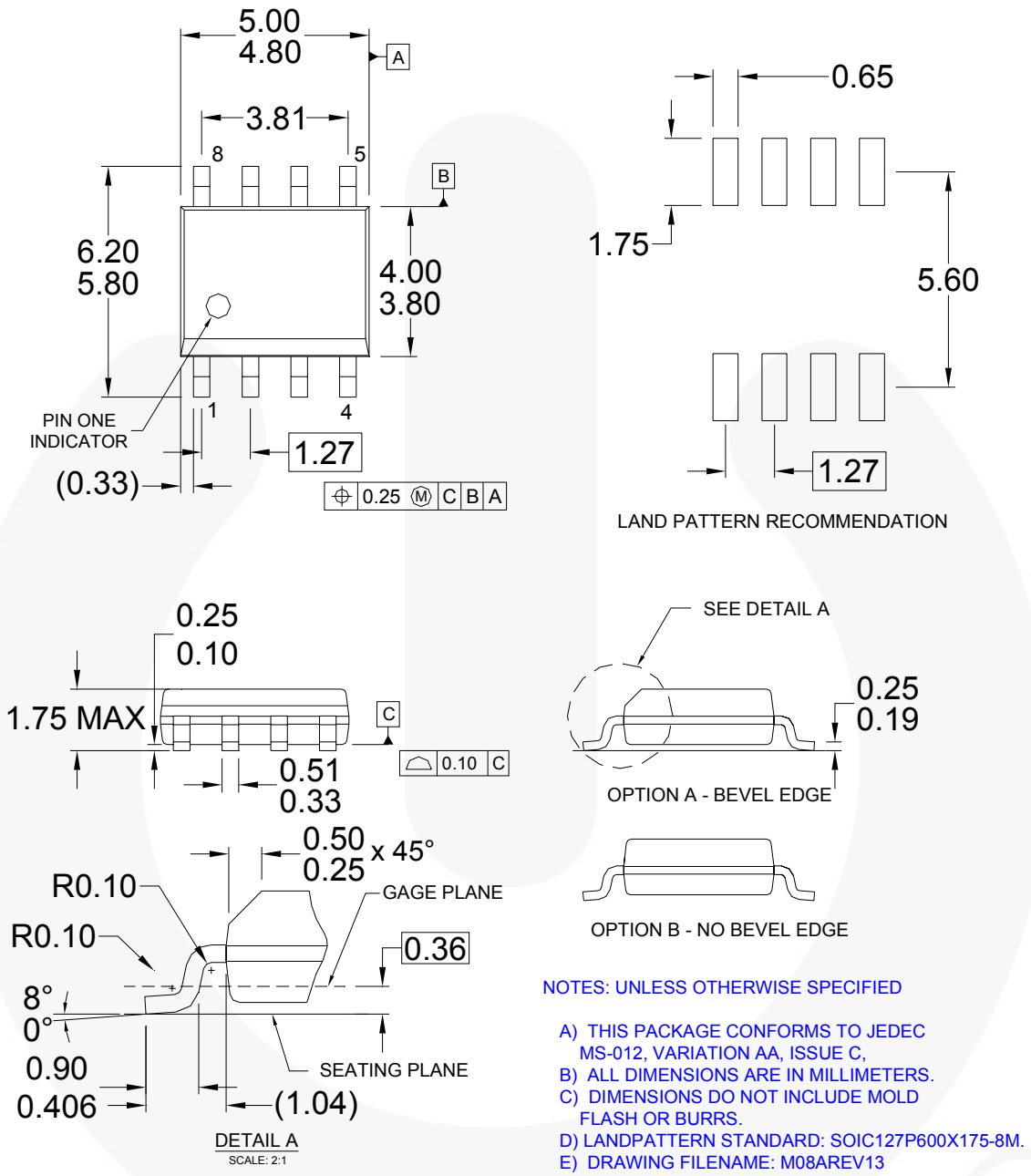


**Figure 15. 8-Pin Small Outline Package (SOP)**

*Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.*

*Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:*
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FACT Quiet Series™
FACT®
FAST®
FastvCore™
FlashWriter®*
FPS™
F-PFS™
FRFET®
Global Power Resource SM
Green FPS™
Green FPS™ e-Series™
GTO™
IntelliMAX™
ISOPLANAR™
MegaBuck™
MICROCOUPLER™
MicroFET™
MicroPak™
MillerDrive™
MotionMax™
Motion-SPM™
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