HYS72T256000HR–[3.7/5]–A

240-Pin Registered-DDR2-SDRAM Modules

RDIMM
DDR2 SDRAM
RoHS Compliant

Memory Products

Infineon technologies

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20	IDD currents are final	
26	SPD Code Byte 41 updated for DDR400	

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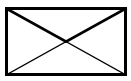

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1 Overview

This chapter gives an overview of the 1.8 V 240-Pin Registered DDR2 SDRAM Modules and describes its main characteristics.

1.1 Features

- 240-Pin PC2-4200 and PC2-3200 DDR2 SDRAM Module for PC, Workstation and Server main memory applications
- One rank 256M x 72 module organization and 256M ×4 chip organization
- JEDEC standard Double-Data-Rate-Two Synchronous DRAMs (DDR2 SDRAM) with a single + 1.8 V (± 0.1 V) power supply
- Built with 1 Gb DDR2 SDRAMs in P-TFBGA-68 chipsize packages.
- Programmable CAS Latencies (3, 4 & 5), Burst Length (4 & 8) and Burst Type
- Auto Refresh (CBR) and Self Refresh
- All inputs and outputs SSTL_1.8 compatible
- Off-Chip Driver Impedance Adjustment (OCD) and On-Die Termination (ODT)
- Serial Presence Detect with E^2PROM
- RDIMM Dimensions (nominal): 30,00 mm high, 133.35 mm wide
- Based on JEDEC standard reference card layouts Raw Card “H”
- RoHS Compliant Products[1)]

Table 1 Performance

Product Type Speed Code			–3.7	–5	Units
Speed Grade			PC2–4200 4–4–4	PC2–3200 3–3–3	—
max. Clock Frequency	@CL5	f_{CK5}	266	200	MHz
	@CL4	f_{CK4}	266	200	MHz
	@CL3	f_{CK3}	200	200	MHz
min. RAS-CAS-Delay		t_{RCD}	15	15	ns
min. Row Precharge Time		t_{RP}	15	15	ns
min. Row Active Time		t_{RAS}	45	40	ns
min. Row Cycle Time		t_{RC}	60	55	ns

1.2 Description

The INFINEON HYS72T256000HR–[3.7/5]–A module family are Registered DIMM modules with 30,0 mm height based on DDR2 technology. DIMMs are available as ECC modules in 256M x 72 (2 GByte) organization and density, intended for mounting into 240-Pin connector sockets.

The memory array is designed with 1 Gb Double-Data-Rate-Two (DDR2) Synchronous DRAMs. All control and address signals are re-driven on the DIMM using register devices and a PLL for the clock distribution. This reduces capacitive loading to the system bus, but adds one cycle to the SDRAM timing. Decoupling capacitors are mounted on the PCB board. The DIMMs feature serial presence detect based on a serial E^2PROM device using the 2-pin I^2C protocol. The first 128 bytes are programmed with configuration data and the second 128 bytes are available to the customer.

1) RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers.

Table 2 Ordering Information for RoHS Compliant Products

Product Type[1]	Compliance Code[2]	Description	SDRAM Technology
PC2-3200			
HYS72T256000HR–5–A	2 GB 1R×4 PC2–3200R–333–11–H1	1 Rank, ECC	1 Gbit (×4)
PC2–4200			
HYS72T256000HR–3.7–A	2 GB 1R×4 PC2–4200R–444–11–H1	1 Rank, ECC	1 Gbit (×4)

1) All part numbers end with a place code, designating the silicon die revision. Example: HYS72T256000HR–5–A, indicating Rev. “A” dies are used for DDR2 SDRAM components. For all INFINEON DDR2 module and component nomenclature see **Chapter 7** of this data sheet.

2) The Compliance Code is printed on the module label and describes the speed grade, for example “PC2–4200R–444–11–H1”, where 4200R means Registered DIMM modules with 4.26 GB/sec Module Bandwidth and “444-11” means Column Address Strobe (CAS) latency = 4, Row Column Delay (RCD) latency = 4 and Row Precharge (RP) latency = 4 using the latest JEDEC SPD Revision 1.1 and produced on the Raw Card “F”

Table 3 Address Format

DIMM Density	Module Organization	Memory Ranks	ECC/ Non-ECC	# of SDRAMs	# of row/bank/columns bits	Raw Card
2 GB	256M ×72	1	ECC	18	14/3/11	H

Table 4 Components on Modules [1]

Product Type[2]	DRAM Components[2]	DRAM Density	DRAM Organization
HYS72T256000HR–3.7–A	HYB18T1G400AF–3.7	1 Gbit	256M ×4
HYS72T256000HR–5–A	HYB18T1G400AF–5	1 Gbit	256M ×4

1) For a detailed description of all functionalities of the DRAM components on these modules see the referenced component data sheet.

2) Green Product

2 Pin Configuration

The pin configuration of the Registered DDR2 SDRAM DIMM is listed by function in Table 5 (240 pins). The abbreviations used in columns Pin and Buffer Type are explained in Table 6 and Table 7 respectively. The pin numbering is depicted in Figure 1.

Table 5 Pin Configuration of RDIMM

Pin#	Name	Pin Type	Buffer Type	Function
Clock Signals				
185	CK0	I	SSTL	**Clock Signal CK0, Complementary Clock Signal $\overline{CK0}$**
186	$\overline{CK0}$	I	SSTL	*Note: The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and the falling edge of $\overline{CK}$. A Delay Locked Loop (DLL) circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock.*
52	CKE0	I	SSTL	**Clock Enables 1:0**
171	CKE1	I	SSTL	*Note: Activates the DDR2 SDRAM CK signal when HIGH and deactivates the CK signal when LOW. By deactivating the clocks, CKE0 initiates the Power Down Mode or the Self Refresh Mode.* *Note: 2-Ranks module*
	NC	NC	—	*Note: 1-Rank module*
Control Signals				
193	$\overline{S0}$	I	SSTL	**Chip Select Rank 1:0**
76	$\overline{S1}$	I	SSTL	*Note: Enables the associated DDR2 SDRAM command decoder when LOW and disables the command decoder when HIGH. When the command decoder is disabled, new commands are ignored but previous operations continue. Rank 0 is selected by $\overline{S0}$; Rank 1 is selected by $\overline{S1}$. The input signals also disable all outputs (except CKE and ODT) of the register(s) on the DIMM when both inputs are high. When $\overline{S}$ is HIGH, all register outputs (except CK, ODT and Chip select) remain in the previous state.* *Note: 2-Ranks module*
	NC	NC	—	*Note: 1-Rank module*
192	$\overline{RAS}$	I	SSTL	**Row Address Strobe (RAS), Column Address Strobe (CAS), Write Enable (WE)**
74	$\overline{CAS}$	I	SSTL	
73	$\overline{WE}$	I	SSTL	*Note: When sampled at the cross point of the rising edge of CK, and falling edge of $\overline{CK}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ define the operation to be executed by the SDRAM.*
18	$\overline{RESET}$	I	CMOS	**Register Reset** *Note: The RESET pin is connected to the RST pin on the register and to the OE pin on the PLL. When LOW, all register outputs will be driven LOW and the PLL clocks to the DRAMs and the register(s) will be set to low-level. The PLL will remain synchronized with the input clock.*
Address Signals				

Table 5 Pin Configuration of RDIMM (cont'd)

Pin#	Name	Pin Type	Buffer Type	Function
71	BA0	I	SSTL	**Bank Address Bus 1:0**
190	BA1	I	SSTL	*Note: Selects internal SDRAM memory bank*
54	BA2	I	SSTL	**Bank Address Bus 2** *Note: Greater than 512Mb DDR2 SDRAMS*
	NC	I	SSTL	*Note: Less than 1Gb DDR2 SDRAMS*
188	A0	I	SSTL	**Address Bus 12:0, Address Signal 10/AutoPrecharge**
183	A1	I	SSTL	*Note: During a Bank Activate command cycle, defines the row address when sampled at the crosspoint of the rising edge of CK and falling edge of $\overline{CK}$. During a Read or Write command cycle, defines the column address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is HIGH, autoprecharge is selected and BA[2:0] defines the bank to be precharged. If AP is LOW, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA[2:0] to control which bank(s) to precharge. If AP is HIGH, all banks will be precharged regardless of the state of BA[2:0] inputs. If AP is LOW, then BA[2:0] are used to define which bank to precharge.*
63	A2	I	SSTL	
182	A3	I	SSTL	
61	A4	I	SSTL	
60	A5	I	SSTL	
180	A6	I	SSTL	
58	A7	I	SSTL	
179	A8	I	SSTL	
177	A9	I	SSTL	
70	A10	I	SSTL	
	AP	I	SSTL	
57	A11	I	SSTL	
176	A12	I	SSTL	
196	A13	I	SSTL	**Address Signal 13** *Note: modules based on ×4, ×8*
	NC	NC	–	*Note: modules based on ×16*
174	A14	I	SSTL	**Address Signal 14** *Note: 2 Gbit based module*
	NC	NC	–	*Note: 1 Gbit based module or smaller*

Table 5 Pin Configuration of RDIMM (cont'd)

Pin#	Name	Pin Type	Buffer Type	Function
Data Signals				
3	DQ0	I/O	SSTL	**Data Bus 63:0**
4	DQ1	I/O	SSTL	*Note: Data Input/Output pins*
9	DQ2	I/O	SSTL	
10	DQ3	I/O	SSTL	
122	DQ4	I/O	SSTL	
123	DQ5	I/O	SSTL	
128	DQ6	I/O	SSTL	
129	DQ7	I/O	SSTL	
12	DQ8	I/O	SSTL	
13	DQ9	I/O	SSTL	
21	DQ10	I/O	SSTL	
22	DQ11	I/O	SSTL	
131	DQ12	I/O	SSTL	
132	DQ13	I/O	SSTL	
140	DQ14	I/O	SSTL	
141	DQ15	I/O	SSTL	
24	DQ16	I/O	SSTL	
25	DQ17	I/O	SSTL	
30	DQ18	I/O	SSTL	
31	DQ19	I/O	SSTL	
143	DQ20	I/O	SSTL	
144	DQ21	I/O	SSTL	
149	DQ22	I/O	SSTL	
150	DQ23	I/O	SSTL	
33	DQ24	I/O	SSTL	
34	DQ25	I/O	SSTL	
39	DQ26	I/O	SSTL	
40	DQ27	I/O	SSTL	

Table 5 Pin Configuration of RDIMM (cont'd)

Pin#	Name	Pin Type	Buffer Type	Function
152	DQ28	I/O	SSTL	**Data Bus 63:0**
153	DQ29	I/O	SSTL	
158	DQ30	I/O	SSTL	
159	DQ31	I/O	SSTL	
80	DQ32	I/O	SSTL	
81	DQ33	I/O	SSTL	
86	DQ34	I/O	SSTL	
87	DQ35	I/O	SSTL	
199	DQ36	I/O	SSTL	
200	DQ37	I/O	SSTL	
205	DQ38	I/O	SSTL	
206	DQ39	I/O	SSTL	
89	DQ40	I/O	SSTL	
90	DQ41	I/O	SSTL	
95	DQ42	I/O	SSTL	
96	DQ43	I/O	SSTL	
208	DQ44	I/O	SSTL	
209	DQ45	I/O	SSTL	
214	DQ46	I/O	SSTL	
215	DQ47	I/O	SSTL	
98	DQ48	I/O	SSTL	
99	DQ49	I/O	SSTL	
107	DQ50	I/O	SSTL	
108	DQ51	I/O	SSTL	
217	DQ52	I/O	SSTL	
218	DQ53	I/O	SSTL	
226	DQ54	I/O	SSTL	
227	DQ55	I/O	SSTL	
110	DQ56	I/O	SSTL	
111	DQ57	I/O	SSTL	
116	DQ58	I/O	SSTL	
117	DQ59	I/O	SSTL	
229	DQ60	I/O	SSTL	
230	DQ61	I/O	SSTL	
235	DQ62	I/O	SSTL	
236	DQ63	I/O	SSTL	

Table 5 Pin Configuration of RDIMM (cont'd)

Pin#	Name	Pin Type	Buffer Type	Function
42	CB0	I/O	SSTL	**Check Bits 7:0**
43	CB1	I/O	SSTL	*Note: Check Bit Input / Output pins*
48	CB2	I/O	SSTL	*Note: NC on Non-ECC module*
49	CB3	I/O	SSTL	
161	CB4	I/O	SSTL	
162	CB5	I/O	SSTL	
167	CB6	I/O	SSTL	
168	CB7	I/O	SSTL	
Data Strobe Bus				
7	DQS0	I/O	SSTL	**Data Strobes 17:0**
6	$\overline{\text{DQS0}}$	I/O	SSTL	*Note: The data strobes, associated with one data byte, sourced with data transfers. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode the data strobe is sourced by the DDR2 SDRAM and is sent at the leading edge of the data window. $\overline{\text{DQS}}$ signals are complements, and timing is relative to the crosspoint of respective DQS and $\overline{\text{DQS}}$. If the module is to be operated in single ended strobe mode, all $\overline{\text{DQS}}$ signals must be tied on the system board to V_{SS} through a 20 ohm to 10 Kohm resistor and DDR2 SDRAM mode registers programmed appropriately.*
16	DQS1	I/O	SSTL	
15	$\overline{\text{DQS1}}$	I/O	SSTL	
28	DQS2	I/O	SSTL	
27	$\overline{\text{DQS2}}$	I/O	SSTL	
37	DQS3	I/O	SSTL	
36	$\overline{\text{DQS3}}$	I/O	SSTL	
84	DQS4	I/O	SSTL	
83	$\overline{\text{DQS4}}$	I/O	SSTL	
93	DQS5	I/O	SSTL	*Note: See block diagram for corresponding DQ signals*
92	$\overline{\text{DQS5}}$	I/O	SSTL	
105	DQS6	I/O	SSTL	
104	$\overline{\text{DQS6}}$	I/O	SSTL	
114	DQS7	I/O	SSTL	
113	$\overline{\text{DQS7}}$	I/O	SSTL	
46	DQS8	I/O	SSTL	
45	$\overline{\text{DQS8}}$	I/O	SSTL	
126	$\overline{\text{DQS9}}$	I/O	SSTL	*Note: ×8 based DIMMs only*
	NC	NC	–	*Note: ×4 based DIMMs*
135	$\overline{\text{DQS10}}$	I/O	SSTL	*Note: ×8 based DIMMs only*
	NC	NC	–	*Note: ×4 based DIMMs*
147	$\overline{\text{DQS11}}$	I/O	SSTL	*Note: ×8 based DIMMs only*
	NC	NC	–	*Note: ×4 based DIMMs*
156	$\overline{\text{DQS12}}$	I/O	SSTL	*Note: ×8 based DIMMs only*
	NC	NC	–	*Note: ×4 based DIMMs*
203	$\overline{\text{DQS13}}$	I/O	SSTL	*Note: ×8 based DIMMs only*
	NC	NC	–	*Note: ×4 based DIMMs*
212	$\overline{\text{DQS14}}$	I/O	SSTL	*Note: ×8 based DIMMs only*
	NC	NC	–	*Note: ×4 based DIMMs*

Table 5 Pin Configuration of RDIMM (cont'd)

Pin#	Name	Pin Type	Buffer Type	Function
224	$\overline{\text{DQS15}}$	I/O	SSTL	*Note: ×8 based DIMMs only*
	NC	NC	–	*Note: ×4 based DIMMs*
233	$\overline{\text{DQS16}}$	I/O	SSTL	*Note: ×8 based DIMMs only*
	NC	NC	–	*Note: ×4 based DIMMs*
165	$\overline{\text{DQS17}}$	I/O	SSTL	*Note: ×8 based DIMMs only*
	NC	NC	–	*Note: ×4 based DIMMs*
125	DQS9	I/O	SSTL	**Data Strobes 17:9**
134	DQS10	I/O	SSTL	*Note: ×4 based module*
146	DQS11	I/O	SSTL	
155	DQS12	I/O	SSTL	
202	DQS13	I/O	SSTL	
211	DQS14	I/O	SSTL	
223	DQS15	I/O	SSTL	
232	DQS16	I/O	SSTL	
164	DQS17	I/O	SSTL	
125	DM0	I	SSTL	**Data Masks 7:0**
134	DM1	I	SSTL	*Note: The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is LOW but blocks the write operation if it is HIGH. In Read mode, DM lines have no effect.*
146	DM2	I	SSTL	
155	DM3	I	SSTL	
202	DM4	I	SSTL	
211	DM5	I	SSTL	*Note: ×8 based module*
223	DM6	I	SSTL	
232	DM7	I	SSTL	
164	DM8	I	SSTL	
EEPROM				
120	SCL	I	CMOS	**Serial Bus Clock** *Note: This signal is used to clock data into and out of the SPD EEPROM.*
119	SDA	I/O	OD	**Serial Bus Data** *Note: This is a bidirectional pin used to transfer data into or out of the SPD EEPROM. A resistor must be connected from SDA to V_{DDSPD} on the motherboard to act as a pull-up.*
239	SA0	I	CMOS	**Serial Address Select Bus 2:0**
240	SA1	I	CMOS	*Note: These signals are tied at the system planar to either V_{SS} or V_{DDSPD} to configure the serial SPD EEPROM address range*
101	SA2	I	CMOS	
Power Supplies				
1	V_{REF}	AI	–	**I/O Reference Voltage** *Note: Reference voltage for the SSTL-18 inputs.*

Table 5 Pin Configuration of RDIMM (cont'd)

Pin#	Name	Pin Type	Buffer Type	Function
238	V_{DDSPD}	PWR	–	**EEPROM Power Supply** *Note: Serial EEPROM positive power supply, wired to a separated power pin at the connector which supports from 1.7 Volt to 3.6 Volt.*
51, 56, 62, 72, 75, 78, 170, 175, 181, 191, 194	V_{DDQ}	PWR	–	**I/O Driver Power Supply** *Note: Power and ground for the DDR SDRAM*
53, 59, 64, 67, 69, 172, 178, 184, 187, 189, 197	V_{DD}	PWR	–	**Power Supply** *Note: Power and ground for the DDR SDRAM*
2, 5, 8, 11, 14, 17, 20, 23, 26, 29, 32, 35, 38, 41, 44, 47, 50, 65, 66, 79, 82, 85, 88, 91, 94, 97, 100, 103, 106, 109, 112, 115, 118, 121, 124, 127, 130, 133, 136, 139, 142, 145, 148, 151, 154, 157, 160, 163, 166, 169, 198, 201, 204, 207, 210, 213, 216, 219, 222, 225, 228, 231, 234, 237	V_{SS}	GND	–	**Ground Plane** *Note: Power and ground for the DDR SDRAM*
Other Pins				
19, 55, 68, 102, 137, 138, 173, 220, 221	NC	NC	–	**Not connected** Pins not connected on Infineon RDIMM's
195	ODT0	I	SSTL	**On-Die Termination Control 1:0**
77	ODT1	I	SSTL	*Note: Asserts on-die termination for DQ, DM, DQS, and $\overline{DQS}$ signals if enabled via the DDR2 SDRAM mode register.* *Note: 2-Ranks module*
	NC	NC	–	*Note: 1-Rank modules*

Table 6 Abbreviations for Buffer Type

Abbreviation	Description
SSTL	Serial Stub Terminated Logic (SSTL_18)
CMOS	CMOS Levels
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR.

Table 7 Abbreviations for Pin Type

Abbreviation	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
PWR	Power
GND	Ground
NU	Not Usable
NC	Not Connected

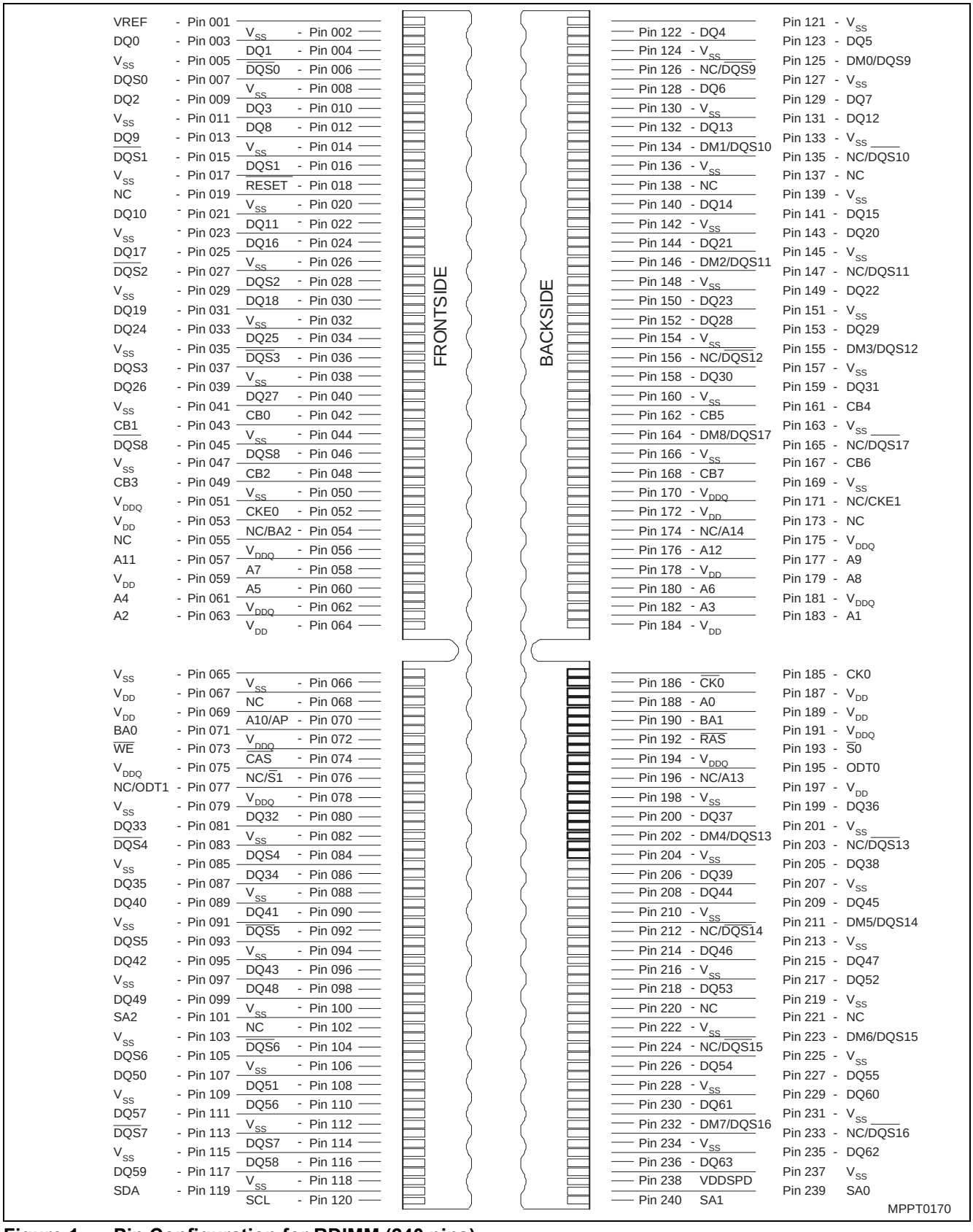

Figure 1 Pin Configuration for RDIMM (240 pins)

2.1 Block Diagrams

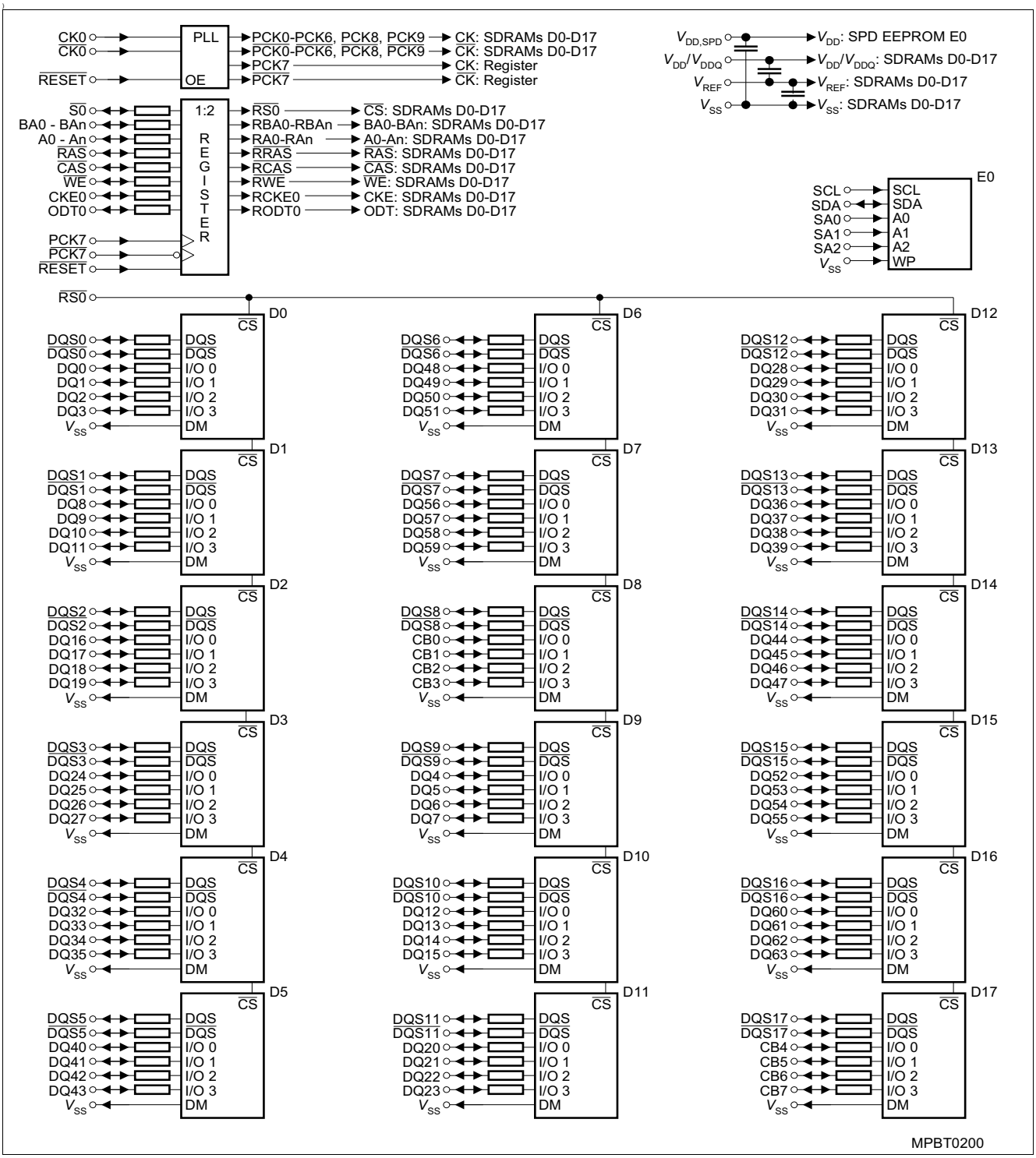

Figure 2 Block Diagram Raw Card H RDIMM (x72, 1Rank, x4)

Notes

1. *Unless otherwise noted, resistors are 22 Ω ± 5 %*
2. *S0 connects to DCS of register1 and CSR of register2.*
3. *CSR of register1 and DCS of register2 connects to V_{DD}.*
4. *RESET, PCK7 and PCK7 connect to both registers.*

3 I_{DD} Specifications and Conditions

Table 8 I_{DD} Measurement Conditions[1)2)3)4)5)6)7)8)]

Parameter	Symbol
Operating Current 0 One bank Active - Precharge; $t_{CK} = t_{CK.MIN}$, $t_{RC} = t_{RC.MIN}$, $t_{RAS} = t_{RAS.MIN}$, CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING.	I_{DD0}
Operating Current 1 One bank Active - Read - Precharge; I_{OUT} = 0 mA, BL = 4, $t_{CK} = t_{CK.MIN}$, $t_{RC} = t_{RC.MIN}$, $t_{RAS} = t_{RAS.MIN}$, $t_{RCD} = t_{RCD.MIN}$, AL = 0, CL = CL_{MIN}; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING.	I_{DD1}
Precharge Standby Current All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; $t_{CK} = t_{CK.MIN}$; Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	I_{DD2N}
Precharge Power-Down Current Other control and address inputs are STABLE, Data bus inputs are FLOATING.	I_{DD2P}
Precharge Quiet Standby Current All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; $t_{CK} = t_{CK.MIN}$; Other control and address inputs are STABLE, Data bus inputs are FLOATING.	I_{DD2Q}
Active Standby Current Burst Read: All banks open; Continuous burst reads; BL = 4; AL = 0, CL = CL_{MIN}; $t_{CK} = t_{CK.MIN}$; $t_{RAS} = t_{RAS.MAX}$, $t_{RP} = t_{RP.MIN}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING; I_{OUT} = 0 mA.	I_{DD3N}
Active Power-Down Current All banks open; $t_{CK} = t_{CK.MIN}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to LOW (Fast Power-down Exit);	$I_{DD3P(0)}$
Active Power-Down Current All banks open; $_{tCK} = t_{CK.MIN}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to HIGH (Slow Power-down Exit);	$I_{DD3P(1)}$
Operating Current Burst Read: All banks open; Continuous burst reads; BL = 4; AL = 0, CL = CL_{MIN}; $t_{CK} = t_{CK.MIN}$; $t_{RAS} = t_{RAS.MAX.}$, $t_{RP} = t_{RP.MIN}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING; I_{OUT} = 0 mA.	I_{DD4R}
Operating Current Burst Write: All banks open; Continuous burst writes; BL = 4; AL = 0, CL = CL_{MIN}; $t_{CK} = t_{CK.MIN}$; $t_{RAS} = t_{RAS.MAX.}$, $t_{RP} = t_{RP.MAX}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING;	I_{DD4W}
Burst Refresh Current $t_{CK} = t_{CK.MIN.}$, Refresh command every $t_{RFC} = t_{RFC.MIN}$ interval, CKE is HIGH, $\overline{CS}$ is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	I_{DD5B}
Distributed Refresh Current $t_{CK} = t_{CK.MIN.}$, Refresh command every $t_{RFC} = t_{REFI}$ interval, CKE is LOW and $\overline{CS}$ is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	I_{DD5D}

Table 8 I_{DD} Measurement Conditions[1)2)3)4)5)6)7)8)]

Parameter	Symbol
Self-Refresh Current CKE ≤ 0.2 V; external clock off, CK and $\overline{CK}$ at 0 V; Other control and address inputs are FLOATING, Data bus inputs are FLOATING. RESET is LOW. I_{DD6} current values are guaranteed up to T_{CASE} of 85 °C max.	I_{DD6}
All Bank Interleave Read Current All banks are being interleaved at minimum t_{RC} without violating t_{RRD} using a burst length of 4. Control and address bus inputs are STABLE during DESELECTS. I_{OUT} = 0 mA.	I_{DD7}

1) V_{DDQ} = 1.8 V ± 0.1 V; V_{DD} = 1.8 V ± 0.1 V
2) I_{DD} specifications are tested after the device is properly initialized and I_{DD} parameter are specified with ODT disabled.
3) Definitions for I_{DD}:
   LOW is defined as $V_{IN} \leq V_{IL(ac).MAX}$, HIGH is defined as $V_{IN} \geq V_{IH(ac).MIN}$
   STABLE is defined as: inputs are stable at a HIGH or LOW level
   FLOATING is defined as: inputs are V_{REF} = V_{DDQ} /2
   SWITCHING is defined as: inputs are changing between HIGH and LOW every other clock (once per 2 cycles) for address and control signals, and inputs changing between HIGH and LOW every other data transfer (once per cycle) for DQ signals not including mask or strobes.
4) I_{DD1}, I_{DD4R} and I_{DD7} current measurements are defined with the outputs disabled (I_{OUT} = 0 mA). To achieve this on module level the output buffers can be disabled using an EMRS(1) (Extended Mode Register Command) by setting A12 bit to HIGH.
5) For two rank modules: for all active current measurements the other rank is in Precharge Power-Down Mode I_{DD2P}
6) RESET signal is HIGH for all currents, except for I_{DD6} (Self Refresh)
7) All current measurements includes Register and PLL current consumption
8) For details and notes see the relevant INFINEON component data sheet

Table 9 I_{DD} Specification for HYS72T256000HR–[3.7/5]

Product Type	HYS72T256000HR–3.7–A	HYS72T256000HR–5–A	Unit	Notes[1]
Organization	**2 GB**	**2 GB**		
	1 Rank	**1 Rank**		
	×72	**×72**		
	–3.7	**–5**		
Symbol	**Max.**	**Max.**		
I_{DD0}	1850	1670	mA	2)
I_{DD1}	2030	1850	mA	2)
I_{DD2N}	1330	1040	mA	3)
I_{DD2P}	590	500	mA	3)
I_{DD2Q}	1080	910	mA	3)
I_{DD3N}	1400	1130	mA	3)
$I_{DD3P(MRS=0)}$	810	640	mA	3)
$I_{DD3P(MRS=1)}$	610	500	mA	3)
I_{DD4R}	2480	2030	mA	2)
I_{DD4W}	2570	2120	mA	2)
I_{DD5B}	3830	3650	mA	2)
I_{DD5D}	630	530	mA	3)
I_{DD6}	90	90	mA	3)
I_{DD7}	4190	3920	mA	2)

1) Module I_{DD} is calculated on the basis of component I_{DD} and currents includes Registers and PLL. ODT disabled. I_{DD1}, I_{DD4R} and I_{DD7} are defined with the outputs disabled.

2) The other rank is in I_{DD2P} Precharge Power-Down Standby Current mode

3) Both ranks are in the same I_{DD} mode

3.1 I_{DD} Test Conditions

For testing the I_{DD} parameters, the following timing parameters are used:

Table 10 I_{DD} Measurement Test Conditions

Parameter		Symbol	–3.7	–5	Unit
			PC2-4200-4-4-4	PC2-3200-3-3-3	
CAS Latency		$CL_{(IDD)}$	4	3	t_{CK}
Clock Cycle Time		$t_{CK(IDD)}$	3.75	5	ns
Active to Read or Write delay		$t_{RCD(IDD)}$	15	15	ns
Active to Active / Auto-Refresh command period		$t_{RC(IDD)}$	60	55	ns
Active bank A to Active bank B command delay	×8[1)]	$t_{RRD(IDD)}$	7.5	7.5	ns
	×16[2)]	$t_{RRD(IDD)}$	10	10	ns
Active to Precharge Command		$t_{RAS.MIN(IDD)}$	45	40	ns
		$t_{RAS.MAX(IDD)}$	70000	70000	ns
Precharge Command Period		$t_{RP(IDD)}$	15	15	ns
Auto-Refresh to Active / Auto-Refresh command period		$t_{RFC(IDD)}$	127.5	127.5	ns
Average periodic Refresh interval		t_{REFI}	7.8	7.8	µs

1) *For modules based on ×8 components*

2) *For modules based on ×16 components*

3.2 ODT (On Die Termination) Current

The ODT function adds additional current consumption to the DDR2 SDRAM when enabled by the EMRS(1). Depending on address bits A[6,2] in the EMRS(1) a “weak” or “strong” termination can be selected. The current consumption for any terminated input pin, depends on the input pin is in tristate or driving 0 or 1, as long a ODT is enabled during a given period of time.

Table 11 ODT current per terminated pin

Parameter	Symbol	Min.	Typ.	Max.	Unit	EMRS(1) State
Enabled ODT current per DQ added I_{DDQ} current for ODT enabled; ODT is HIGH; Data Bus inputs are FLOATING	I_{ODTO}	5	6	7.5	mA/DQ	A6 = 0, A2 = 1
		2.5	3	3.75	mA/DQ	A6 = 1, A2 = 0
Active ODT current per DQ added I_{DDQ} current for ODT enabled; ODT is HIGH; worst case of Data Bus inputs are STABLE or SWITCHING.	I_{ODTT}	10	12	15	mA/DQ	A6 = 0, A2 = 1
		5	6	7.5	mA/DQ	A6 = 1, A2 = 0

4 Electrical Characteristics

4.1 Operating Conditions

Table 12 Absolute Maximum Ratings

Parameter	Symbol	Values		Unit	Note/Test Condition
		Min.	Max.		
Voltage on any pins relative to V_{SS}	V_{IN}, V_{OUT}	– 0.5	2.3	V	1)
Voltage on V_{DD} relative to V_{SS}	V_{DD}	– 1.0	2.3	V	1)
Voltage on $V_{DD\,Q}$ relative to V_{SS}	V_{DDQ}	– 0.5	2.3		1)
Storage Humidity (without condensation)	H_{STG}	5	95	%	1)

1) Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

Table 13 Operating Conditions

Parameter	Symbol	Values		Unit	Notes
		Min.	Max.		
DIMM Module Operating Temperature Range (ambient)	T_{OPR}	0	+55	°C	
DRAM Component Case Temperature Range	T_{CASE}	0	+95	°C	1)2)3)4)
Storage temperature range	T_{STG}	–55	+100	°C	1)
Barometric Pressure (operating & storage)	PBar	+69	+105	kPa	5)
Operating Humidity (relative)	H_{OPR}	10	90	%	

1) DRAM Component Case Temperature is the surface temperature in the center on the top side of any of the DRAMs.

2) Within the DRAM Component Case Temperature range all DRAM specification will be supported.

3) Above 85 °C DRAM case temperature the Auto-Refresh command interval has to be reduced to t_{REFI} = 3.9 µs.

4) Self-Refresh period is hard-coded in the DRAMs and therefore it is imperative that the system ensures the DRAM is below 85 °C case temperature before initiating self-refresh operation.

5) Up to 3000 m

Table 14 Supply Voltage Levels and DC Operating Conditions

Parameter	Symbol	Values			Unit	Notes
		Min.	Nom.	Max.		
Device Supply Voltage	V_{DD}	1.7	1.8	1.9	V	
Output Supply Voltage	V_{DDQ}	1.7	1.8	1.9	V	1)
Input Reference Voltage	V_{REF}	0.49 x V_{DDQ}	0.5 x V_{DDQ}	0.51 x V_{DDQ}	V	2)
EEPROM Supply Voltage	V_{DDSPD}	1.7	—	3.6	V	
DC Input Logic High	$V_{IH\,(DC)}$	V_{REF} + 0.125	—	V_{DDQ} + 0.3	V	
DC Input Logic Low	$V_{IL\,(DC)}$	– 0.30	—	V_{REF} – 0.125	V	
In / Output Leakage Current	I_L	– 5		5	µA	3)

1) Under all conditions, V_{DDQ} must be less than or equal to V_{DD}

2) Peak to peak AC noise on V_{REF} may not exceed ± 2% V_{REF} (DC). V_{REF} is also expected to track noise variations in V_{DDQ}.

3) Input voltage for any connector pin under test of 0 V ≤ V_{IN} ≤ V_{DDQ} + 0.3 V; all other pins at 0 V. Current is per pin

Table 15 Speed Grade Definition Speed Bins

Speed Grade			DDR2–533C		DDR2–400B		Unit	Notes
IFX Sort Name			–3.7		–5			
CAS-RCD-RP latencies			4–4–4		3–3–3		t_{CK}	
Parameter		Symbol	Min.	Max.	Min.	Max.	—	
Clock Frequency	@ CL = 3	t_{CK}	5	8	5	8	ns	1)2)3)4)
	@ CL = 4	t_{CK}	3.75	8	5	8	ns	1)2)3)4)
	@ CL = 5	t_{CK}	3.75	8	5	8	ns	1)2)3)4)
Row Active Time		t_{RAS}	45	70000	40	70000	ns	1)2)3)4)5)
Row Cycle Time		t_{RC}	60	—	55	—	ns	1)2)3)4)
RAS-CAS-Delay		t_{RCD}	15	—	15	—	ns	1)2)3)4)
Row Precharge Time		t_{RP}	15	—	15	—	ns	1)2)3)4)

1) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode. Timings are further guaranteed for normal OCD drive strength (EMRS(1) A1 = 0) only.

2) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS / $\overline{DQS}$, RDQS / $\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode

3) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.

4) The output timing reference voltage level is V_{TT}.

5) $t_{RAS.MAX}$ is calculated from the maximum amount of time a DDR2 device can operate without a refresh command which is equal to 9 x t_{REFI}.

Table 16 Timing Parameter by Speed Grade - DDR2-400B & DDR2-533C

Parameter	Symbol	–3.7 DDR2–533 4–4–4		–5 DDR2–400 3–3–3		Unit	Notes[1)]
		Min.	Max.	Min.	Max.		
DQ output access time from CK / $\overline{CK}$	t_{AC}	–500	+500	–600	+600	ps	
$\overline{CAS}$ A to $\overline{CAS}$ B command period	t_{CCD}	2	—	2	—	t_{CK}	
CK, $\overline{CK}$ high-level width	t_{CH}	0.45	0.55	0.45	0.55	t_{CK}	
CKE minimum high and low pulse width	t_{CKE}	3	—	3	—	t_{CK}	
CK, $\overline{CK}$ low-level width	t_{CL}	0.45	0.55	0.45	0.55	t_{CK}	
Auto-Precharge write recovery + precharge time	t_{DAL}	WR + t_{RP}	—	WR + t_{RP}	—	t_{CK}	
Minimum time clocks remain ON after CKE asynchronously drops LOW	t_{DELAY}	t_{IS} + t_{CK} + t_{IH}	—	t_{IS} + t_{CK} + t_{IH}	—	ns	
DQ and DM input hold time (differential data strobe)	t_{DH}(base)	225	—	275	—	ps	
DQ and DM input hold time (single ended data strobe)	t_{DH1}(base)	–25	—	25	—	ps	
DQ and DM input pulse width (each input)	t_{DIPW}	0.35	—	0.35	—	t_{CK}	
DQS output access time from CK / $\overline{CK}$	t_{DQSCK}	–450	+450	–500	+500	ps	
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	0.35	—	t_{CK}	

Table 16 Timing Parameter by Speed Grade - DDR2-400B & DDR2-533C (cont'd)

Parameter	Symbol	–3.7 DDR2–533 4–4–4		–5 DDR2–400 3–3–3		Unit	Notes[1)]
		Min.	Max.	Min.	Max.		
DQS-DQ skew (for DQS & associated DQ signals)	t_{DQSQ}	—	300	—	350	ps	
Write command to 1st DQS latching transition	t_{DQSS}	WL – 0.25	WL + 0.25	WL – 0.25	WL + 0.25	t_{CK}	
DQ and DM input setup time (differential data strobe)	t_{DS}(base)	100	—	150	—	ps	
DQ and DM input setup time (single ended data strobe)	t_{DS1}(base)	–25	—	25	—	ps	
DQS falling edge hold time from CK (write cycle)	t_{DSH}	0.2	—	0.2	—	t_{CK}	
DQS falling edge to CK setup time (write cycle)	t_{DSS}	0.2	—	0.2	—	t_{CK}	
Four Activate Window period	t_{FAW}	37.5	—	37.5	—	ns	2)3)
Clock half period	t_{HP}	MIN. (t_{CL}, t_{CH})		MIN. (t_{CL}, t_{CH})			
Data-out high-impedance time from CK / $\overline{CK}$	t_{HZ}	—	$t_{AC.MAX}$	—	$t_{AC.MAX}$	ps	
Address and control input hold time	t_{IH}(base)	375	—	475	—	ps	
Address and control input pulse width (each input)	t_{IPW}	0.6	—	0.6	—	t_{CK}	
Address and control input setup time	t_{IS}(base)	250	—	350	—	ps	
DQ low-impedance time from CK / $\overline{CK}$	$t_{LZ(DQ)}$	$2 \times t_{AC.MIN}$	$t_{AC.MAX}$	$2 \times t_{AC.MIN}$	$t_{AC.MAX}$	ps	
DQS low-impedance from CK / $\overline{CK}$	$t_{LZ(DQS)}$	$t_{AC.MIN}$	$t_{AC.MAX}$	$t_{AC.MIN}$	$t_{AC.MAX}$	ps	
Mode register set command cycle time	t_{MRD}	2	—	2	—	t_{CK}	
OCD drive mode output delay	t_{OIT}	0	12	0	12	ns	
Data output hold time from DQS	t_{QH}	$t_{HP} - t_{QHS}$	—	$t_{HPQ} - t_{QHS}$	—		
Data hold skew factor	t_{QHS}	—	400	—	450	ps	
Average periodic refresh Interval	t_{REFI}	—	7.8	—	7.8	µs	4)
		—	3.9	—	3.9	µs	5)
Auto-Refresh to Active/Auto-Refresh command period	t_{RFC}	127.5	—	127.5	—	ns	
Precharge-All (8 banks) command period	t_{RP}	15 + 1t_{CK}	—	15 + 1t_{CK}	—	ns	
Read preamble	t_{RPRE}	0.9	1.1	0.9	1.1	t_{CK}	
Read postamble	t_{RPST}	0.40	0.60	0.40	0.60	t_{CK}	
Active bank A to Active bank B command period	t_{RRD}	7.5	—	7.5	—	ns	
		10	—	10	—	ns	
Internal Read to Precharge command delay	t_{RTP}	7.5	—	7.5	—	ns	
Write preamble	t_{WPRE}	0.35xt_{CK}	—	0.35xt_{CK}	—	t_{CK}	
Write postamble	t_{WPST}	0.40	0.60	0.40	0.60	t_{CK}	

Table 16 Timing Parameter by Speed Grade - DDR2-400B & DDR2-533C (cont'd)

Parameter	Symbol	–3.7 DDR2–533 4–4–4		–5 DDR2–400 3–3–3		Unit	Notes[1)]
		Min.	Max.	Min.	Max.		
Write recovery time for write without Auto-Precharge	t_{WR}	15	—	15	—	ns	
Write recovery time for write with Auto-Precharge	WR	t_{WR}/t_{CK}		t_{WR}/t_{CK}		t_{CK}	
Internal Write to Read command delay	t_{WTR}	7.5	—	10	—	ns	
Exit power down to any valid command (other than NOP or Deselect)	t_{XARD}	2	—	2	—	t_{CK}	
Exit active power-down mode to Read command (slow exit, lower power)	t_{XARDS}	6 – AL	—	6 – AL	—	t_{CK}	
Exit precharge power-down to any valid command (other than NOP or Deselect)	t_{XP}	2	—	2	—	t_{CK}	
Exit Self-Refresh to non-Read command	t_{XSNR}	t_{RFC} +10	—	t_{RFC} +10	—	ns	
Exit Self-Refresh to Read command	t_{XSRD}	200	—	200	—	t_{CK}	

1) For details and notes see the relevant INFINEON component data sheet
2) ×4 & ×8 (1k page size)
3) 8 bank device Sequential Activation Restriction. No more than 4 banks may be activated in a rolling t_{FAW} window.
4) $0 \leq T_{CASE} \leq 85$ °C
5) 85 °C < $T_{CASE} \leq 95$ °C

Table 17 ODT AC Electrical Characteristics and Operating Conditions

Symbol	Parameter / Condition	Values		Unit	Notes
		Min.	Max.		
t_{AOND}	ODT turn-on delay	2	2	t_{CK}	
t_{AON}	ODT turn-on	$t_{AC.MIN}$	$t_{AC.MAX}$ + 1 ns	ns	1)
t_{AONPD}	ODT turn-on (Power-Down Modes)	$t_{AC.MIN}$ + 2 ns	2 t_{CK} + $t_{AC.MAX}$ + 1 ns	ns	
t_{AOFD}	ODT turn-off delay	2.5	2.5	t_{CK}	
t_{AOF}	ODT turn-off	$t_{AC.MIN}$	$t_{AC.MAX}$ + 0.6 ns	ns	2)
t_{AOFPD}	ODT turn-off (Power-Down Modes)	$t_{AC.MIN}$ + 2 ns	2.5 t_{CK} + $t_{AC.MAX}$ + 1 ns	ns	
t_{ANPD}	ODT to Power Down Mode Entry Latency	3	—	t_{CK}	
t_{AXPD}	ODT Power Down Exit Latency	8	—	t_{CK}	

1) ODT turn on time min. is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measure from t_{AOND}.
2) ODT turn off time min. is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from t_{AOFD}.

5 SPD Codes

Table 18 SPD Codes for HYS72T256000HR–[3.7/5]–A

Product Type		**HYS72T256000HR–3.7–A**	**HYS72T256000HR–5–A**
Organization		**2 GByte**	**2 GByte**
		×72	**×72**
		1 Rank (×4)	**1 Rank (×4)**
Label Code		**PC2–4200R–444**	**PC2–3200R–333**
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**
0	Programmed SPD Bytes in EEPROM	80	80
1	Total number of Bytes in EEPROM	08	08
2	Memory Type (DDR2)	08	08
3	Number of Row Addresses	0E	0E
4	Number of Column Addresses	0B	0B
5	DIMM Rank and Stacking Information	60	60
6	Data Width	48	48
7	Not used	00	00
8	Interface Voltage Level	05	05
9	t_{CK} @ CL_{MAX} (Byte 18) [ns]	3D	50
10	t_{AC} SDRAM @ CL_{MAX} (Byte 18) [ns]	50	60
11	Error Correction Support (non-ECC, ECC)	02	02
12	Refresh Rate and Type	82	82
13	Primary SDRAM Width	04	04
14	Error Checking SDRAM Width	04	04
15	Not used	00	00
16	Burst Length Supported	0C	0C
17	Number of Banks on SDRAM Device	08	08
18	Supported CAS Latencies	38	38
19	DIMM Mechanical Characteristics	00	00
20	DIMM Type Information	01	01
21	DIMM Attributes	05	05
22	Component Attributes	01	01
23	t_{CK} @ CL_{MAX} -1 (Byte 18) [ns]	3D	50
24	t_{AC} SDRAM @ CL_{MAX} -1 [ns]	50	60

Table 18 SPD Codes for HYS72T256000HR–[3.7/5]–A (cont'd)

Product Type		**HYS72T256000HR–3.7–A**	**HYS72T256000HR–5–A**
Organization		**2 GByte**	**2 GByte**
		×72	**×72**
		1 Rank (×4)	**1 Rank (×4)**
Label Code		**PC2–4200R–444**	**PC2–3200R–333**
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**
25	t_{CK} @ CL_{MAX} -2 (Byte 18) [ns]	50	50
26	t_{AC} SDRAM @ CL_{MAX} -2 [ns]	60	60
27	$t_{RP.MIN}$ [ns]	3C	3C
28	$t_{RRD.MIN}$ [ns]	1E	1E
29	$t_{RCD.MIN}$ [ns]	3C	3C
30	$t_{RAS.MIN}$ [ns]	2D	28
31	Module Density per Rank	02	02
32	$t_{AS.MIN}$ and $t_{CS.MIN}$ [ns]	25	35
33	$t_{AH.MIN}$ and $t_{CH.MIN}$ [ns]	37	47
34	$t_{DS.MIN}$ [ns]	10	15
35	$t_{DH.MIN}$ [ns]	22	27
36	$t_{WR.MIN}$ [ns]	3C	3C
37	$t_{WTR.MIN}$ [ns]	1E	28
38	$t_{RTP.MIN}$ [ns]	1E	1E
39	Analysis Characteristics	00	00
40	t_{RC} and t_{RFC} Extension	00	00
41	$t_{RC.MIN}$ [ns]	3C	37
42	$t_{RFC.MIN}$ [ns]	7F	7F
43	$t_{CK.MAX}$ [ns]	80	80
44	$t_{DQSQ.MAX}$ [ns]	1E	23
45	$t_{QHS.MAX}$ [ns]	28	2D
46	PLL Relock Time	0F	0F
47	$T_{CASE.MAX}$ Delta / ΔT_{4R4W} Delta	51	51
48	Psi(T-A) DRAM	60	60
49	ΔT_0 (DT0)	36	32
50	ΔT_{2N} (DT2N, UDIMM) or ΔT_{2Q} ((DT2Q, RDIMM)	1D	1A
51	ΔT_{2P} (DT2P)	1E	1E

Table 18 SPD Codes for HYS72T256000HR–[3.7/5]–A (cont'd)

Product Type		**HYS72T256000HR–3.7–A**	**HYS72T256000HR–5–A**
Organization		**2 GByte**	**2 GByte**
		×72	**×72**
		1 Rank (×4)	**1 Rank (×4)**
Label Code		**PC2–4200R–444**	**PC2–3200R–333**
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**
52	ΔT_{3N} (DT3N)	1E	18
53	$\Delta T_{3P.fast}$ (DT3P fast)	1F	18
54	$\Delta T_{3P.slow}$ (DT3P slow)	16	12
55	ΔT_{4R} (DT4R) / $\Delta T_{4R4W\ S}$ Sign (DT4R4W)	32	2A
56	ΔT_{5B} (DT5B)	22	21
57	ΔT_{7} (DT7)	25	24
58	Psi(ca) PLL	C4	C4
59	Psi(ca) REG	8C	8C
60	ΔT_{PLL} (DTPLL)	61	59
61	ΔT_{REG} (DTREG) / Toggle Rate	78	5C
62	SPD Revision	11	11
63	Checksum of Bytes 0-62	82	B6
64	JEDEC ID Code of Infineon (1)	C1	C1
65	JEDEC ID Code of Infineon (2)	00	00
66	JEDEC ID Code of Infineon (3)	00	00
67	JEDEC ID Code of Infineon (4)	00	00
68	JEDEC ID Code of Infineon (5)	00	00
69	JEDEC ID Code of Infineon (6)	00	00
70	JEDEC ID Code of Infineon (7)	00	00
71	JEDEC ID Code of Infineon (8)	00	00
72	Module Manufacturer Location	xx	xx
73	Product Type, Char 1	37	37
74	Product Type, Char 2	32	32
75	Product Type, Char 3	54	54
76	Product Type, Char 4	32	32
77	Product Type, Char 5	35	35
78	Product Type, Char 6	36	36

Table 18 SPD Codes for HYS72T256000HR–[3.7/5]–A (cont'd)

Product Type		**HYS72T256000HR–3.7–A**	**HYS72T256000HR–5–A**
Organization		**2 GByte**	**2 GByte**
		×72	**×72**
		1 Rank (×4)	**1 Rank (×4)**
Label Code		**PC2–4200R–444**	**PC2–3200R–333**
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**
79	Product Type, Char 7	30	30
80	Product Type, Char 8	30	30
81	Product Type, Char 9	30	30
82	Product Type, Char 10	48	48
83	Product Type, Char 11	52	52
84	Product Type, Char 12	33	35
85	Product Type, Char 13	2E	41
86	Product Type, Char 14	37	20
87	Product Type, Char 15	41	20
88	Product Type, Char 16	20	20
89	Product Type, Char 17	20	20
90	Product Type, Char 18	20	20
91	Module Revision Code	1x	1x
92	Test Program Revision Code	xx	xx
93	Module Manufacturing Date Year	xx	xx
94	Module Manufacturing Date Week	xx	xx
95	Module Serial Number (1)	xx	xx
96	Module Serial Number (2)	xx	xx
97	Module Serial Number (3)	xx	xx
98	Module Serial Number (4)	xx	xx
99 - 127	Not used	00	00

6 Package Outlines

6.1 Raw Card H

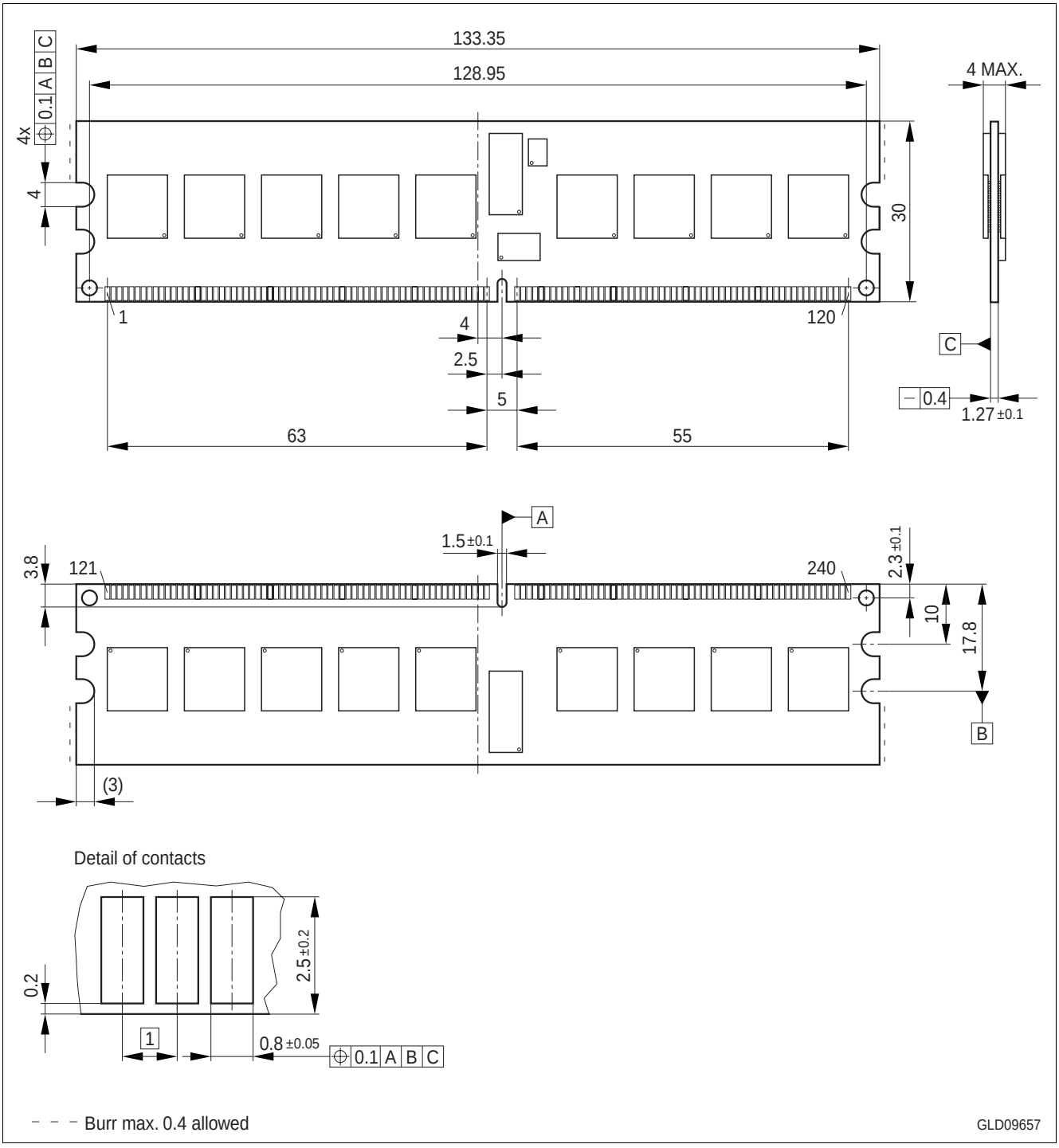

Figure 3 Package Outline L-DIM-240-13

7 Product Type Nomenclature (DDR2 DRAMs and DIMMs)

Infineon's nomenclature uses simple coding combined with some proprietary coding. Table 19 provides examples for module and component product type number as well as the field number. The detailed field description together with possible values and coding explanation is listed for modules in Table 20 and for components in Table 21.

Table 19 Nomenclature Fields and Examples

Example for	Field Number										
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**
Micro-DIMM	HYS	64	T	128	0	2	0	K	M	–5	–A
DDR2 DRAM	HYB	18	T	1G	16		0	A	C	–5	

Table 20 DDR2 DIMM Nomenclature

Field	Description	Values	Coding
1	INFINEON Modul Prefix	HYS	Constant
2	Module Data Width [bit]	64	Non-ECC
		72	ECC
3	DRAM Technology	T	DDR2
4	Memory Density per I/O [Mbit]; Module Density[1)]	32	256 MByte
		64	512 MByte
		128	1 GByte
		256	2 GByte
5	Raw Card Generation	0 .. 9	look up table
6	Number of Module Ranks	0, 2, 4	1, 2, 4
7	Product Variations	0 .. 9	look up table
8	Package, Lead-Free Status	A .. Z	look up table
9	Module Type	D	SO-**D**IMM
		M	**M**icro-DIMM
		R	**R**egistered
		U	**U**nbuffered
10	Speed Grade	–3.7	PC2–4200 4–4–4
		–5	PC2–3200 3–3–3
11	Die Revision	–A	First
		–B	Second

1) Multiplying "Memory Density per I/O" with "Module Data Width" and dividing by 8 for Non-ECC and 9 for ECC modules gives the overall module memory density in MBytes as listed in column "Coding".

Table 21 DDR2 DRAM Nomenclature

Field	Description	Values	Coding
1	INFINEON Component Prefix	HYB	Constant
2	Interface Voltage [V]	18	SSTL1.8
3	DRAM Technology	T	DDR2
4	Component Density [Mbit]	256	256 Mbit
		512	512 Mbit
		1G	1 Gbit
		2G	2 Gbit
5+6	Number of I/Os	40	×4
		80	×8
		16	×16
7	Product Variations	0 .. 9	look up table
8	Die Revision	A	First
		B	Second
9	Package, Lead-Free Status	C	FBGA, lead-containing
		F	FBGA, lead-free
10	Speed Grade	–3.7	DDR2-533C
		–5	DDR2-400B
11	N/A for Components		

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