

DESCRIPTION

The HY514100 is the new generation and fast dynamic RAM organized 4,194,304 x 1-bit. The HY514100 utilizes Hyundai's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins to the users. Multiplexed address inputs permit the HY514100 to be packaged in a standard 20/26 pin plastic SOJ.

The package size provides high system bit densities and is compatible with widely available automated-test equipments. System oriented-feature includes single power supply of 5V± 10% tolerance and direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- Low power dissipation
Max. CMOS standby 5.5mW
Max. TTL standby 11.0mW
Max. operating

Speed	Power
70	495mW
80	440mW
10	385mW

- Single power supply of 5V± 10%
- TTL compatible inputs and outputs
- Fast access time

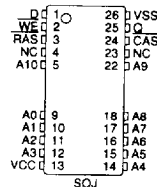
Speed	tRAC	tCAC	tPC
70	70ns	20ns	50ns
80	80ns	25ns	50ns
10	100ns	25ns	60ns

- Fast page mode operation
- Multi-bit test capability
- Read-Modify-Write capability
- CAS-before-RAS, RAS-only, Hidden refresh
- 1024 refresh cycles / 16ms

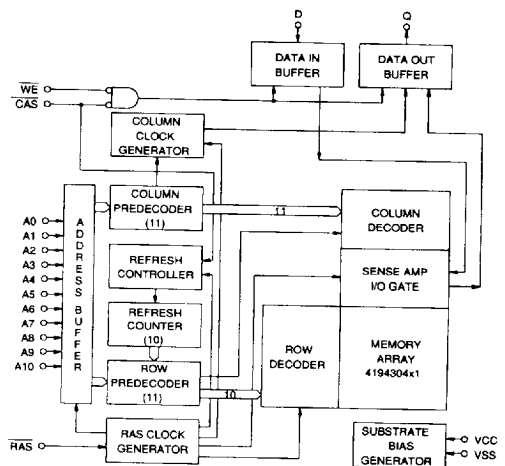
PIN DESCRIPTION

RAS	Row Address Strobe
CAS	Column Address Strobe
WE	Write Enable
A0-A10	Address Input
D	Data Input
Q	Data Output
VCC	Power (+ 5V)
VSS	Ground

PIN CONNECTION



BLOCK DIAGRAM



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1AC01-20-MAY94

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
TA	Ambient Temperature	0 to 70	°C
TSTG	Storage Temperature	-55 to 150	°C
VIN, VOUT	Voltage on Any Pin Relative to VSS	-1.0 to 7.0	V
VCC	Voltage on VCC Relative to VSS	-1.0 to 7.0	V
Ios	Short Circuit Output Current	50	mA
Pd	Power Dissipation	0.63	W
TSOLDER	Soldering Temperature• Time	260• 10	°C•sec

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(TA= 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VCC	Supply Voltage	4.5	5.0	5.5	V
VIH	Input High Voltage	2.4	-	VCC+ 1.0	V
VIL	Input Low Voltage	-1.0	-	0.8	V

NOTE : All voltages are referenced to VSS.

DC CHARACTERISTICS

(TA= 0°C to 70°C, VCC= 5V± 10%, VSS= 0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	MIN.	MAX.	UNIT	NOTE
ILI	Input Leakage Current (Any Input Pins)	VSS ≤ VIN ≤ 6.5V, All other pins not under test= VSS		-	10	μA	
ILO	Output Leakage Current (High Impedance State)	VSS ≤ VOUT ≤ 5.5V, RAS & CAS at VIH		-	10	μA	
ICC1	VCC Supply Current, Operating	tRC= tRC (min.)	70 80 10	- - -	90 80 70	mA	1,2,3
ICC2	VCC Supply Current, TTL Standby	RAS & CAS at VIH		-	2	mA	
ICC3	VCC Supply Current, RAS-only refresh	tRC= tRC (min.)	70 80 10	- - -	90 80 70	mA	1,3
ICC4	VCC Supply Current, Fast Page mode	tPC= tPC (min.)	70 80 10	- - -	70 60 50	mA	1,2,3
ICC5	VCC Supply Current, CMOS Standby	RAS & CAS ≤ VCC-0.2V		-	1	mA	
ICC6	VCC Supply Current, CAS-before-RAS refresh	tRC= tRC (min.)	70 80 10	- - -	90 80 70	mA	1,3
VOL	Output Low Voltage	IOL= 4.2mA		-	0.4	V	
VOH	Output High Voltage	IOH= -5mA		2.4	-	V	

NOTE :

1. ICC1, ICC3, ICC4 and ICC6 depend on cycle rate.
2. ICC1 and ICC4 depend on output loading. Specified values are obtained with the output open.
3. It depends on user whether column address is changed or not at least once while RAS= VIL and CAS= VIH.

AC CHARACTERISTICS

(TA= 0°C to 70°C, VCC= 5V± 10%, VSS= 0V, unless otherwise noted.) NOTE : 1, 2, 3

(TA= 0°C to 70°C, VCC= 5V± 10%, VSS= 0V, unless otherwise noted.)										
HY514100J										
#	SYMBOL	PARAMETER	-70		-80		-10		UNIT	NOTE
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	130	-	150	-	180	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	155	-	180	-	210	-	ns	
3	tPC	Fast Page Mode Cycle Time	50	-	50	-	60	-	ns	
4	tPRWC	Fast Page Mode Read-Modify-Write Cycle Time	75	-	80	-	90	-	ns	
5	tRAC	Access Time from RAS	-	70	-	80	-	100	ns	4,9,10
6	tCAC	Access Time from CAS	-	20	-	25	-	25	ns	4,9
7	tAA	Access Time from Column Address	-	35	-	40	-	45	ns	4,10
8	tCPA	Access Time from CAS Precharge	-	45	-	45	-	55	ns	4
9	tCLZ	CAS to Output Low Impedance	0	-	0	-	0	-	ns	4
10	tOFF	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	5
11	tT	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	3
12	tRP	RAS Precharge Time	50	-	60	-	70	-	ns	
13	tRAS	RAS Pulse Width	70	10K	80	10K	100	10K	ns	
14	tRASP	RAS Pulse Width (Fast Page Mode)	70	200K	80	200K	100	200K	ns	
15	tRSH	RAS Hold Time	20	-	25	-	25	-	ns	
16	tCSH	CAS Hold Time	70	-	80	-	100	-	ns	
17	tCAS	CAS Pulse Width	20	10K	25	10K	25	10K	ns	
18	tRCD	RAS to CAS Delay	20	50	20	55	25	75	ns	9
19	tRAD	RAS to Column Address Delay Time	15	35	15	40	20	55	ns	10
20	tCRP	CAS to RAS Precharge Time	5	-	5	-	10	-	ns	
21	tCP	CAS Precharge Time	10	-	10	-	10	-	ns	
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold Time	10	-	10	-	15	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	
25	tCAH	Column Address Hold Time	15	-	15	-	20	-	ns	
26	tAR	Column Address Hold Time from RAS	55	-	60	-	80	-	ns	
27	tRAL	Column Address to RAS Lead Time	35	-	40	-	45	-	ns	
28	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	
29	tRCH	Read Command Hold Time Referenced to CAS	0	-	0	-	0	-	ns	6
30	tRRH	Read Command Hold Time Referenced to RAS	0	-	0	-	0	-	ns	6
31	tWCH	Write Command Hold Time	15	-	15	-	20	-	ns	
32	tWCR	Write Command Hold Time from RAS	55	-	60	-	80	-	ns	
33	tWP	Write Command Pulse Width	15	-	15	-	20	-	ns	
34	tRWL	Write Command to RAS Lead Time	20	-	25	-	25	-	ns	
35	tCWL	Write Command to CAS Lead Time	20	-	25	-	25	-	ns	
36	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	7
37	tDH	Data-In Hold Time	15	-	15	-	20	-	ns	7
38	tDHR	Data-In Hold Time Referenced to RAS	55	-	60	-	80	-	ns	
39	tREF	Refresh Period (1024 cycles)	-	16	-	16	-	16	ms	
40	tWCS	Write Command Set-up Time	0	-	0	-	0	-	ns	8

AC CHARACTERISTICS

(continued)

HY514100J										
#	SYMBOL	PARAMETER	HY514100J						UNIT	NOTE
			-70		-80		-10			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	tCWD	CAS to WE Delay Time	20	-	25	-	25	-	ns	8
42	tRWD	RAS to WE Delay Time	70	-	80	-	100	-	ns	8
43	tAWD	Column Address to WE Delay Time	35	-	40	-	45	-	ns	8
44	tCSR	CAS Set-up Time (CBR Cycle)	10	-	10	-	10	-	ns	
45	tCHR	CAS Hold Time (CBR Cycle)	30	-	30	-	30	-	ns	
46	tRPC	RAS to CAS Precharge Time	0	-	0	-	0	-	ns	
47	tCPT	CAS Precharge Time (CBR Counter Test)	40	-	40	-	50	-	ns	
48	tCPWD	WE Delay Time from CAS Precharge	10	-	10	-	10	-	ns	
49	tRHCP	RAS Hold Time from CAS Precharge	10	-	10	-	10	-	ns	
50	tWRP	WE to RAS Precharge Time (CBR Cycle)	10	-	10	-	10	-	ns	
51	tWRH	WE to RAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	
52	tWTS	Write Command Set-up Time (Test Mode In)	40	-	45	-	50	-	ns	
53	tWTH	Write Command Hold Time (Test Mode In)	40	-	45	-	50	-	ns	

AC CHARACTERISTICS IN TEST MODE NOTE : 11

#	SYMBOL	PARAMETER	HY514100J						UNIT	NOTE
			-70		-80		-10			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	135	-	155	-	185	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	160	-	185	-	215	-	ns	
3	tPC	Fast Page Mode Cycle Time	55	-	55	-	65	-	ns	
4	tPRWC	Fast Page Mode Read-Modify-Write Cycle Time	80	-	85	-	95	-	ns	
5	tRAC	Access Time from RAS	-	75	-	85	-	105	ns	4,9,10
6	tCAC	Access Time from CAS	-	25	-	30	-	30	ns	4,9
7	tAA	Access Time from Column Address	-	40	-	45	-	50	ns	4,10
8	tCPA	Access Time from CAS Precharge	-	50	-	50	-	60	ns	4
13	tRAS	RAS Pulse Width	75	10K	85	10K	105	10K	ns	
14	tRASP	RAS Pulse Width (Fast Page Mode)	75	200K	85	200K	105	200K	ns	
15	tRSH	RAS Hold Time	25	-	30	-	30	-	ns	
16	tCSH	CAS Hold Time	75	-	85	-	105	-	ns	
17	tCAS	CAS Pulse Width	25	10K	30	10K	30	10K	ns	
27	tRAL	Column Address to RAS Lead Time	35	-	45	-	50	-	ns	
41	tCWD	CAS to WE Delay Time	25	-	30	-	30	-	ns	8
42	tRWD	RAS to WE Delay Time	75	-	86	-	105	-	ns	8
43	tAWD	Column Address to WE Delay Time	40	-	45	-	50	-	ns	8

NOTE :

1. An initial pause of 200 μ s is required after power-up followed by 8 RAS cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS-before-RAS initialization cycles instead of 8 RAS-only refresh cycles are required. The device should be carefully initialized to be prevented from being entered into multi bit test mode during initialization.
2. AC measurements assume $t_T = 5$ ns.
3. $V_{IH}(\text{min.})$ and $V_{IL}(\text{max.})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
4. Measured with a load equivalent to 2 TTL loads and 100pF.
5. $t_{OFF}(\text{max.})$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to CAS leading edge in early write cycles and to WE leading edge in Read-Modify-Write cycles.
8. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\text{min.})$, the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If $t_{RWD} \geq t_{RWD}(\text{min.})$, $t_{CWD} \geq t_{CWD}(\text{min.})$, $t_{AWD} \geq t_{AWD}(\text{min.})$, and $t_{CPWD} \geq t_{CPWD}(\text{min.})$, the cycle is a Read-Modify-Write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminated.
9. Operation within the $t_{RCD}(\text{max.})$ limit insures that $t_{RA}(\text{max.})$ can be met. $t_{RCD}(\text{max.})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\text{max.})$ limit, then access time is controlled by t_{CAC} .
10. Operation within the $t_{RAD}(\text{max.})$ limit insures that $t_{RA}(\text{max.})$ can be met. $t_{RAD}(\text{max.})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\text{max.})$ limit, then access time is controlled by t_{AA} .
11. These specifications are applied to the Test Mode.

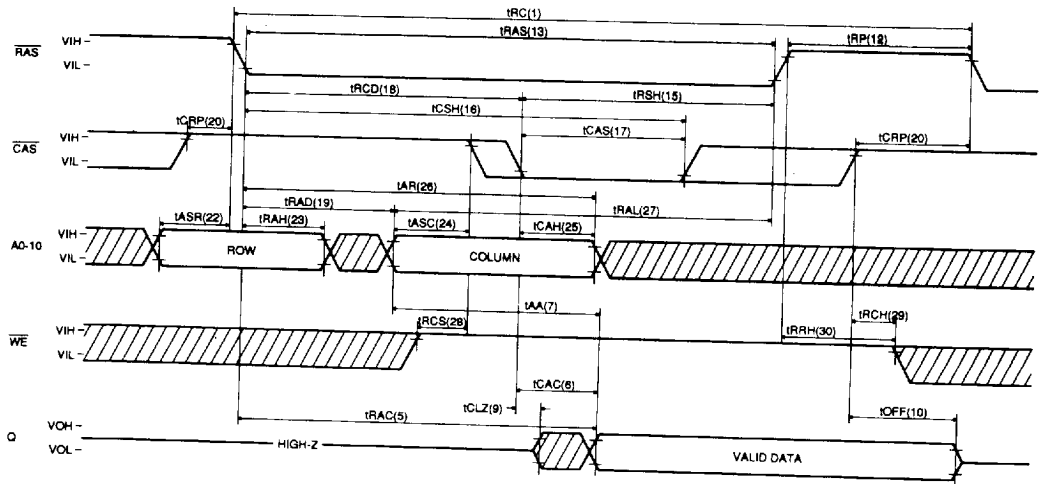
CAPACITANCE

($T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$, $f = 1\text{MHz}$, unless otherwise noted.)

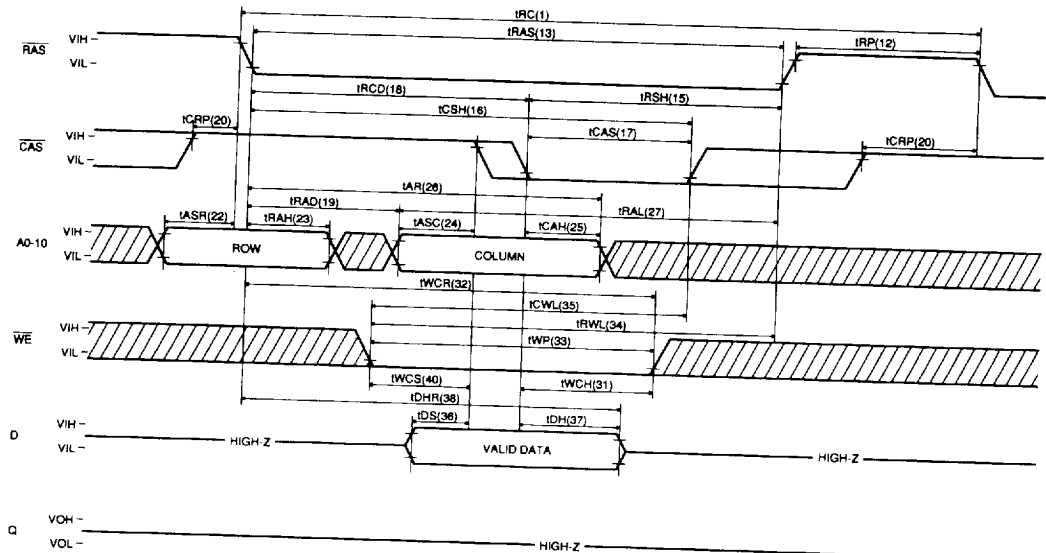
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance (A0-A10, D)	-	5	pF
C_{IN2}	Input Capacitance (RAS, CAS, WE)	-	7	pF
C_{OUT}	Output Capacitance (Q)	-	7	pF

TIMING DIAGRAM

READ CYCLE



EARLY WRITE CYCLE

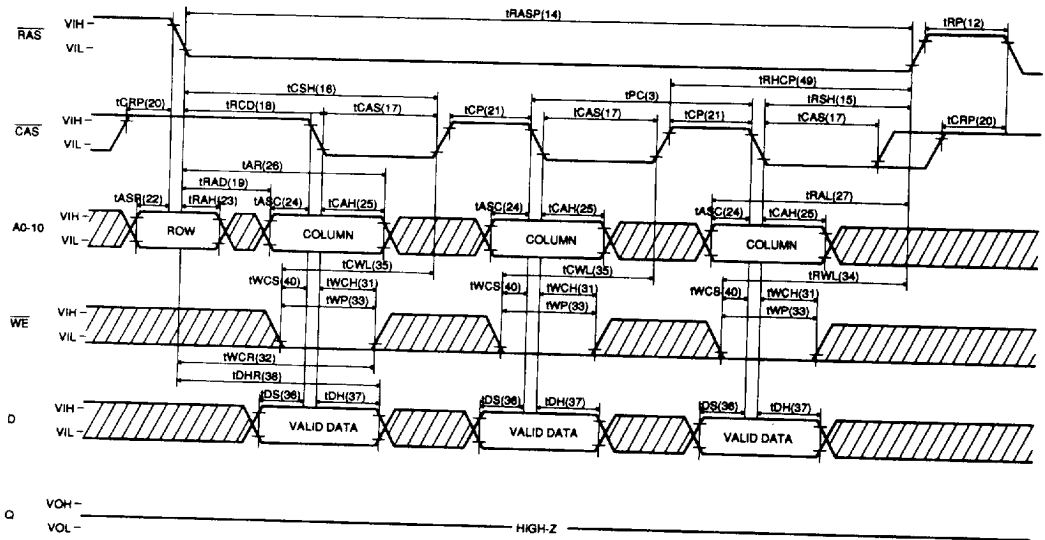


The timing diagram illustrates the relationship between several input and output signals and their associated timing parameters. The signals shown are RAS, CAS, A0-10, WE, D, and Q. The timing parameters are defined as follows:

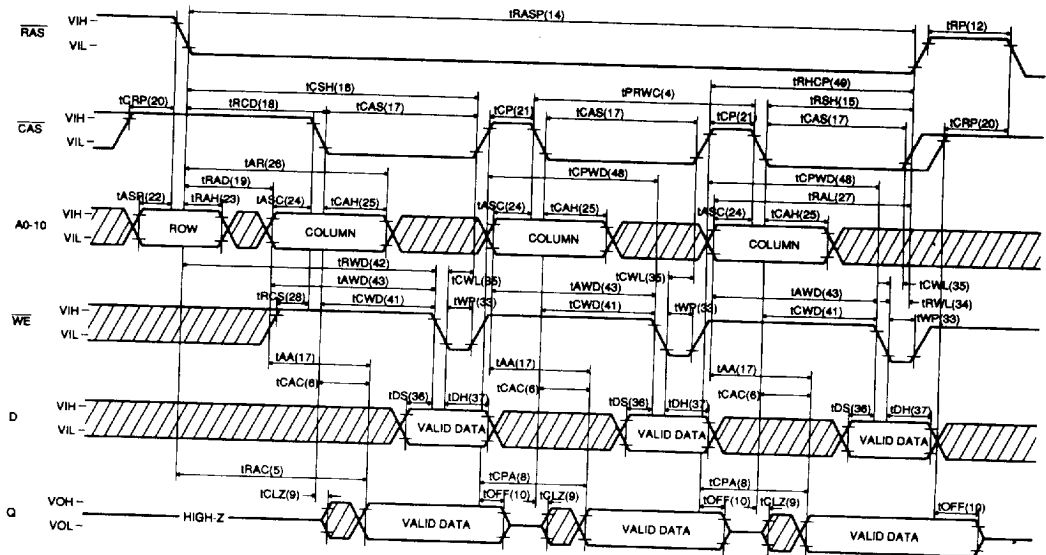
- RAS:** $t_{RAB}(13)$, $t_{RWC}(2)$, $t_{RP}(18)$
- CAS:** $t_{CSH}(18)$, $t_{RSH}(15)$, $t_{CAS}(17)$, $t_{CRP}(20)$
- A0-10:** $t_{ASR}(22)$, $t_{RAD}(19)$, $t_{RAH}(23)$, $t_{ASC}(24)$, $t_{CAH}(25)$, $t_{RAL}(27)$, $t_{RCS}(28)$, $t_{CWD}(41)$, $t_{CWL}(35)$, $t_{RWD}(42)$, $t_{RWL}(34)$, $t_{AWD}(43)$
- WE:** $t_{VAA}(7)$, $t_{CAC}(6)$, $t_{WP}(33)$
- D:** $t_{DB}(36)$, $t_{DH}(37)$, **VALID DATA**
- Q:** t_{VQH} , t_{VQL} , **HIGH-Z**, $t_{CLZ}(8)$, $t_{RAC}(5)$, $t_{IOFF}(10)$, **VALID DATA**

[illegible]

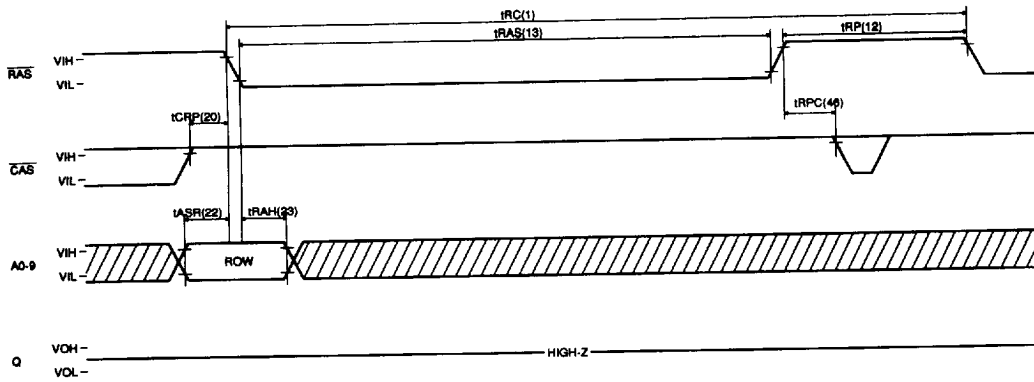
FAST PAGE MODE EARLY WRITE CYCLE



FAST PAGE MODE READ-MODIFY-WRITE CYCLE

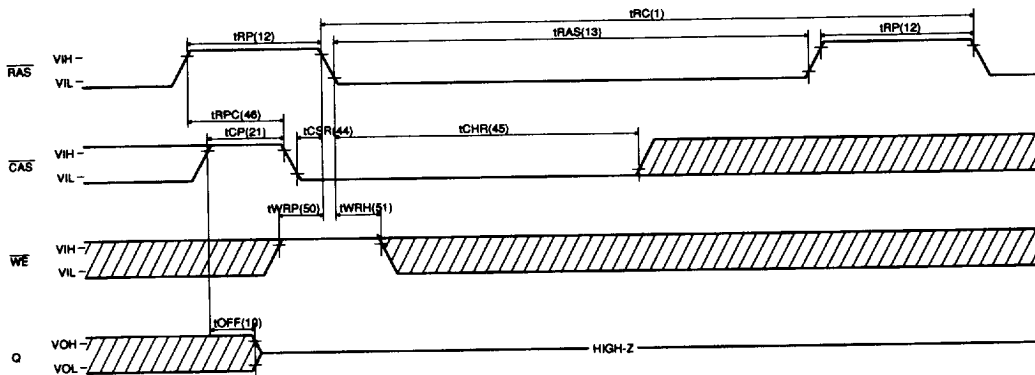


RAS-ONLY REFRESH CYCLE



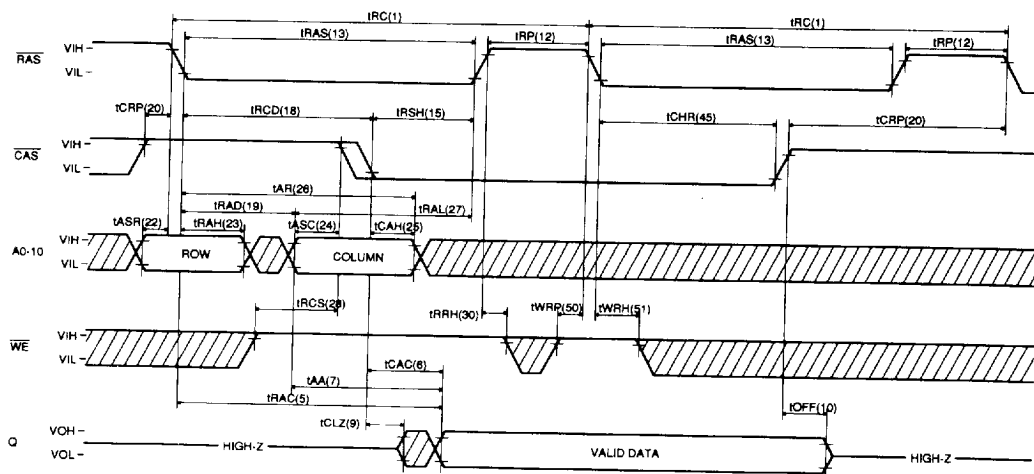
NOTE : WE="H" or "L"

CAS-BEFORE-RAS REFRESH CYCLE

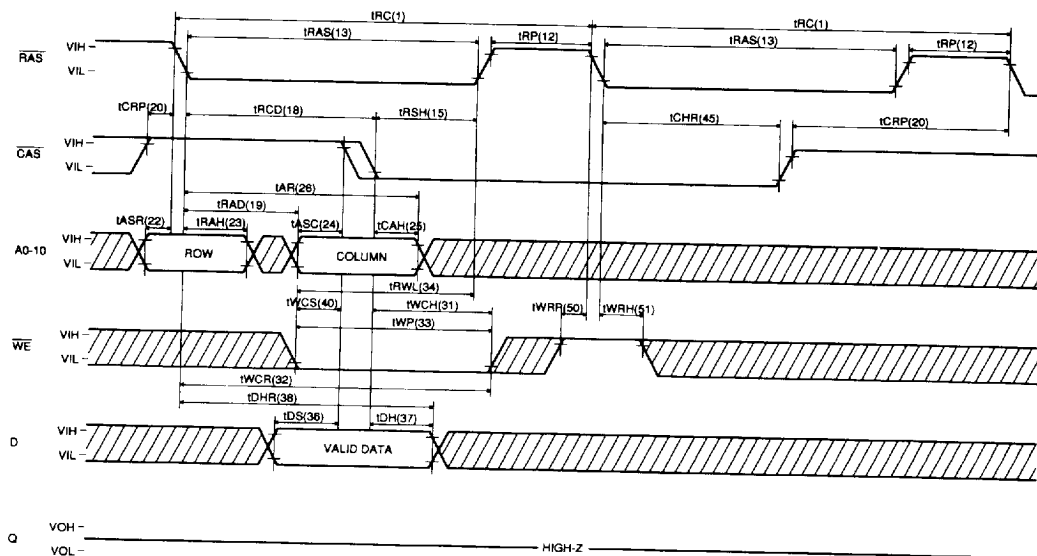


NOTE : A0-10="H" or "L"

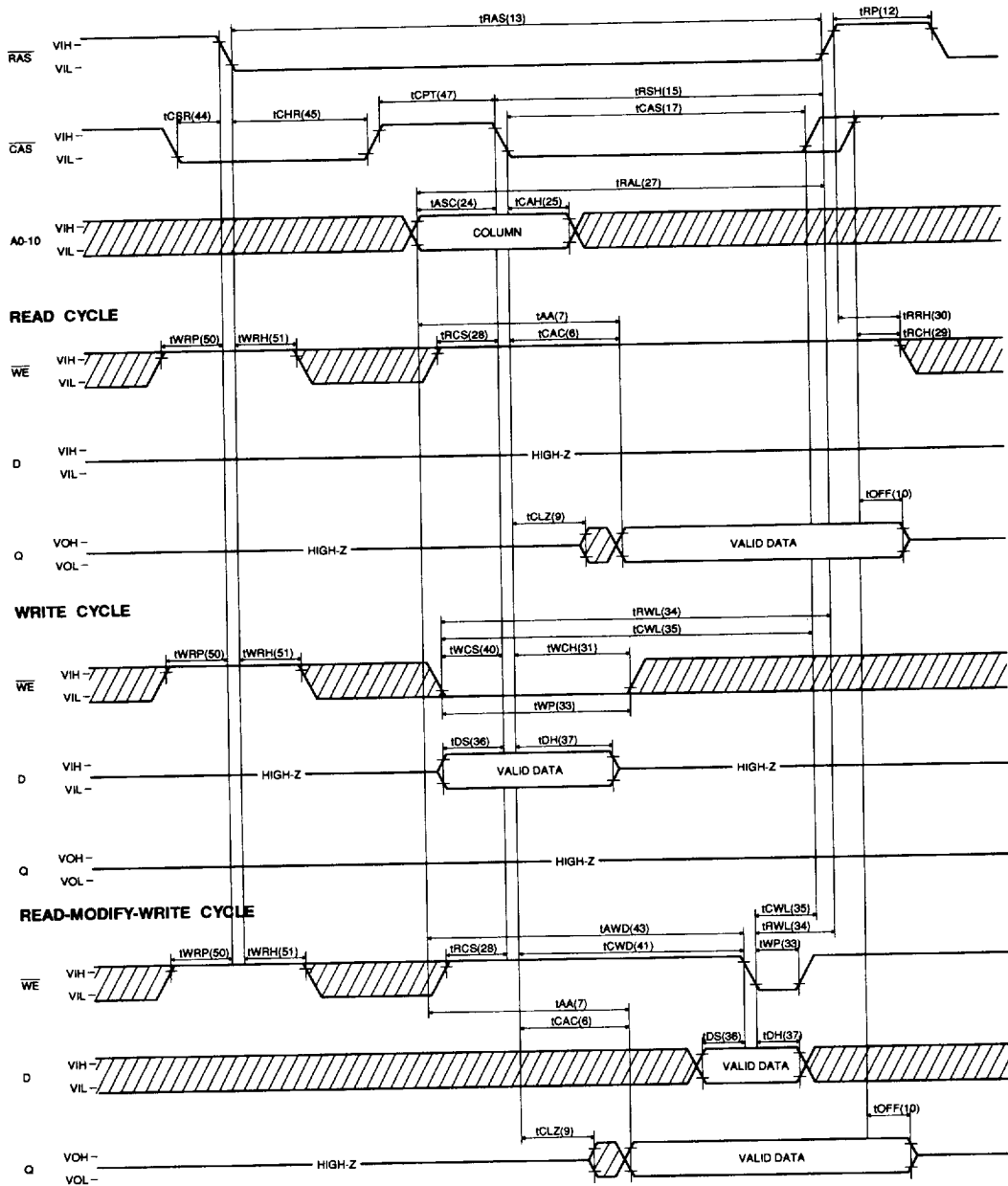
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



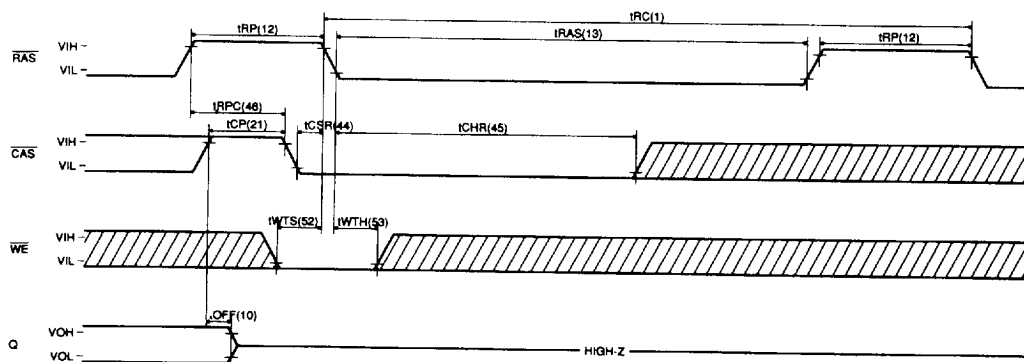
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



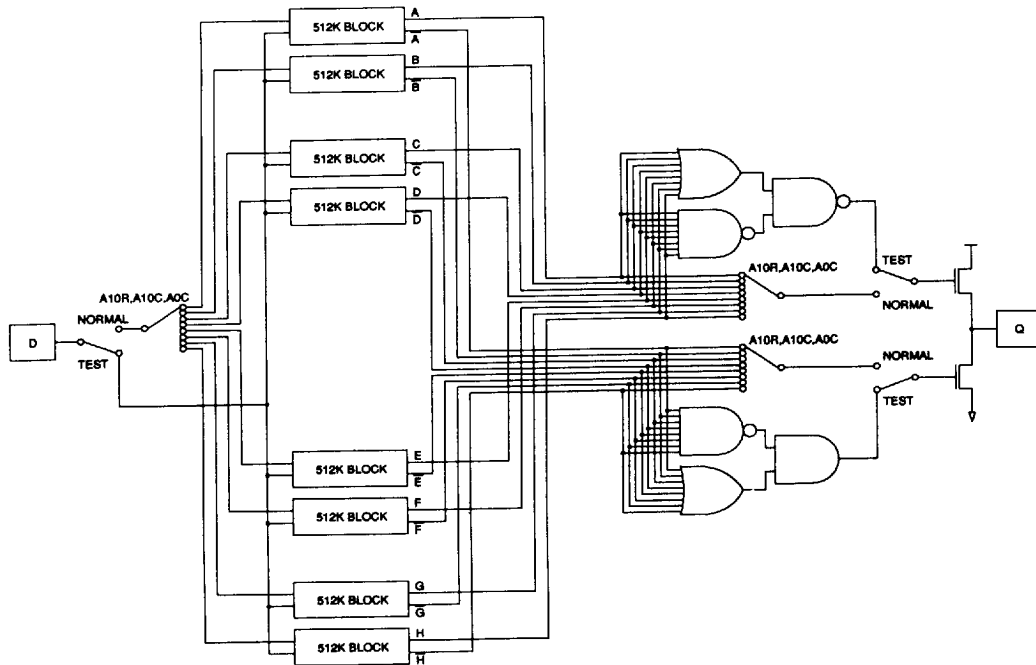
TEST MODE

The HY514100 is a DRAM organized 4,194,304 x 1-bit. It is internally organized 524,288 x 8-bit. In Test Mode, data are written into 8 sectors (Each is composed of 512K bits) in parallel and retrieved in the same way. Row address A10 and column address A0 and A10 are not used. If, upon reading, all bits are equal (all "1"s or "0"s), the Q pin indicates a "1". If they are not equal, the Q pin indicates a "0". The diagram below shows the timing of the HY514100 to enter Test Mode. In Test Mode, the 4Mx1 DRAM can be tested as if it were a 512Kx1 DRAM. **WE, CAS-before-RAS** cycle (Test Mode In Cycle) puts the HY514100 into Test Mode and **CAS-before-RAS** or **RAS-only** refresh cycle puts it back into Normal Mode. In Test Mode, **WE, CAS-before-RAS** cycle shall be used for the refresh operation. The Test Mode function reduces test time. (1/8 in case of N test pattern.)

TEST MODE IN CYCLE

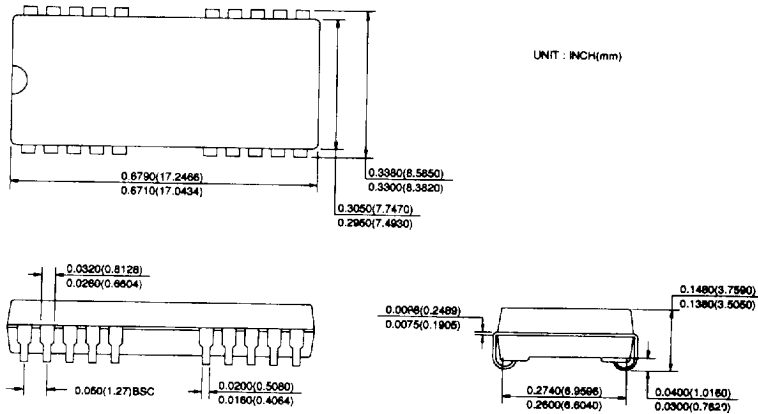


BLOCK DIAGRAM IN TEST MODE



PACKAGE INFORMATION

300 mil 20/26 pin Small Outline J-form Package (J)



ORDERING INFORMATION

PART NO	SPEED	POWER	PACKAGE
HY514100J	70/80/10		SOJ