FAIRCHILD SEMICONDUCTOR ™

March 1999

FDC6324L
Integrated Load Switch

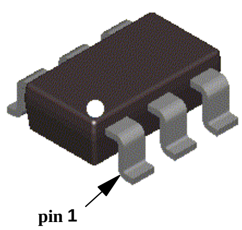
General Description

These Integrated Load Switches are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage high side load switch application where low conduction loss and ease of driving are needed.

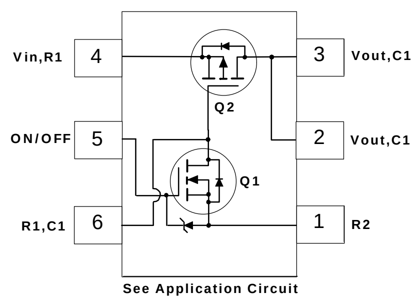
Features

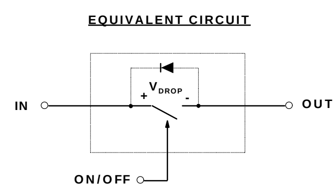
- V_{DROP}=0.2V @ V_{IN}=12V, I_L=1A, $V_{ON/OFF}$=1.5 to 8V
  V_{DROP}=0.3V @ V_{IN}=5V, I_L=1A, $V_{ON/OFF}$=1.5 to 8V.
- High density cell design for extremely low on-resistance.
- $V_{ON/OFF}$ Zener protection for ESD ruggedness. >6KV Human Body Model.
- SuperSOT™-6 package design using copper lead frame for superior thermal and electrical capabilities.

SOT-23 | SuperSOT™-6 | SuperSOT™-8 | SO-8 | SOT-223 | SOIC-16



SuperSOT ™-6





Absolute Operating Range
T_A = 25°C unless otherwise noted

Symbol	Parameter	FDC6324L	Units
V_{IN}	Input Voltage Range	3 - 20	V
$V_{ON/OFF}$	ON/OFF Voltage Range	1.5 - 8	V
I_L	Load Current @ V_{DROP}=0.5V - Continuous (Note 1)	1.5	A
	- Pulsed (Note 1 & 3)	2.5	
P_D	Maximum Power Dissipation (Note 2a)	0.7	W
T_J,T_{STG}	Operating and Storage Temperature Range	-55 to 150	°C
ESD	Electrostatic Discharge Rating MIL-STD-883D Human Body Model (100pf/1500Ohm)	6	kV
THERMAL CHARACTERISTICS			
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 2a)	180	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 2)	60	°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
I_{FL}	Forward Leakage Current	V_{IN} = 20 V, $V_{ON/OFF}$ = 0 V			1	µA
I_{RL}	Reverse Leakage Current	V_{IN} = -20 V, $V_{ON/OFF}$ = 0 V			-1	µA
ON CHARACTERISTICS (Note 3)						
V_{IN}	Input Voltage		3		20	V
$V_{ON/OFF}$	On/Off Voltage		1.5		8	V
V_{DROP}	Conduction Voltage Drop @ 1A	V_{IN} = 10 V, $V_{ON/OFF}$ = 3.3V		0.135	0.2	V
		V_{IN} = 5 V, $V_{ON/OFF}$ = 3.3 V		0.215	0.3	
I_L	Load Current	V_{DROP} = 0.2 V, V_{IN} = 10 V, $V_{ON/OFF}$ = 3.3 V	1			A
		V_{DROP} = 0.3 V, V_{IN} = 5 V, $V_{ON/OFF}$ = 3.3 V	1			

Notes:

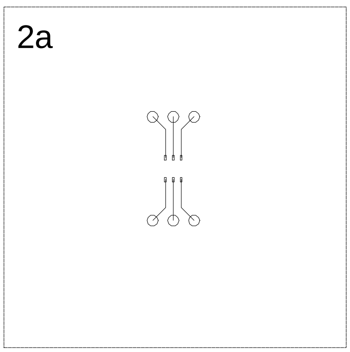
1. V_{IN}=20V, $V_{ON/OFF}$=8V, V_{DROP}=0.5V, T_A=25°C

2. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ for single device operation using the board layouts shown below on FR-4 PCB in a still air environment:

a. 180°C/W when mounted on a 2oz minimum copper pad.



Scale 1 : 1 on letter size paper

3. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%

Typical Electrical Characteristics (T_A = 25 °C unless otherwise noted)

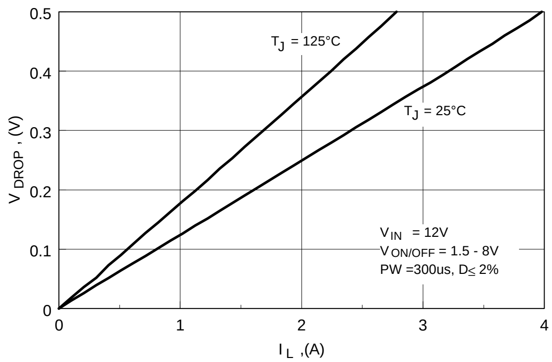


Figure 1. V_{DROP} Versus I_L at V_{IN}=12V.

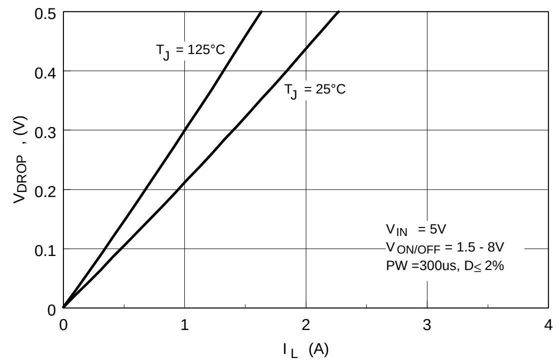


Figure 2. V_{DROP} Versus I_L at V_{IN}=5.0V.

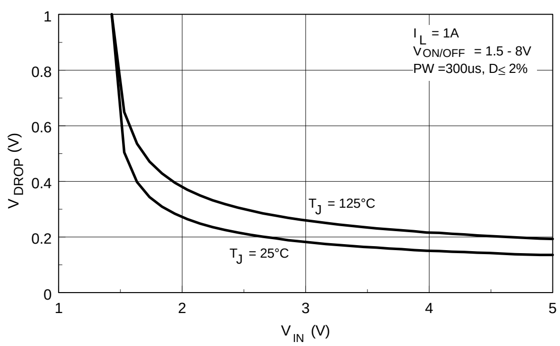


Figure 3. V_{DROP} Versus V_{IN} at I_L=1A.

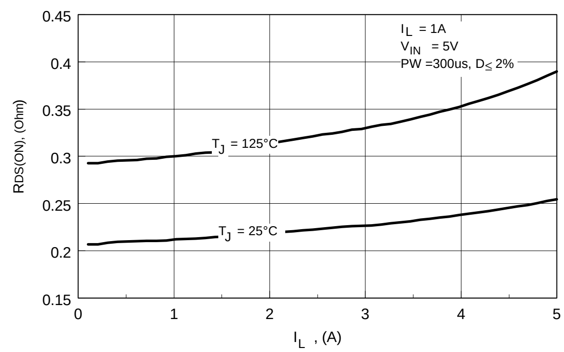


Figure 4. $R_{(ON)}$ Versus I_L at V_{IN}=5.0V.

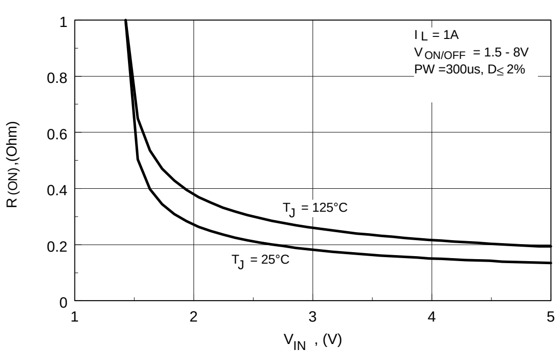


Figure 5. On Resistance Variation with Input Voltage.

Typical Electrical Characteristics (T_A = 25 ^oC unless otherwise noted)

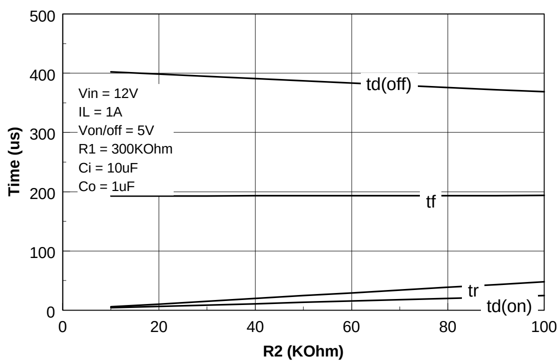


Figure 6. Switching Variation with R2 at Vin = 12V and R1 = 300KOhm.

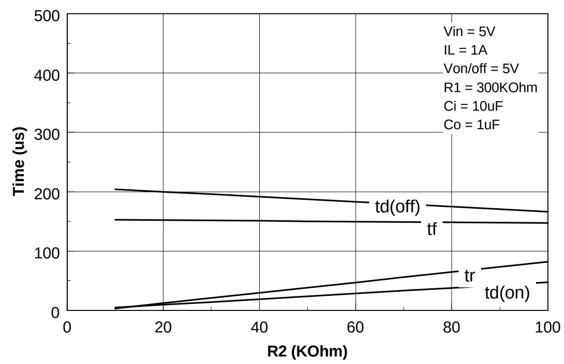


Figure 7. Switching Variation with R2 at Vin=5V and R1=300KOhm.

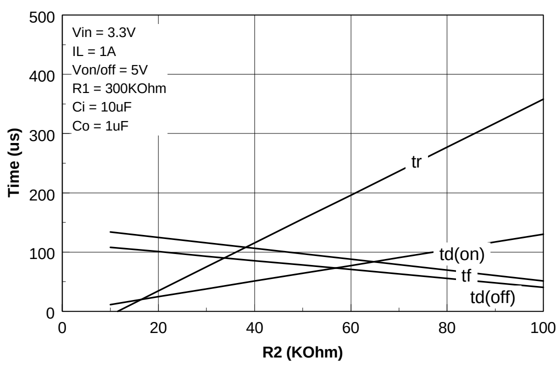


Figure 8. Switching Variation with R2 at Vin=3.3V and R1=300KOhm.

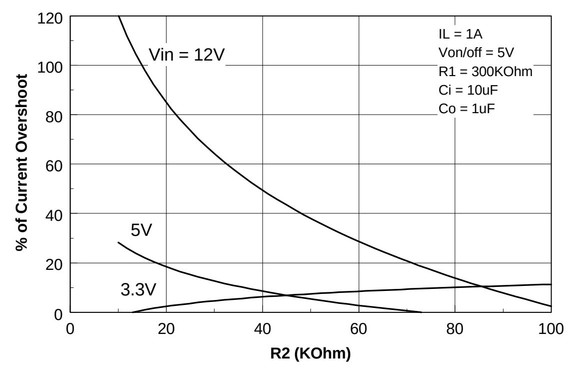


Figure 9. % of Current Overshoot Variation with Vin and R2.

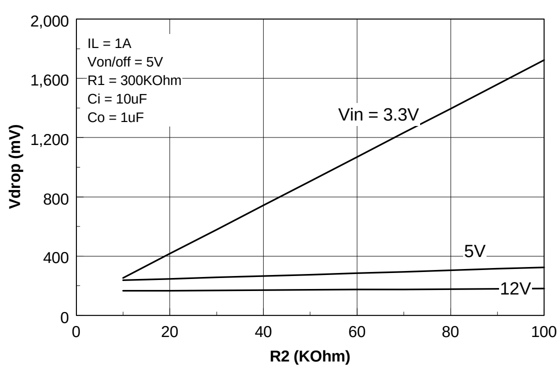


Figure 10. Vdrop Variation with Vin and R2.

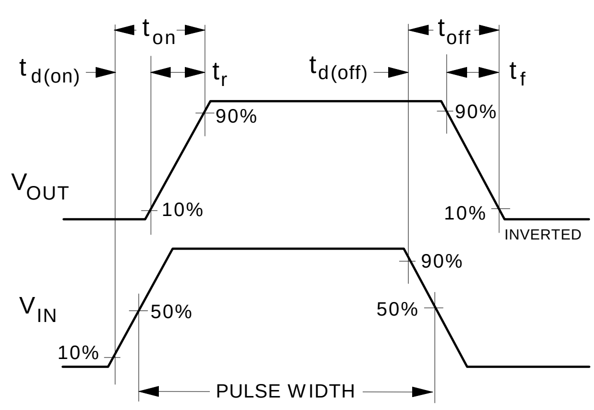


Figure 11. Switching Waveforms.

Typical Electrical Characteristics (T_A = 25 ^oC unless otherwise noted)

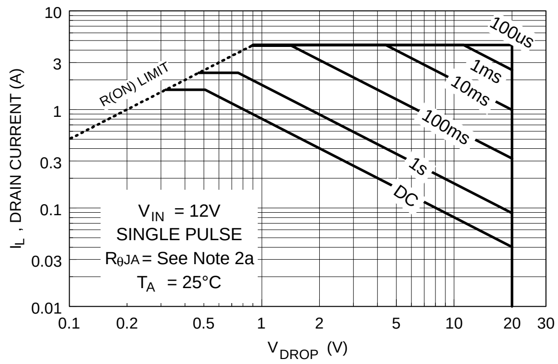


Figure 12. Safe Operating Area.

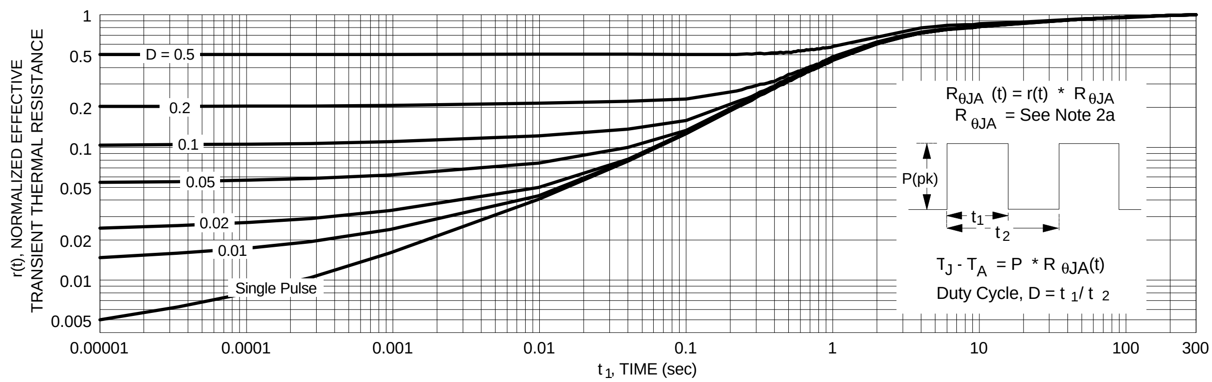
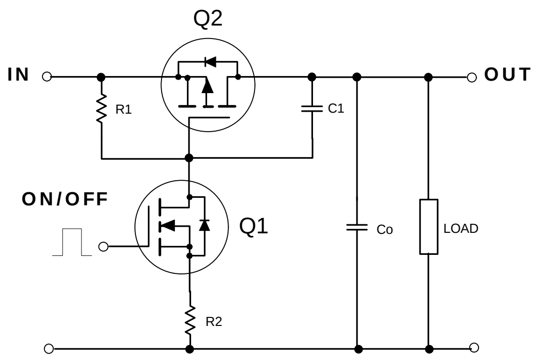


Figure 13. Transient Thermal Response Curve.

Note: Thermal characterization performed on the conditions described in Note 2a. Transient thermal response will change depends on the circuit board design.

FDC6324L Load Switch Application

APPLICATION CIRCUIT



General Description

This device is particularly suited for computer peripheral switching applications where 20V input and 1A output current capability are needed. This load switch integrates a small N-Channel Power MOSFET (Q1) which drives a large P-Channel Power MOSFET (Q2) in one tiny SuperSOT^{TM}-6 package.

A load switch is usually configured for high side switching so that the load can be isolated from the active power source. A P-Channel Power MOSFET, because it does not require its drive voltage above the input voltage, is usually more cost effective than using an N-Channel device in this particular application. A large P-Channel Power MOSFET minimizes voltage drop. By using a small N-Channel device the driving stage is simplified.

Component Values

R1	Typical	10k - 1MΩ	
R2	Typical	0 - 10kΩ	(optional)
C1	Typical	1000pF	(optional)

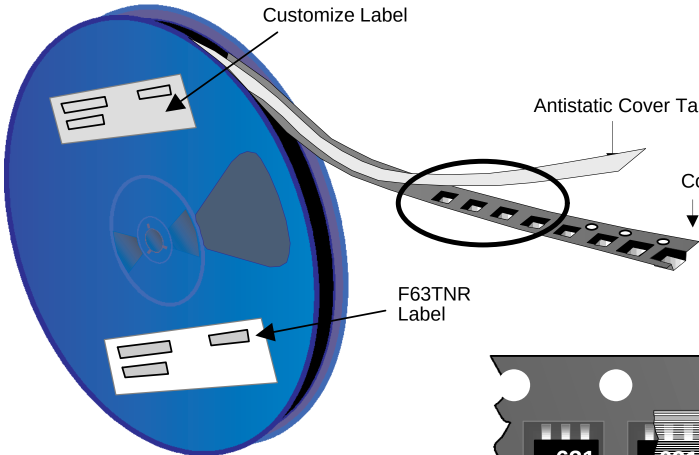
Design Notes

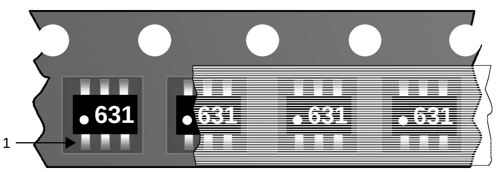
- R1 is needed to turn off Q2.
- R2 can be used to soft start the switch in the case the output capacitance Co is small.
- R2 ≤ should be at least 10 times smaller than R1 to guarantee Q1 turns on.
- By using R1 and R2 a certain amount of current is lost from the input. This bias current loss is given by the equation

  $I_{BIAS\_LOSS} = \frac{Vin}{R1 + R2}$ when the switch is ON. I_{BIAS_LOSS} can be minimized by large R1.
- R2 and C_{RSS} of Q2 make ramp for slow turn on. If excessive overshoot current occurs due to fast turn on, additional capacitance C1 can be added externally to slow down the turn on.

SuperSOT™-6 Tape and Reel Data and Package Dimensions

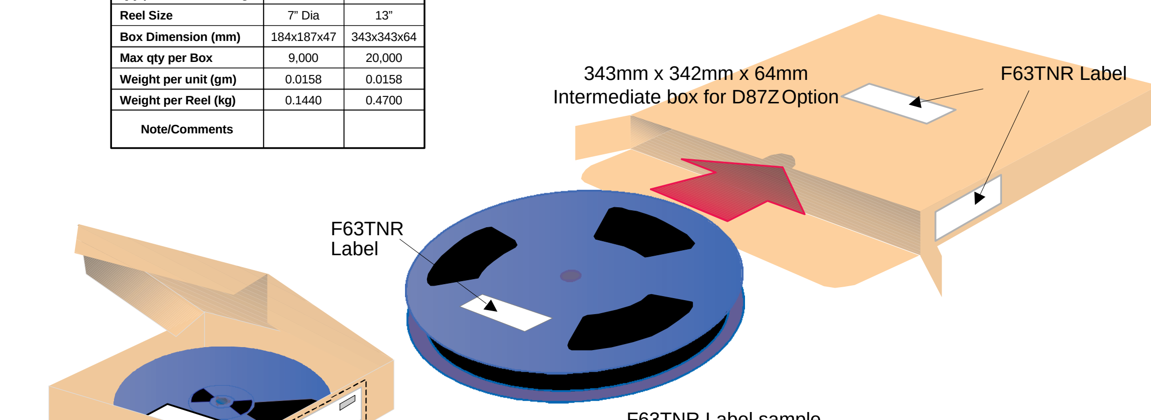
SSOT-6 Packaging
Configuration: Figure 1.0



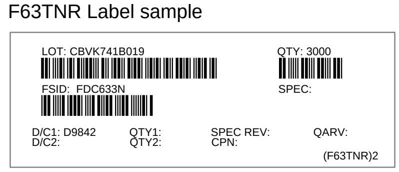


SSOT-6 Unit Orientation

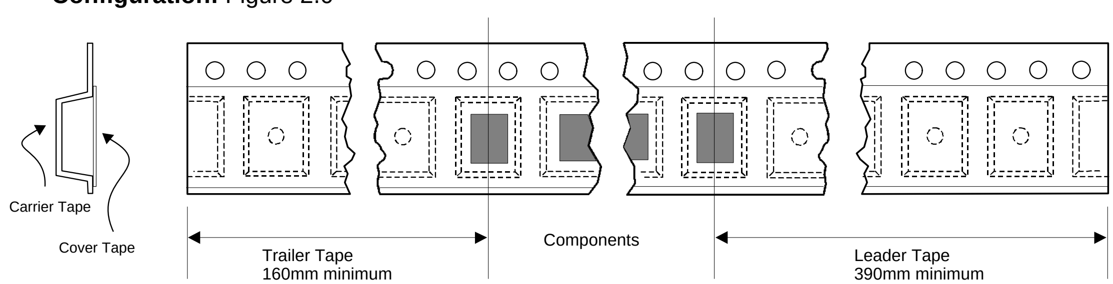
SSOT-6 Packaging Information		
Packaging Option	Standard (no flow code)	D87Z
Packaging type	TNR	TNR
Qty per Reel/Tube/Bag	3,000	10,000
Reel Size	7" Dia	13"
Box Dimension (mm)	184x187x47	343x343x64
Max qty per Box	9,000	20,000
Weight per unit (gm)	0.0158	0.0158
Weight per Reel (kg)	0.1440	0.4700
Note/Comments		



F63TNR Label sample



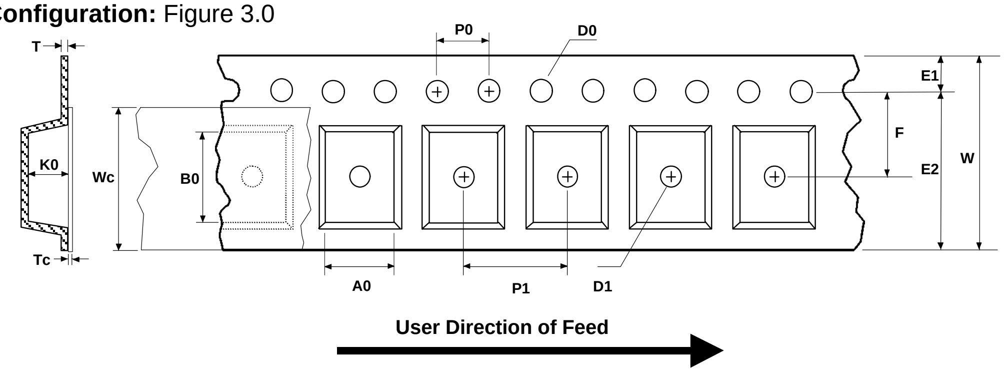
SSOT-6 Tape Leader Trailer
Configuration: Figure 2.0



SuperSOT™-6 Tape and Reel Data and Package Dimensions, continued

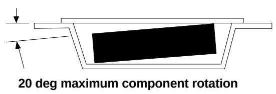
SSOT-6 Embossed Carrier Tape

Configuration: Figure 3.0

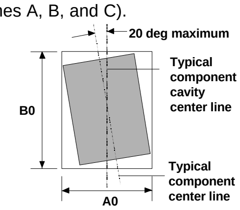


Dimensions are in millimeter													
Pkg type	**A0**	**B0**	**W**	**D0**	**D1**	**E1**	**E2**	**F**	**P1**	**P0**	**K0**	**T**	**Wc**	**Tc**
SSOT-6 (8mm)	3.23 +/-0.10	3.18 +/-0.10	8.0 +/-0.3	1.55 +/-0.05	1.00 +/-0.125	1.75 +/-0.10	6.25 min	3.50 +/-0.05	4.0 +/-0.1	4.0 +/-0.1	1.37 +/-0.10	0.255 +/-0.150	5.2 +/-0.3	0.06 +/-0.02

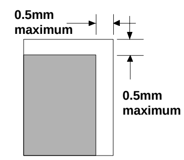
Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



Sketch A (Side or Front Sectional View)
Component Rotation

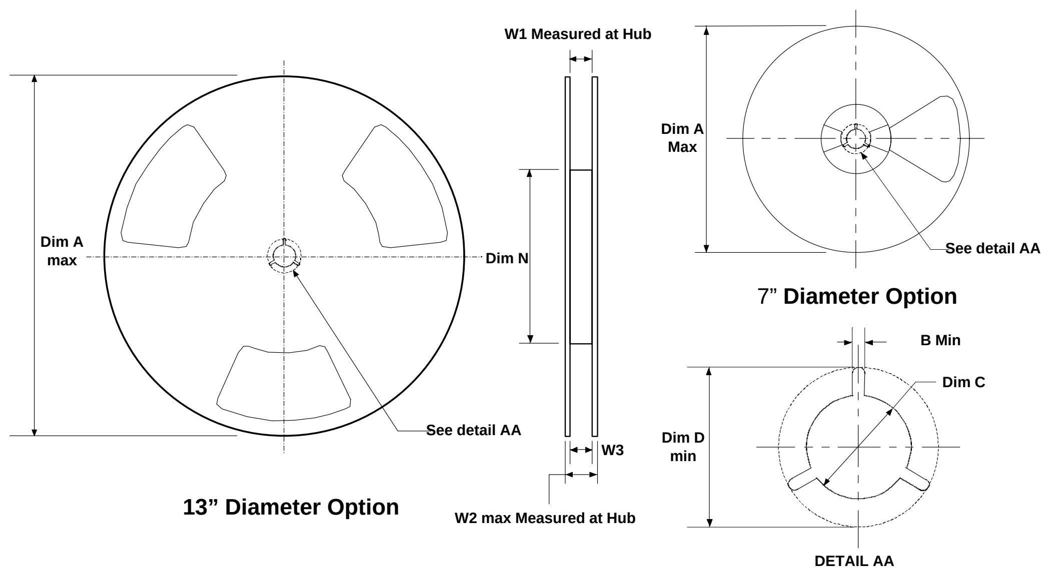


Sketch B (Top View)
Component Rotation



Sketch C (Top View)
Component lateral movement

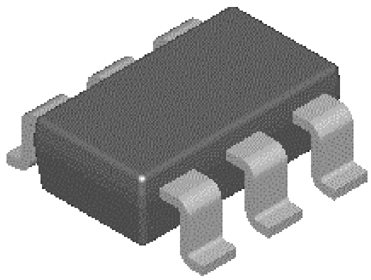
SSOT-6 Reel Configuration: Figure 4.0

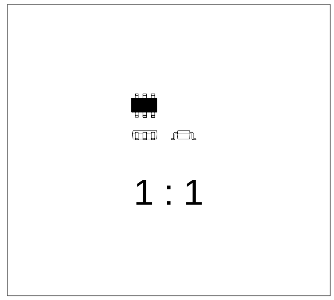


Dimensions are in inches and millimeters									
Tape Size	**Reel Option**	**Dim A**	**Dim B**	**Dim C**	**Dim D**	**Dim N**	**Dim W1**	**Dim W2**	**Dim W3 (LSL-USL)**
8mm	7" Dia	7.00 177.8	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	2.165 55	0.331 +0.059/-0.000 8.4 +1.5/0	0.567 14.4	0.311 – 0.429 7.9 – 10.9
8mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	4.00 100	0.331 +0.059/-0.000 8.4 +1.5/0	0.567 14.4	0.311 – 0.429 7.9 – 10.9

SuperSOT™-6 Tape and Reel Data and Package Dimensions, continued

SuperSOT™-6 (FS PKG Code 31, 33)

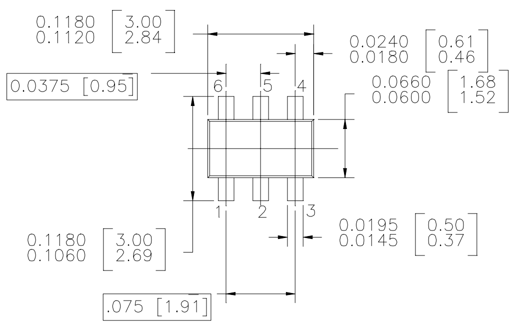


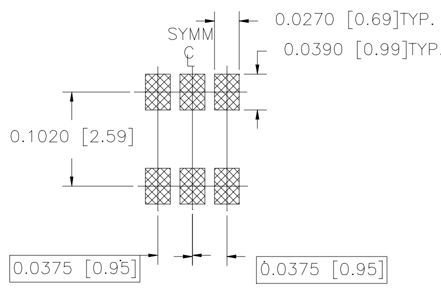


Scale 1:1 on letter size paper

Dimensions shown below are in:
inches [millimeters]

Part Weight per unit (gram): 0.0158





LAND PATTERN RECOMMENDATION

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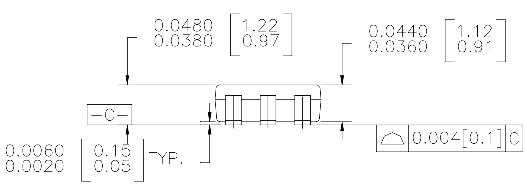

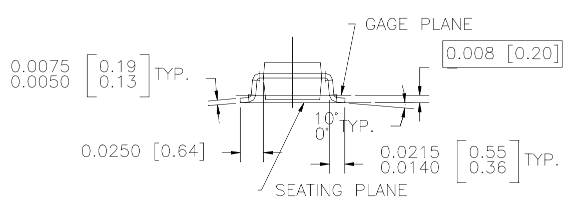

SUPER SOT 6 LEADS

NOTES : UNLESS OTHERWISE SPECIFIED

1.0 STANDARD LEAD FINISH : 150 MICROINCHES 93.81 MICROMETERS)
MINIMUM TIN / LEAD (SOLDER) ON COPPER.

2.0 NO JEDEC REGISTRATION AS OF JULY 1996

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SuperSOT™-6
SuperSOT™-8
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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.