PowerPC™

IBM

PowerPC 401x2 Embedded Cores

Optimized low-cost cores utilizing IBM Blue Logic technology*

Highlights

401 CPU

- *Compatible with PowerPC User Instruction Set Architecture*
- *84 MIPS (Dhrystone 2.1) @ 80MHz*
- *3.1 mm^2, in 0.35µ CMOS process, (.27µ L_{eff}), three levels of metal*
- *32-bit x 32 general purpose registers*
- *Hardware multiply and divide*

Cache Controllers

- *Fill-first, data forwarding*
- *Non-blocking flush operations*
- *Separate I and D controllers*

Virtual Mode MMU

- *Variable page sizes (1 KB-16 MB)*
- *64-entry fully-associative TLB*

I/O Interfaces

- *Processor local bus (PLB)*
- *Auxiliary process unit (APU)*
- *On-chip memory (OCM)*
- *Device control register (DCR)*
- *Interrupts*
- *JTAG*

Timers

- *64-bit time-base*
- *Programmable interval timer*
- *Fixed interval timer*
- *Watchdog timer*

Trace FIFO

- *Real-time non-invasive trace*
- *Exclusive traceback capability*

The Core Solution

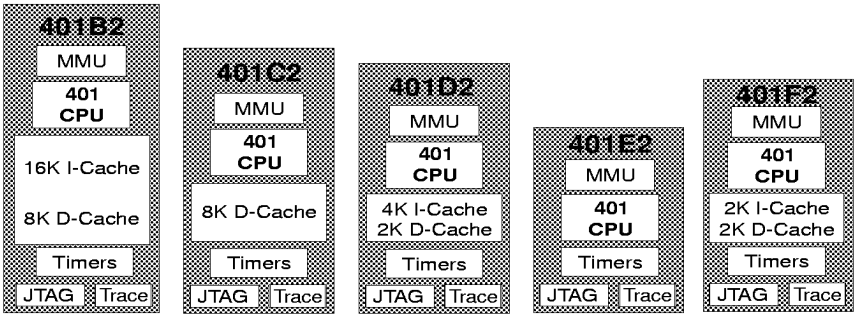
PowerPC 401x2 embedded cores (401B2, 401C2, 401D2, 401E2 and 401F2) are 32-bit RISC cores for use in custom logic applications. These embedded cores integrate a PowerPC 401 CPU, separate instruction and data caches, a JTAG port, trace FIFO, multiple timers and a memory management unit (MMU). These cores are available as hard macros in the IBM ASIC library and can be integrated with peripheral and application-specific macro cores to develop system-on-a-chip solutions. The five cores are optimized for low-cost, low-power consumer electronics, communications, and imaging applications.

The PowerPC 401 CPU is compatible with the scalable and flexible PowerPC instruction set architecture, so code written for a PowerPC 401x2 is compatible with 4xx, 6xx and 7xx PowerPC embedded processors. The PowerPC 401 CPU implements a simple 3-stage pipeline (fetch, decode, execute) in order to minimize silicon area, thus optimizing system-on-a-chip designs for low cost.

For optimal performance and cost-control, the PowerPC 401x2 cores integrate tightly coupled features to the 401 CPU. The cache controllers use sophisticated design techniques typically found in high-performance devices. The MMU implementation is optimal for low-cost embedded applications due to its small size and flexibility. JTAG and trace FIFO ports enable robust debug capabilities, even in complex system-on-a-chip designs.

PowerPC 401x2 embedded cores are supported by the PowerPC Embedded Tools* Program. In this program, IBM and over 75 select third-party vendors offer a full range of embedded system development tools. Available tools include compilers, debuggers, real-time operating systems and logic analyzers.

Full-function simulation models are available to support all SWIFT compliant VHDL and Verilog simulation environments.



PowerPC 401x2 Embedded Cores

Specifications	401B2	401C2	401D2	401E2	401F2
Technology	.35µ CMOS (.27µ L_{eff})	.35µ CMOS (.27µ L_{eff})	.35µ CMOS (.27µ L_{eff})	.35µ CMOS (.27µ L_{eff})	.35µ CMOS (.27µ L_{eff})
Frequency (MHz)	0 to 80[WC] 110[TC]	0 to 80[WC] 110[TC]	0 to 80[WC] 110[TC]	0 to 80[WC] 110[TC]	0 to 80[WC] 110[TC]
Power Dissipation (80 MHz, 3.3V, 55° C)	260mW	190mW	180mW	160mW	170mW
Voltage	3.3V	3.3V	3.3V	3.3V	3.3V
I-Cache	16K	0K	4K	0K	2K
D-Cache	8K	8K	2K	0K	2K
MMU	Y	Y	Y	Y	Y
Timers	Y	Y	Y	Y	Y
JTAG	Y	Y	Y	Y	Y
Trace FIFO	Y	Y	Y	Y	Y

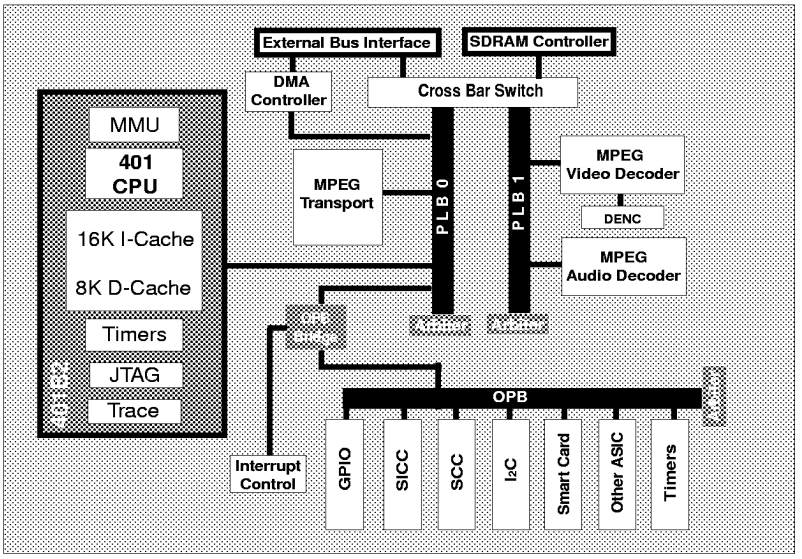
[WC] Worst case conditions (3.0V, 85° C, slow silicon)

[TC] Typical conditions (3.3V, 55° C, nominal silicon)

401x2 Core Integration

Through the IBM Blue Logic Core Program, PowerPC 401x2 CPU cores integrate on-chip with other reusable peripheral and application-specific cores. High speed, high bandwidth peripherals, such as the embedded controller cores, directly attach to the processor local bus (PLB). Less performance-critical cores attach to the on-chip peripheral bus (OPB). Toolkits are available to assist designing ASICs to the OPB/PLB standard.

For more information on IBM Microelectronics core offerings, view the ever expanding core library on the WWW at http://www.chips.ibm.com/products/asics/ or contact your local IBM Microelectronics sales office.



Example 401B2 Core-Based Digital Video Application

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