Revision History

No.	History	Draft Date	Remark
0.1	Defined Target Spec.	May. 2004	
	Corrected Pin assignment table	July 2004	

DESCRIPTION

Hynix HYMP112R72(L)8 series is registered 240-pin double data rate 2 Synchronous DRAM Dual In-Line Memory Modules(DIMMs) which are organized as 128Mx72 high-speed memory arrays. Hynix HYMP112R72(L)8 series consists of nine 128Mx8 DDR2 SDRAMs in 68 ball FBGA chipsize packages. Hynix HYMP112R72(L)8 series provide a high performance 8-byte interface in 133.35mm width form factor of industry stanard. It is suitable for easy interchange and addition. Hynix HYM112R72(L)8 series is designed for high speed and offers fully synchronous operations referenced to both rising and falling edges of differential clock inputs. While all addresses and control inputs are latched on the rising edges of the clock, Data, Data strobes and Write data masks inputs are sampled on both rising and falling edges of it. The data paths are internally pipelined and 4-bit prefetched to achieve very high bandwidth. All input and output voltage levels are compatible with SSTL_1.8. High speed frequencies, programmable latencies and burst lengths allow variety of device operation in high performance memory system.

Hynix HYMP112R72(L)8 series incorporates SPD(serial presence detect). Serial presence detect function is implemented via a serial 2,048-bit EEPROM. The first 128 bytes of serial PD data are programmed by Hynix to identify DIMM type, capacity and other the information of DIMM and the last 128 bytes are available to the customer.

FEATURES

- 1GB (128M x 72) Registered DDR2 DIMM based on 128Mx8 DDR2 SDRAM
- JEDEC standard Double Data Rate2 Synchronous DRAMs (DDR2 SDRAMs) with 1.8V +/- 0.1V Power Supply
- JEDEC Standard 240-pin dual in-line memory module (DIMM)
- Error Check Correction (ECC) Capability
- All inputs and outputs are compatible with SSTL_1.8 interface
- OCD (Off-Chip Driver Impedance Adjustment) and ODT (On-Die Termination)
- Fully differential clock operations (CK & /CK)
- Programmable CAS Latency 3 / 4 /5 supported
- Programmable Burst Length 4 / 8 with both sequential and interleave mode
- All inputs and outputs SSTL_1.8 compatible
- Auto refresh and self refresh supported
- 7.8us refresh period at Lower than T_{CASE} 85℃, 3.9us(85 ℃ < T_{CASE} ≤ 95℃)
- Serial Presence Detect(SPD) with EEPROM
- DDR2 SDRAM Package: 68ball FBGA

ORDERING INFORMATION

Type	Part No.	Description	CL-tRCD-tRP	Form Factor
PC2-3200 (DDR2-400)	HYMP112R72(L)8-E4	one rank 1GB Reg. DIMM	4-4-4	240pin Registered DIMM 133.35 mm x 30,00 mm (MO-237)
	HYMP112R72(L)8-E3		3-3-3	
PC2-4300 (DDR2-533)	HYMP112R72(L)8-C5		5-5-5	
	HYMP112R72(L)8-C4		4-4-4	
PC2-5300 (DDR2-667)	HYMP112R72(L)8-Y6		6-6-6	
	HYMP112R72(L)8-Y5		5-5-5	

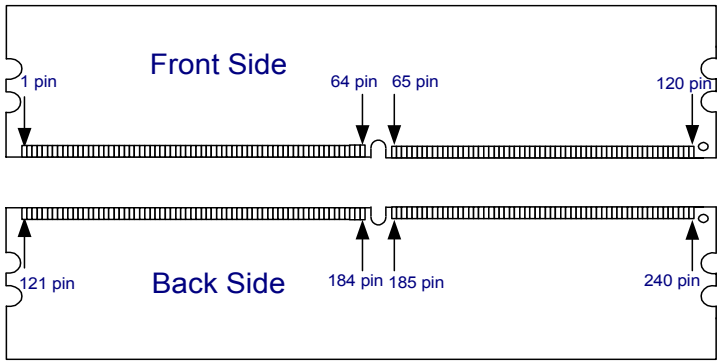
Input/Output Functional Description

Symbol	Type	Polarity	Pin Description
CK0~CK1	IN	Positive Edge	Positive line of the differential pair of system clock inputs that drives input to the on-DIMM PLL.
$\overline{CK0}$~$\overline{CK1}$	IN	Negative Edge	Negative line of the differential pair of system clock inputs that drives input to the on-DIMM PLL.
CKE0~CKE1	IN	Active High	Activates the DDR2 SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode or the Self Refresh mode.
$\overline{S0}$~$\overline{S1}$	IN	Active Low	Enables the associated DDR2 SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. Rank 0 is selected by $\overline{S0}$; Rank 1 is selected by $\overline{S1}$
ODT0~ODT1	IN	Active High	On-Die Termination signals.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	IN	Active Low	When sampled at the positive rising edge of the clock. $\overline{RAS}$,$\overline{CAS}$ and $\overline{WE}$(ALONG WITH S) define the command being entered.
Vref	Supply		Reference voltage for SSTL18 inputs
V_{DDQ}	Supply		Power supplies for the DDR2 SDRAM output buffers to provide improved noise immunity. For all current DDR2 unbuffered DIMM designs, V_{DDQ} shares the same power plane as V_{DD} pins.
BA0~BA2	IN	-	Selects which DDR2 SDRAM internal bank of eight is activated.
A0~A9, A10/AP A11~A13	IN	-	During a Bank Activate command cycle, Address input difines the row address(RA0~RA13) During a Read or Write command cycle, Address input defines the column address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high., autoprecharge is selected and BA0-BAn defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle., AP is used in conjunction with BA0-BAn to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0-BAn inputs. If AP is low, then BA0-BAn are used to define which bank to precharge.
DQ0~DQ63, CB0~CB7	IN	-	Data and Check Bit Input/Output pins.
DM0~DM8	IN	Active High	DM is an input mask signal for write data. Input data is masked when DM is sampled High coincident with that input data during a write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading.
V_{DD},V_{SS}	Supply		Power and ground for the DDR2 SDRAM input buffers, and core logic. V_{DD} and V_{DDQ} pins are tied to V_{DD}/V_{DDQ} planes on these modules.
DQS0~ DQS17	I/O	Positive Edge	Positive line of the differential data strobe for input and output data
$\overline{DQS0}$~ $\overline{DQS17}$	I/O	Negative Edge	Negative line of the differential data strobe for input and output data
SA0~SA1	IN	-	These signals are tied at the system planar to either V_{SS} or V_{DDSPD} to configure the serial SPD EEPROM address range.
SDA	I/O	-	This is a bidirectional pin used to transfer data into or out of the SPD EEPROM. A resister may be connected from the SDA bus line to V_{DDSPD} on the system planar to act as a pull up.
SCL	IN	-	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from SCL to V_{DDSPD} to act as a pull up on the system board.
VDDSPD	Supply		Power supply for SPD EEPROM. This supply is separate from the VDD/VDDQ power plane. EEPROM supply is operable from 1.7V to 3.6V.
RESET	IN		The RESET pin is connected to the RST pin on the register and to the OE pin on the PLL. When low, all register outputs will be driven low and the PLL clocks to the DRAMs and register(s) will be set to low level (the PLL will remain synchronized with the input clock)
Par_In	IN		Parity bit for the Address and Control bus(“1”. Odd, “0”.Even)
Err_Out	OUT		Parity error found in the Address and Control bus
TEST			Used by memory bus analysis tools(unused on memory DIMMs)

PIN DESCRIPTION

Pin	Pin Description	Pin	Pin Description
CK0	Clock Input,positive line	ODT[1:0]	On Die Termination Inputs
$\overline{CK0}$	Clock input,negative line	VDDQ	DQs Power Supply
CKE0~CKE1	Clock Enable Input	DQ0~DQ63	Data Input/Output
$\overline{RAS}$	Row Address Strobe	CB0~CB7	Data check bits Input/Output
$\overline{CAS}$	Column Address Strobe	DQS(0~8)	Data strobes
$\overline{WE}$	Write Enable	DQS(0~8)	Data strobes,negative line
$\overline{S0}$	Chip Select Input	DM(0~8),DQS(9~17)	Data Maskes/Data strobes
A0~A9,A11~A13	Address input	DQS(9~17)	Data strobes,negative line
A10/AP	Address input/Autoprecharge	RFU	Reserved for Future Use
BA0-BA2	SDRAM Bank Address	NC	No Connect
SCL	Serial Presence Detect(SPD) Clock Input	TEST	Memory bus test tool(Not Connected and Not Useable on DIMMs)
SDA	SPD Data Input/Output	VDD	Core Power
SA0~SA2	E^2PROM Address Inputs	VDDQ	I/O Power Supply
Par_In	Parity bit for the Address and Con-trol bus	VSS	Ground
$\overline{Err\_Out}$	Parity error found on the Addre	VREF	Reference Power Supply
$\overline{RESET}$	Reset Enable	VDDSPD	Power Supply for SPD
CB0~CB7	Data Strobe Inputs/Outputs		

PIN Location



PIN ASSIGNMENT

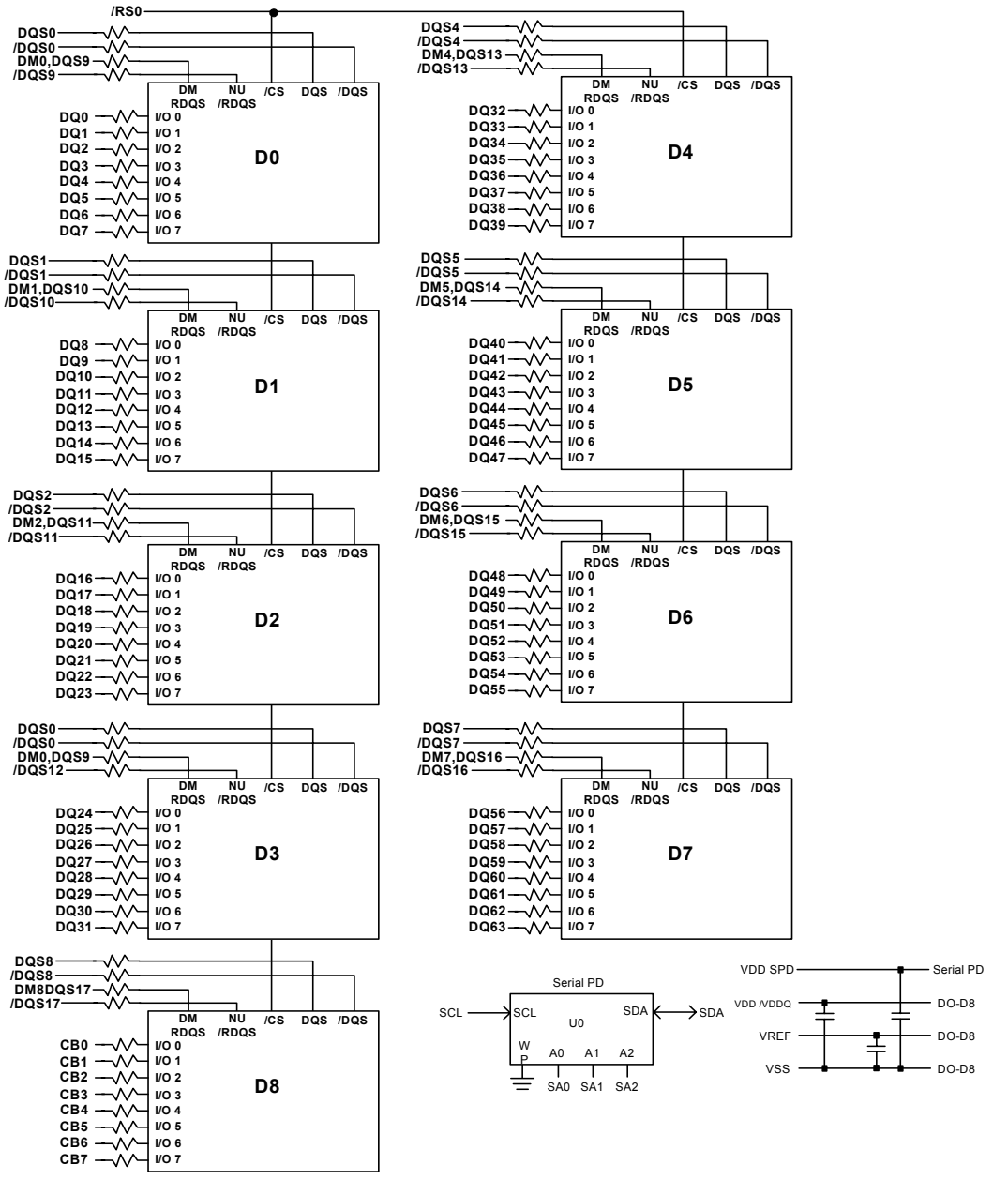
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VREF	41	VSS	81	DQ33	121	VSS	161	CB4	201	VSS
2	VSS	42	CB0	82	VSS	122	DQ4	162	CB5	202	DM4/DQS13
3	DQ0	43	CB1	83	$\overline{DQS}$4	123	DQ5	163	VSS	203	$\overline{DQS}$13
4	DQ1	44	VSS	84	DQS4	124	VSS	164	DM8,DQS17	204	VSS
5	VSS	45	$\overline{DQS}$8	85	VSS	125	DM0/DQS9	165	$\overline{DQS}$17	205	DQ38
6	$\overline{DQS}$0	46	DQS8	86	DQ34	126	$\overline{DQS}$9	166	VSS	206	DQ39
7	DQS0	47	VSS	87	DQ35	127	VSS	167	CB6	207	VSS
8	VSS	48	CB2	88	VSS	128	DQ6	168	CB7	208	DQ44
9	DQ2	49	CB3	89	DQ40	129	DQ7	169	VSS	209	DQ45
10	DQ3	50	VSS	90	DQ41	130	VSS	170	VDDQ	210	VSS
11	VSS	51	VDDQ	91	VSS	131	DQ12	171	NC,CKE1	211	DM5/DQS14
12	DQ8	52	CKE0	92	$\overline{DQS}$5	132	DQ13	172	VDD	212	$\overline{DQS}$14
13	DQ9	53	VDD	93	DQS5	133	VSS	173	A15,NC	213	VSS
14	VSS	54	BA2,NC	94	VSS	134	DM1/DQS10	174	A14,NC	214	DQ46
15	$\overline{DQS}$1	55	NC,$\overline{Err_Out}$	95	DQ42	135	$\overline{DQS}$10	175	VDDQ	215	DQ47
16	DQS1	56	VDDQ	96	DQ43	136	VSS	176	A12	216	VSS
17	VSS	57	A11	97	VSS	137	RFU	177	A9	217	DQ52
18	$\overline{RESET}$	58	A7	98	DQ48	138	RFU	178	VDD	218	DQ53
19	NC	59	VDD	99	DQ49	139	$\overline{VSS}$	179	A8	219	VSS
20	VSS	60	A5	100	VSS	140	DQ14	180	A6	220	RFU
21	DQ10	61	A4	101	SA2	141	DQ15	181	VDDQ	221	RFU
22	DQ11	62	VDDQ	102	NC(TEST)	142	VSS	182	A3	222	VSS
23	VSS	63	A2	103	VSS	143	DQ20	183	A1	223	DM6/DQS15
24	DQ16	64	VDD	104	$\overline{DQS}$6	144	DQ21	184	VDD	224	NC,$\overline{DQS}$15
25	DQ17	Key		105	DQS6	145	VSS	Key		225	VSS
26	VSS	65	VSS	106	VSS	146	DM2/DQS11	185	CK0	226	DQ54
27	$\overline{DQS}$2	66	VSS	107	DQ50	147	$\overline{DQS}$11	186	$\overline{CK}$0	227	DQ55
28	DQS2	67	VDD	108	DQ51	148	VSS	187	VDD	228	VSS
29	VSS	68	NC,$\overline{Err\_Out}$	109	VSS	149	DQ22	188	A0	229	DQ60
30	DQ18	69	VDD	110	DQ56	150	DQ23	189	VDD	230	DQ61
31	DQ19	70	A10/AP	111	DQ57	151	VSS	190	BA1	231	VSS
32	VSS	71	BA0	112	VSS	152	DQ28	191	VDDQ	232	DM7/DQS16
33	DQ24	72	VDDQ	113	$\overline{DQS}$7	153	DQ29	192	$\overline{RAS}$	233	NC,$\overline{DQS}$16
34	DQ25	73	$\overline{WE}$	114	DQS7	154	VSS	193	$\overline{S}$0	234	VSS
35	VSS	74	$\overline{CAS}$	115	VSS	155	DM3/DQS12	194	VDDQ	235	DQ62
36	$\overline{DQS}$3	75	VDDQ	116	DQ58	156	$\overline{DQS}$12	195	ODT0	236	DQ63
37	DQS3	76	NC, $\overline{S}$1	117	DQ59	157	VSS	196	A13,NC	237	VSS
38	VSS	77	NC, ODT1	118	VSS	158	DQ30	197	VDD	238	VDDSPD
39	DQ26	78	VDDQ	119	SDA	159	DQ31	198	VSS	239	SA0
40	DQ27	79	VSS	120	SCL	160	VSS	199	DQ36	240	SA1
		80	DQ32					200	DQ37		

NC= No Connect, RFU= Reserved for Future Use.

Note:

1. RESET(Pin 18) is connected to both OE of PLL and Reset of register.
2. NC/Err_out (Pin 55) and NC/Par_In(Pin68) are for optional function to check address and command parity.
3. The Test pin(Pin 102) is reserved for bus analysis probes and is not connected on normal memory modules(DIMMs)

FUNCTIONAL BLOCK DIAGRAM



* : /S0 connects to D/CS and VDD connects to /CSR on register.

Notes :

1. DQ to I/O wiring may be changed within a byte.
2. Unless otherwise noted, register valutes are 22 Ohms.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit	Note
Operating temperature(ambient)	T_{OPR}	0 ~ +55	°C	1
DRAM Component Case Temperature Range	TCASE	0 ~+95	°C	2
Operating Humidity(relative)	H_{OPR}	10 to 90	%	1
Storage Temperature	TSTG	-50 ~ +100	°C	1
Storage Humidity(without condensation)	H_{STG}	5 to 95	°C	1
Barometric Pressure(operating & storage)	P_{BAR}	105 to 69	K Pascal	1,3

Note :

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Expousure to absolute maximum rating conditions for extended periods may affect reliablility.
2. If the DRAM case temperature is Above 85°C, the Auto-Refresh command interval has to be reduced to tREFI=3.9μs.
   For Measurement conditions of T_{CASE}, please refer to the JEDEC document JESD51-2.
3. Up to 9850 ft.

Operating Condtions(AC&DC)

DC OPERATING CONDITIONS (SSTL_1.8)

Parameter	Symbol	Min	Max	Unit	Note
Power Supply Voltage	VDD	1.7	1.9	V	
	VDDQ	1.7	1.9	V	1
Input Reference Voltage	VREF	0.49 x VDDQ	0.51 x VDDQ	V	2
EEPROM Supply Voltage	VDDSPD	1.7	3.6	V	
Termination Voltage	VTT	VREF-0.04	VREF+0.04	V	3

Note :

1.V_{DDQ} must be less than or equal to V_{DD}.
2. Peak to peak ac noise on V_{REF} may not exeed +/-2% V_{REF}(dc)
3. VTT of transmitting device must track VREF of receiving device.

Input DC Logic Level

Parameter	Symbol	Min	Max	Unit	Note
Input High Voltage	VIH(DC)	VREF + 0.125	VDDQ + 0.3	V	
Input Low Voltage	VIL(DC)	-0.30	VREF - 0.125	V	

Input AC Logic Level

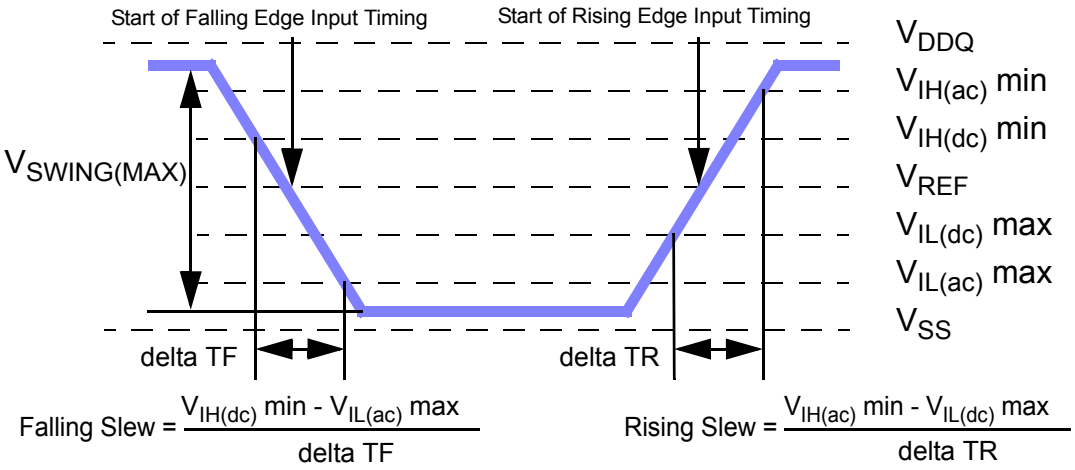
Parameter	Symbol	Min	Max	Unit	Note
AC Input logic High	VIH(AC)	VREF + 0.250	-	V	
AC Input logic Low	VIL(AC)	-	VREF - 0.250	V	

AC Input Test Conditions

Symbol	Condition	Value	Units	Notes
V_{REF}	Input reference voltage	0.5 * V_{DDQ}	V	1
$V_{SWING(MAX)}$	Input signal maximum peak to peak swing	1.0	V	1
SLEW	Input signal minimum slew rate	1.0	V/ns	2, 3

Note:

1. Input waveform timing is referenced to the input signal crossing through the V_{REF} level applied to the device under test.
2. The input signal minimum slew rate is to be maintained over the range from $V_{IL(dc)}$ max to $V_{IH(ac)}$ min for rising edges and the range from $V_{IH(dc)}$ min to $V_{IL(ac)}$ max for falling edges as shown in the below figure.
3. AC timings are referenced with input waveforms switching from VIL(ac) to VIH(ac) on the positive transitions and VIH(ac) to VIL(ac) on the negative transitions.



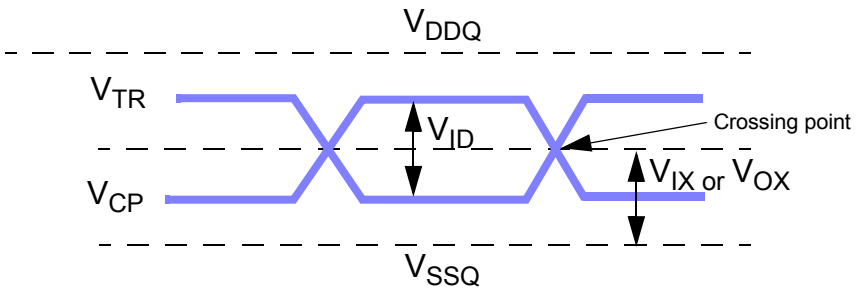
< Figure : AC Input Test Signal Waveform >

Differential Input AC logic Level

Symbol	Parameter	Min.	Max.	Units	Notes
V_{ID} (ac)	ac differential input voltage	0.5	VDDQ + 0.6	V	1
V_{IX} (ac)	ac differential cross point voltage	0.5 * VDDQ - 0.175	0.5 * VDDQ + 0.175	V	2

Note:

1. $V_{IN(DC)}$ specifies the allowable DC execution of each input of differential pair such as CK, $\overline{CK}$, DQS, $\overline{DQS}$, LDQS, $\overline{LDQS}$, UDQS and $\overline{UDQS}$.
2. $V_{ID(DC)}$ specifies the input differential voltage $|V_{TR} - V_{CP}|$ required for switching, where V_{TR} is the true input (such as CK, DQS, LDQS or UDQS) level and V_{CP} is the complementary input (such as $\overline{CK}$, $\overline{DQS}$, $\overline{LDQS}$ or $\overline{UDQS}$) level. The minimum value is equal to $V_{IH(DC)} - V_{IL(DC)}$.



< Differential signal levels >

Note:

1. $V_{ID(AC)}$ specifies the input differential voltage $|V_{TR} - V_{CP}|$ required for switching, where V_{TR} is the true input signal (such as CK, DQS, LDQS or UDQS) and V_{CP} is the complementary input signal (such as $\overline{CK}$, $\overline{DQS}$, $\overline{LDQS}$ or $\overline{UDQS}$). The minimum value is equal to $V_{IH(AC)} - V_{IL(AC)}$.
2. The typical value of $V_{IX(AC)}$ is expected to be about 0.5 * VDDQ of the transmitting device and $V_{IX(AC)}$ is expected to track variations in VDDQ . $V_{IX(AC)}$ indicates the voltage at whitch differential input signals must cross.

Differential AC output parameters

Symbol	Parameter	Min.	Max.	Units	Notes
V_{OX} (ac)	ac differential cross point voltage	0.5 * VDDQ - 0.125	0.5 * VDDQ + 0.125	V	1

Note:

1. The typical value of $V_{OX(AC)}$ is expected to be about 0.5 * V DDQ of the transmitting device and $V_{OX(AC)}$ is expected to track variations in VDDQ . $V_{OX(AC)}$ indicates the voltage at whitch differential output signals must cross.

Output Buffer Levels

Output AC Test Conditions

Symbol	Parameter	SSTL_18 Class II	Units	Notes
V_{OH}	Minimum Required Output Pull-up under AC Test Load	V_{TT} + 0.603	V	
V_{OL}	Maximum Required Output Pull-down under AC Test Load	V_{TT} - 0.603	V	
V_{OTR}	Output Timing Measurement Reference Level	0.5 * V_{DDQ}	V	1

1. The VDDQ of the device under test is referenced.

Output DC Current Drive

Symbol	Parameter	SSTI_18 Class II	Units	Notes
$I_{OH(dc)}$	Output Minimum Source DC Current	- 13.4	mA	1, 3, 4
$I_{OL(dc)}$	Output Minimum Sink DC Current	13.4	mA	2, 3, 4

1. V_{DDQ} = 1.7 V; V_{OUT} = 1420 mV. (V_{OUT} - V_{DDQ})/I_{OH} must be less than 21 ohm for values of V_{OUT} between V_{DDQ} and V_{DDQ} - 280 mV.
2. V_{DDQ} = 1.7 V; V_{OUT} = 280 mV. V_{OUT}/I_{OL} must be less than 21 ohm for values of V_{OUT} between 0 V and 280 mV.
3. The dc value of V_{REF} applied to the receiving device is set to V_{TT}
4. The values of $I_{OH(dc)}$ and $I_{OL(dc)}$ are based on the conditions given in Notes 1 and 2. They are used to test device drive current capability to ensure V_{IH} min plus a noise margin and V_{IL} max minus a noise margin are delivered to an SSTL_18 receiver. The actual current values are derived by shifting the desired driver operating point (see Section 3.3) along a 21 ohm load line to define a convenient driver current for measurement.

OCD defalut characteristics

Description	Parameter	Min	Nom	Max	Unit	Notes
Output impedance		12.6	18	23.4	ohms	1,2
Pull-up and pull-down mismatch		0		4	ohms	1,2,3
Output slew rate	Sout	1.5	-	5	V/ns	1,4,5,6

Note:

1. Absolute Specifications (0°C ≤ T_{CASE} ≤ +tbd°C; VDD = +1.8V ±0.1V, VDDQ = +1.8V ±0.1V)
2. Impedance measurement condition for output source dc current: VDDQ = 1.7V; VOUT = 1420mV; (VOUT-VDDQ)/Ioh must be less than 23.4 ohms for values of VOUT between VDDQ and VDDQ-280mV. Impedance measurement condition for output sink dc current: VDDQ = 1.7V; VOUT = 280mV; VOUT/Iol must be less than 23.4 ohms for values of VOUT between 0V and 280mV.
3. Mismatch is absolute value between pull-up and pull-dn, both are measured at same temperature and voltage.
4. Slew rate measured from vil(ac) to vih(ac).
5. The absolute value of the slew rate as measured from DC to DC is equal to or greater than the slew rate as measured from AC to AC.
6. DRAM output slew rate specification applies to 400MT/s & 533MT/s speed bins.

PIN CAPACITANCE (VDD=1.8V,VDDQ=1.8V, TA=25℃. f=1MHz)

Parameter	Pin	Symbol	Min	Max	Unit
Input Capacitance	CK0, /CK0	C_{CK}	7	11	pF
Input Capacitance	CKE, ODT	C_{I1}	8	12	pF
Input Capacitance	/CS	C_{I2}	8	12	pF
Input Capacitance	Address, /RAS, /CAS, /WE	C_{I3}	8	12	pF
Input Capacitance	DQ,DM,DQS, /DQS	C_{IO}	7	11	pF

Note :
1. Pins not under test are tied to GND.
2. These value are guaranteed by design and tested on a sample basis only.

IDD Specifications

HYMP112R72(L)8		PC2 3200	PC2 4300	PC2 5300	
Parameter	**Symbol**	**max.**	**max.**	**max.**	**Unit**
Operating one bank active-precharge current	I_{DD0}	1550	1640	1730	mA
Operating one bank active-read-precharge current	I_{DD1}	1640	1730	1820	mA
Precharge power-down current	I_{DD2P}	695	704	713	mA
Precharge quiet standby current	I_{DD2Q}	1010	1100	1190	mA
Precharge standby current	I_{DD2N}	1055	1100	1190	mA
Active power-down current	$I_{DD3P(F)}$	875	920	965	mA
	$I_{DD3P(S)}$	713	722	731	mA
Active Standby Current	I_{DD3N}	1190	1280	1370	mA
Operating burst read current	I_{DD4R}	1820	2180	2780	mA
Operating Current	I_{DD4W}	1910	2270	2810	mA
Burst auto refresh current	I_{DD5B}	2780	2780	2780	mA
Self Refresh Current	I_{DD6}	413	413	413	mA
	$I_{DD6(L)}$	395	395	395	mA
Operating bank interleave read current	I_{DD7}	2810	3350	3620	mA

IDD Meauarement Conditions

Symbol	Conditions		Units
IDD0	**Operating one bank active-precharge current**; ^{t}CK = ^{t}CK(IDD), ^{t}RC = ^{t}RC(IDD), ^{t}RAS = ^{t}RAS-min(IDD);CKE is HIGH, $\overline{CS}$ is HIGH between valid commands;Address bus inputs are SWITCHING;Data bus inputs are SWITCHING		mA
IDD1	**Operating one bank active-read-precharge curren** ; IOUT = 0mA;BL = 4, CL = CL(IDD), AL = 0; ^{t}CK = ^{t}CK(IDD), ^{t}RC = ^{t}RC (IDD), ^{t}RAS = ^{t}RASmin(IDD), ^{t}RCD = ^{t}RCD(IDD) ; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands ; Address bus inputs are SWITCHING ; Data pattern is same as IDD4W		mA
IDD2P	**Precharge power-down current** ; All banks idle ; ^{t}CK = ^{t}CK(IDD) ; CKE is LOW ; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		mA
IDD2Q	**Precharge quiet standby current**;All banks idle; ^{t}CK = ^{t}CK(IDD);CKE is HIGH, $\overline{CS}$ is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		mA
IDD2N	**Precharge standby current**; All banks idle; ^{t}CK = ^{t}CK(IDD); CKE is HIGH, $\overline{CS}$ is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA
IDD3P	**Active power-down current**; All banks open; ^{t}CK = ^{t}CK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0	mA
		Slow PDN Exit MRS(12) = 1	mA
IDD3N	**Active standby current**; All banks open; ^{t}CK = ^{t}CK(IDD), ^{t}RAS = ^{t}RASmax(IDD), ^{t}RP =^{t}RP(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA
IDD4W	**Operating burst write current**; All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; ^{t}CK = ^{t}CK(IDD), ^{t}RAS = ^{t}RASmax(IDD), ^{t}RP = ^{t}RP(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA
IDD4R	**Operating burst read current**; All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; ^{t}CK = ^{t}CK(IDD), ^{t}RAS = ^{t}RASmax(IDD), ^{t}RP = ^{t}RP(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING;; Data pattern is same as IDD4W		mA
IDD5B	**Burst refresh current**; ^{t}CK = ^{t}CK(IDD); Refresh command at every ^{t}RFC(IDD) interval; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA
IDD6	**Self refresh current**; CK and $\overline{CK}$ at 0V; CKE ≤ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING		mA
IDD7	**Operating bank interleave read current**; All bank interleaving reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = ^{t}RCD(IDD)-1*^{t}CK(IDD); ^{t}CK = ^{t}CK(IDD), ^{t}RC = ^{t}RC(IDD), ^{t}RRD = ^{t}RRD(IDD), ^{t}RCD = 1*^{t}CK(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R; - Refer to the following page for detailed timing conditions		mA

Note:

1. IDD specifications are tested after the device is properly initialized
2. Input slew rate is specified by AC Parametric Test Condition
3. IDD parameters are specified with ODT disabled.
4. Data bus consists of DQ, DM, DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$, LDQS, $\overline{LDQS}$, UDQS, and $\overline{UDQS}$. IDD values must be met with all combinations of EMRS bits 10 and 11.
5. Definitions for IDD
   LOW is defined as Vin ≤ VILAC(max)
   HIGH is defined as Vin ≥ VIHAC(min)
   STABLE is defined as inputs stable at a HIGH or LOW level
   FLOATING is defined as inputs at VREF = VDDQ/2
   SWITCHING is defined as:
   inputs changing between HIGH and LOW every other clock cycle (once per two clocks) for address and control signals, and
   inputs changing between HIGH and LOW every other data transfer (once per clock) for DQ signals not including masks or strobes.

Electrical Characteristics & AC Timings

Speed Bins and CL,tRCD,tRP,tRC and tRAS for Corresponding Bin

Speed	DDR2-667(Y5)	DDR2-667(Y6)	DDR2-533(C4)	DDR2-533(C5)	DDR2-400(E3)	DDR2-400(E4)	Unit
Bin(CL-tRCD-tRP)	5-5-5	6-6-6	4-4-4	5-5-5	3-3-3	4-4-4	
Parameter	min	min	min	min	min	min	
CAS Latency	5	6	4	5	3	4	ns
tRCD	15	18	15	18.75	15	20	ns
tRP	15	18	15	18.75	15	20	ns
tRC	55	63	60	63.75	55	65	ns
tRAS	40	45	45	45	40	45	ns

AC Timing Parameters by Speed Grade

Parameter	Symbol	DDR2-400		DDR2-533		DDR2-667		Unit	Note
		Min	Max	Min	Max	Min	Max		
Data-Out edge to Clock edge Skew	tAC	-600	600	-500	500	-450	450	ps	
DQS-Out edge to Clock edge Skew	tDQSCK	-500	500	-500	450	-400	400	ns	
Clock High Level Width	tCH	0.45	0.55	0.45	0.55	0.45	0.55	CK	
Clock Low Level Width	tCL	0.45	0.55	0.45	0.55	0.45	0.55	CK	
Clock Half Period	tHP	min (tCL,tCH)	-	min (tCL,tCH)	-	min (tCL,tCH)	-	ns	
System Clock Cycle Time	tCK	5000	8000	3750	8000	3000	8000	ps	
DQ and DM input hold time	tDH	400	-	350	-	300	-	ps	1
DQ and DM input setup time	tDS	400	-	350	-	300	-	ps	1
Control & Address input Pulse Width for each input	tIPW	0.6	-	0.6	-	0.6	-	tCK	
DQ and DM input pulse witdth for each input pulse width for each input	tDIPW	0.35	-	0.35	-	0.35	-	tCK	
Data-out high-impedance window from CK, /CK	tHZ	-	tAC max	-	tAC max	-	tAC max	ps	
DQS low-impedance time from CK/$\overline{CK}$	tLZ(DQS)	tAC min	tAC max	tAC min	tAC max	tAC min	tAC max	ps	
DQ low-impedance time from CK/$\overline{CK}$	tLZ(DQ)	2*tAC min	tAC max	2*tAC min	tAC max	2*tAC min	tAC max	ps	
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	-	350	-	300	-	tbd	ps	
DQ hold skew factor	tQHS	-	450	-	400	-	tbd	ps	
DQ/DQS output hold time from DQS	tQH	tHP - tQHS	-	tHP - tQHS	-	tHP - tQHS	-	ps	
Write command to first DQS latching transition	tDQSS	WL - 0.25	WL + 0.25	WL - 0.25	WL + 0.25	WL - 0.25	WL + 0.25	tCK	
DQS input high pulse width	tDQSH	0.35	-	0.35	-	0.35	-	tCK	
DQS input low pulse width	tDQSL	0.35	-	0.35	-	0.35	-	tCK	
DQS falling edge to CK setup time	tDSS	0.2	-	0.2	-	0.2	-	tCK	
DQS falling edge hold time from CK	tDSH	0.2	-	0.2	-	0.2	-	tCK	
Mode register set command cycle time	tMRD	2	-	2	-	2	-	tCK	
Write postamble	tWPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK	

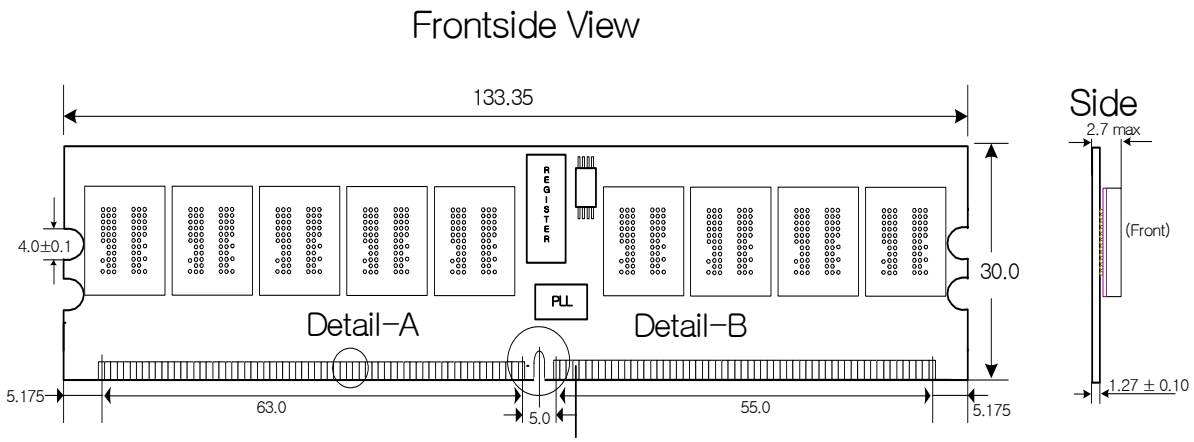
- continued -

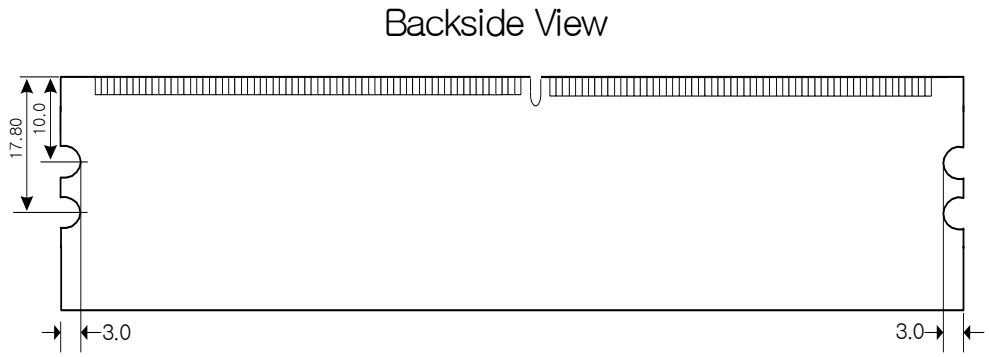
Parameter	Symbol	DDR2 400		DDR2 533		DDR2 667		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write preamble	tWPRE	0.25	-	0.25	-	0.25	-	tCK	
Address and control input hold time	tIH	600	-	500	-	500	-	ps	
Address and control input setup time	tIS	600	-	500	-	500	-	ps	
Read preamble	tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	tCK	
Read postamble	tRPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
Auto-Refresh to Active/Auto-Refresh command period	tRFC	127.5	-	127.5	-	127.5	-	ns	
Row Active to Row Active Delay	tRRD	7.5	-	7.5	-	7.5	-	ns	
$\overline{CAS}$ to $\overline{CAS}$ command delay	tCCD	2		2		2		tCK	
Write recovery time	tWR	15	-	15	-	15	-	ns	
Auto Precharge Write Recovery + Precharge Time	tDAL	(tWR/tCK) + (tRP/tCK)	-	(tWR/tCK) + (tRP/tCK)	-	(tWR/tCK) + (tRP/tCK)	-	tCK	
Write to Read Command Delay	tWTR	10	-	7.5	-	7.5	-	ns	
Internal read to precharge command delay	tRTP	7.5		7.5		7.5		ns	
Exit self refresh to a non-read command	tXSNR	tRFC + 10		tRFC + 10		tRFC + 10		ns	
Exit self refresh to a read command	tXSRD	200	-	200	-	200	-	tCK	
Exit precharge power down to any non-read command	tXP	2	-	2	-	2	-	tCK	
Exit active power down to read command	tXARD	2		2		2		tCK	
Exit active power down to read command (Slow exit, Lower power)	tXARDS	6 - AL		6 - AL		6 - AL		tCK	
CKE minimum pulse width (high and low pulse width)	tCKE	3		3		3		tCK	
ODT turn-on delay	tAOND	2	2	2	2	2	2	tCK	
ODT turn-on	tAON	tAC(min)	tAC(max) +1	tAC(min)	tAC(max) +1	tAC(min)	tAC(max) +0.7	ns	
ODT turn-on(Power-Down mode)	tAONPD	tAC(min)+2	2tCK+tAC (max)+1	tAC(min)+2	2tCK+tAC (max)+1	tAC(min)+2	2tCK+tAC (max)+1	ns	
ODT turn-off delay	tAOFD	2.5	2.5	2.5	2.5	2.5	2.5	tCK	
ODT turn-off	tAOF	tAC(min)	tAC(max) + 0.6	tAC(min)	tAC(max) + 0.6	tAC(min)	tAC(max) + 0.6	ns	
ODT turn-off (Power-Down mode)	tAOFPD	tAC(min)+2	2.5tCK+t AC(max)+ 1	tAC(min)+2	2.5tCK+t AC(max)+ 1	tAC(min)+2	2.5tCK+t AC(max)+ 1	ns	
ODT to power down entry latency	tANPD	3		3		3		tCK	
ODT power down exit latency	tAXPD	8		8		8		tCK	
OCD drive mode output delay	tOIT	0	12	0	12	0	12	ns	
Minimum time clocks remains ON after CKE asynchronously drops LOW	tDelay	tIS+tCK+tI H		tIS+tCK+tI H		tIS+tCK+tI H		ns	
Average periodic Refresh Interval	tREFI	-	7.8	-	7.8	-	7.8	us	2
	tREFI	-	3.9	-	3.9	-	3.9	us	3

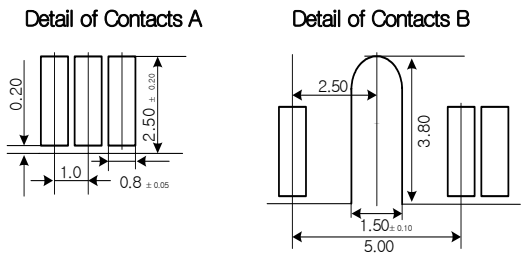
Note :

1. For details and notes, please refer to the relevant HYNIX component datasheet(HY5PS1G831(L)F).
2. 0°C ≤ TCASE ≤ 85°C
3. 85°C < TCASE ≤ 95°C

PACKAGE OUTLINE







Note) All dimensions are typical millimeter scale unless otherwise stated.

SPD SPECIFICATION

(128Mx72 Registered DDR2 DIMM)

SERIAL PRESENCE DETECT

Bin Sort : E3(DDR2 400 3-3-3), E4(DDR2 400 4-4-4), C4(DDR2 533 4-4-4), C5(DDR2 533 5-5-5)

Byte#	Function Description	Speed Grade	Function Supported	Hexa Value	Note
0	Number of bytes utilized by module manufacturer	all	128 Bytes	80	
1	Total number of Bytes in SPD device	all	256 Bytes	08	
2	Fundamental memory type	all	DDR2 SDRAM	08	
3	Number of row address on this assembly	all	14	0E	1
4	Number of column address on this assembly	all	10	0A	1
5	Number of DIMM ranks	all	1 rank	60	
6	Module data width	all	72 Bits	48	
7	Module data width (continued)	all	-	00	
8	Voltage Interface level of this assembly	all	SSTL 1.8V	05	
9	DDR SDRAM cycle time at CL=5	E3,E4	5.0 ns	50	2
		C4,C5	3.75 ns	3D	2
10	DDR SDRAM access time from clock (tAC)	E3,E4	+/-0.6ns	60	
		C4,C5	+/-0.5ns	50	
11	DIMM Configuration type	all	ECC	02	
12	Refresh Rate and Type	all	7.8us & Self refresh	82	
13	Primary DDR SDRAM width	all	x8	08	
14	Error Checking DDR SDRAM data width	all	x8	08	
15	Reserved		-	00	
16	Burst Lengths Supported	all	4,8	0C	
17	Number of banks on each SDRAM Device	all	8	08	
18	CAS latency supported	all	3, 4, 5	38	
19	Reserved		-	00	
20	DIMM Type	all	Regular RDIMM	01	
21	DDR SDRAM module attributes	all	Normal	00	
22	DDR SDRAM device attributes : General	all	Supports weak driver	01	
23	DDR SDRAM cycle time at CL=4(tCK)	E3,E4,C5	5.0ns	50	2
		C4	3.75ns	3D	
24	DDR SDRAM access time from clock at CL=4(tAC)	E3,E4,C5	+/-0.6ns	60	2
		C4	+/-0.5ns	50	
25	DDR SDRAM cycle time at CL=3(tCK)	E3,C4	5.0ns	50	2
		E4,C5	Undefined	00	
26	DDR SDRAM access time from clock at CL=3(tAC)	E3,C4	-	00	2
		E4,C5			
27	Minimum Row Precharge Time(tRP)	E3, C4	15ns	3C	
		E4	20ns	50	
		C5	18.75ns	4B	
28	Minimum Row Activate to Row Active delay(tRRD)	all	7.5ns	1E	
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ delay(tRCD)	E3, C4	15ns	3C	
		E4	20ns	50	
		C5	18.75ns	4B	
30	Minimum active to precharge time(tRAS)	E3	40ns	28	
		E4,C4,C5	45ns	2D	
31	Module rank density	all	1GB	01	
32	Address and command input setup time before clock (tIS)	E3, E4	0.6ns	60	
		C4, C5	0.5ns	50	
33	Address and command input hold time after clock (tIH)	E3, E4	0.6ns	60	
		C4, C5	0.5ns	50	
34	Data input setup time before clock (tDS)	E3, E4	0.40ns	40	
		C4, C5	0.35ns	35	
35	Data input hold time after clock (tDH)	E3, E4	0.40ns	40	
		C4, C5	0.35ns	35	
36	Write recovery time(tWR)	all	15ns	3C	
37	Internal write to read command delay(tWTR)	E3, E4	10ns	28	
		C4, C5	7.5ns	1E	
38	Internal read to precharge command delay(tRTP)	all	7.5ns	1E	
39	Memory analysis probe characteristics		Undefined	00	
40	Extension of byte 41 tRC and byte 42 tRFC	E3,E4,C4	tRC extended	06	
		C5	tRC extended	56	
41	Minimum active / auto-refresh time (tRC)	E3	55ns	37	
		C4	60ns	3C	
		E4	65ns	41	
		C5	63.75ns	3F	

- continued -

Byte#	Function Description	Speed Grade	Function Supported	Hexa Value	Note
42	Minimum auto-refresh to active/auto-refresh command period(tRFC)	all	127.5ns	7F	
43	Maximum cycle time (tCK max)	all	8.0ns	80	
44	Maximim DQS-DQ skew time(tDQSQ)	E3, E4	0.35ns	23	
		C4, C5	0.30ns	1E	
45	Maximum read data hold skew factor(tQHS)	E3, E4	0.45ns	2D	
		C4, C5	0.40ns	28	
46	PLL Relock time		15us	0F	
47~61	Superset information(may be used in future)		Undefined	00	
62	SPD Revision code		1.0	10	
63	Checksum for Bytes 0~62	E3	-	73	
		E4	-	FA	
		C4	-	ED	
		C5	-	D1	
64	Manufacturer JEDEC ID Code		Hynix JEDEC ID	AD	
65~71	--------- Manufacturer JEDEC ID Code		-	00	
72	Manufacturing location		Hynix(Korea Area) HSA(United States Area) HSE(Europe Area) HSJ(Japan Area) Singapore Asia Area	0* 1* 2* 3* 4* 5*	6
73	Manufacture part number(Hynix Memory Module)		H	48	
74	-------- Manufacture part number(Hynix Memory Module)		Y	59	
75	-------- Manufacture part number(Hynix Memory Module)		M	4D	
76	Manufacture part number (DDR2 SDRAM)		P	50	
77	---------Manufacture part number(Memory density)		1	31	
78	Manufacture part number(Module Depth)		1	31	
79	------- Manufacture part number(Module Depth)		2	32	
80	Manufacture part number(Module type)		R	52	
81	Manufacture part number(Data width)		7	37	
82	-------Manufacture part number(Data width)		2	32	
83	Manufacture part number(Component configuration)		8	38	
84	Manufacture part number(Hyphen)		'-'	2D	
85	Manufacture part number(Minimum cycle time)	E3, E4	E	45	
		C4, C5	C	43	
86	-------Manufacture part number(Minimum cycle time)	E3	3	33	
		E4,C4	4	34	
		C5	5	35	
87~90	Manufacture part number(T.B.D)		Blank	20	
91	Manufacture revision code(for Component)				
92	Manufacture revision code (for PCB)				
93	Manufacturing date(Year)				3
94	Manufacturing date(Week)				3
95~98	Module serial number				4
99~127	Manufacturer specific data (may be used in future)		Undefined	00	5
128~255	Open for customer use		Undefined	00	5

Note :
1. The bank address is excluded
2. This value is based on the component specification
3. These bytes are programmed by code of date week & date year
4. These bytes apply to Hynix's own Module Serial Number System
5. These bytes undefined and coded as '00h'
6. Refer to Hynix Web Site

Byte 83~84, Low Power Part

Byte #	Function Description	Speed Grade	Function Supported	Hexa Value	Note
83	Manufacture part number(Low power part)		L	4C	
84	Manufacture part number(Component Configuration)		8	38	