Intel® 80200 Processor based on Intel® XScale™ Microarchitecture

Datasheet

Product Features

- High Performance Processor based on Intel® XScale™ Microarchitecture
  - —7-8 stage Intel® Superpipelined Technology
  - —32-Entry Instruction Memory Management Unit
  - —32-Entry Data Memory Management Unit
  - —32 KByte, 32-way Set Associative Instruction Cache
  - —32 KByte, 32-way Set Associative Data Cache
  - —2 KByte, 2-way Set Associative Mini-Data Cache
  - —128-Entry Branch Target Buffer
  - —8-Entry Write Buffer
  - —4-Entry Fill and Pend Buffers
- Intel® Dynamic Voltage Management
  - —Core Voltage Range: 0.95 V to 1.55 V
  - —Internal Clock Scalable by Software up to 733 MHz
  - —Input Clock: 33-66 MHz
- ARM* Version 5TE Compliant
- Application-Code Compatible with Intel® StrongARM* SA-110
- Power Management
  - —Core Power is ~500mW at 600MHz
  - —Core Voltage Operation Down to 0.95 V
  - —Idle and Sleep Modes
- Intel® Media Processing Technology
  - —Multiply-Accumulate Coprocessor
- High Performance External Bus
  - —64- or 32-Bit Data Interface
  - —Optional ECC Protection
  - —Frequency up to 100 MHz
  - —Asynchronous to Processor Clock
- Performance Monitoring Unit
  - —Two 32-Bit Event Counters
  - —One 32-Bit Clock Counter
  - —Monitors Occurrence and Duration Events
- Debug Unit
  - —Accessible through JTAG Port
  - —Hardware Breakpoints
  - —256-Entry Trace Buffer

August 2002

Reference Number: 273414-004

Contents

Figures

Tables

1.0 About this Document

This is the Advance Information data sheet for the Intel® 80200 processor based on Intel® XScale™ microarchitecture (ARM* architecture compliant). This data sheet contains a functional overview, mechanical data (package signal locations and simulated thermal characteristics), targeted electrical specifications (simulated), and bus functional waveforms. Detailed functional descriptions other than parametric performance is published in the *Intel® 80200 Processor based on Intel® XScale™ Microarchitecture Developer's Manual*.

Table 1. Related Documentation

Document Title	Document #
Intel® 80200 Processor based on Intel® XScale™ Microarchitecture Developer's Manual	273411
Intel® 80200 Processor based on Intel® XScale™ Microarchitecture Specification Update	273415
Intel® 80310 I/O Processor Chipset Design Guide	273354
Intel® 80312 I/O Companion Chip Developer's Manual	273410
Intel® 80312 I/O Companion Chip Datasheet	273425
Intel® 80312 I/O Companion Chip Specification Update	273416

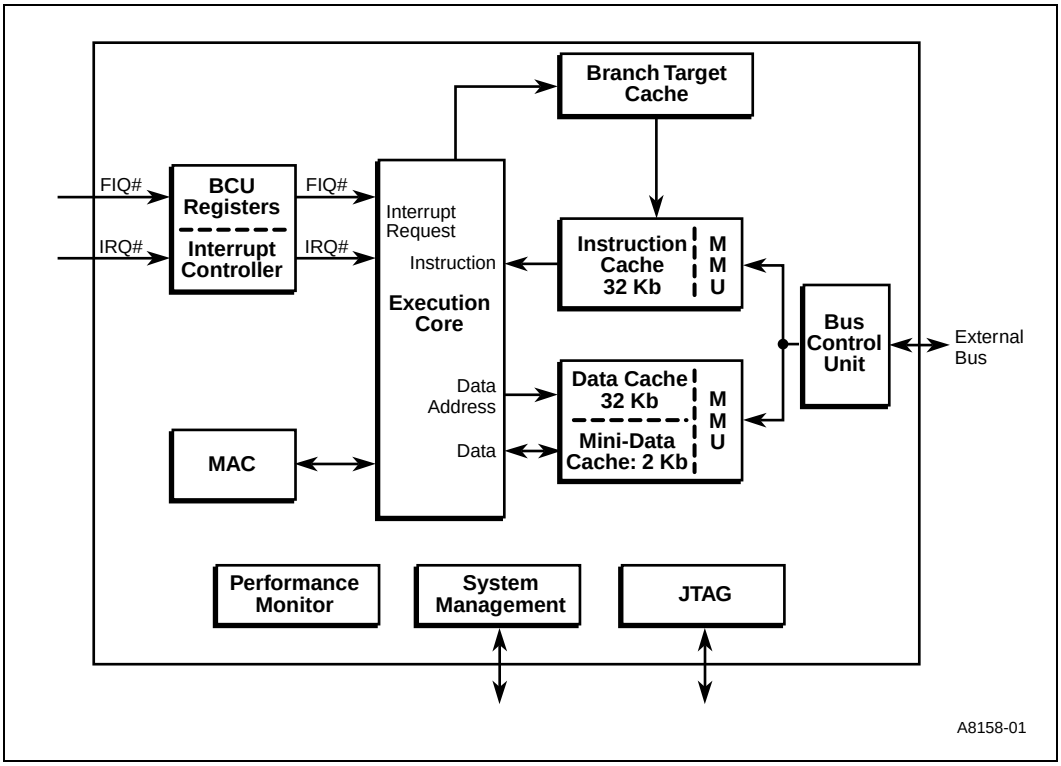
2.0 Functional Overview

The Intel® 80200 processor technology is compliant with the ARM* Version 5TE instruction set architecture (ISA). The Intel® 80200 processor is designed with Intel state-of-the-art 0.18 micron production semiconductor process technology. This process technology, along with the compactness of the ARM RISC ISA, enables the Intel® 80200 processor to operate over a wide speed/power range, producing industry-leading mW/MIPS performance.

- 7-8 stage Superpipeline promotes high speed, efficient core performance
- 128-entry Branch Target Buffer keeps pipeline filled with statistically correct branch choices
- 32-entry Instruction Memory Management Unit for logical-to-physical address translation, access permissions, I-Cache attributes
- 32-entry Data Memory Management Unit for logical-to-physical address translation, access permissions, D-Cache attributes
- 32 KB Instruction Cache can hold entire programs, preventing core stalls caused by multicycle memory accesses
- 32 KB Data Cache reduces core stalls caused by multicycle memory accesses
- 2 KB Minidata Cache for frequently changing data streams avoids "thrashing" of the D-Cache
- 4-entry Fill and Pend Buffers promote core efficiency by allowing "hit-under- miss" operation with Data Caches
- Power Management Unit gives power savings via idle, and sleep modes
- 8-entry Write Buffer allows the core to continue execution while data is written to memory
- Multiply-Accumulate Coprocessor can do two simultaneous 16-bit SIMD multiplies with 40-bit accumulation for efficient, high quality audio

- Performance Monitoring Unit furnishes two 32-bit event counters and one 32-bit cycle counter for analysis of hit rates, etc.
- JTAG Debug Unit uses Hardware Breakpoints and 256-entry Trace History Buffer (for flow change messages) to debug programs
- Dynamic clocking allows optimized performance

Figure 1. Intel® 80200 Processor Block Diagram



2.1 Superpipeline

The Superpipeline is composed of Integer, Multiply-Accumulate (MAC), and memory pipes.

The Integer pipe has seven stages:

- Branch Target Buffer (BTB)/Fetch 1
- Fetch 2
- Decode
- Register File/Shift
- ALU Execute
- State Execute
- Integer Writeback

The Memory pipe has eight stages:

- the first five stages of the Integer pipe (BTB/Fetch 1 through ALU Execute)

. . . then finish with Memory stages:

- Data Cache 1
- Data Cache 2
- Data Cache Writeback

The MAC pipe has six to nine stages:

- the first four stages of the Integer pipe (BTB/Fetch 1 through Register File/ Shift)

. . . then finish with MAC stages:

- MAC1
- MAC2
- MAC3
- MAC4
- Register Writeback

The MAC pipe supports a data-dependent early terminate where stages MAC2, MAC3, and/or MAC4 are by-passed.

Deep pipes promote high instruction execution rates only when a means exists to successfully predict the outcome of branch instructions. The Branch Target Buffer provides such a means.

2.2 Branch Target Buffer (BTB)

Each entry of the 128-entry BTB contains the address of a branch instruction, the target address associated with the branch instruction, and a previous history of the branch being taken or not taken. The history is recorded as one of four states: strongly taken, weakly taken, weakly not-taken, or strongly not-taken. The BTB can be enabled or disabled via coprocessor 15, register 1.

When the address of the branch instruction hits in the BTB and its history is strongly or weakly taken, the instruction at the branch target address is fetched; when its history is strongly or weakly not-taken, the next sequential instruction is fetched. In either case the history is updated.

Data associated with a branch instruction enters the BTB the first time the branch is taken. This data enters the BTB in a slot with a history of strongly not-taken (overwriting previous data when present).

Successfully predicted branches avoid any branch-latency penalties in the superpipeline. Unsuccessfully predicted branches result in a 4-5 cycle branch-latency penalty in the superpipeline.

2.3 Instruction Memory Management Unit (IMMU)

For instruction prefetches the IMMU controls logical-to-physical address translation, memory access permissions, memory domain identifications, and attributes (governing operation of the instruction cache). The IMMU contains a 32-entry, fully associative Instruction Translation Look-A-Side Buffer (ITLB) that has a round-robin replacement policy. ITLB entries 0-30 can be locked.

When an instruction prefetch misses in the ITLB, the IMMU invokes an automatic table-walk mechanism that fetches an associated descriptor from memory and loads it into the ITLB. The descriptor contains information for logical-to-physical address translation, memory access permissions, memory domain identifications, and attributes governing operation of the i-cache. The IMMU then continues the instruction prefetch by using the address translation just entered into the ITLB. When an instruction prefetch hits in the ITLB, the IMMU continues the prefetch using the address translation already resident in the ITLB.

Access permissions for each of up to sixteen memory domains can be programmed. When an instruction prefetch is attempted to an area of memory in violation of access permissions, then the attempt is aborted and a prefetch abort is sent to the core for exception processing. The IMMU and DMMU can be enabled or disabled together.

2.4 Data Memory Management Unit (DMMU)

For data fetches, the DMMU controls logical-to-physical address translation, memory access permissions, memory domain identifications, and attributes (governing operation of the data cache or mini-data cache and write buffer). The DMMU contains a 32-entry, fully associative data translation look-a-side buffer (DTLB) that has a round-robin replacement policy. DTLB entries 0-30 can be locked.

When a data fetch misses in the DTLB, the DMMU invokes an automatic table-walk mechanism that fetches an associated descriptor from memory and loads it into the DTLB. The descriptor contains information for logical-to-physical address translation, memory access permissions, memory domain identifications, and attributes (governing operation of the d-cache or mini-data cache and write buffer). The DMMU then continues the data fetch by using the address translation just entered into the DTLB. When a data fetch hits in the DTLB, the DMMU continues the fetch using the address translation already resident in the DTLB.

Access permissions for each of up to sixteen memory domains can be programmed. When a data fetch is attempted to an area of memory in violation of access permissions, then the attempt is aborted and a data abort is sent to the core for exception processing. The IMMU and DMMU can be enable or disable together.

2.5 Instruction Cache (I-Cache)

The I-Cache can contain high-use multiple code segments or entire programs, allowing the core access to instructions at core frequencies. This prevents core stalls caused by multicycle accesses to external memory.

The 32 KByte i-cache is 32-set/32-way associative, where each set contains 32-ways and each way contains a tag address, a cache line (eight 32-bit words and one parity bit per word) of instructions, and a line-valid bit. For each of the 32 sets, 0-28 ways can be locked. Unlocked ways are replaceable via a round robin policy.

The i-cache can be enabled or disabled. Attribute bits within the descriptors contained in the ITLB of the IMMU provide some control over an enabled i-cache.

When a needed line (eight 32-bit words) is not present in the i-cache, the line is fetched (critical word first) from memory via a two-level-deep fetch queue.

2.6 Data Cache (D-Cache)

The D-Cache can contain high-use data such as lookup tables and filter coefficients, allowing the core access to data at core frequencies. This prevents core stalls caused by multicycle accesses to external memory.

The 32 KByte d-cache is 32-set/32-way associative, where each set contains 32-ways and each way contains a tag address, a cache line (32 bytes with one parity bit per byte) of data, two dirty bits (one for each of two 8-byte groupings in a line), and one valid bit. For each of the 32 sets, 0-28 ways can be locked, unlocked, or used as local SRAM. Unlocked ways are replaceable via a round robin policy.

The d-cache (together with the mini-data cache) can be enabled or disabled. Attribute bits within the descriptors contained in the DTLB of the DMMU provide significant control over an enabled d-cache. These bits specify cache operating modes such as read and write allocate, write-back, write-through, and d-cache versus mini-data cache targeting

The d-cache (and mini-data cache) work with the load buffer and pend buffer to provide “hit-under- miss” capability that allows the core to access other data in the cache after a “miss” is encountered (see Section 2.8, “Fill Buffer (FB) and Pend Buffer (PB)” on page 11 for more information). The d-cache (and mini-data cache) works in conjunction with the write buffer for data that is to be stored to memory (see Section 2.9, “Write Buffer (WB)” on page 11 for more information).

2.7 Mini-Data Cache

The Mini-data Cache can contain frequently changing data streams such as MPEG video, allowing the core access to data streams at core frequencies. This prevents core stalls caused by multicycle accesses to external memory. The mini-data cache relieves the d-cache of data “thrashing” caused by frequently changing data streams.

The 2 KByte mini-data cache is 32-set/2-way associative, where each set contains 2-ways and each way contains a tag address, a cache line (32 bytes with one parity bit per byte) of data, two dirty bits (one for each of two 8-byte groupings in a line), and a valid bit. The mini-data cache uses a round robin replacement policy, and cannot be locked.

The mini-data cache (together with the d-cache) can be enabled or disabled. Attribute bits contained within a coprocessor register specify operating modes write and/or read allocate, write-back, and write-through.

The mini-data cache (and d-cache) work with the load buffer and pend buffer to provide “hit-under-miss” capability that allows the core to access other data in the cache after a “miss” is encountered (see Section 2.8, “Fill Buffer (FB) and Pend Buffer (PB)” on page 11 for more information). The mini-data cache (and d-cache) works in conjunction with the write buffer for data that is to be stored to memory (see Section 2.9, “Write Buffer (WB)” on page 11 for more information).

2.8 Fill Buffer (FB) and Pend Buffer (PB)

The 4-entry Fill Buffer works with the core to hold loads until the bus controller can act on them. The FB and the 4-entry Pend Buffer work with the d-cache and mini-data cache to provide “hit-under-miss” capability, allowing the core to seek other data in the caches while “miss” data is being fetched from memory. The FB can contain up to four unique “miss” addresses (logical), allowing four “misses” before the core is stalled. The PB holds up to four addresses (logical) for additional “misses” to those addresses that are already in the FB. A coprocessor register can specify draining of the Fill and Pend (Write) Buffers.

2.9 Write Buffer (WB)

The Write Buffer holds data for storage to memory until the bus controller can act on it. The WB is 8-entries deep, where each entry holds 16 bytes. The WB is constantly enabled, and accepts data from the core, d-cache, or mini-data cache.

Coprocessor 15, register 1 specifies whether WB coalescing is enabled or disabled. When coalescing is disabled, stores to memory occur in program order regardless of the attribute bits within the descriptors located in the DTLB. When coalescing is enabled, the attribute bits within the descriptors located in the DTLB are examined to determine when coalescing is enabled for the destination region of memory. When coalescing is enabled in both CP15, R1 and the DTLB, then data entering the WB can coalesce with any of the 8-entries (16 bytes) and then be stored to the destination memory region, but possibly out of program order.

Stores to a memory region specified to be non-cacheable and non-bufferable by the attribute bits within the descriptors located in the DTLB causes the Core to stall until the store completes. A coprocessor register can specify draining of the write buffer.

2.10 Multiply-Accumulate Coprocessor (CP0)

For efficient processing of high-quality audio algorithms, CP0 provides 40-bit accumulation of 16x16, dual-16x16 (SIMD), and 32x32 signed multiplies. Special MAR and MRA instructions are implemented to Move 40-bit Accumulator to Two Core General Registers (MAR) and Move Two Core General Registers to 40-bit Accumulator (MRA). The 40-bit accumulator can be stored or loaded to or from d-cache, mini-data cache, or memory using two STC or LDC instructions.

16x16 signed multiply-accumulates (MIAxy) multiply either the high/high, low/low, high/low, or low/high 16 bits of a 32-bit core general register (multiplier) and another 32-bit core general register (multiplicand) to produce a full 32-bit product which is sign-extended to 40 bits and then added to the 40-bit accumulator.

Dual signed 16x16 (SIMD) multiply-accumulates (MIAPH) multiply the high/high and low/low 16-bits of a packed 32-bit core general register (multiplier) and another packed 32-bit core general register (multiplicand) to produce two 16-bits products which are both sign-extended to 40 bits and then both added to the 40-bit accumulator.

32x32 signed multiply-accumulates (MIA) multiply a 32-bit core general register (multiplier) and another 32-bit core general register (multiplicand) to produce a 64-bit product where the 40 LSBs are added to the 40-bit accumulator. 16x32 versions of the multiply-accumulate instructions complete in a single cycle.

2.11 Clock and Power Management

The Intel® 80200 processor was designed with power saving techniques that power-up a functional block only when it is needed. Low power modes are selectable by programming CP 14, register 6.

The Intel® 80200 processor was designed to allow dynamic clocking. The core clock frequency is set by programming CP14, Register 7. This enables software to conserve power by matching the core clock frequency to the current workload.

2.12 Performance Monitoring Unit (PMU)

The Performance Monitoring Unit contains two 32-bit event counters and one 32-bit clock counter. The event counters can be programmed to monitor i-cache hit rate, data caches hit rate, ITLB hit rate, DTLB hit rate, pipeline stalls, BTB prediction hit rate, and instruction execution count.

2.13 Debug Unit

The Debug Unit is accessed through the JTAG port. The industry-standard IEEE1149.1 JTAG port consists of a Test Access Port (TAP) controller, Boundary-Scan register, instruction and data registers, and dedicated signals TDI, TDO, TCK, TMS, and TRST#. The debug unit, when used with debugger application code running on a host system outside of the Intel® 80200 processor, allows a program running on the Intel® 80200 processor to be debugged. It allows the debugger application code or a debug exception to stop program execution and re-direct execution to a debug handling routine. Debug exceptions are instruction breakpoint, data breakpoint, software breakpoint, external debug breakpoint, exception vector trap, and trace buffer full breakpoint. Once execution has stopped, the debugger application code can examine or modify the core's state, co-processor state, or memory. The debugger application code can then restart program execution.

The debug unit has two hardware instruction breakpoint registers, two hardware data breakpoint registers, and a hardware data breakpoint control register. The second data breakpoint register can be alternatively used as a mask register for the first data breakpoint register. A 256-entry trace buffer provides the ability to capture control flow messages or addresses. A JTAG instruction (LDIC) can be used to download a debug handler via the JTAG port to the mini-instruction cache (the i-cache has a 2 KByte mini-instruction cache, like the mini-data cache, that is used only to hold a debug handler).

3.0 Package Information

3.1 Package Introduction

The Intel® 80200 processor is offered in a Plastic Ball Grid Array (PBGA) package. See Figure 2 “241-Lead PBGA Package” on page 17.

3.1.1 Functional Signal Definitions

This section defines the pins and signals in the following tables:

- Table 2 “Pin Description Nomenclature” on page 13
- Table 3 “Power Pins” on page 14
- Table 4 “Signal Pin Description” on page 14
- Table 5 “JTAG Pins” on page 16

3.1.1.1 Signal Pin Descriptions

Table 2. Pin Description Nomenclature

Symbol	Description
I	Input pin only
O	Output pin only
I/O	Pin can be either an input or output
-	Pin must be connected as described
N/C	NO CONNECT. Do not make electrical connections to these balls.
Rst(...)	While the **RESETOUT#** pin is asserted, the pin: • Rst(1) Is driven to Vcc • Rst(0) Is driven to Vss • Rst(X) Is driven to unspecified state (1 or 0, buses may contain a mix of 1 and 0 signals) • Rst(H) Is pulled up to Vcc • Rst(L) Is pulled down to Vss • Rst(Z) Floats • Rst(Q) Is a valid output Since RESET# is asynchronous, these are asynchronous events.
Hld(...)	While the Intel® 80200 processor is in HOLD mode (**HOLD** asserted and took effect), the pin: • Hld(Z) Floats • Hld(Q) is a valid output • Hld(1) is driven to Vcc Note: When both **HLDA** and **RESETOUT#** are asserted, then HOLD mode takes priority; the output pins assume the state specified by Hld(...). The **HOLD** pin is also honored during Idle and Sleep modes; the output pins assume the state specified by Hld(...).
Slp(...)	While the Intel® 80200 processor is in Idle or Sleep mode (software selected), pin: • Slp(1) Is driven to Vcc • Slp(0) Is driven to Vss • Slp(X) Is driven to unspecified state • Slp(Q) Is a valid output

Table 3. Power Pins

Name	Count	Description
V_{CC}	17	Positive supply for the core.
V_{SS}	70	Ground.
V_{CCP}	25	Positive supply for the I/O pins.
V_{CCA}	1	Positive supply for the analog circuitry (PLL).

Table 4. Signal Pin Description (Sheet 1 of 2)

Name	Count	Type	Description
A[15:0]	16	O Rst(X) Hld(Z) Slp(X)	**Address Bus**: Conveys either the upper or lower half of a 32-bit address during the issue phase of a bus transaction.
ABORT	1	I	**Abort Transaction**: When asserted during the data phase of a transaction, this signal causes the remainder of that transaction to be aborted.
ADS#/LEN[2]	1	O Rst(1) Hld(Z) Slp(1)	**Address Strobe/Length**: During the first cycle of the issue phase, this signal indicates the start of a bus request. During the second cycle of the issue phase, this signal is the MSB of a value which indicates the length of the transaction.
BE[7:0]#	8	O Rst(Z) Hld(Q)[1] Slp(Z)	**Byte Enable**: Signifies which bytes are valid during a write transaction. When not in use, this bus is floated (Z).
CLK	1	I	**CLK**: Clock input for the core logic.
CWF/ DBusWidth (Config. Pin)	1	I	**Critical Word First**: When active during a data read transaction, **CWF** informs the core of the data wrap order. **DBusWidth**: While **RESET#** is asserted, this pin is sampled by the Intel® 80200 processor to determine when the data bus is to be configured as 32-bits or 64-bits. When the pin is sampled as '0' during reset, the 80200 assumes a 64-bit bus. When the pin is '1' at reset, a 32-bit bus is assumed.
D[63:0]	64	I/O Rst(Z) Hld(Q)[1] Slp(Z)	**Data Bus**: Carries data to/from the processor during a bus transaction. When not in use, this bus is floated (Z).
DCB[7:0]	8	I/O Rst(Z) Hld(Q)[1] Slp(Z)	**Data Check Byte**: Carries the optional ECC information associated with the data on the Data bus. When not in use, this bus is floated (Z).
DVALID	1	I	**Data Valid**: Asserted when **the Data bus** carries valid data.
FIQ#	1	I	**Fast Interrupt Request**: When FIQs are enabled, the processor responds to a low level on this input by taking the FIQ interrupt exception.
HLDA	1	O Rst(0) Hld(1) Slp(0)	**HLDA**: This output is asserted when the 80200 has floated the shared bus signals in response to **HOLD**.

Table 4. Signal Pin Description (Sheet 2 of 2)

Name	Count	Type	Description
HOLD	1	I	**HOLD**: Requests the Intel® 80200 processor to float shared bus signals.
IRQ#	1	I	**Interrupt Request**: When IRQs are enabled, the processor responds to a low level on this input by taking the IRQ interrupt exception.
LOCK/LEN[1]	1	O Rst(X) Hld(Z) Slp(X)	**Atomic Transaction Indicator/Length**: During the first cycle of the issue phase, this signal indicates the current transaction is part of an atomic read-write pair. During the second cycle of the issue phase, this signal is the middle bit of a value which indicates the length of the transaction.
LOWVPP	1	I	**Pad Voltage Level:** When tied to the same level as V_{CCP}, indicates voltage for the device pins (V_{CCP}) is less than 2.5V. When tied to V_{SS}, indicates voltage at the device pins is greater than or equal to 2.5V.
LOWVCC	1	I	**Core Voltage Level:** When tied to the same level as V_{CCP}, indicates voltage for the core (V_{CC}) is less than 1.0V. When tied to V_{SS}, indicates voltage for the core is greater than or equal to 1.0V.
MCLK	1	I	**Memory Clock**: all bus signals must be synchronous to this clock.
N/C	8	N/C	**NO CONNECT**. Do not make electrical connections to these balls.
PLLCFG (Config. Pin)	1	I	**PLL Configuration:** While RESET# is asserted, this pin is sampled by the 80200 to select the initial clock multiplier value. When tied high, the initial clock multiplier is 6. When tied low, the initial clock multiplier is 3. This signal must be tied to a valid level at all times. When using the Intel 80312 I/O companion chip, this signal must be tied high.
PWRSTATUS[1:0]	2	O Rst(0) Hld(Q) Slp(Q)	**Power Status Indicator**: Indicates the current power mode of the Intel® 80200 processor**.** This signal contains an encoded value to indicate the current power state: 00 for Normal 01 for Idle 10 for Reserved (Do Not Use) 11 for Sleep
RESET#	1	I	**Reset**: When asserted, this signal resets the processor. This signal must be asserted for at least 32 consecutive MCLK cycles to achieve a valid reset.
RESETOUT#	1	O Rst(0) Hld(Q) Slp(1)	**Reset Status Output**: This signal is asserted when the processor detects **RESET#**, and deasserts when the processor has completed resetting.
W_R#/LEN[0]	1	O Rst(X) Hld(Z) Slp(X)	**Address Strobe/Length**: During the first cycle of the issue phase, this signal indicates that the current transaction is a read (**W_R#** = 0) or a write (**W_R#** = 1). During the second cycle of the issue phase, this signal is the LSB of a value which indicates the length of the transaction.

1. For signals **D**, **DCB**, **BE#** during Hold mode, these continue to carry valid data until all pending transactions from the 80200 have been completed. Then these signals float.

Table 5. JTAG Pins

Name	Count	Type	Description
TCK	1	I	**TEST CLOCK** is an input which provides the clocking function for the IEEE 1149.1 Boundary Scan Testing (JTAG). State information and data are clocked into the component on the rising edge and data is clocked out of the component on the falling edge.
TDI	1	I	**TEST DATA INPUT** is the serial input pin for the JTAG feature. TDI is sampled on the rising edge of **TCK**, during the SHIFT-IR and SHIFT-DR states of the Test Access Port. This signal has a weak internal pullup to ensure proper operation when this signal is unconnected.
TDO	1	O	**TEST DATA OUTPUT** is the serial output pin for the JTAG feature. **TDO** is driven on the falling edge of **TCK** during the SHIFT-IR and SHIFT-DR states of the Test Access Port. At other times, **TDO** floats.
TRST#	1	I	**TEST RESET** asynchronously resets the Test Access Port (TAP) controller function of IEEE 1149.1 Boundary Scan Testing (JTAG). This signal has a weak internal pullup to ensure proper operation when this signal is unconnected. **TRST#** must be driven low during processor reset to ensure proper operation. Additionally, before performing JTAG test, the processor should be reset and should have a valid clock at **CLK** to ensure it does not enter a low-power mode.
TMS	1	I	**TEST MODE SELECT** is sampled at the rising edge of **TCK** to select the operation of the test logic for IEEE 1149.1 Boundary Scan testing. This signal has a weak internal pullup to ensure proper operation when this signal is unconnected.

3.1.2 241 Lead PBGA Package

Figure 2. 241-Lead PBGA Package

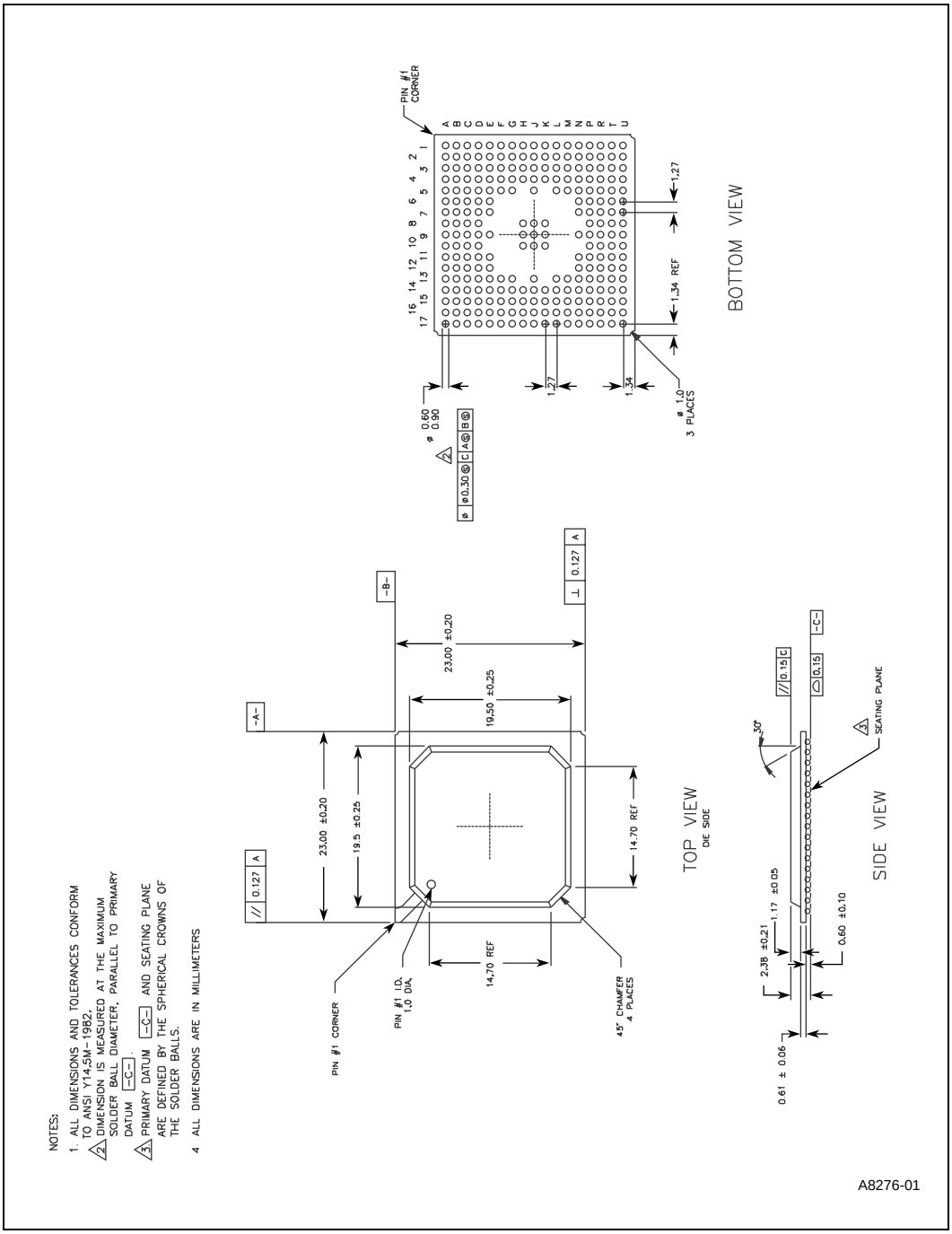


Table 6. 241-Lead PBGA Pinout — Ballpad Number Order (Sheet 1 of 2)

Ball #	Signal	Ball #	Signal	Ball #	Signal
A1	V_{SS}	C8	BE1#	E17	FIQ#
A2	V_{CCP}	C9	BE4#	F1	D32
A3	V_{CC}	C10	ADS#	F2	D6
A4	DCB1	C11	W/R#	F3	D7
A5	DCB2	C12	ABORT	F4	V_{SS}
A6	DCB6	C13	PWRSTATUS1	F5	V_{SS}
A7	BE0#	C14	V_{SS}	F13	V_{SS}
A8	BE3#	C15	V_{SS}	F14	V_{SS}
A9	BE5#	C16	V_{SS}	F15	V_{SS}
A10	BE6#	C17	NC	F16	V_{SS}
A11	LOCK	D1	D0	F17	V_{CC}
A12	NC	D2	D1	G1	D33
A13	RESETOUT#	D3	D2	G2	V_{SS}
A14	PWRSTATUS0	D4	NC	G3	D34
A15	V_{SS}	D5	V_{SS}	G4	D35
A16	V_{CCP}	D6	V_{SS}	G5	V_{CC}
A17	V_{SS}	D7	DCB5	G13	V_{CC}
B1	V_{CCP}	D8	V_{SS}	G14	V_{SS}
B2	V_{SS}	D9	V_{CCP}	G15	V_{SS}
B3	V_{SS}	D10	V_{SS}	G16	V_{CCP}
B4	DVALID	D11	HOLD	G17	RESET#
B5	V_{SS}	D12	V_{CC}	H1	D36
B6	DCB4	D13	V_{SS}	H2	D37
B7	V_{CCP}	D14	V_{SS}	H3	D38
B8	BE2#	D15	NC	H4	V_{SS}
B9	V_{SS}	D16	LOWVCC	H8	V_{SS}
B10	BE7#	D17	V_{CCP}	H9	V_{SS}
B11	V_{CCP}	E1	D3	H10	V_{SS}
B12	CWF	E2	V_{CC}	H14	V_{CCP}
B13	V_{SS}	E3	D4	H15	V_{SS}
B14	HLDA	E4	D5	H16	PLLCFG
B15	V_{CC}	E5	V_{CCP}	H17	NC
B16	V_{SS}	E6	V_{SS}	J1	D39
B17	V_{CC}	E7	V_{CC}	J2	V_{CCP}
C1	V_{CC}	E9	V_{SS}	J3	D8
C2	V_{CCP}	E11	V_{SS}	J4	D9
C3	V_{SS}	E12	V_{SS}	J5	V_{CCP}
C4	V_{CCP}	E13	V_{CCP}	J8	V_{SS}
C5	DCB0	E14	V_{SS}	J9	V_{SS}
C6	DCB3	E15	IRQ#	J10	V_{SS}
C7	DCB7	E16	V_{SS}	J13	V_{CCP}

Table 6. 241-Lead PBGA Pinout — Ballpad Number Order (Sheet 2 of 2)

Ball #	Signal	Ball #	Signal	Ball #	Signal
J14	V_{SS}	N7	V_{CC}	R16	V_{CC}
J15	NC	N9	V_{CCP}	R17	A0
J16	V_{SS}	N11	V_{CC}	T1	D18
J17	NC	N12	V_{SS}	T2	D19
K1	D10	N13	V_{CCP}	T3	V_{CC}
K2	D11	N14	V_{SS}	T4	D50
K3	D12	N15	V_{SS}	T5	V_{SS}
K4	V_{SS}	N16	V_{SS}	T6	D53
K8	V_{SS}	N17	V_{CCP}	T7	V_{CCP}
K9	V_{SS}	P1	D45	T8	D28
K10	V_{SS}	P2	D46	T9	V_{SS}
K14	V_{CCA}	P3	D16	T10	D58
K15	V_{SS}	P4	V_{SS}	T11	V_{CCP}
K16	CLK	P5	D21	T12	D63
K17	MCLK	P6	V_{SS}	T13	V_{SS}
L1	D13	P7	D55	T14	A10
L2	V_{SS}	P8	V_{SS}	T15	V_{SS}
L3	D14	P9	D56	T16	A3
L4	D40	P10	V_{SS}	T17	A1
L5	V_{CC}	P11	A13	U1	D20
L13	V_{CC}	P12	A8	U2	D23
L14	V_{SS}	P13	A4	U3	D48
L15	TRST#	P14	V_{SS}	U4	D49
L16	V_{CCP}	P15	TMS	U5	D51
L17	TCK	P16	NC	U6	D24
M1	D15	P17	TD0	U7	D25
M2	D41	R1	D47	U8	D27
M3	D42	R2	V_{SS}	U9	D30
M4	V_{CC}	R3	D17	U10	D57
M5	V_{SS}	R4	D22	U11	D60
M13	V_{SS}	R5	D52	U12	D62
M14	V_{CCP}	R6	D54	U13	A15
M15	V_{SS}	R7	D26	U14	A14
M16	LOWVPP	R8	D29	U15	A11
M17	TDI	R9	D31	U16	A7
N1	D43	R10	D59	U17	A5
N2	V_{CCP}	R11	D61		
N3	D44	R12	A12		
N4	V_{SS}	R13	A9		
N5	V_{CCP}	R14	A6		
N6	V_{SS}	R15	A2		

Table 7. 241-Lead PBGA Pinout — Signal Name Order (Sheet 1 of 2)

Signal	Ball #	Signal	Ball #	Signal	Ball #
A0	R17	D14	L3	D55	P7
A1	T17	D15	M1	D56	P9
A2	R15	D16	P3	D57	U10
A3	T16	D17	R3	D58	T10
A4	P13	D18	T1	D59	R10
A5	U17	D19	T2	D60	U11
A6	R14	D20	U1	D61	R11
A7	U16	D21	P5	D62	U12
A8	P12	D22	R4	D63	T12
A9	R13	D23	U2	DCB0	C5
A10	T14	D24	U6	DCB1	A4
A11	U15	D25	U7	DCB2	A5
A12	R12	D26	R7	DCB3	C6
A13	P11	D27	U8	DCB4	B6
A14	U14	D28	T8	DCB5	D7
A15	U13	D29	R8	DCB6	A6
ABORT	C12	D30	U9	DCB7	C7
BE0#	A7	D31	R9	DVALID	B4
BE1#	C8	D32	F1	HLDA	B14
BE2#	B8	D33	G1	HOLD	D11
BE3#	A8	D34	G3	LOCK	A11
BE4#	C9	D35	G4	LOWVCC	D16
BE5#	A9	D36	H1	LOWVPP	M16
BE6#	A10	D37	H2	MCLK	K17
BE7#	B10	D38	H3	ADS#	C10
CLK	K16	D39	J1	NC	A12
CWF	B12	D40	L4	NC	C17
D0	D1	D41	M2	NC	D4
D1	D2	D42	M3	NC	D15
D2	D3	D43	N1	NC	J15
D3	E1	D44	N3	NC	J17
D4	E3	D45	P1	NC	H17
D5	E4	D46	P2	NC	P16
D6	F2	D47	R1	FIQ#	E17
D7	F3	D48	U3	IRQ#	E15
D8	J3	D49	U4	RESET#	G17
D9	J4	D50	T4	RESETOUT#	A13
D10	K1	D51	U5	TRST#	L15
D11	K2	D52	R5	PLLCFG	H16
D12	K3	D53	T6	PWRSTATUS0	A14
D13	L1	D54	R6	PWRSTATUS1	C13

Table 7. 241-Lead PBGA Pinout — Signal Name Order (Sheet 2 of 2)

Signal	Ball #	Signal	Ball #	Signal	Ball #
TCK	L17	V_{CC}	L5	V_{SS}	H15
TD0	P17	V_{CC}	M4	V_{SS}	H4
TDI	M17	V_{CC}	N11	V_{SS}	H8
TMS	P15	V_{CC}	N7	V_{SS}	H9
V_{CCA}	K14	V_{CC}	R16	V_{SS}	J10
V_{CCP}	A16	V_{CC}	T3	V_{SS}	J14
V_{CCP}	A2	V_{SS}	A1	V_{SS}	J16
V_{CCP}	B1	V_{SS}	A15	V_{SS}	J8
V_{CCP}	B11	V_{SS}	A17	V_{SS}	J9
V_{CCP}	B7	V_{SS}	B13	V_{SS}	K10
V_{CCP}	C2	V_{SS}	B16	V_{SS}	K15
V_{CCP}	C4	V_{SS}	B2	V_{SS}	K4
V_{CCP}	D17	V_{SS}	B3	V_{SS}	K8
V_{CCP}	D9	V_{SS}	B5	V_{SS}	K9
V_{CCP}	E13	V_{SS}	B9	V_{SS}	L14
V_{CCP}	E5	V_{SS}	C14	V_{SS}	L2
V_{CCP}	G16	V_{SS}	C15	V_{SS}	M13
V_{CCP}	H14	V_{SS}	C16	V_{SS}	M15
V_{CCP}	J13	V_{SS}	C3	V_{SS}	M5
V_{CCP}	J2	V_{SS}	D10	V_{SS}	N12
V_{CCP}	J5	V_{SS}	D13	V_{SS}	N14
V_{CCP}	L16	V_{SS}	D14	V_{SS}	N15
V_{CCP}	M14	V_{SS}	D5	V_{SS}	N16
V_{CCP}	N13	V_{SS}	D6	V_{SS}	N4
V_{CCP}	N17	V_{SS}	D8	V_{SS}	N6
V_{CCP}	N2	V_{SS}	E11	V_{SS}	P10
V_{CCP}	N5	V_{SS}	E12	V_{SS}	P14
V_{CCP}	N9	V_{SS}	E14	V_{SS}	P4
V_{CCP}	T11	V_{SS}	E16	V_{SS}	P6
V_{CCP}	T7	V_{SS}	E6	V_{SS}	P8
V_{CC}	A3	V_{SS}	E9	V_{SS}	R2
V_{CC}	B15	V_{SS}	F13	V_{SS}	T13
V_{CC}	B17	V_{SS}	F14	V_{SS}	T15
V_{CC}	C1	V_{SS}	F15	V_{SS}	T5
V_{CC}	D12	V_{SS}	F16	V_{SS}	T9
V_{CC}	E2	V_{SS}	F4	W/R#	C11
V_{CC}	E7	V_{SS}	F5		
V_{CC}	F17	V_{SS}	G14		
V_{CC}	G13	V_{SS}	G15		
V_{CC}	G5	V_{SS}	G2		
V_{CC}	L13	V_{SS}	H10		

3.2 Package Thermal Specifications

3.3 Package Thermal Resistance

The Intel® 80200 processor is specified for operation when T_C (case temperature) is within the range of 0°C to 90°C. Case temperature may be measured in any environment to determine whether the device is within its specified operating range. The case temperature should be measured at the center of the top surface, opposite the pins.

θ_{CA} is the thermal resistance from case to ambient. Use the following equation to calculate T_A, the maximum ambient temperature to conform to a particular case temperature:

$$T_A = T_C - P (\theta_{CA})$$

Junction temperature (T_J) is commonly used in reliability calculations. T_J can be calculated from θ_{JC} (thermal resistance from junction to case) using the following equation:

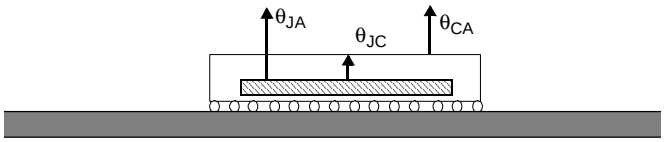
$$T_J = T_C + P (\theta_{JC})$$

Similarly, when T_A is known, the corresponding case temperature (T_C) can be calculated as follows:

$$T_C = T_A + P (\theta_{CA})$$

Table 8. Package Thermal Resistance — °C/Watt

Parameter	Airflow — ft./min (m/sec)			
	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)
θ_{JC} (Junction-to-Case)	1.5	1.5	1.5	1.5
θ_{CA} (Case-to-Ambient) (No Heatsink)	28.5	20.0	18.1	17.1



NOTES:
1. This table applies to an PBGA device soldered directly into a board with all V_{SS} connections.
2. $\theta_{JA} = \theta_{JC} + \theta_{CA}$

Figure 3 and Figure 4 show an application of the supplied thermal data. Here, we plot the case temperature under several conditions.

Figure 3. Case Temperature with No Air Flow

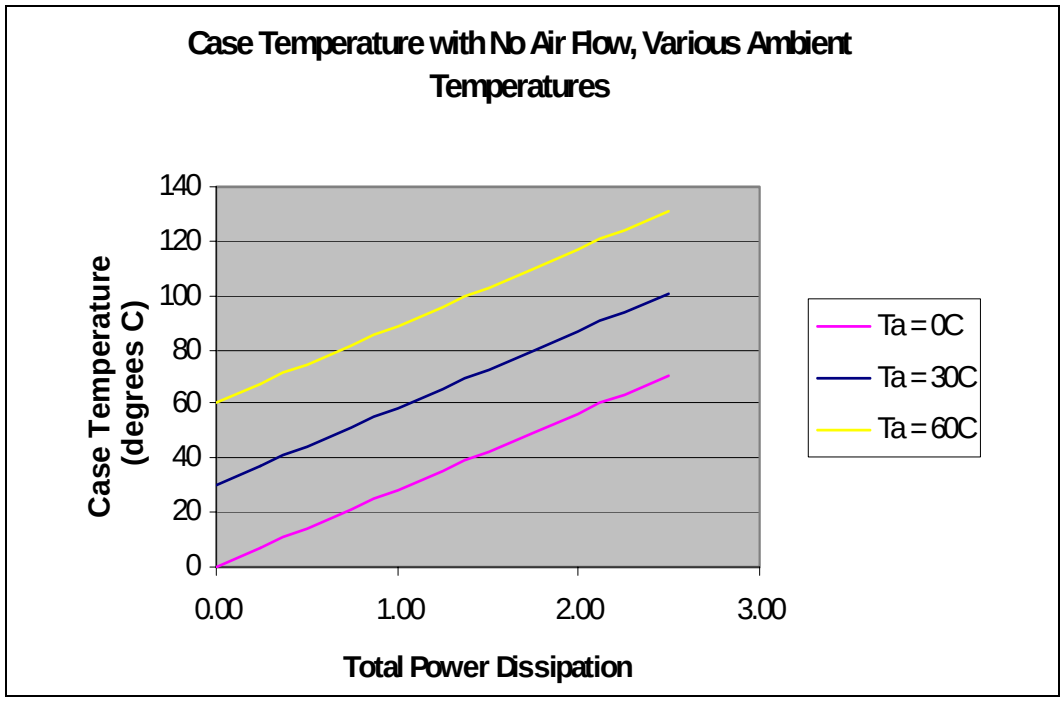
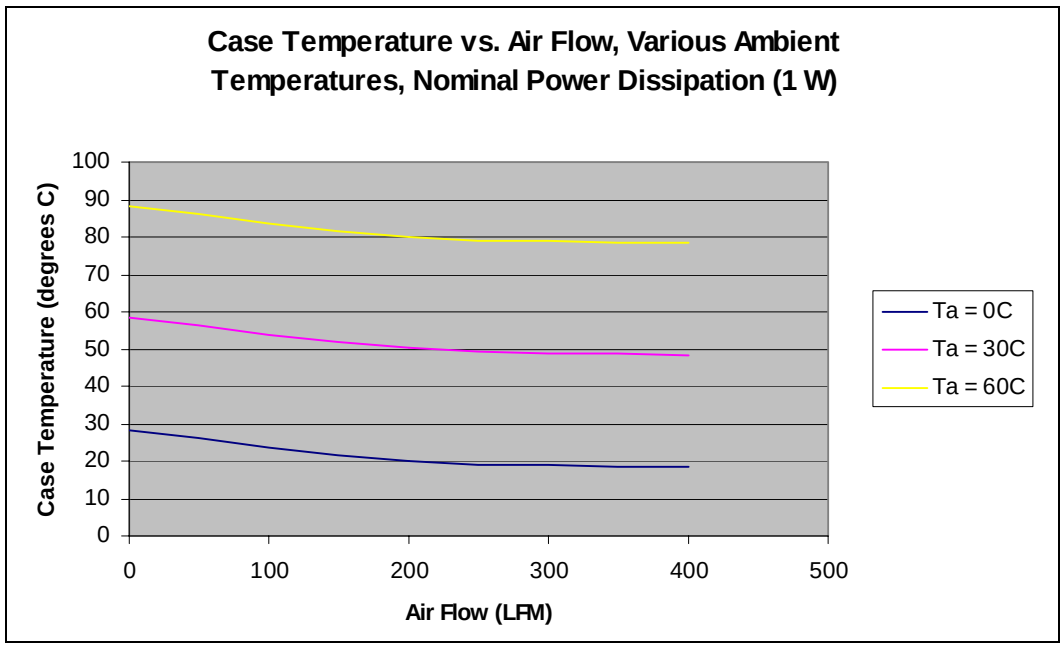


Figure 4. Case Temperature at Nominal Power Dissipation



4.0 Electrical Specifications

4.1 Absolute Maximum Ratings

Parameter	Maximum Rating
Storage Temperature	–55°C to + 125°C
Case Temperature Under Bias	0°C to + 90°C
Supply Voltage V_{CC} wrt. V_{SS}	2.1V
Supply Voltage V_{CCP} wrt. V_{SS}	5.0V
Supply Voltage V_{CCA} wrt. V_{SS}	2.1V
Voltage on Any Ball wrt. V_{SS}	–0.5 V to V_{CCP} + 0.5 V

NOTICE: This data sheet contains information on products in the design phase of development. Do not finalize a design with this information. Revised information is published when the product becomes available. The specifications are subject to change without notice. Contact your local Intel representative before finalizing a design.

†**WARNING:** Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

Table 9. Operating Conditions

Symbol	Parameter	Min	Max	Units	Notes
V_{CC}	Core Supply Voltage	0.95	1.55	V	
V_{CCP}	Periphery Supply Voltage	3.0	3.6	V	
V_{CCA}	Analog Supply Voltage	0.95	1.55	V	
F_{P_CLK}	Input Clock Frequency	33.33	66.66	MHz	
T_C	Case Temperature Under Bias	0	90	°C	

Table 10. Voltage Range Requirements for Intel® 80200 Processor Product Options

Product Options	Operating @ 333MHz	Operating @ 400MHz	Operating @ 600MHz	Operating @ 733MHz
80200M733	1.0v — 1.5v	1.1v — 1.5v	1.3v — 1.5v	1.5v ±5%
80200M600	1.1v — 1.5v	1.3v —1.5v	1.5v ±5%	—
80200M400	1.1v — 1.3v	1.3v ±5%	—	—

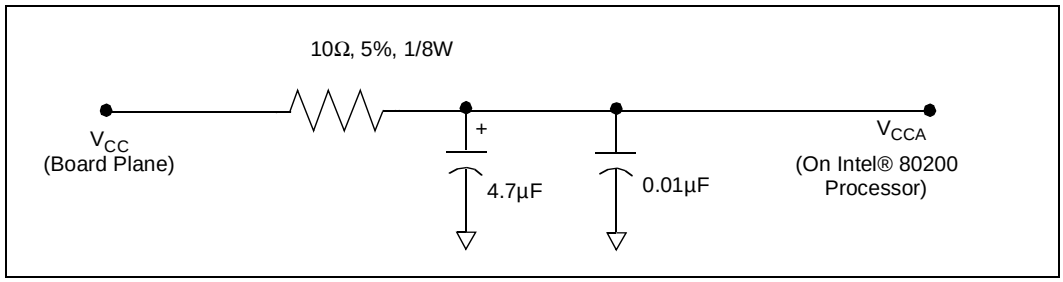
NOTES:
1. Processor operation beyond the voltage and frequency (as marked on the device) is not guaranteed.
2. Includes VCC and VCCA.

4.2 V_{CCA} Pin Requirements

To reduce voltage supply noise on the Intel® 80200 processor, the V_{CCA} pin for the Phase Lock Loop (PLL) circuit is isolated on the pinout. The lowpass filter, as shown in Figure 5, reduces noise induced clock jitter and its effects on timing relationships in system designs.

The trace lengths between the 4.7µF capacitor, the 0.01µF capacitor, and V_{CCA} must be as short as possible.

Figure 5. V_{CCA} Lowpass Filter



4.3 Targeted DC Specifications

Table 11. DC Characteristics

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.4 2.1	V_{CCP} + 0.5 V_{CCP} + 0.5	V	A-1 step D-0 step
V_{OL}	Output Low Voltage		0.3	V	1
V_{OH}	Output High Voltage	V_{CCP} - 0.3		V	2
C_{IN}	Input Capacitance		5	pF	
C_{OUT}	I/O or Output Capacitance		5	pF	
C_{CLK}	CLK Capacitance		5	pF	
L_{PIN}	Ball Inductance		TBD	nH	

NOTES:
1. V_{OL} measured at I_{OL} = 3mA
2. V_{OH} measured at I_{OH} = 2mA

Table 12. I_{CC} Characteristics

Symbol	Parameter	Typ	Max	Units	Notes
I_{LO}	Output Leakage Current		220	µA	$0.4 \le V_{OUT} \le V_{CC}$
I_{LI}	Input Leakage Current		220	µA	$0 \le V_{IN} \le V_{CC}$
I_{CC} Active (Power Supply)	**Core and Analog Current** 733MHz at 1.5v Icc Icca 600MHz at 1.3v Icc Icca 400MHz at 1.3v Icc Icca **Periphery Current** 100MHz at 3.6v Iccp		 720 95 520 65 410 13 165	 mA mA mA mA mA mA mA	For typical power dissipation, see section 4.9
I_{CC} Active (Idle Mode)	Idle Mode at 1.5v Icc Icca at 1.3v Icc Icca		 190 700 135 600	 mA µA mA µA	
I_{CC} Active (Sleep Mode)	Sleep Mode	TBD	TBD	mA	

4.4 Targeted AC Specifications

4.4.1 Clock Signal Timings

Table 13. Input Clock Timings

Symbol	Parameter	Min	Max	Units	Notes
T_F	**CLK** Frequency	33.33	66.66	MHz	
T_C	**CLK** Period	15	30	ns	(1)
T_{CS}	**CLK** Period Stability		20	ps	Adjacent Clocks (2)
T_{CH}	**CLK** High Time	5		ns	Measured at 1.5 V (2)
T_{CL}	**CLK** Low Time	5		ns	Measured at 1.5 V (2)
T_{CR}	**CLK** Rise Slew Rate	1.5	3.5	V/ns	0.4 V to 2.4 V (2)
T_{CF}	**CLK** Fall Slew Rate	1.5	3.5	V/ns	2.4 V to 0.4 V (2)
T_{MF}	**MCLK** Frequency	0	100	MHz	
T_{MC}	**MCLK** Period	10		ns	(1)
T_{MCS}	**MCLK** Period Stability		250	ps	Adjacent Clocks (2)
T_{MCH}	**MCLK** High Time	2.5		ns	Measured at 1.5 V (2)
T_{MCL}	**MCLK** Low Time	2.5		ns	Measured at 1.5 V (2)
T_{MCR}	**MCLK** Rise Slew Rate	1.5	4.5	V/ns	0.4 V to 2.4 V (2)
T_{MCF}	**MCLK** Fall Slew Rate	1.5	4.5	V/ns	2.4 V to 0.4 V (2)

NOTES:
1. See Figure 6 and Figure 7.
2. Not tested.

4.4.2 Bus Signal Timings

Table 14. Output Timings

Symbol	Parameter	Min	Max	Units	Notes
T_{OV1}	Output valid delay from **MCLK** -- **D[63:0], DCB,** and **BE#**	1.5	6.9	ns	(1, 2)
T_{OF1}	Output float delay from **MCLK** -- **D[63:0]**, **DCB,** and **BE#**	1.1	6.0	ns	(1, 2, 3)
T_{OS1}	Output Slew Rate -- **D[63:0], DCB,** and **BE#**	1.0	4.0	V/ns	0.4 V to 2.4 V (1, 2, 4)
T_{OV2}	Output valid delay from **MCLK** -- **A[15:0], HLDA, W/R#, LOCK,** and **ADS#**	1.5	6.8	ns	(1, 2, 4)
T_{OF2}	Output float delay from **MCLK** -- **A[15:0], HLDA, W/R#, LOCK, ADS#, RESETOUT#,** and **PWRSTATUS**	1.1	6.0	ns	(1, 2, 3, 4)
T_{OS2}	Output Slew Rate -- **A[15:0], HLDA, W/R#, LOCK, ADS#, RESETOUT#,** and **PWRSTATUS**	1.0	4.0	V/ns	0.4 V to 2.4 V (1, 2, 4)

NOTES:
1. Minimum values characterized with a 10 pF load at 3.6 V, 0°C
2. Maximum values characterized with a 30 pF load at 2.9 V., 110°C
3. Pin is floating when its output falls to I_{LO}
4. Not tested

Table 15. Input Timings

Symbol	Parameter	Min	Max	Units	Notes
T_{IS}	Input setup time to **MCLK** -- **ABORT, CWF, DVALID, D,** and **DCB**	1.2		ns	
T_{IH}	Input hold time from **MCLK** -- **ABORT, CWF, DVALID, D,** and **DCB**	1.5		ns	
T_{ISH}	Input setup time to **MCLK** -- **HOLD**	1.3		ns	
T_{IHH}	Input hold time from **MCLK** -- **HOLD**	0.9		ns	

4.4.3 Boundary Scan Test Signal Timings

Table 16. Boundary Scan Test Signal Timings

Symbol	Parameter	Min	Max	Units	Notes
T_{BSF}	**TCK** Frequency	0.0	40.0	MHz	
T_{BSCH}	**TCK** High Time	12.5		ns	Measured at 1.5 V
T_{BSCL}	**TCK** Low Time	12.5		ns	Measured at 1.5 V
T_{BSCR}	**TCK** Rise Time		5.0	ns	0.8 V to 2.0 V
T_{BSCF}	**TCK** Fall Time		5.0	ns	2.0 V to 0.8 V
T_{BSIS1}	Input Setup to **TCK** — **TDI**, **TMS**	4.0		ns	
T_{BSIH1}	Input Hold from **TCK** — **TDI**, **TMS**	6.0		ns	
T_{BSIS2}	Input Setup to **TCK** — **TRST#**	25.0		ns	
T_{BSIH2}	Input Hold from **TCK** — **TRST#**	3.0		ns	
T_{BSOV1}	**TDO** Valid Delay	1.5	6.9	ns	Relative to falling edge of **TCK**
T_{OF1}	**TDO** Float Delay	1.1	5.4	ns	Relative to falling edge of **TCK**
T_{OV12}	All Outputs (Non-Test) Valid Delay	1.5	6.9	ns	Relative to falling edge of **TCK**
T_{OF2}	All Outputs (Non-Test) Float Delay	1.1	5.4	ns	Relative to falling edge of **TCK**
T_{IS10}	Input Setup to **TCK** — All Inputs (Non-Test)	4.0		ns	
T_{IH8}	Input Hold from **TCK** — All Inputs (Non-Test)	6.0		ns	

4.5 AC Timing Waveforms

Figure 6. CLK Waveform

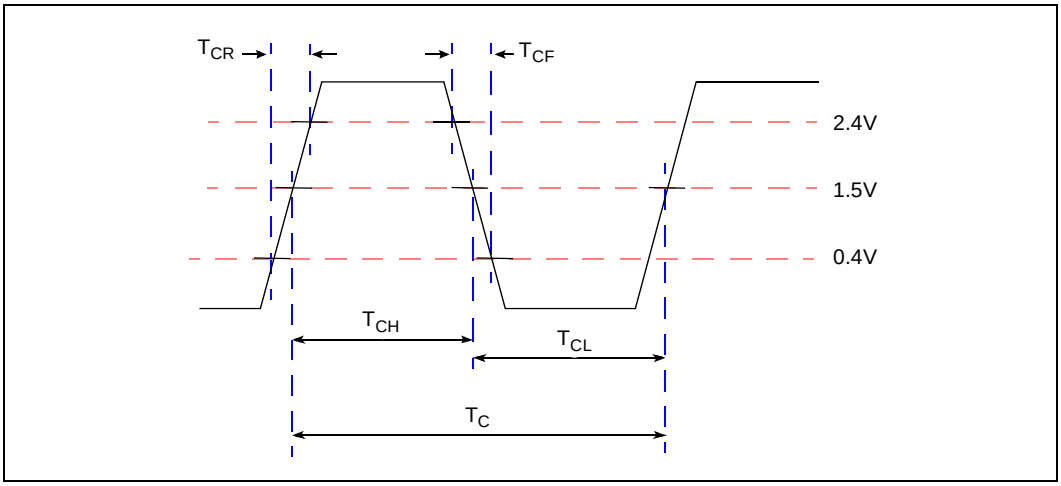


Figure 7. MCLK Waveform

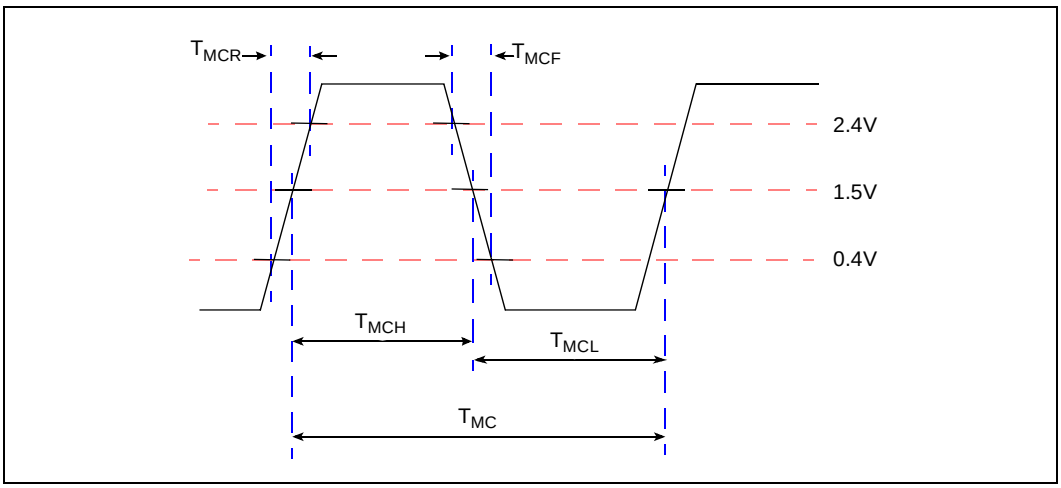
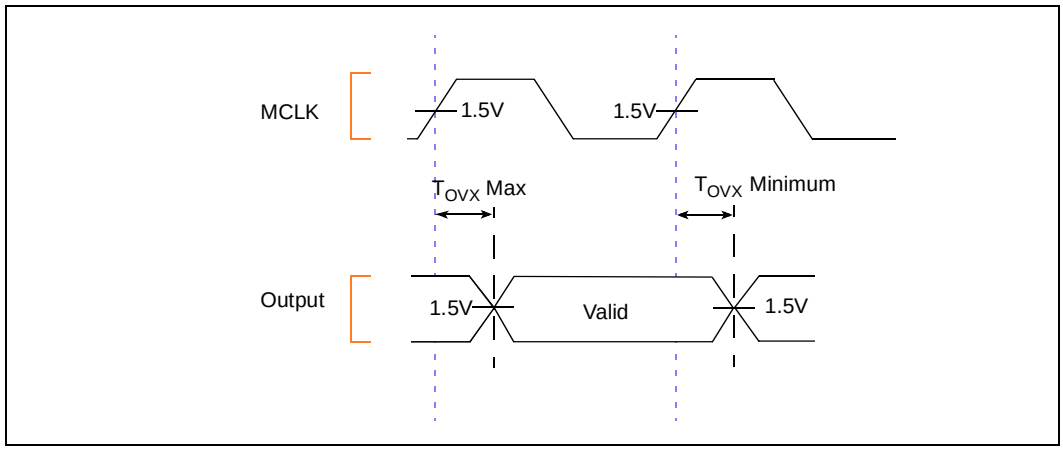


Figure 8. T_{OV} Output Delay Waveform



4.6 Power Sequence

Power must be supplied to the component's pads (V_{CCP}) before or concurrently with power to the components core (V_{CC}). Power must not be applied to V_{CC} prior to V_{CCP}. Figure 9 and Figure 10 show correct power sequences. Figure 11 shows an incorrect power sequence; do not allow this.

Figure 9. Correct Power Sequence for V_{CC}, V_{CCP}

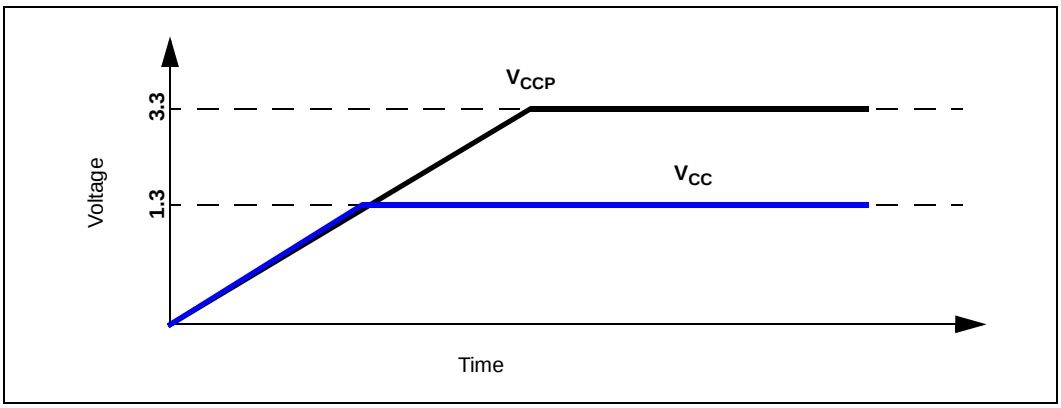


Figure 10. Another Correct Power Sequence for V_{CC}, V_{CCP}

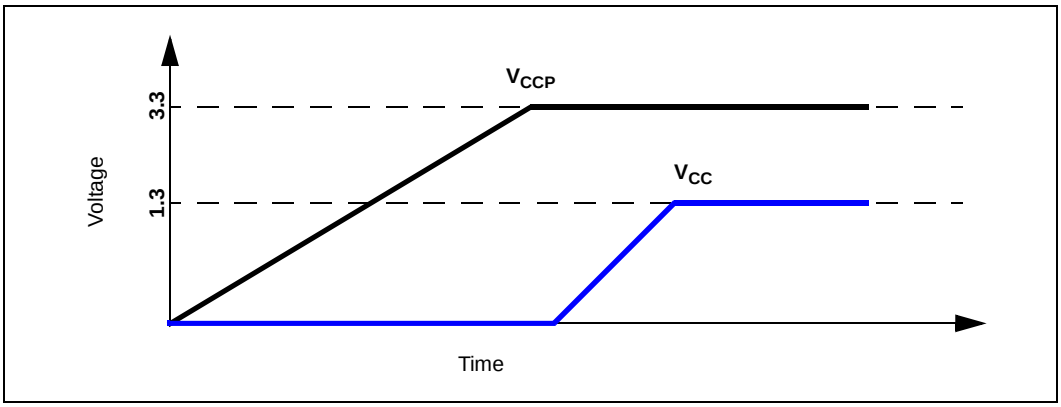
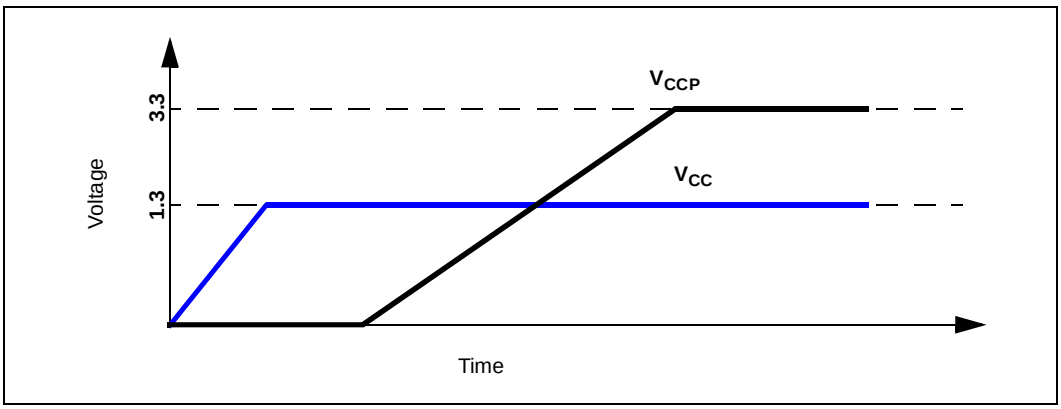


Figure 11. Incorrect Power Sequence for V_{CC}, V_{CCP}



V_{CC} and V_{CCA} (PLL supply) should be brought up concurrently. When this cannot be attained, V_{CC} should be brought up before V_{CCA}. Figure 12 shows the preferred method where V_{CC} and V_{CCA} are brought up at the same time. Figure 13 shows the alternative.

Figure 12. Preferred Power Sequence for VCC, VCCa

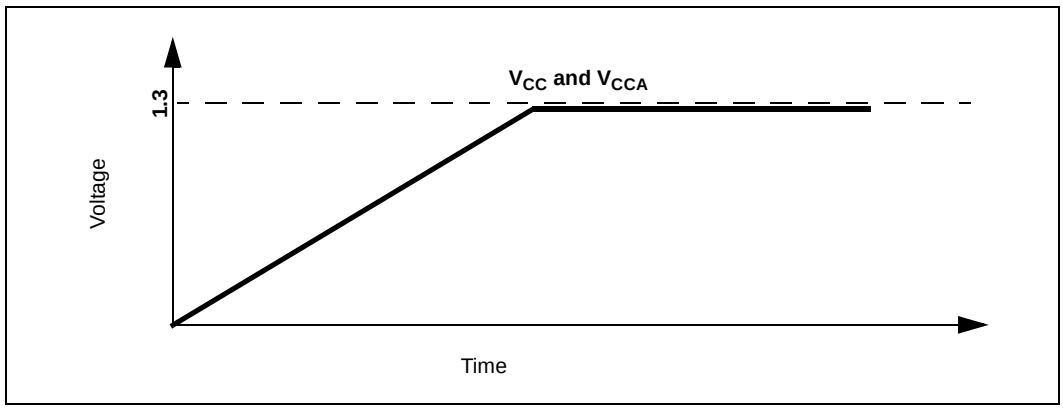
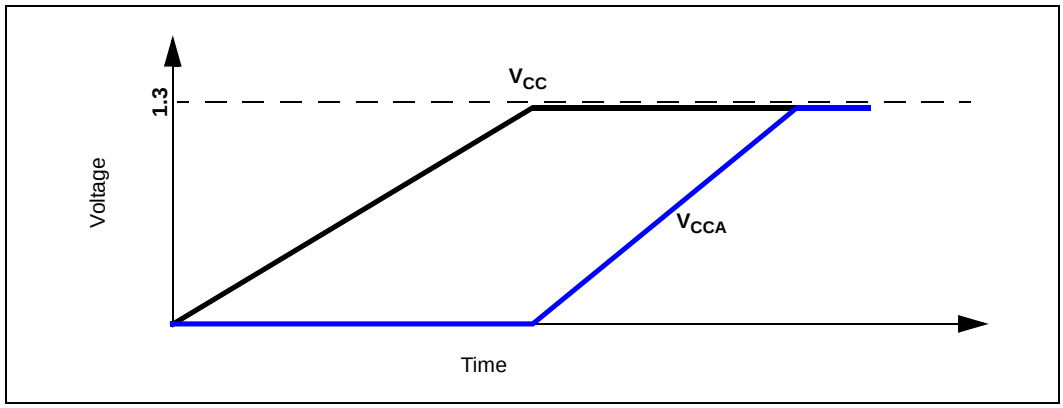


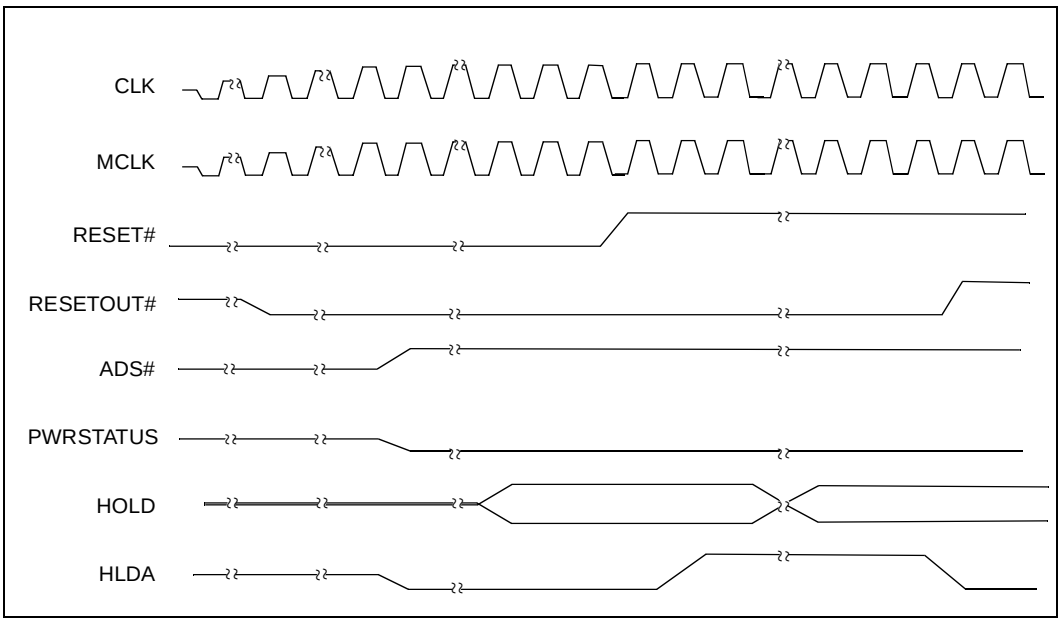
Figure 13. Correct Power Sequence for VCC, VCCa



4.7 Reset Timing

Figure 14 shows the sequence of pin states that may be assumed at processor reset. See the *Intel® 80200 Processor based on Intel® XScale™ Microarchitecture Developer's Manual* for more information on reset timing.

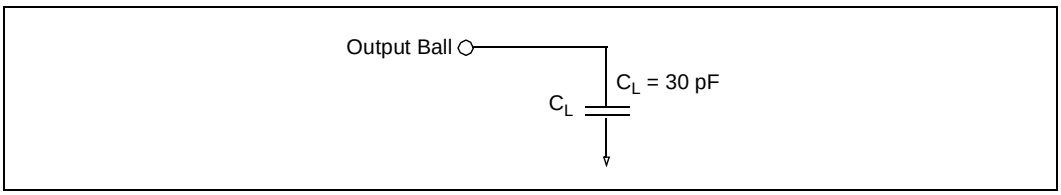
Figure 14. Pins' State at Reset



4.8 AC Test Conditions

The AC specifications in Section 4.4, "Targeted AC Specifications" on page 27 are tested with a 30 pF load indicated in Figure 15.

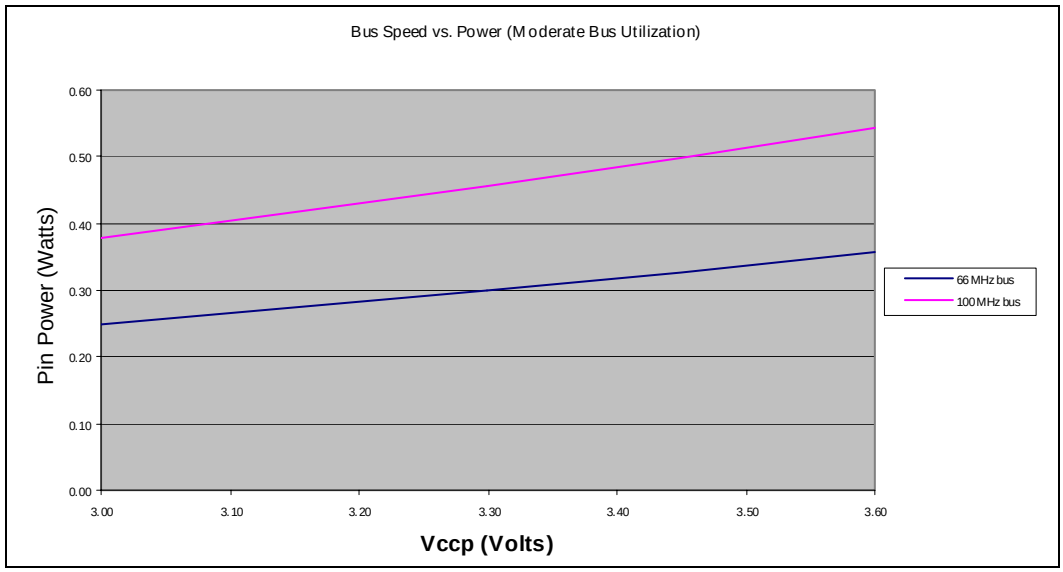
Figure 15. AC Test Load



4.9 Typical Power Dissipation

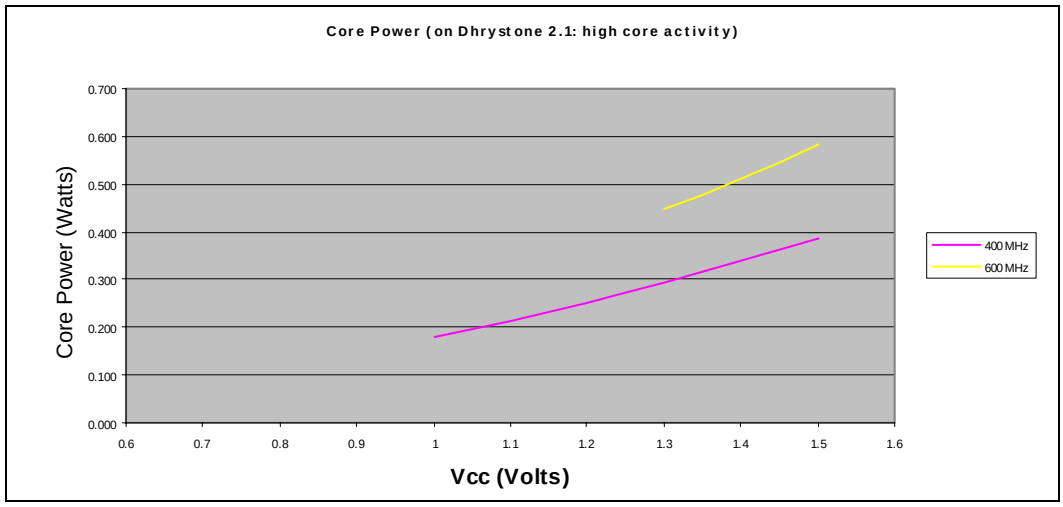
The total dissipated power is the sum of the power requirements from the device pins and the internal logic. Both are dependent on the operating frequency, voltage, and activity. Because the device pins are operating under different conditions than the internal logic, the typical power dissipation curves for both are in this section.

Figure 16. Typical Pin Power Dissipation[1]



1. Assume system driving one PC-100 DIMM and a companion chip with 10pF/pin capacitance.

Figure 17. Typical Core Power Dissipation



This Page Intentionally Left Blank