aSC7621

HARDWARE MONITOR WITH INTEGRATED FAN CONTROL

Preliminary Specification

PRODUCT SPECIFICATION

Product Description

The aSC7621 has a two wire digital interface compatible with SMBus 2.0. Using a 10-bit ΣΔ- ADC, the aSC7621 measures the temperature of two remote diode connected transistors as well as its own die. Support for Platform Environmental Control Interface (PECI) is included.

Using temperature information from these four zones, an automatic fan speed control algorithm is employed to minimize acoustic impact while achieving recommended CPU temperature under varying operational loads.

To set fan speed, the aSC7621 has three independent pulse width modulation (PWM) outputs that are controlled by one, or a combination of three, temperature zones. Both high- and low-frequency PWM ranges are supported. The aSC7621 also includes a digital filter that can be invoked to smooth temperature readings for better control of fan speed and minimum acoustic impact. The aSC7621 has tachometer inputs to measure fan speed on up to four fans. Limit and status registers for all measured values are included to alert the system host that any measurements are outside of programmed limits via status registers.

System voltages of VCCP, 2.5V, 3.3V, 5.0V, and 12V motherboard power are monitored efficiently with internal scaling resistors.

Features

- Supports PECI interface and monitors internal and remote thermal diodes
- 2-wire, SMBus 2.0 compliant, serial interface
- 10-bit ΣΔ-ADC
- Monitors VCCP, 2.5V, 3.3V, 5.0V, and 12V motherboard/processor supplies
- Programmable autonomous fan control based on temperature readings
- Noise filtering of temperature reading for fan speed control
- 0.25°C digital temperature sensor resolution
- 3 PWM fan speed control outputs for 2-, 3- or 4-wire fans and up to 4 fan tachometer inputs
- Enhanced measured temperature to Temperature Zone assignment.
- Provides high and low PWM frequency ranges
- 3 GPIO pins for custom use
- 24-Lead QSOP package

Measurement System

Temperature:

- 0.25°C resolution, ±2°C accuracy on remote diode
- 0.25°C resolution, ±3°C accuracy on local sensor
- Temperature measurement range on remote sensor –55°C to +125°C using 2's complement coding.

Voltage:

- 10-bit Resolution, ±2% (TUE)

Fan Tachometer:

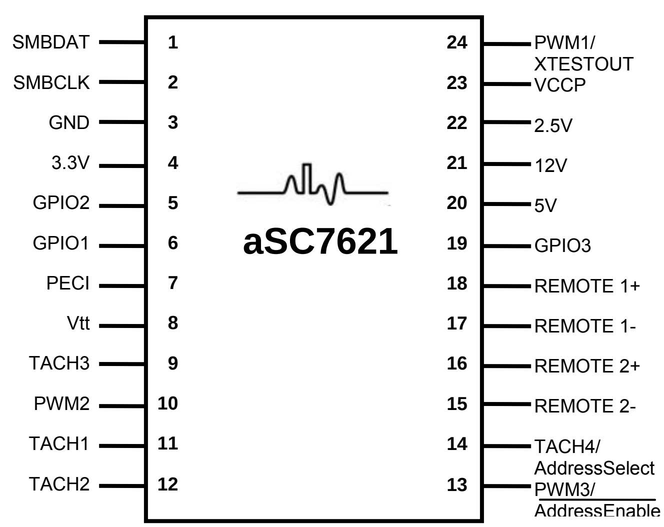
- 16-bit count of 90kHz clock periods

Limit alarms for all measured values

Applications

- Desktop Computers – Motherboards and Graphics Cards
- Microprocessor based equipment (e.g. Base-stations, Routers, ATMs, Point of Sales)

Connection Diagram



Ordering Information

Part Number	Package	Temperature Range and Operating Voltage	Marking	How Supplied
aSC7621QS24	24-lead QSOP	0°C to +120°C, 3.3V	aSC7621 Ayww	2500 units Tape & Reel

Ayww – Assembly site, year, workweek

Block Diagram

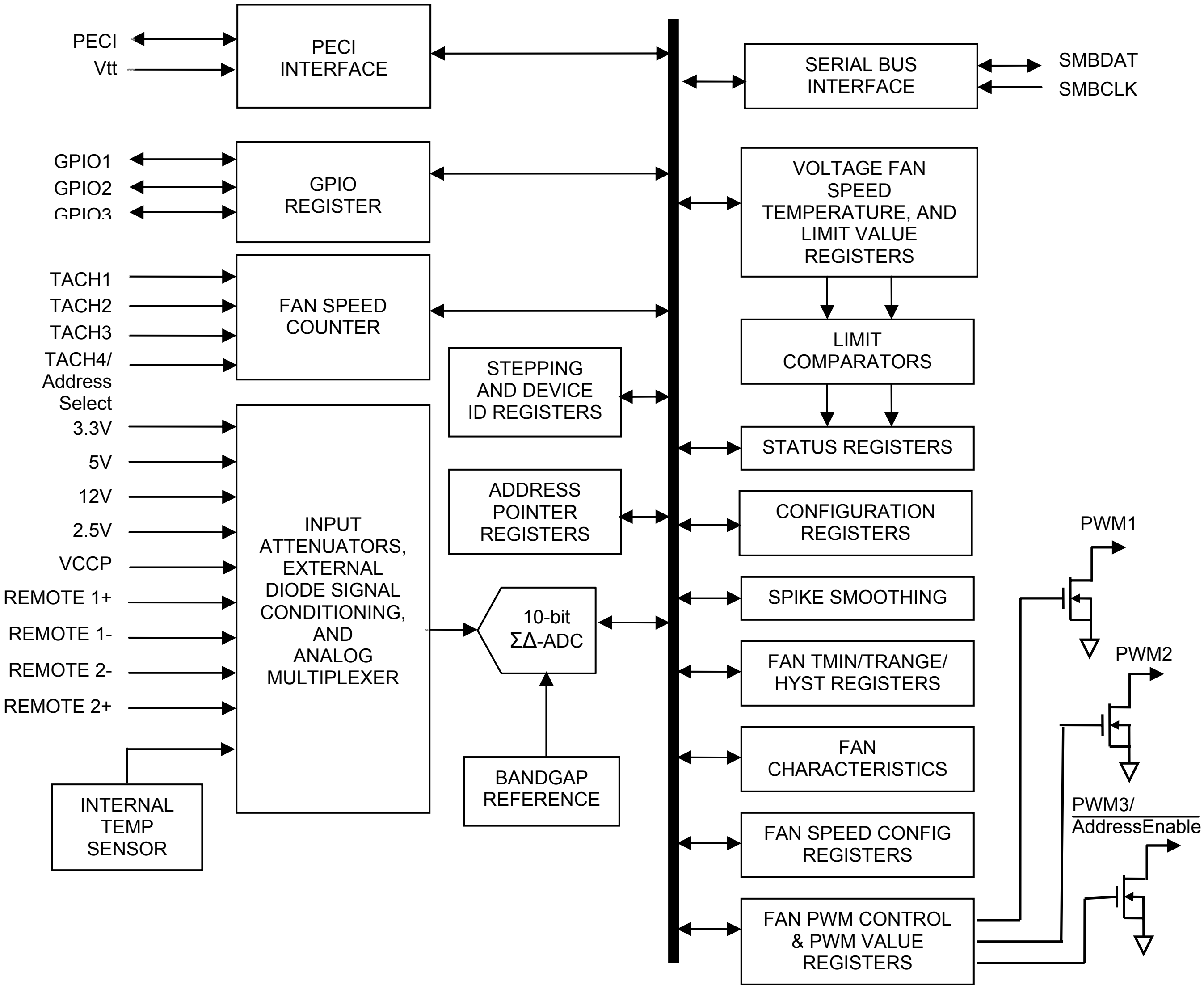


Figure 1 Block Diagram

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Pin Descriptions

	Symbol	Pin	Type	Name and Function/Connection
SMBus	SMBDAT	1	Digital I/O (Open-Drain)	System Management Bus Data. Open-drain output. 5V tolerant, SMBus 2.0 compliant.
	SMBCLK	2	Digital Input	System Management Bus Clock. Tied to Open-drain output. 5V tolerant, SMBus 2.0 compliant.
PECI	PECI	7	Digital I/O	Platform Environmental Control Interface (PECI). PECI 1.0 compliant, CPU digital thermometer input
	Vtt	8	Analog Input	PECI reference voltage.
Power	3.3V	4	POWER	+3.3V pin. Can be powered by +3.3V Standby power if monitoring in low power states is required. This pin should be bypassed with a 0.1µF capacitor in parallel with 100pF. A bulk capacitance of approximately 10µF needs to be in near vicinity of the aSC7621.
	GND	3	GROUND	Ground for all analog and digital circuitry.
Voltage Inputs	5V	20	Analog Input	Analog Input for +5V monitoring.
	12V	21	Analog Input	Analog Input for +12V monitoring.
	2.5V	22	Analog Input	Analog Input for +2.5V monitoring..
	VCCP	23	Analog Input	Analog Input for VCCP (processor voltage) monitoring.
Remote	Remote 1+	18	Remote Thermal Diode Positive Input	Positive input (current source) from the first remote thermal diode Serves as the positive input into the A/D. Connected to THERMDA pin of Pentium processor.
	Remote 1-	17	Remote Thermal Diode Negative Input	Negative input (current sink) from the first remote thermal diode Serves as the negative input into the A/D. Connected to THERMDC pin of Pentium processor.
	Remote 2+	16	Remote Thermal Diode Positive Output	Positive input (current source) from the second remote thermal diode Serves as the positive input into the A/D. Connected to the base of a diode connected MMBT3904 NPN transistor.
	Remote 2-	15	Remote Thermal Diode Negative Input	Negative input (current sink) from the second remote thermal diode Serves as the negative input into the A/D. Connected to the emitter of a diode connected MMBT3904 NPN transistor.
Fan Tachometer Inputs	TACH1	11	Digital Input	Input for monitoring tachometer output of fan 1.
	TACH2	12	Digital Input	Input for monitoring tachometer output of fan 2.
	TACH3	9	Digital Input	Input for monitoring tachometer output of fan 3. During power-up, if held low through a 10KΩ resistor, SMBus address may be selected based on the state of TACH4 pin.
	TACH4/AddressSelect	14	Digital Input	Input for monitoring tachometer output of fan 4. If in Address Select Mode, determines the SMBus address of aSC7621.
Fan Control	PWM1/XTESTOUT	24	Digital Open-Drain Output	Fan speed control 1. When in XOR tree test mode, functions as XOR Tree output.
	PWM2	10	Digital Open-Drain Output	Fan speed control 2.
	PWM3/$\overline{\text{Address Enable}}$	13	Digital Open-Drain Output	Fan speed control 3. Pull to ground at power on to enable Address Select Mode (Address Select pin controls SMBus address of the device).

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	Symbol	Pin	Type	Name and Function/Connection
GPIO	GPIO1	6	Digital I/O	Alert Out / Zone # THERM Out. Default is GPIO input
	GPIO2	5	Digital I/O	Alert Out / Zone # THERM Out. Default is GPIO input
	GPIO3	19	Digital I/O	Alert Out / Zone # THERM Out. Default is GPIO input

Absolute Maximum Ratings[1]

Parameter		Rating
Supply Voltage, V_{DD}		3.6V
Voltage on Any Digital Input or Output Pin other than PWM Outputs		-0.3V to V_{DD} +0.3V
Voltage on PWM Outputs		-0.3V to 5.5V
Voltage on 12V Analog Input		-0.5V to 16V
Voltage on 5V Analog Input		-0.5V to 6.5V
Voltage on Remote 1 +, Remote 2 +		-0.5V to (V_{DD} + 0.50V)
Voltage on Other Analog Inputs		-0.5V to 6.0V
Current on Remote 1 -, Remote 2 -		±1mA
Input Current on Any Pin[2]		±5mA
Package Input Current[2]		±20mA
Package Dissipation at T_A = 25°C		See (Note 3)
Storage Temperature		-65°C to +150°C
ESD[4]	Human Body Model	4000 V
	Machine Model	250 V
	Charged Device Model	2000V

Operating Ratings[1]

Parameter	Rating
aSC7621 Operating Temperature Range, Ambient Temperature, T_{MIN} to T_{MAX}	0°C ≤ T_A ≤ +120°C
Remote Diode Temperature Range	-55°C ≤ T_D ≤ +125°C
Supply Voltage (3.3V nominal)	+3.0V to +3.6V
V_{IN} Voltage Range	
+12V V_{IN}	-0.05V to 16V
+5V V_{IN}	-0.05V to 6.5V
+3.3V V_{IN}	3.0V to 4.4V
VCCP and All Other Inputs	-0.05V to V_{DD} + 0.05V
Typical Supply Current	1.8mA

Notes:

1. Absolute maximum ratings are limits beyond which operation may cause permanent damage to the device. These are stress ratings only; functional operation at or above these limits is not implied.
2. When the input voltage (V_{IN}) at any pin exceeds the power supplies (V_{IN} < GND or V_{IN} > V_{DD}), the current at that pin should be limited to 5mA. The 20mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 5mA to four. Parasitic components and/or ESD protection circuitry are present on the aSC7621 pins. Care should be taken not to forward bias the parasitic diode present on pins D+ and D-. Doing so by more than 50mV may corrupt temperature measurements.
3. Thermal resistance junction-to-ambient when attached to a double-sided printed circuit board with 1oz. foil is 115°C/W
4. Human Body Model: 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Machine Model: 200pF capacitor discharged directly into each pin. Charged-Device Model is per JESD22-C101C.

DC Electrical Characteristics[5]

The following specifications apply for V_{DD} = 3.0V to 3.6V, and all analog input source impedance R_s = 50Ω unless otherwise specified in conditions. **Boldface limits apply for $T_A = T_J$ over T_{MIN} to T_{MAX}**; all other limits $T_A = T_J$ = 25°C. T_A is the ambient temperature of the aSC7621; T_J is the junction temperature of aSC7621; T_D is the remote thermal diode junction temperature. Specifications subject to change without notice

Parameter		Conditions	Min	Typ	Max	Units
POWER SUPPLY CHARACTERISTICS						
Supply Current		Converting, Interface and Fans Inactive, Peak Current		1.8	**3.5**	mA(max)
		Converting, Interface and Fans inactive, Average Current		0.5		mA
Power-On Reset Threshold Voltage			**1.6**		**2.8**	V
TEMPERATURE TO DIGITAL CONVERTER CHARACTERISTICS						
Resolution				0.25 10		°C Bits
Remote Sensor Accuracy[6]		$0°C \le T_A \le +100°C$, $0°C \le T_D \le +100°C$, $3V \le V_{DD} \le 3.6V$			±2	°C
		$0°C \le T_A \le +120°C$, $-55°C \le T_D \le +125°C$, $3V \le V_{DD} \le 3.6V$			±3	°C
Temperature Accuracy using Internal Diode[7]		$0°C \le T_A \le +120°C$, $3V \le V_{DD} \le 3.6V$		±1	±3	°C
External Diode Current Source	I_{DS}	High Level		96		µA(max)
		Low Level		6		µA
External Diode Current Ratio				16		
ANALOG TO DIGITAL CONVERTER CHARACTERISTICS						
Total Unadjusted Error[8]	TUE				**±2**	%(max)
Differential Non-linearity	DNL			1		LSB
Power Supply Sensitivity				±1		%/V
Total Monitoring Cycle Time[9]		All Voltage and Temperature readings		200	**250**	ms (max)
Input Resistance, all analog inputs			**140**	210	**400**	kΩ
DIGITAL OUTPUT: PWM1, PWM2, PWM3, XTESTOUT						
Logic Low Sink Current	I_{OL}	V_{OL} = 0.4V	**8**			mA (min)
Logic Low Level	V_{OL}	I_{OUT} = +8mA			**0.4**	V (max)
SMBUS OPEN-DRAIN OUTPUT: SMBDAT						
Logic Low Output Voltage	V_{OL}	I_{OUT} = +4mA			**0.4**	V (max)
High Level Output Current	I_{OH}	V_{OUT} = V+		0.1	**10**	µA(max)
SMBUS INPUTS: SMBCLK, SMBDAT						
Logic Input High Voltage	V_{IH}		**2.1**			V (min)
Logic Input Low Voltage	V_{IL}				**0.8**	V (max)
Logic Input Hysteresis Voltage	V_{HYST}			300		mV
DIGITAL INPUTS: ALL						
Logic Input High Voltage	V_{IH}		**2.1**			V (min)

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Parameter		Conditions	Min	Typ	Max	Units
Logic Input Low Voltage	V_{IL}				**0.8**	V (max)
Logic Input Threshold Voltage	V_{TH}			1.5		V
Logic High Input Current	I_{IH}	V_{IN} = V+		0.005	**10**	µA(max)
Logic Low Input Current	I_{IL}	V_{IN} = GND		-0.005	**-10**	µA(max)
Digital Input Capacitance	C_{IN}			20		pF

AC Electrical Characteristics

The following specifications apply for V_{DD} = 3.0V to 3.6V unless otherwise specified in conditions. **Boldface limits apply for $T_A = T_J$ over T_{MIN} to T_{MAX}**; all other limits $T_A = T_J$ = 25°C.

Parameter		Conditions	Min	Typ	Max	Units
TACHOMETER						
Fan Full-Scale Count					**65535**	(max)
Fan Counter Clock Frequency				90		kHz
Fan Count Conversion Time			**0.3**		**1.0**	sec(max)
FAN PWM OUTPUT						
Frequency Range		Low-Frequency Range		10 94		Hz Hz
		High-Frequency Range		23 30		kHz kHz
Duty-Cycle Range					**0 to 100**	%(max)
Duty-Cycle Resolution (8-bits)				0.3906		%/count
Spin-Up Time Interval Range				0 4000		ms ms

Logic Electrical Characteristics

(T_A = 25 °C, V_{DD} = 3.3V unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Voltage Logic High	V_{IH}	$3V \le V_{DD} \le 3.6V$	2.1			V
Input Voltage Logic Low	V_{IL}	$3V \le V_{DD} \le 3.6V$			0.8	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or 5.5V, $0°C \le T_A \le +125°C$			±1.0	µA
SMBus Output Sink Current	I_{OL}	T_A = 25 °C, V_{OL} = 0.6V	6			mA
SMBus Logic Input Current	I_{IH}, I_{IL}		-1		+1	µA
Output Leakage Current	I_{OH}	$V_{OH} = V_{DD}$ = 5.5V		0.1	1	µA
Output Transition Time	t_F	C_L= 400pF, I_{OL} = -3mA			250	ns
Input Capacitance	C_{IN}	All Digital Inputs			5	pF

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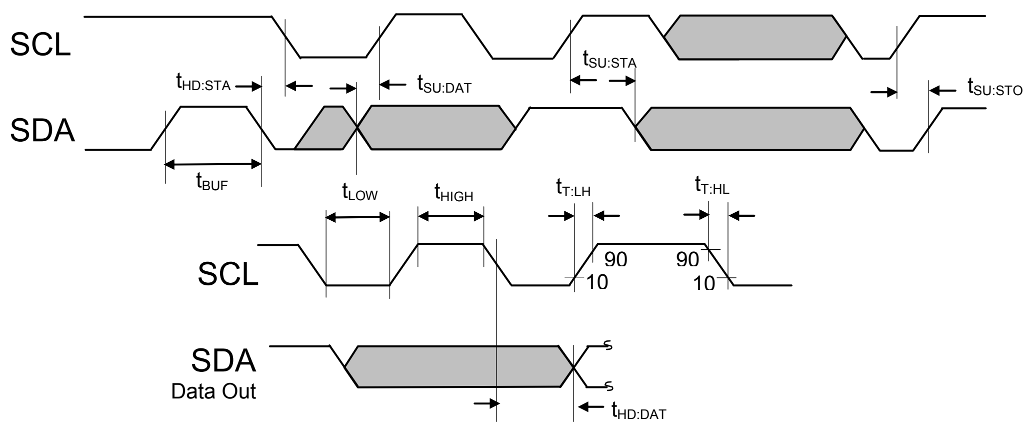
Serial Port Timing

(T_A = 25 °C, V_{DD} = 3.3V unless otherwise noted, Guaranteed by design, not production tested)

Parameter	Symbol	Min	Typ	Max	Units
SCL Operating Frequency	f_{SCL}			400	kHz
SCL Clock Transition Time	$t_{T:LH}$, $t_{T:HL}$			300	ns
SCL Clock Low Period	t_{LOW}	1.3			µs
SCL Clock High Period	t_{HIGH}	0.6		50	µs
Bus free time between a Stop and a new Start Condition	t_{BUF}	1.3			µs
Data in Set-Up to SCL High	$t_{SU:DAT}$	100			ns
Data Out Stable after SCL Low	$t_{HD:DAT}$	300			ns
SCL Low Set-up to SDA Low (Repeated Start Condition)	$t_{SU:STA}$	600			ns
SCL High Hold after SDA Low (Start Condition)	$t_{HD:STA}$	600			ns
SDA High after SCL High (Stop Condition)	$t_{SU:STO}$	600			ns
Time in which aSC7621 must be operational after a power-on reset	t_{POR}			500	ms
SMBus Time-out before device communication interface reset[10]	$t_{TIMEOUT}$	25		35	ms



Notes (cont'd):

5. These specifications are guaranteed only for the test conditions listed.
6. The accuracy of the aSC7621 is guaranteed when using the thermal diode of Intel Pentium 4, 65nm processors or any thermal diode with a non-ideality of 1.009 and series resistance of 4.52Ω. When using a 2N3904 type transistor or an CPU with a different non-ideality the error band will be typically shifted depending on transistor diode or CPU characteristics. See applications section for details.
7. Accuracy (expressed in °C) = Difference between the aSC7621 reported output temperature and the temperature being measured. Local temperature accuracy does not include the effects of self-heating. The rise in temperature due to self-heating is the product of the internal power dissipation of the aSC7621 and the thermal resistance. See (Note 3) for the thermal resistance to be used in the self-heating calculation.
8. TUE, total unadjusted error, includes ADC gain, offset, linearity and reference errors. TUE is defined as the "actual V_{in}" to achieve a given code transition minus the "theoretical V_{in} " for the same code. Therefore, a positive error indicates that the input voltage is greater than the theoretical input voltage for a given code. If the theoretical input voltage was applied to an aSC7621 that has positive error, the aSC7621's reading would be less than the theoretical.
9. This specification is provided only to indicate how often temperature and voltage data is updated. The aSC7621 can be read at any time without regard to conversion state (and will yield last conversion result).
10. Holding the SMBCLK line low for a time interval greater than $t_{TIMEOUT}$ will reset the aSC7621's SMBus state machine, therefore setting the SMBDAT pin to a high impedance state.

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Control Communication

SMBus

The aSC7621 is compatible with devices that are compliant to the SMBus 2.0 specifications. More information on this bus can be found at http://www.smbus.org/. Compatibility of SMBus2.0 to other buses is discussed in the SMBus 2.0 specification.

General Operation

Writing to and reading from the aSC7621 registers is accomplished via the SMBus-compatible two-wire serial interface. SMBus protocol requires that one device on the bus initiate and control all read and write operations. This device is called the “master” device. The master device also generates the SCL signal that is the clock signal for all other devices on the bus. All other devices on the bus are called “slave” devices. The aSC7621 is a slave device. Both the master and slave devices can send and receive data on the bus.

During SMBus operations, one data bit is transmitted per clock cycle. All SMBus operations follow a repeating nine clock-cycle pattern that consists of eight bits (one byte) of transmitted data followed by an acknowledge (ACK) or not acknowledge (NACK) from the receiving device. Note that there are no unused clock cycles during any operation—therefore there must be no breaks in the stream of data and ACKs / NACKs during data transfers.

For most operations, SMBus protocol requires the SDA line to remain stable (unmoving) whenever SCL is high — i.e. any transitions on the SDA line can only occur when SCL is low. The exceptions to this rule are when the master device issues a start or stop condition. Note that the slave device cannot issue a start or stop condition.

SMBus Definitions

The following are definitions for some general SMBus terms:

Start Condition: This condition occurs when the SDA line transitions from high to low while SCL is high. The master device uses this condition to indicate that a data transfer is about to begin.

Stop Condition: This condition occurs when the SDA line transitions from low to high while SCL is high. The master device uses this condition to signal the end of a data transfer.

Acknowledge and **Not Acknowledge:** When data are transferred to the slave device it sends an “acknowledge” (ACK) after receiving each byte. The receiving device sends an ACK by pulling SDA low for one clock. Following the last byte, a master device sends a "not acknowledge" (NACK) followed by a stop condition. A NACK is indicated by forcing SDA high during the clock after the last byte.

Slave Address

aSC7621 is designed to be used primarily in desktop systems that require only one monitoring device. If only one aSC7621 is used on the motherboard, the designer should be sure that the $\overline{\text{AddressEnable}}$ /PWM3 pin is High during the first SMBus communication addressing the aSC7621. $\overline{\text{AddressEnable}}$ /PWM3 is an open drain I/O pin that at power-on defaults to the input state of $\overline{\text{AddressEnable}}$. A maximum of 10k pull-up resistance on $\overline{\text{AddressEnable}}$ /PWM3 is required to assure that the SMBus address of the device will be locked at 010 1110b, which is the default address of the aSC7621.

During the first SMBus communication TACH4 and PWM3 can be used to change the SMBus address of the aSC7621 to 0101101b or 0101100b. aSC7621 address selection procedure:

> A 10kΩ pull-down resistor to ground on the $\overline{\text{AddressEnable}}$ /PWM3 pin is required. Upon power up, the aSC7621 will be placed into $\overline{\text{AddressEnable}}$ mode and assign itself on SMBus address according to the state of the Address Select input. The aSC7621 will latch the address during the first valid SMBus transaction in which the first five bits of the targeted address match those of the aSC7621 address, 0 1011b. This feature eliminates the possibility of a glitch on the SMBus interfering with address selection. When the $\overline{\text{AddressEnable}}$ /PWM3 pin is not used to change the SMBus address of the aSC7621, it will remain in a high state until the first communication with the aSC7621. After the first SMBus transaction is completed PWM3 and TACH4 will return to normal operation.

$\overline{\text{Address Enable}}$	Address Select	Board Implementation	SMBus Address	
			Binary	Hex
0	0	Both pins pulled to ground through a 10 kΩ resistor	010 1100	2Ch
0	1	Address Select pulled to 3.3V and $\overline{\text{AddressEnable}}$ pulled to GND through a 10 kΩ resistor	010 1101	2Dh
1	X	$\overline{\text{AddressEnable}}$ pulled to 3.3V through a 10 kΩ resistor	010 1110	2Eh

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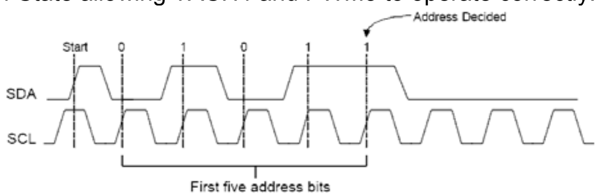
In this way, up to three aSC7621 devices can exist on a SMBus at any time. Multiple aSC7621 devices can be used to monitor additional processors in the temperature zones. When using the non-default addresses, additional circuitry will be required if Tach4 and PWM3 require to function correctly. Such circuitry could consist of GPIO pins from a micro-controller. During the first communication the micro-controller would drive the $\overline{\text{AddressEnable}}$ and Address Select pins to the proper state for the required address. After the first SMBus communication the micro-controller would drive its pins into Tri-State allowing TACH4 and PWM3 to operate correctly.



Writing to and Reading from the aSC7621

All read and write operations must begin with a start condition generated by the master device. After the start condition, the master device must immediately send a slave address (7-bits) followed by a R/$\overline{W}$ bit. If the slave address matches the address of the aSC7621, it sends an ACK by pulling the SDA line low for one clock. Read or write operations may contain one- or two-bytes. See Figures 2 through 6 for timing diagrams for all aSC7621 operations.

Setting the Register Address Pointer

For all operations, the address pointer stored in the address pointer register must be pointing to the register address that is going to be written to or read from. This register's content is automatically set to the value of the first byte following the R/$\overline{W}$ bit being set to 0.

After the aSC7621 sends an ACK in response to receiving the address and R/$\overline{W}$ bit, the master device must transmit an appropriate 8-bit address pointer value as explained in the Registers section of this data sheet. The aSC7621 will send an ACK after receiving the new pointer data.

The register address pointer set operation is illustrated in Figure 2. If the address pointer is not a valid address the aSC7621 will internally terminate the operation. Also recall that the address register retains the current address pointer value between operations. Therefore, once a register is being pointed to, subsequent read operations do not require another Address Pointer set cycle.

Writing to Registers

All writes must start with a pointer set as described previously, even if the pointer is already pointing to the desired register. The sequence is described in Figure 2.

Immediately following the pointer set, the master must begin transmitting the data to be written. After transmitting each byte of data, the master must release the SDA line for one clock to allow the aSC7621 to acknowledge receiving the byte. The write operation should be terminated by a stop condition from the master.

Reading from Registers

To read from a register other than the one currently being pointed to by the address pointer register, a pointer set sequence to the desired register must be done as described previously. Immediately following the pointer set, the master must perform a repeat start condition that indicates to the aSC7621 that a read is about to occur. It is important to note that if the repeat start condition does not occur, the aSC7621 will assume that a write is taking place, and the selected register will be overwritten by the upcoming data on the data bus. The read sequence is described in Figure 4. After the start condition, the master must again send the device address and read/write bit. This time the R/$\overline{W}$ bit must be set to 1 to indicate a read. The rest of the read cycle is the same as described in the previous paragraph for reading from a preset pointer location.

If the pointer is already pointing to the desired register, the master can read from that register by setting the R/$\overline{W}$ bit (following the slave address) to a 1. After sending an ACK, the aSC7621 will begin transmitting data during the following clock cycle. After receiving the 8 data bits, the master device should respond with a NACK followed by a stop condition.

If the master is reset while the aSC7621 is in the process of being read, the master should perform an SMBus reset. This is done by holding the clock low for more than 35ms, allowing all SMBus devices to be reset. This follows the SMBus 2.0 specification of 25-35ms.

When the aSC7621 detects an SMBus reset, it will prepare to accept a new start sequence and resume communication from a known state.

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Note: The following figures assume that Device Address 2Ch has been chosen by the user via address selection.

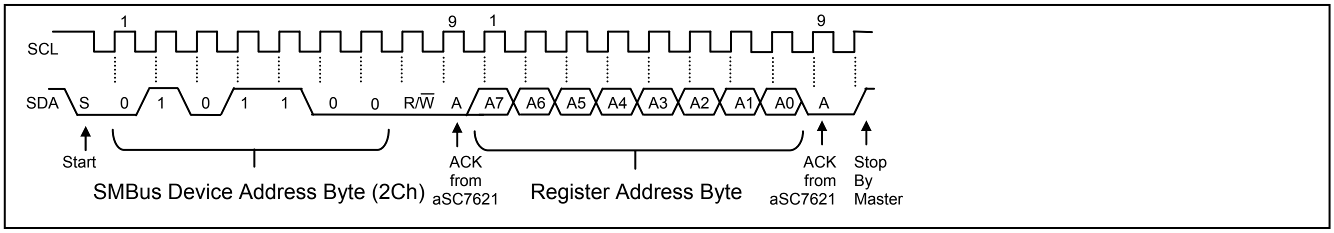

Figure 2 Register Address Pointer Set

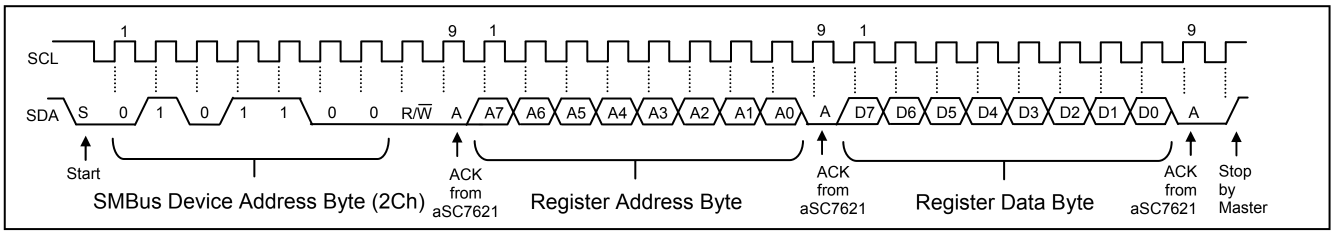

Figure 3 Register Write

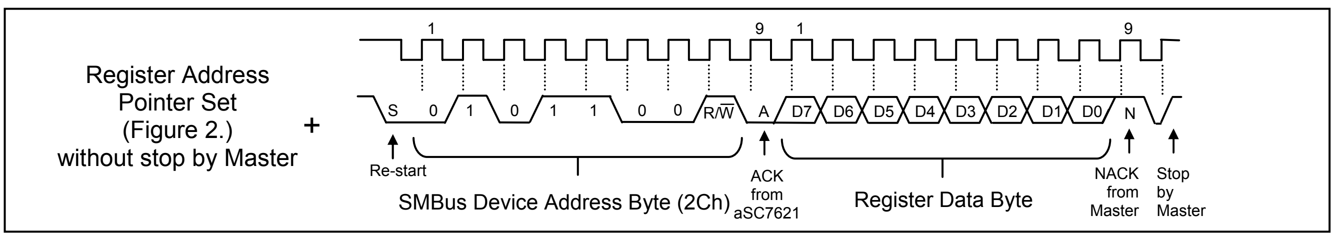

Figure 4 Register Read

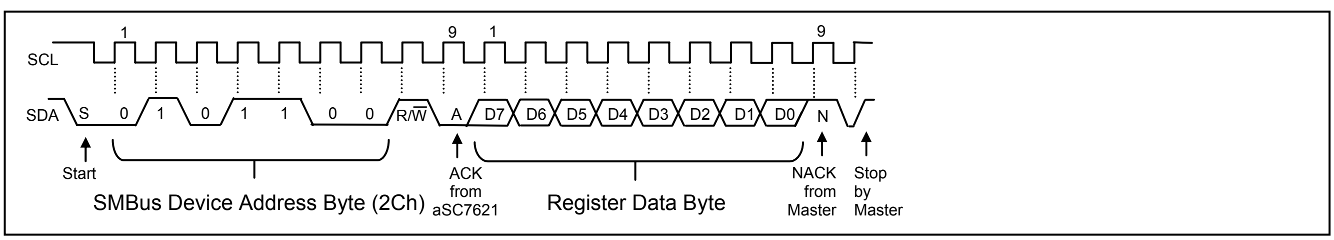

Figure 5 Register Read When Read Address Already Set

PECI

The aSC7621 is compatible with devices that are compliant with Intel's PECI 1.0 specifications. More information on this interface may be found in their PECI interface specifications.

Temperatures sent over the PECI interface from the CPU are in Celsius degrees relative to the Thermal Control Circuit (TCC) temperature stored internally in the CPU and accessed only through BIOS. This is the temperature limit where internal measures are taken to reduce power dissipation. Fan speed control settings sent by the BIOS over the SMBus to registers in the aSC7621 are made using this relative temperature rather than the absolute readings of remote or on-chip diodes.

As many as four CPU clients on the PECI bus are addressed in the range of 0x30 to 0x33. Currently, each address is a single-packaged device that may have up to two domains or CPU-measured digital temperatures.

General Operation

The PECI host in aSC7621 performs the following functions:

- Responds to SMBus configuration identifying the presence of PECI clients and the Thermal Zone associated with each client.
- Reads the PECI temperature of the domain(s) of each client processor addressed.
- Stores the highest result from each PECI address into Temperature Zone register associated to the measurement received from the client. (each address may be associated with any one Temperature Zone.)
- Flags an error if no valid PECI temperature can be read.
- Continuously monitors the state of the PECI interface for fault conditions.

PECI Temperature Format and Range

The PECI temperatures read from the processor will be in the range 0°C to -127°C where 0°C is the hottest temperature and has the following format:

Temperature	2's Complement Representation
0° C	0000 0000 00.00 0000
-1° C	1111 1111 11.00 0000
-5° C	1111 1110 11.00 0000
-32° C	1111 1000 00.00 0000
-127° C	1111 0000 01.00 0000

Table 1 Raw PECI Temperature Format

These readings are not accessible to the user but are filtered, re-formatted and assigned to a Temperature Zone. Filtered PECI Temperature readings are accessible by the user before they are assigned to a Temperature Zone by reading registers F6h through FDh. These readings follow the format described in Table 2. The PECI temperatures assigned to a Temperature Zone are reported over SMBus interface in Temperature Zone registers also will be in the range 0°C to -127°C. The format reported through Temperature Zone registers is re-aligned to agree with diode measurements. It is stored in two register locations in the following format with integer high byte and fractional low byte to be consistent with all other temperature reports:

Temperature	2's Complement Representation	
	High Byte	Low Byte
0° C	0000 0000	.0000 0000
-1° C	1111 1111	.0000 0000
-5° C	1111 1011	.0000 0000
-32° C	1110 0000	.0000 0000
-127° C	1000 0001	.0000 0000

Table 2 PECI Temperature Report Format

PECI Errors

A specific set of temperature reading value encodings, well outside the operational range of 0°C to -127°C, are reserved to signal temperature sensor faults on the CPU to aSC7621 interface. These encodings are in the PECI temperature format as delivered by the CPU and are converted to the appropriate Interrupt Status Register 3 error bits described in the Interrupt Status register section below.

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Register Set

Register Address	R/W	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (hex)	Lock
00h	R	Fan Zone Status	Fan 3 Zone #		Fan 2 Zone #		Fan 1 Zone #		RES	RES	N/A	
			1	0	1	0	1	0				
02h	R/W	Zone 1 & 2 Assignment	RES	Zone 1 Source			RES	Zone 2 Source			00	X
				2	1	0		2	1	0		
03h	R/W	Zone 3 & 4 Assignment	RES	Zone 3 Source			RES	Zone 4 Source			00	X
				2	1	0		2	1	0		
04h	R/W	Tach 1 Configuration	3-Wire Enable1	3-Wire Enable0	Meas Blank1	Meas Blank 0	Meas Dwell 1	Meas Dwell 0	Meas Duration 1	Meas Duration 0	36	X
05h	R/W	Tach 2 Configuration	3-Wire Enable1	3-Wire Enable0	Meas Blank1	Meas Blank 0	Meas Dwell 1	Meas Dwell 0	Meas Duration 1	Meas Duration 0	36	X
06h	R/W	Tach 3 Configuration	3-Wire Enable1	3-Wire Enable0	Meas Blank1	Meas Blank 0	Meas Dwell 1	Meas Dwell 0	Meas Duration 1	Meas Duration 0	36	X
07h	R/W	Tach 4 Configuration	3-Wire Enable1	3-Wire Enable0	Meas Blank1	Meas Blank 0	Meas Dwell 1	Meas Dwell 0	Meas Duration 1	Meas Duration 0	36	X
0Eh	R/W	PECI Extended Configuration	Four Domain Enable	Diode Filter2	Diode Filter1	Diode Filter0	Proc 3 Enable	Proc 2 Enable	Proc 1 Enable	Proc 0 Enable	21	X
10h	R	Zone 1 Temperature (LS Byte)	1	0	X	X	X	X	X	X	N/A	
11h	R	3.3V (LS Byte)	1	0	X	X	X	X	X	X	N/A	
12h	R	5V (LS Byte)	1	0	X	X	X	X	X	X	N/A	
13h	R	2.5V (LS Byte)	1	0	X	X	X	X	X	X	N/A	
14h	R	12V (LS Byte)	1	0	X	X	X	X	X	X	N/A	
15h	R	Zone 2 Temperature (LS Byte)	1	0	X	X	X	X	X	X	N/A	
16h	R	Zone 3 Temperature (LS Byte)	1	0	X	X	X	X	X	X	N/A	
17h	R	Zone 4 Temperature (LS Byte)	1	0	X	X	X	X	X	X	N/A	
18h	R	Vccp (LS Byte)	1	0	X	X	X	X	X	X	N/A	
19h	R/W	GPIO 1 Configuration	RES	RES	Alert Assignment		GPIO 1 bit	GPIO 1 Function			00	X
					1	0		2	1	0		
1Ah	R/W	GPIO 2 & 3 Configuration	GPIO 2 bit	GPIO 2 Function			GPIO 3 bit	GPIO 3 Function			00	X
				2	1	0		2	1	0		
1Ch	R/W	Remote 1 offset	7	6	5	4	3	2	1	0	00	X
1Dh	R/W	Remote 2 offset	7	6	5	4	3	2	1	0	00	X
20h	R	2.5V (MS Byte)	7	6	5	4	3	2	1	0	N/A	
21h	R	Vccp (MS Byte)	7	6	5	4	3	2	1	0	N/A	
22h	R	3.3 V (MS Byte)	7	6	5	4	3	2	1	0	N/A	
23h	R	5V (MS Byte)	7	6	5	4	3	2	1	0	N/A	
24h	R	12V (MS Byte)	7	6	5	4	3	2	1	0	N/A	
25h	R	Zone 1 Temperature (MS Byte)	9	8	7	6	5	4	3	2	N/A	
26h	R	Zone 2 Temperature (MS Byte)	9	8	7	6	5	4	3	2	N/A	
27h	R	Zone 3 Temperature (MS Byte)	9	8	7	6	5	4	3	2	N/A	

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Register Address	R/W	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	De-fault Value (hex)	Lock
28h	R	Tach 1 LS Byte	7	6	5	4	3	2	1	0	FF	
29h	R	Tach 1 MS Byte	15	14	13	12	11	10	9	8	FF	
2Ah	R	Tach 2 LS Byte	7	6	5	4	3	2	1	0	FF	
2Bh	R	Tach 2 MS Byte	15	14	13	12	11	10	9	8	FF	
2Ch	R	Tach 3 LS Byte	7	6	5	4	3	2	1	0	FF	
2Dh	R	Tach 3 MS Byte	15	14	13	12	11	10	9	8	FF	
2Eh	R	Tach 4 LS Byte	7	6	5	4	3	2	1	0	FF	
2Fh	R	Tach 4 MS Byte	15	14	13	12	11	10	9	8	FF	
30h	R/W	Fan 1 Current PWM Duty	7	6	5	4	3	2	1	0	FF	
31h	R/W	Fan 2 Current PWM Duty	7	6	5	4	3	2	1	0	FF	
32h	R/W	Fan 3 Current PWM Duty	7	6	5	4	3	2	1	0	FF	
33h	R	Zone 4 Temperature (MS Byte)	9	8	7	6	5	4	3	2	N/A	
34h	R/W	Zone 4 Low Temp	7	6	5	4	3	2	1	0	81h	
35h	R/W	Zone 4 High Temp	7	6	5	4	3	2	1	0	00h	
36h	R/W	PECI Configuration	RES	RES	RES	LEG	DOM	AVG2	AVG1	AVG0	00h	X
38h	R/W	Fan 1 Max Duty Cycle	7	6	5	4	3	2	1	0	FF	X
39h	R/W	Fan 2 Max Duty Cycle	7	6	5	4	3	2	1	0	FF	X
3Ah	R/W	Fan 3 Max Duty Cycle	7	6	5	4	3	2	1	0	FF	X
3Bh	R/W	Zone 4 Fan Temp Limit	7	6	5	4	3	2	1	0	E0h	X
3Ch	R/W	Zone 4 Range, Spike Smoothing	RAN3	RAN2	RAN1	RAN0	ZN4E	ZN4-2	ZN4-1	ZN4-0	C3h	X
3Dh	R/W	Zone 4 Absolute Temp Limit	7	6	5	4	3	2	1	0	00h	X
3Eh	R	Company ID	7	6	5	4	3	2	1	0	61	
3Fh	R	Version/ Stepping	VER3	VER2	VER1	VER0	4WIRE	PECI	STP1	STP0	6C	
40h	R/W	Ready/Lock/ Start/Override	RES	RES	SAFE	PECI	OVRID	READY	LOCK	START	00	X^2
41h	R	Interrupt Status Register 1	ERR	ZN3	ZN2	ZN1	5V	3.3V	VCCP	2.5V	00	
42h	R	Interrupt Status Register 2	ERR2	ERR1	FAN4	FAN3	FAN2	FAN1	ERR	12V	00	
43h	R	Interrupt Status Register 3	ERR	RES	RES	RES	ALOVR	COMM	DATA	ZN4	00h	

Register Address	R/W	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	De-fault Value (hex)	Lock
44h	R/W	2.5V Low Limit	7	6	5	4	3	2	1	0	00	
45h	R/W	2.5V High Limit	7	6	5	4	3	2	1	0	FF	
46h	R/W	Vccp Low Limit	7	6	5	4	3	2	1	0	00	
47h	R/W	Vccp High Limit	7	6	5	4	3	2	1	0	FF	
48h	R/W	3.3V Low Limit	7	6	5	4	3	2	1	0	00	
49h	R/W	3.3V High Limit	7	6	5	4	3	2	1	0	FF	
4Ah	R/W	5V Low Limit	7	6	5	4	3	2	1	0	00	
4Bh	R/W	5V High Limit	7	6	5	4	3	2	1	0	FF	
4Ch	R/W	12V Low Limit	7	6	5	4	3	2	1	0	00	
4Dh	R/W	12V High Limit	7	6	5	4	3	2	1	0	FF	
4Eh	R/W	Zone 1 Low Temperature	7	6	5	4	3	2	1	0	81	
4Fh	R/W	Zone 1 High Temperature	7	6	5	4	3	2	1	0	7F	
50h	R/W	Zone 2 Low Temperature	7	6	5	4	3	2	1	0	81	
51h	R/W	Zone 2 High Temperature	7	6	5	4	3	2	1	0	7F	
52h	R/W	Zone 3 Low Temperature	7	6	5	4	3	2	1	0	81	
53h	R/W	Zone 3 High Temperature	7	6	5	4	3	2	1	0	7F	
54h	R/W	Tach 1 Minimum LS Byte	7	6	5	4	3	2	1	0	FF	
55h	R/W	Tach 1 Minimum MS Byte	15	14	13	12	11	10	9	8	FF	
56h	R/W	Tach 2 Minimum LS Byte	7	6	5	4	3	2	1	0	FF	
57h	R/W	Tach 2 Minimum MS Byte	15	14	13	12	11	10	9	8	FF	
58h	R/W	Tach 3 Minimum LS Byte	7	6	5	4	3	2	1	0	FF	
59h	R/W	Tach 3 Minimum MS Byte	15	14	13	12	11	10	9	8	FF	
5Ah	R/W	Tach 4 Minimum LS Byte	7	6	5	4	3	2	1	0	FF	
5Bh	R/W	Tach 4 Minimum MS Byte	15	14	13	12	11	10	9	8	FF	
5Ch	R/W	Fan 1 Configuration	ZON2	ZON1	ZON0	INV	ALT	SPIN2	SPIN1	SPIN0	62	X
5Dh	R/W	Fan 2 Configuration	ZON2	ZON1	ZON0	INV	ALT	SPIN2	SPIN1	SPIN0	62	X
5Eh	R/W	Fan 3 Configuration	ZON2	ZON1	ZON0	INV	ALT	SPIN2	SPIN1	SPIN0	62	X
5Fh	R/W	Zone 1 Range/ Fan 1 Frequency	RAN3	RAN2	RAN1	RAN0	HLFRQ	FRQ2	FRQ1	FRQ0	C3	X

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Register Address	R/W	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	De-fault Value (hex)	Lock
60h	R/W	Zone 2 Range/ Fan 2 Frequency	RAN3	RAN2	RAN1	RAN0	HLFRQ	FRQ2	FRQ1	FRQ0	C3	X
61h	R/W	Zone 3 Range/ Fan 3 Frequency	RAN3	RAN2	RAN1	RAN0	HLFRQ	FRQ2	FRQ1	FRQ0	C3	X
62h	R/W	Min/Off, Zone 1 Spike Smoothing	OFF3	OFF2	OFF1	RES	ZN1E	ZN1-2	ZN1-1	ZN1-0	00	X
63h	R/W	Zone 2 / Zone 3 Spike Smoothing	ZN2E	ZN2-2	ZN2-1	ZN2-0	ZN3E	ZN3-2	ZN3-1	ZN3-0	00	X
64h	R/W	Fan 1 PWM Minimum	7	6	5	4	3	2	1	0	80	X
65h	R/W	Fan 2 PWM Minimum	7	6	5	4	3	2	1	0	80	X
66h	R/W	Fan 3 PWM Minimum	7	6	5	4	3	2	1	0	80	X
67h	R/W	Zone 1 Fan Temp Limit	7	6	5	4	3	2	1	0	5A	X
68h	R/W	Zone 2 Fan Temp Limit	7	6	5	4	3	2	1	0	5A	X
69h	R/W	Zone 3 Fan Temp Limit	7	6	5	4	3	2	1	0	5A	X
6Ah	R/W	Zone 1 Temp Absolute Limit	7	6	5	4	3	2	1	0	64	X
6Bh	R/W	Zone 2 Temp Absolute Limit	7	6	5	4	3	2	1	0	64	X
6Ch	R/W	Zone 3 Temp Absolute Limit	7	6	5	4	3	2	1	0	64	X
6Dh	R/W	Zone 1, Zone 2 Hysteresis	H1-3	H1-2	H1-1	H1-0	H2-3	H2-2	H2-1	H2-0	44	X
6Eh	R/W	Zone 3, Zone 4 Hysteresis	H3-3	H3-2	H3-1	H3-0	H4-3	H4-2	H4-1	H4-0	44	X
6Fh	R/W	XOR Tree Enable	RES	RES	RES	RES	RES	RES	RES	XEN	00	X
75h	R/W	Fan Spin-up Mode	Tach4 Disable	Tach3/4 Disable	Tach2 Disable	Tach1 Disable	RES	PWM3SU	PWM2SU	PWM1SU	00	X

Notes:

1. Reserved bits will always return 0 when read, X-bits in readings may be ignored.
2. When register 40h is locked, all bits are locked except 0 and 3 which remain user changeable.
3. Two-byte or extended resolution temperature, voltage and tachometer values are protected from changing when only one of the bytes is read. The implementation of a data word latch involves the register pairs in the table below. When one of the address pairs is read, the mating data is latched at the same time. The next SMBus access MUST be the mating address or the latch will be released. This implementation allows that the data may be read in the order of LS-MS or MS-LS and the pair will remain coherent.

MS-Byte Address (hex)	LS-Byte Address (hex)	Data Field Name
25	10	Zone 1 Temperature
26	15	Zone 2 Temperature
27	16	Zone 3 Temperature
33	17	Zone 4 Temperature
20	13	2.5V
21	18	VCCP
22	11	3.3V
23	12	5V
24	14	12V
29	28	Tach 1
2B	2A	Tach 2
2D	2C	Tach 3
2F	2E	Tach 4

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Temperature Measurement

Diode temperatures are measured with a precision Delta-V_{BE} methodology converted to a digital temperature reading by a 10-bit sigma-delta converter. PECI interface to the CPU provide Digital Thermometer readings of substrate temperature. The measurement system provides a means for assigning any of the temperature inputs to a Temperature Zone. The user may set limits on these readings to be continuously monitored and alarm bits set when they are exceeded. Separately, the measurements are also delivered to the automatic fan control system to adjust fan speed. The following registers contain the readings from the internal and remote sensors.

Registers 25-10h, 26-15h and 27-0Eh: Temperature Zone Readings (10-Bit, 2's Complement Reporting)

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
25h	R	Zone 1 Temperature (MS Byte)	9	8	7	6	5	4	3	2	N/A
10h	R	Zone 1 Temperature (LS Byte)	1	0	X	X	X	X	X	X	N/A
26h	R	Zone 2 Temperature (MS Byte)	9	8	7	6	5	4	3	2	N/A
15h	R	Zone 2 Temperature (LS Byte)	1	0	X	X	X	X	X	X	N/A
27h	R	Zone 3 Temperature (MS Byte)	9	8	7	6	5	4	3	2	N/A
16h	R	Zone 3 Temperature (LS Byte)	1	0	X	X	X	X	X	X	N/A
33h	R	Zone 4 Temperature (MS Byte)	9	8	7	6	5	4	3	2	N/A
17h	R	Zone 4 Temperature (LS Byte)	1	0	X	X	X	X	X	X	N/A

The Temperature Zone registers reflect the current temperature of the internal and remote diodes or PECI CPU Digital Thermometers. Filtering is applied to all readings and this is described in the Spike & Smoothing Filter section below. Any temperature input may be assigned to any zone, according to the settings in the Zone Assignment Registers, [02h] and [03h]. The default assignment is as follows:

Zone 1 Temperature register reports the temperature measured by the thermal diode connected to the Remote 1- and Remote 1+ pins if either:

1. PECI monitoring is disabled (register [40h] bit 4=0)
2. PECI monitoring is enabled but in legacy mode, (register [36h] bit 4, LEG = 0).

If PECI Monitoring is enabled (register [40h] bit 4=1) AND legacy mode is LEG = legacy mode (register [36h] bit 4, LEG = 1), the register reports the highest Digital Thermometer reading by the processor.

Zone 2 Temperature register reports the temperature measured by the internal (junction) temperature sensor.

Zone 3 Temperature register reports the temperature measured by the thermal diode connected to the second set of Remote 2- and Remote 2+ pins.

Zone 4 reports temperatures as follows:

1. By default and if PECI temperature is disabled (register [36h] bit 4, LEG = 0) the Zone 4 register is not used. In this case, special temperature value of 80h will be reported to indicate that no temperature is available. If this zone is associated with any fan PWM controller(s), this will result in these controller(s) being overridden to 100% duty cycle. No error bits will be set in the Interrupt Status Registers.
2. If PECI Monitoring is enabled [40h] bit 4=1) AND legacy mode is in standard mode (register [36h] bit 4, LEG = 0), the register will report the highest Digital Thermometer reading by the processor.
3. Temperatures are represented as 10-bit, 2's complement, signed numbers, in degrees Celsius, as shown below in Table 3.
4. If PECI Monitoring is enabled [40h] bit 4=1) AND legacy mode is in legacy mode (register [36h] bit 4, LEG = 1), the register will report the temperature measured by the thermal diode connected to the Remote 1- and Remote 1+ pins.

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A remote diode temperature reading register will return a value of 8000h if the remote diode pins are not used by the board designer or is not functioning properly. This reading will cause the zone limit bits (bits 4 and 6) in the Interrupt Status Register (41h) and the remote diode fault status bit (bits 6 and 7) in the Interrupt Status Register 2 (42h) to be set. These registers are read-only – a write to these registers has no effect.

Temperature	Digital Output (2's Complement)				
	High Byte		Low Byte		
	10-Bit Resolution			Ignore	
+125°C	0111	1101	.00	XX	XXXX
+100°C	0110	0100	.00	XX	XXXX
+50°C	0011	0010	.00	XX	XXXX
+25°C	0001	1001	.00	XX	XXXX
+10°C	0000	1010	.00	XX	XXXX
+1.75°C	0000	0001	.11	XX	XXXX
+0.25°C	0000	0000	.01	XX	XXXX
0°C	0000	0000	.00	XX	XXXX
-1.75°C	1111	1110	.01	XX	XXXX
-55°C	1100	1001	.00	XX	XXXX

Table 3 Relationship between Temperature and 2's Complement Digital Output, -55°C to +125°C

Temperature	Digital Output (2's Complement)				
	High Byte		Low Byte		
	10-Bit Resolution				Ignore
0°C	0000	0000	.0000	00	XX
-0.015625°C	1111	1111	.1111	11	XX
-0.03125°C	1111	1111	.1111	10	XX
-0.0625°C	1111	1111	.1111	00	XX
-0.125°C	1111	1111	.1110	00	XX
-0.25°C	1111	1111	.1100	00	XX
-0.5°C	1111	1111	.1000	00	XX
-1.0°C	1111	1111	.0000	00	XX
-1.75°C	1111	1110	.0100	00	XX
-2.0°C	1111	1110	0000	00	XX
-25.0°C	1110	0111	0000	00	XX
-100°C	1001	1100	0000	00	XX
-127°C	1000	0001	0000	00	XX

Table 4 PECI Temperature Format

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Temperature Measurement Configuration

Registers 02h and 03h: Zone Assignments

Register Address	R/W	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Lock
02h	R/W	Zone 1 & 2 Assignment	RES	Zone 1 Source			RES	Zone 2 Source			00	X
				6	5	4		2	1	0		
03h	R/W	Zone 3 & 4 Assignment	RES	Zone 3 Source			RES	Zone 4 Source			00	X
				6	5	4		2	1	0		

The temperature measurement system has access to more temperature measuring devices than there are Temperature Zones that may be reported to the user or used to control a fan. It is allowed that any data input may be associated with any single Temperature Zone. However, if an attempt is made to assign a data source to more than one Temperature Zone report, the lowest order will be assigned and the other assignment will be ignored. Do not attempt to assign a data source to more than one Temperature Zone or multiple data sources to the same Temperature Zone.

This register becomes read-only when the Ready/Lock/Start/Override register Lock bit is set. Any further attempts to write to this register shall have no effect.

Bit	Name	Zone 1 & 2 Assignment [02h]	
2:0	Zone 2 Source	**Value**	**Data Source**
		000	Internal Temperature
		001	Remote 1 Temperature
		010	Remote 2 Temperature
		011	Internal Temperature
		100	PECI Processor Temperature 0
		101	PECI Processor Temperature 1
		110	PECI Processor Temperature 2
		111	PECI Processor Temperature 3
3	Reserved	Reserved	
6:4	Zone 1 Source	**Value**	**Data Source**
		000	LEG = 0, Remote 1 Temperature
			LEG = 1, PECI Processor Temperature 0
		001	Remote 1 Temperature
		010	Remote 2 Temperature
		011	Internal Temperature
		100	PECI Processor Temperature 0
		101	PECI Processor Temperature 1
		110	PECI Processor Temperature 2
		111	PECI Processor Temperature 3
7	Reserved	Reserved	

Table 5 Zone 1 & 2 Temperature Reading Assignment [02h]

<table>
<tr><th>Bit</th><th>Name</th><th colspan="2">Zone 3 & 4 Assignment [03h]</th></tr>
<tr><td rowspan="10">2:0</td><td rowspan="10">Zone 4 Source</td><td>Value</td><td>Data Source</td></tr>
<tr><td rowspan="2">000</td><td>LEG = 0, PECI Processor Temperature 0</td></tr>
<tr><td>LEG = 1, Remote 1 Temperature</td></tr>
<tr><td>001</td><td>Remote 1 Temperature</td></tr>
<tr><td>010</td><td>Remote 2 Temperature</td></tr>
<tr><td>011</td><td>Internal Temperature</td></tr>
<tr><td>100</td><td>PECI Processor Temperature 0</td></tr>
<tr><td>101</td><td>PECI Processor Temperature 1</td></tr>
<tr><td>110</td><td>PECI Processor Temperature 2</td></tr>
<tr><td>111</td><td>PECI Processor Temperature 3</td></tr>
<tr><td>3</td><td>Reserved</td><td colspan="2">Reserved</td></tr>
<tr><td rowspan="9">6:4</td><td rowspan="9">Zone 3 Source</td><td>Value</td><td>Data Source</td></tr>
<tr><td>000</td><td>Remote 2 Temperature</td></tr>
<tr><td>001</td><td>Remote 1 Temperature</td></tr>
<tr><td>010</td><td>Remote 2 Temperature</td></tr>
<tr><td>011</td><td>Internal Temperature</td></tr>
<tr><td>100</td><td>PECI Processor Temperature 0</td></tr>
<tr><td>101</td><td>PECI Processor Temperature 1</td></tr>
<tr><td>110</td><td>PECI Processor Temperature 2</td></tr>
<tr><td>111</td><td>PECI Processor Temperature 3</td></tr>
<tr><td>7</td><td>Reserved</td><td colspan="2">Reserved</td></tr>
</table>

Table 6 Zone 3 & 4 Temperature Reading Assignment [03h]

Bit	Name	Default	Description
3:0	Reserved	0	Reserved
4	PECI One-Shot Enable	0	0 = Disable PECI One Shot, 1 = Enable PECI One-Shot
5	Reserved	0	Reserved
6	Run/Stop	0	Measurement system run(default) or stop (set to 1), places aSC7621 in a low-power or standby mode.
7	Reserved	0	Reserved

Table 7 Configuration Register [09h] bits

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Register 36h: PECI Configuration

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Lock
36h	R/W	PECI Configuration	RES	RES	RES	LEG	DOM	AVG2	AVG1	AVG0	00h	X

This register establishes legacy diode register assignment condition of Temperature Zones 1 and 4, LEG; the number of domains per client, DOM; and PECI input filter coefficients, AVG[2:0]. This register becomes read-only when the Ready/Lock/Start/Override register Lock bit is set. Any further attempts to write to this register shall have no effect.

Bit	Field	Value	Function
2:0	AVG (PECI Input Filter)	000 (default)	0 Sec. (no Smoothing)
		001	0.25 Sec.
		010	0.5 Sec.
		011	1.0 Sec.
		100	2.0 Sec.
		101	4.0 Sec.
		110	8.0 Sec.
		111	0 Sec.
3	DOM	0 (default)	Processor contains a single domain (0)
		1	Processor contains two domains (0,1)
4	LEG	0 (default) (Standard Mode)	Remote Diode 1 reading is associated with Temperature Zone 1, PECI is associated with Zone 4
		1 (Legacy Mode)	PECI is associated with Temperature Zone 1, Remote Diode 1 is associated with Zone 4
5:7	Reserved	0	Reserved

Table 8 PECI Configuration [36h]

Register 0Eh: PECI Extended Configuration

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Lock
0Eh	R/W	PECI Extended Configuration	Four Domain Enable	Diode Filter2	Diode Filter1	Diode Filter0	Proc 3 Enable	Proc 2 Enable	Proc 1 Enable	Proc 0 Enable	21	X

This register establishes the number of domains per PECI address and enables up to four PECI clients to be polled for temperatures. If bit-0 through bit-3 are reset, PECI will not be available.

In addition, a remote diode noise filter may be tuned for optimum performance when excessive noise is present in remote diode readings. This is a low-pass filter that also eliminates single sample spikes before they are stored in Temperature Zone registers. Filter algorithm is described in the section on Spike Smoothing registers 62h, 63h and 3Ch. Times indicated in Table 9 show the approximate filter response time to a step function in temperature diode measurement as applied to the assigned Temperature Zone reading. This register becomes read-only when the Ready/Lock/Start/Override register Lock bit is set. Any further attempts to write to this register shall have no effect.

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Bit	Field	Value	Function
0	Processor 0 Enable	0	PECI Processor 0 disabled
		1 (default)	PECI Processor 0 enabled
1	Processor 1 Enable	0 (default)	PECI Processor 1 disabled
		1	PECI Processor 1 enabled
2	Processor 2 Enable	0 (default)	PECI Processor 2 disabled
		1	PECI Processor 2 enabled
3	Processor 3 Enable	0 (default)	PECI Processor 3 disabled
		1	PECI Processor 3 enabled
6:4	Diode Filter	000	0.25 Sec.
		001	1.1 Sec.
		010 (default)	2.4 Sec.
		011	3.4 Sec.
		100	5.0 Sec.
		101	6.8 Sec.
		110	10.2 Sec.
		111	16.4 Sec.
7	Four Domain Enable	0 (default)	1 or 2 Domains for enabled processors
		1	3 or 4 Domains for enabled processors

Table 9 PECI Extended Configuration [0Eh]

Register 1Ch and 1Dh: Remote Offset Registers

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
1Ch	R/W	Remote 1 offset	7	6	5	4	3	2	1	0	00
1Dh	R/W	Remote 2 offset	7	6	5	4	3	2	1	0	00

This register provides a means to offset readings from remote diodes to compensate for errors due to system noise or series resistance. It may also be used to compensate for a difference in temperature between the remote diode and the temperature of interest once that is characterized by the user. It is in 2's Complement format with 0.25 degree resolution.

The range is -32 to +31.75°C and is described in Table 10:

Offset Temperature	Value[7:0]	
+31.75°C	0111	11.11
+31°C	0111	11.10
+1°C	0000	01.00
+0.5°C	0000	00.10
+0.25°C	0000	00.01
0°C	0000	00.00
-0.25°C	1111	11.11
-1°C	1111	11.00
-31°C	1000	01.00
-31.75°C	1000	00.01
-32°C	1000	00.00

Table 10 Offset Temperature Data Format

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Voltage Measurement and Limits

Register 20-24h: Voltage Reading

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
20h	R	2.5V (MS Byte)	9	8	7	6	5	4	3	2	N/A
13h	R	2.5V (LS Byte)	1	0	X	X	X	X	X	X	N/A
21h	R	VCCP (MS Byte)	9	8	7	6	5	4	3	2	N/A
18h	R	VCCP (LS Byte)	1	0	X	X	X	X	X	X	N/A
22h	R	3.3V (MS Byte)	9	8	7	6	5	4	3	2	N/A
11h	R	3.3V (LS Byte)	1	0	X	X	X	X	X	X	N/A
23h	R	5V (MS Byte)	9	8	7	6	5	4	3	2	N/A
12h	R	5V (LS Byte)	1	0	X	X	X	X	X	X	N/A
24h	R	12V (MS Byte)	9	8	7	6	5	4	3	2	N/A
14h	R	12V (LS Byte)	1	0	X	X	X	X	X	X	N/A

The Register Names define the typical input voltage at which the reading is ¾ full scale or C000h. High byte readings are 8-bits with an LS bit value of Nominal divided by 192 and 2-bits in the high-order portion of the LS Byte having a value corresponding to ½ and ¼ of that high byte LS bit value. Ignore the lower 6-bits of the LS Byte.

The Voltage Reading registers are updated automatically by the aSC7621 at a minimum frequency of 4Hz and a typical frequency of 5 Hz. These registers are read only – a write to these registers has no effect.

Register 44-4Dh: Voltage Limit Registers

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
44h	R/W	2.5V Low Limit	7	6	5	4	3	2	1	0	00h
45h	R/W	2.5V High Limit	7	6	5	4	3	2	1	0	FFh
46h	R/W	VCCP Low Limit	7	6	5	4	3	2	1	0	00h
47h	R/W	VCCP High Limit	7	6	5	4	3	2	1	0	FFh
48h	R/W	3.3V Low Limit	7	6	5	4	3	2	1	0	00h
49h	R/W	3.3V High Limit	7	6	5	4	3	2	1	0	FFh
4Ah	R/W	5V Low Limit	7	6	5	4	3	2	1	0	00h
4Bh	R/W	5V High Limit	7	6	5	4	3	2	1	0	FFh
4Ch	R/W	12V Low Limit	7	6	5	4	3	2	1	0	00h
4Dh	R/W	12V High Limit	7	6	5	4	3	2	1	0	FFh

If a voltage input either exceeds the value set in the voltage high limit register or falls below the value set in the voltage low limit register, the corresponding bit will be set automatically by the aSC7621 in the interrupt status registers (41-42h). The binary value of the voltage limits are extended to 16-bits and compared with the two-bytes of the voltage reading. Voltages are presented in the registers at ¾ of full-scale for the nominal voltage, meaning that at nominal voltage, each input will be C0h, as shown in Table 11. Note that 3.3V input is Vdd and is not allowed to go below 3.0V during normal operation.

Setting the Ready/Lock/Start/Override register Lock bit has no effect on these registers.

Input	Nominal Voltage	Register Reading at Nominal Voltage	Maximum Voltage	Register Reading at Maximum Voltage	Minimum Voltage	Register Reading at Minimum Voltage
2.5V	2.5V	C0h	3.32V	FFh	0V	00h
VCCP	2.25V	C0h	3.00V	FFh	0V	00h
3.3V	3.3V	C0h	4.38V	FFh	3.0V	AEh
5V	5.0V	C0h	6.64V	FFh	0V	00h
12V	12.0V	C0h	16.00V	FFh	0V	00h

Table 11 Voltage Limits vs Register Setting (MS Byte)

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Temperature Measurement Filtering

Filter Architecture

Each temperature reading is carefully filtered to remove spike transients and noise generated by the computer environment's effect on sensitive analog measurements. Filtering is tunable by the user and is applied in two general areas:

1. Immediately after the measurement process before assigning a measurement to a Temperature Zone.
2. After Temperature Zone assignment but before a fan is assigned to that Temperature Zone.

An overview of this signal flow is in Figure 6 below.

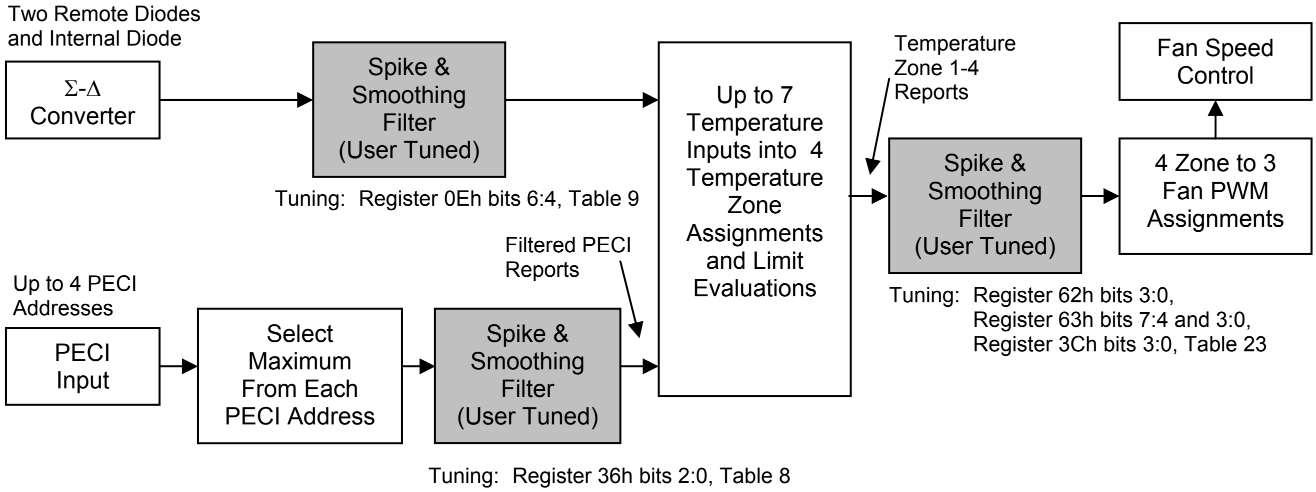

Figure 6 Measurement Filter Block Diagram

Spike & Smoothing Filter Algorithm

The Spike & Smoothing Filter algorithm has two phases of filtering. First, a "No-Spike" value is created from the current and three previous values. The result is an average of the two remaining values when the high and low values are removed.

The second phase is a user specified filter and coefficient. This filter determines a smoothed temperature value, Smooth T_i, by taking the No-Spike T_i, subtracting the previous smoothed temperature, Smooth T_{i-1}, divided by 2^N and adding that to the previously smoothed temperature. N and GAIN are coefficients selected internally to provide the spike filter smoothing time constants (step input response time) shown in Table 8, Table 9 and Table 23.

For the current temperature reading T_i:

No-Spike T_i = (Discard min and max of (T_i, T_{i-1}, T_{i-2}, T_{i-3}))/2

Smooth T_i = GAIN * (No-Spike T_i - Smooth T_{i-1})/2^N + Smooth T_{i-1}

Status Registers

Register 41h: Interrupt Status Register 1

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
41h	R	Interrupt Status 1	ERR	ZN3	ZN2	ZN1	5V	3.3V	VCCP	2.5V	N/A

The Interrupt Status Register 1 bits will be automatically set, by the aSC7621, whenever a fault condition is detected. A fault condition is detected whenever a measured value is outside the window set by its limit registers. ZN1 bit will be set when a diode fault condition, such as an open or short, is detected. More than one fault may be indicated in the interrupt register when read. The register will hold set bit(s) until the event is read by software. The contents of this register will be cleared (set to 0) automatically by the aSC7621 after it is read by software, if the fault condition no longer exists. Once set, the Interrupt Status Register 1 bits will remain set until a read event occurs, even if the fault condition no longer exists. This register is read-only – a write to this register has no effect.

Bit	Name	R/W	Default	Description
0	2.5V Limits Exceeded	R	0	The aSC7621 automatically sets this bit to 1 when the 2.5V input voltage is less than or equal to the limit set in the 2.5V Low Limit register or greater than the limit set in the 2.5V High Limit register.
1	Vccp Limits Exceeded	R	0	The aSC7621 automatically sets this bit to 1 when the VCCP input voltage is less than or equal to the limit set in the VCCP Low Limit register or greater than the limit set in the VCCP High Limit register.
2	3.3V Limits Exceeded	R	0	The aSC7621 automatically sets this bit to 1 when the 3.3V input voltage is less than or equal to the limit set in the 3.3V Low Limit register or greater than the limit set in the 3.3V High Limit register.
3	5V Limits Exceeded	R	0	The aSC7621 automatically sets this bit to 1 when the 5V input voltage is less than or equal to the limit set in the 5V Low Limit register or greater than the limit set in the 5V High Limit register.
4	Zone 1 Limit Exceeded	R	0	The aSC7621 automatically sets this bit to 1 when the temperature input measured by the Remote1- and Remote1+ inputs is less than or equal to the limit set in the Processor (Zone 1) Low Temp register or more than the limit set in the Processor (Zone 1) High Temp register. This bit will be set when a diode fault is detected.
5	Zone 2 Limit Exceeded	R	0	The aSC7621 automatically sets this bit to 1 when the temperature input measured by the internal temperature sensor is less than or equal to the limit set in the thermal (Zone 2) Low Temp register or greater than the limit set in the Internal (Zone 2) High Temp register.
6	Zone 3 Limit Exceeded	R	0	The aSC7621 automatically sets this bit to 1 when the temperature input measured by the second remote temperature sensor is less than or equal to the limit set in the thermal (Zone 3) Low Temp register or greater than the limit set in the Internal (Zone 3) High Temp register.
7	Error in Status Register 2	R	0	If there is a set bit in Status Register 2, this bit will be set to 1.

Table 12 Interrupt Status Register 1

Register 42h: Interrupt Status Register 2

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
42h	R	Interrupt Status 2	ERR2	ERR1	FAN4	FAN3	FAN2	FAN1	ERR	12V	N/A

The Interrupt Status Register 2 bits will be automatically set, by the aSC7621, whenever a fault condition is detected. Interrupt Status Register 2 identifies faults caused by temperature sensor error, fan speed dropping below minimum set by the tachometer minimum register. Interrupt Status Register 2 will hold a set bit until the event is read by software. The contents of this register will be cleared (set to 0) automatically by the aSC7621 after it is read by software, if fault condition no longer exists. Once set, the Interrupt Status Register 2 bits will remain set until a read event occurs, even if the fault no longer exists. This register is read-only – a write to this register has no effect.

Bit	Name	R/W	Default	Description
0	12V Limits Exceeded	R	0	The aSC7621 automatically sets this bit to 1 when the 12V input voltage is less than or equal to the limit set in the 12V Low Limit register or greater than the limit set in the 12V High Limit register.
1	ERROR IN STATUS REGISTER 3	R	0	If there is a set bit in Status Register 3, this bit will be set to 1
2	FAN 1 STALLED	R	0	The aSC7621 automatically sets this bit to 1 when the TACH 1 input reading is above the count value set in the Tach 1 Minimum MSB and LSB registers.
3	FAN 2 STALLED	R	0	The aSC7621 automatically sets this bit to 1 when the TACH 2 input reading is above the count value set in the Tach 2 Minimum MSB and LSB registers.
4	FAN 3 STALLED	R	0	The aSC7621 automatically sets this bit to 1 when the TACH 3 input reading is above the count value set in the Tach 3 Minimum MSB and LSB registers.
5	FAN 4 STALLED	R	0	The aSC7621 automatically sets this bit to 1 when the TACH 4 input reading is above the count value set in the Tach 4 Minimum MSB and LSB registers.

Bit	Name	R/W	Default	Description
6	Remote Diode 1 Fault	R	0	The aSC7621 automatically sets this bit to 1 when there is an open circuit fault on the Remote1+ or Remote1- thermal diode input pins. A diode fault will also set bit 4 Zone 1 Limit bit, of Interrupt Status Register 1.
7	Remote Diode 2 Fault	R	0	The aSC7621 automatically sets this bit to 1 when there is an open circuit fault on the Remote2+ or Remote2- thermal diode input pins. A diode fault will also set bit 6 Zone 3 Limit bit, of Interrupt Status Register 1.

Table 13 Interrupt Status Register 2

Register 43h: Interrupt Status Register 3

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
43h	R	Interrupt Status 3	RES	RES	RES	RES	ALOVR	COMM	DATA	ZN4	N/A

The Interrupt Status Register 3 bits will be automatically set, by the aSC7621, whenever a fault condition is detected. Interrupt Status Register 3 identifies faults caused by Temperature Zone exceeding absolute limits, PECI Communication Error, PECI Data Error and Zone 4 Temperature limit exceeded. Interrupt Status Register 3 will hold a set bit until the event is read by software. The contents of this register will be cleared (set to 0) automatically by the aSC7621 after it is read by software, if fault condition no longer exists. Once set, the Interrupt Status Register 3 bits will remain set until a read event occurs, even if the fault no longer exists. This register is read only – a write to this register has no effect.

Bit	Name	R/W	Default	Description
0	ZN4	R	0	The aSC7621 automatically sets this bit to 1 when the Zone 4 Limit is exceeded.
1	DATA	R	0	The aSC7621 sets this bit when any of the PECI Processor Status reports PECI ERROR = 1 and PECI Underflow = 1, this indicates a Data error occurred with a PECI processor.
2	COMM	R	0	The aSC7621 automatically sets this bit to 1 when any of the PECI Processor Status reports PECI ERROR = 1 and PECI Underflow = 0 this indicates a Communications error occurred with a PECI Processor.
3	ALOVR	R	0	The aSC7621 automatically sets this bit to 1 when any Temperature Zone exceeds its Absolute Temperature Limit.
4	Reserved	R	0	Reserved.
5	Reserved	R	0	Reserved.
6	Reserved	R	0	Reserved.
7	Reserved	R	0	Reserved.

Table 14 Interrupt Status Register 3

Tachometer Measurement and Configuration

Register 28-2Fh: Fan Tachometer Reading

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
28h	R	Tach 1 LS Byte	7	6	5	4	3	2	1	0	N/A
29h	R	Tach 1 MS Byte	15	14	13	12	11	10	9	8	N/A
2Ah	R	Tach 2 LS Byte	7	6	5	4	3	2	1	0	N/A
2Bh	R	Tach 2 MS Byte	15	14	13	12	11	10	9	8	N/A
2Ch	R	Tach 3 LS Byte	7	6	5	4	3	2	1	0	N/A
2Dh	R	Tach 3 MS Byte	15	14	13	12	11	10	9	8	N/A
2Eh	R	Tach 4 LS Byte	7	6	5	4	3	2	1	0	N/A
2Fh	R	Tach 4 MS Byte	15	14	13	12	11	10	9	8	N/A

The Fan Tachometer Reading registers contains the number of 11.111μs periods (90 kHz) between full fan revolutions. The results are based on the time interval of two tachometer pulses, since most fans produce two tachometer pulses per full revolution. These registers will be updated at least once every second. Common interpretation of tachometer readings is to take the binary period measurement and convert it to RPM. This may be done by applying the formula:

RPM = (90,000 x 60)/(Decimal Equivalent of binary Tach Reading)

The value, for each fan, is represented by a 16-bit unsigned number.

The Fan Tachometer Reading registers will always return an accurate fan tachometer measurement, even when a fan is disabled or non-functional, however, if PWM commands for a fan (register 30h to 32h) is zero, tach measurements are suspended and the last reading may remain in the register.

In the case of a three-wire fan being driven by PWM signal connected to fan power, the PWM output is held high for the period of the tachometer measurement. This stretching of the PWM will result in an exaggeration of the PWM command at low RPM. These registers are read-only – a write to these registers has no effect.

When the LS Byte of the aSC7621 16-bit register is read, the other byte (MS Byte) is latched at the current value until it is read. At the end of the MS Byte read the Fan Tachometer Reading registers are updated. During spin-up, the PWM duty cycle reported is 0%.

Registers 54-5Bh: Fan Tachometer Limits

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
54h	R/W	Tach 1 Minimum LS Byte	7	6	5	4	3	2	1	0	FF
55h	R/W	Tach 1 Minimum MS Byte	15	14	13	12	11	10	9	8	FF
56h	R/W	Tach 2 Minimum LS Byte	7	6	5	4	3	2	1	0	FF
57h	R/W	Tach 2 Minimum MS Byte	15	14	13	12	11	10	9	8	FF
58h	R/W	Tach 3 Minimum LS Byte	7	6	5	4	3	2	1	0	FF
59h	R/W	Tach 3 Minimum MS Byte	15	14	13	12	11	10	9	8	FF
5Ah	R/W	Tach 4 Minimum LS Byte	7	6	5	4	3	2	1	0	FF
5Bh	R/W	Tach 4 Minimum MS Byte	15	14	13	12	11	10	9	8	FF

The Fan Tachometer Low Limit registers indicate the tachometer reading under which the corresponding bit will be set in the Interrupt Status Register 2 register. In Auto Fan Control mode, the fan can run at low speeds, so care should be taken in software to ensure that the limit is high enough not to cause sporadic alerts. The fan tachometer will not cause a bit to be set in Interrupt Status Register 2 if the current value in Current PWM Duty registers (30h to 32h) is 00h or if the fan is disabled via the Fan Configuration Register. Interrupts will not be generated for a fan if its minimum is set to FF FFh except for timeout. Setting the Ready/Lock/Start/Override register Lock bit has no effect on these registers.

Given the relative insignificance of Bit 0 and Bit 1, these bits could be programmed to designate the physical location of the fan generating the tachometer signal, as follows:

Register Name	Bit 1	Bit 0 (LSB)
CPU Cooler	0	0
Memory Controller	0	1
Chassis Front	1	0
Chassis Rear	1	1

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Register 04-07h: Fan Tachometer Measurement Configuration

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Lock
04h	R/W	Tach 1 Configuration	3-Wire Enable 1	3-Wire Enable 0	Meas Blank 1	Meas Blank 0	Meas Dwell 1	Meas Dwell 0	Meas Duration 1	Meas Duration 0	36	X
05h	R/W	Tach 2 Configuration	3-Wire Enable 1	3-Wire Enable 0	Meas Blank 1	Meas Blank 0	Meas Dwell 1	Meas Dwell 0	Meas Duration 1	Meas Duration 0	36	X
06h	R/W	Tach 3 Configuration	3-Wire Enable 1	3-Wire Enable 0	Meas Blank 1	Meas Blank 0	Meas Dwell 1	Meas Dwell 0	Meas Duration 1	Meas Duration 0	36	X
07h	R/W	Tach 4 Configuration	3-Wire Enable 1	3-Wire Enable 0	Meas Blank 1	Meas Blank 0	Meas Dwell 1	Meas Dwell 0	Meas Duration 1	Meas Duration 0	36	X

The Fan Tachometer Configuration registers contain the settings that define the modes of measurement of the Tachometer input signals. The user is allowed to disable a tachometer measurement or to request PWM stretching, in the case of a 3-wire fan. Also, the rate, start-up and period of measurements within a fan rotation cycle may be selected. The table below describes the controls.

This register becomes read-only when the Ready/Lock/Start/Override register Lock bit is set. Any further attempts to write to this register shall have no effect.

<table>
<tr><th>Bit</th><th>Name</th><th>R/W</th><th>Default</th><th>Description</th></tr>
<tr><td>1:0</td><td>Measurement Duration</td><td>R/W</td><td>10</td><td>The amount of fan rotation used for the tach measurement. Assumes 2 pulse periods per rotation of fan.
00: ¼ Rotation – Tach Count x4 = Reported Value
01: ½ Rotation – Tach Count x2 = Reported Value
10: 1 Rotation – Tach Count x1 = Reported Value (default)
11: 2 Rotation – Tach Count x1 = Reported Value</td></tr>
<tr><td>3:2</td><td>Measurement Dwell</td><td>R/W</td><td>01</td><td>Delay between Tach Measurements
00: 100 ms
01: 300 ms (default)
10: 500 ms
11: 728 ms</td></tr>
<tr><td>5:4</td><td>Measurement Blank</td><td>R/W</td><td>11</td><td>In 3-wire fan mode, a delay is needed to assure that the tach input has stabilized after the PWM has been set to 100%
00: 11.1 μs
01: 22.2 μs
10: 33.3 μs
11: 44.4 μs (default)</td></tr>
<tr><td>7:6</td><td>3-Wire Enable</td><td>R/W</td><td>00</td><td>For 3-Wire mode, the PWM output will be forced to 100% when the tach measurement is being processed. Each fan has a 3-Wire Mode control that will behave as indicated in this table:
<table>
<tr><th>HLFRQ (5Fh-61h)</th><th colspan="2">3-Wire Enable (7:6)</th><th>3-Wire Mode</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Enabled</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Enabled</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Enabled</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Disabled</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Disabled</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Disabled</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Enabled</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Disabled</td></tr>
</table></td></tr>
</table>

Table 15 Tachometer Configuration Register

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Automatic Fan Control

Auto Fan Control Operating Mode

The aSC7621 includes the circuitry for automatic fan control. In Auto Fan Mode, the aSC7621 will automatically adjust the PWM duty cycle of the PWM output. PWM outputs are assigned to a thermal zone based on the fan configuration registers. At any time, the temperature of a zone exceeds its Absolute Limit, all PWM outputs will go to 100% duty cycle to provide maximum cooling to the system.

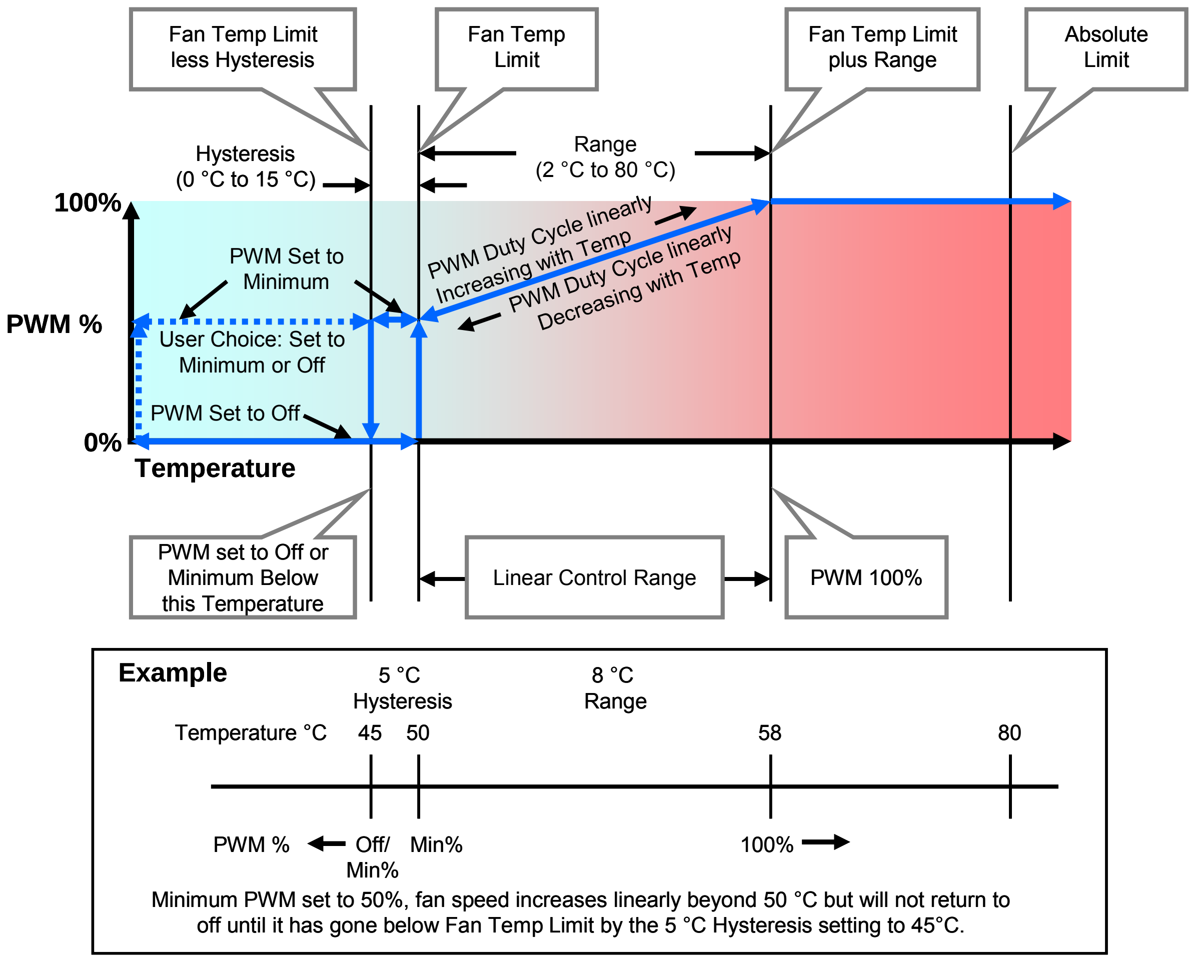

Figure 7 Automatic Fan Speed Control Example

Example for PWM1 assigned to Zone 1:

- Zone 1 Fan Temp Limit (Register 67h) is set to 50°C (32h).
- Zone 1 Range (Register 5Fh) is set to 8°C (6xh).
- Fan PWM Minimum (Register 64h) is set to 50% (80h).

In this case, the PWM duty cycle will be 50% at 50°C.

Since (Zone 1 Fan Temp Limit) + (Zone 1 Range) = 50°C + 8°C = 58°C, the fan will run at 100% duty cycle when the temperature of the Zone 1 sensor reaches 58°C.

Since the midpoint of the fan control range is 54°C, and the median duty cycle is 75% (Halfway between the PWM Minimum and 100%), PWM1 duty cycle would be 75% at 54°C.

Above (Zone 1 Fan Temp Limit) + (Zone 1 Range), the duty cycle will be 100%.

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Automatic Fan Speed Control using Maximum PWM Setting

The previously described and illustrated mode had no restriction on the maximum PWM setting. It is useful to limit the maximum PWM command sent to the fan in order to minimize the acoustic impact. The Maximum PWM setting will clamp the automatic fan PWM command at a user selected value. The Absolute Limit setting will still cause the PWM command to be 100% and that will remain until the temperature falls below the Absolute Limit temperature by an amount equal to the hysteresis setting. This will minimize the acoustic impact of having a temperature moving back and forth close to the Absolute Limit.

The Absolute Limit may be set above or below the Fan Temp Limit plus Range. The PWM value will be overridden and will follow the hysteresis curve in either case, but the acoustic impact will be different, running the fan to 100% PWM at a lower temperature, but enhancing the cooling effect. Absolute Limit set on the low end is shown in Figure 8Figure 7. Setting it above is shown in Figure 9.

It is important to consider the combination of Fan Temp Limit, Range, Maximum PWM and Absolute Limit and their impact on cooling and acoustics. In addition, the capability to operate a fan from a combination of thermal zones allows a compound linear slope to be achieved for further optimization.

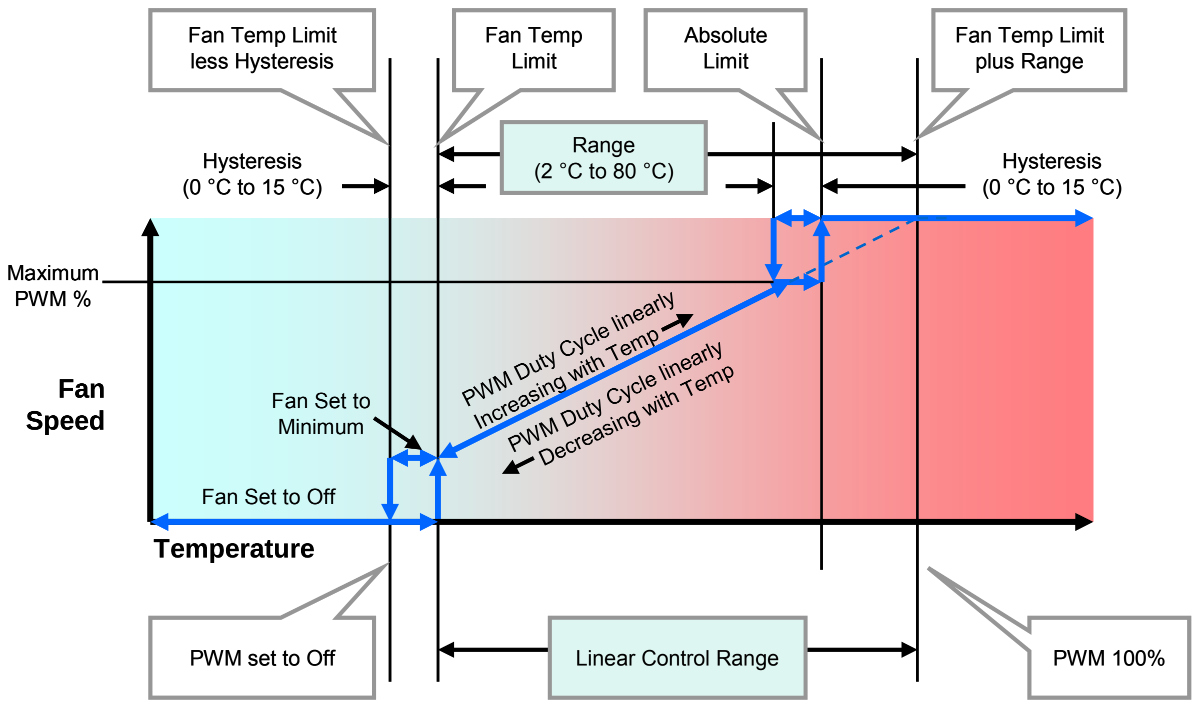

Figure 8 Fan Control with Absolute Limit Set below Fan Temp Limit Plus Range

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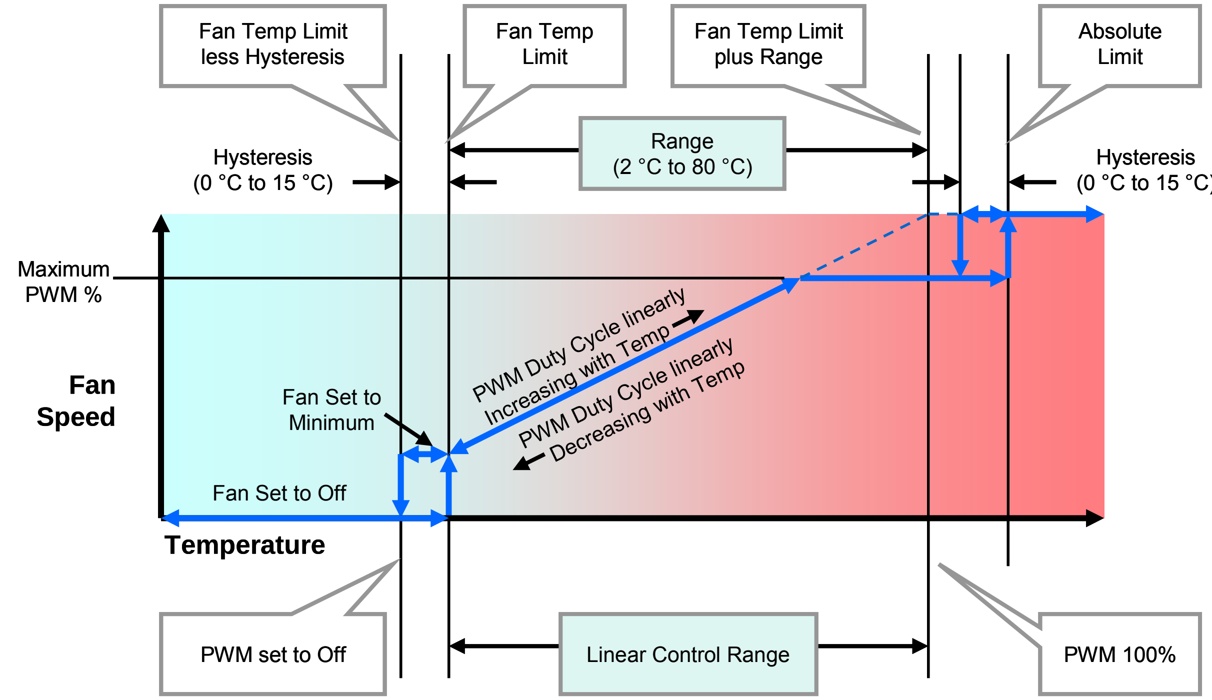

Figure 9 Fan Control with Absolute Limit Set above Fan Temp Limit Plus Range

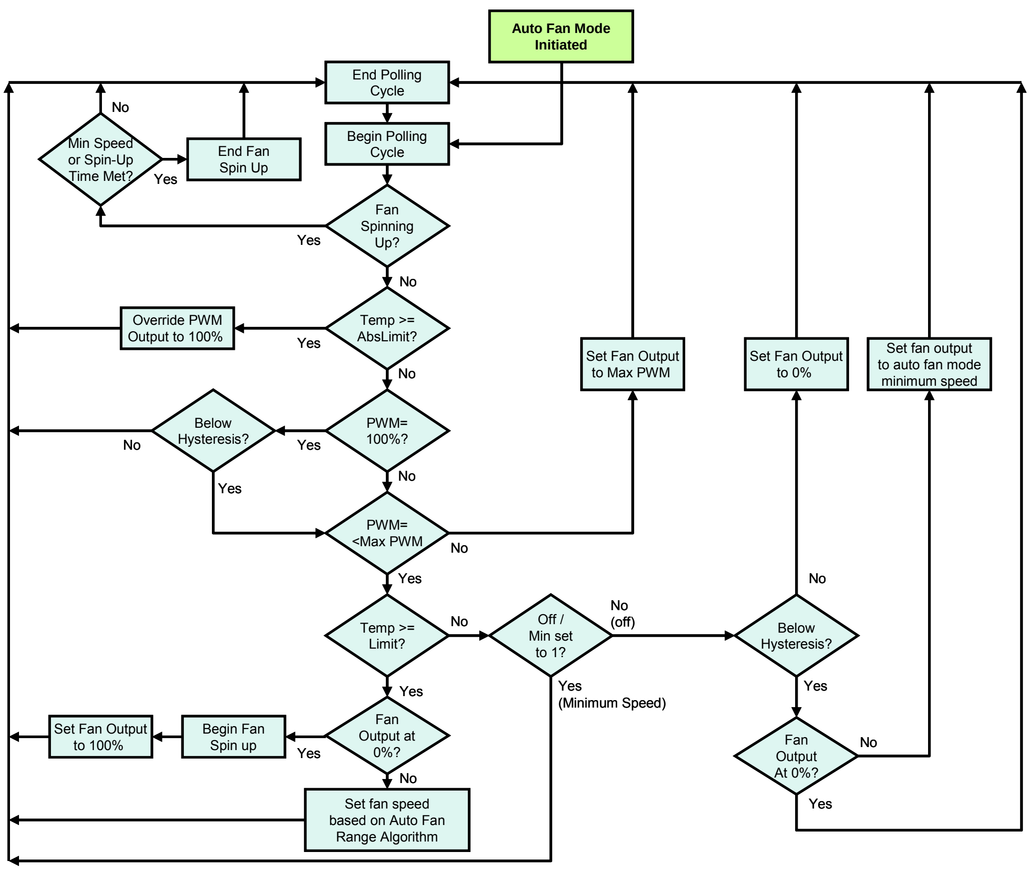

Figure 10 Automatic Fan Control Algorithm

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Fan Register Device Set-Up

The BIOS will follow the following steps to configure the fan registers on the aSC7621. The registers corresponding to each function are listed. All steps may not be necessary if default values are acceptable. Regardless of all changes made by the BIOS to the fan limit and parameter registers during configuration, the aSC7621 will continue to operate based on default values until the START bit (bit 0), in the Ready/Lock/Start/Override register (address 40h), is set. Once the fan mode is updated, by setting the START bit to 1, the aSC7621 will operate using the values that were set by the BIOS in the fan control limit and parameter registers (address in the range 3Ch through 75h). It is assumed that each Temperature Zone has already been configured to be associated with the appropriate temperature measurement either with the default settings or to the user's preference. See previous section on Temperature Zone configuration.

1. Set limits and parameters (not necessarily in this order):
   - [3Ch, 5F-61h] Set PWM frequency for the fan and auto fan control range for each zone.
   - [3Ch, 62-63h] Set spike smoothing and min/off.
   - [5C-5Eh] Set the fan spin-up delay.
   - [75h] Set PWM spin-up mode to terminate after time set in [5C-5Eh]. Value = 00h instead of default 01h.
   - [5C-5Eh] Match fan with a corresponding thermal zone.
   - [3Bh, 67-69h] Set the fan temperature limits.
   - [3Dh, 6A-6Ch] Set the temperature absolute limits.
   - [64-66h] Set the PWM minimum duty cycle.
   - [6D-6Eh] Set the temperature hysteresis values.
2. [40h] Set bit 0 (START) to update fan control and limit register values and start fan control based on these new values.

   [40h] (Optional) Set bit 1 (LOCK) to lock the fan limit and parameter registers. **WARNING:** this is a **non-reversible** change in state and locks out further change in critical fan control parameters until power is removed from the aSC7621.

Register 5F-61h: Auto Fan Speed Range, PWM Frequency

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Lock
5Fh	R/W	Zone 1 Range Fan1 Frequency	RAN3	RAN2	RAN1	RAN0	HLFRQ	FRQ2	FRQ1	FRQ0	C3	X
60h	R/W	Zone 2 Range/ Fan 2 Frequency	RAN3	RAN2	RAN1	RAN0	HLFRQ	FRQ2	FRQ1	FRQ0	C3	X
61h	R/W	Zone 3 Range/ Fan 3 Frequency	RAN3	RAN2	RAN1	RAN0	HLFRQ	FRQ2	FRQ1	FRQ0	C3	X
3Ch	R/W	Zone 4 Range, Spike Smoothing	RAN3	RAN2	RAN1	RAN0	ZN4E	ZN4-2	ZN4-1	ZN4-0	C3h	X

In Auto Fan Mode, when the temperature for a zone is above the Temperature Limit (Registers 3Bh, 67-69h) and below its Absolute Temperature Limit (Registers 3Dh 6A-6Ch), the speed of a fan assigned to that zone is determined as follows:

When the temperature reaches the Fan Temp Limit for a zone, the PWM output assigned to that zone will be Fan PWM Minimum. Between Fan Temp Limit and (Fan Temp Limit + Range), the PWM duty cycle will increase linearly according to the temperature as shown in the figure below. The PWM duty cycle will be 100% at (Fan Temp Limit + Range).

PWM frequency - FRQ[3:0] and HLFRQ

The PWM frequency bits [3:0] determine the PWM frequency for the fan. The aSC7621 has high and low frequency ranges for the PWM outputs that are controlled by the HLFRQ bit.

PWM Frequency Selection (Default = 0011 ≈ 30 Hz).

HLFRQ	FRQ [2:0]	PWM Frequency
0	000	~10 Hz
0	001	~15 Hz
0	010	~23 Hz
0	011	~30 Hz (Default)
0	100	~38 Hz
0	101	~47 Hz
0	110	~62 Hz
0	111	~94 Hz
1	000	~23 kHz
1	001	~24 kHz
1	010	~25 kHz
1	011	~26 kHz
1	100	~27 kHz
1	101	~28 kHz
1	110	~29 kHz
1	111	~30 kHz

Table 16 Register Setting vs PWM Frequency

RAN[3:0]	Linear Control Range (°C)
0000	2
0001	2.5
0010	3.33
0011	4
0100	5
0101	6.67
0110	8
0111	10
1000	13.33
1001	16
1010	20
1011	26.67
1100	32 (default)
1101	40
1110	53.33
1111	80

Table 17 Zone Range Setting, RAN[3:0]

This register becomes Read-Only when the Ready/Lock/Start/Override register Lock bit is set. Any further attempts to write to this register shall have no effect. After power up the default value is used for bits 3:0 of registers 5F-61h whenever the Ready/Lock/Start/Override register Start bit is cleared even though modifications to this register are possible.

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Register 40h: Ready/Lock/Start/Override

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
40h	R/W	Ready/Lock/Start/ Override	RES	RES	SAFE	PECI	OVRID	READY	LOCK	START	00

Bit	Name	R/W	Default	Description
0	START	R/W	0	When software writes a 1 to this bit, the aSC7621 fan monitoring and PWM output control functions will use the values set in the fan control limit and parameter registers (addresses 30-32h and 5Fh through 61h). Before this bit is set, the aSC7621 will not update the used register values, the default values will remain in effect. Whenever this bit is set to 0, the aSC7621 fan monitoring and PWM output control functions use the default fan limits and parameters, regardless of the current values in the limit and parameter registers (addresses 30-32h and 5Fh through 61h). The aSC7621 will preserve the values currently stored in the limit and parameter registers when this bit set or cleared. This bit is not affected by the state of the Lock bit. It is expected that all limit and parameter registers will be set by BIOS or application software prior to setting this bit.
1	LOCK	R/W	0	Setting this bit to 1 locks specified limit and parameter registers. **WARNING:** Once this bit is set, limit and parameter registers become read-only and will remain locked **until the device is powered off**. This register bit becomes read-only once it is set.
2	READY	R	0	The aSC7621 sets this bit automatically after the part is fully powered up, has completed the power-up-reset process, and after all A/D converters are properly functioning.
3	OVRID	R/W	0	If this bit is set to 1, all PWM outputs will go to 100% duty cycle regardless of whether or not the lock bit is set. The OVRID bit has precedence over the disabled mode. Therefore, when OVRID is set the PWM will go to 100% even if the PWM is in the disabled mode.
4	PECI	R/W	0	When software writes a 1 to this bit, support for the monitoring of Processor temperatures via the PECI interface is enabled. This bit becomes read only when the LOCK bit is set to 1.
5	SAFE	R/W	0	When software writes a 1 to this bit, it indicates that when operating the fan in manual mode, the PWM duty cycle will be overridden to 100% when any Zone exceeds its Absolute Limit. When the bit is set to 0, it indicates that when operating the fan in manual mode, the PWM duty cycle will not be overridden to 100% when any Zone exceeds its Absolute Limit.
6-7	RESERVED	R	0	Reserved

Table 18 READY / LOCK / START / OVRID Settings

Register 30-32h: Current PWM Duty Cycle

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
30h	R/W	Fan 1 Current PWM Duty	7	6	5	4	3	2	1	0	FF
31h	R/W	Fan 2 Current PWM Duty	7	6	5	4	3	2	1	0	FF
32h	R/W	Fan 3 Current PWM Duty	7	6	5	4	3	2	1	0	FF

The Current PWM Duty registers store the current duty cycle at each PWM output. At initial power-on, the PWM duty cycle is 100% and thus, when read, this register will return FFh. After the Ready/Lock/Start/Override register Start bit is set, this register and the PWM signals will be updated based on the algorithm described in the Auto Fan Control Operating Mode section. When Ready/Lock/Start/Override register Start bit is zero, default value (FFh) is used.

When read, the Current PWM Duty registers return the current PWM duty cycle. These registers are read-only unless the fan is in manual (test) mode, in which case a write to these registers will directly control the PWM duty cycle for each fan. The PWM duty cycle is represented as shown in Table 19.

If a 3-wire fan is being used and the option to enable 3-wire tach measurement is selected, the effective PWM duty cycle will be impacted by this feature. The 3-wire Enable setting will hold the PWM signal high for the period taken to make a tachometer reading. This period depends on the RPM and various tachometer measurement parameters. Overall impact is that lower PWM commands will be effectively increased and there may be acoustic effects.

Current PWM %	Register Value		
	Binary		Hex
0%	0000	0000	00
~25%	0100	0000	40
~50% (Default)	1000	0000	80
~75%	1100	0000	C0
100%	1111	1111	FF

Table 19 Current PWM Duty Cycle Setting

Register 4E-53h and 39h-3Ah: Temperature Zone Limit Registers

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
4Eh	R/W	Zone 1 Low Temperature	7	6	5	4	3	2	1	0	81
4Fh	R/W	Zone 1 High Temperature	7	6	5	4	3	2	1	0	7F
50h	R/W	Zone 2 Low Temperature	7	6	5	4	3	2	1	0	81
51h	R/W	Zone 2 High Temperature	7	6	5	4	3	2	1	0	7F
52h	R/W	Zone 3 Low Temperature	7	6	5	4	3	2	1	0	81
53h	R/W	Zone 3 High Temperature	7	6	5	4	3	2	1	0	7F
34h	R/W	Zone 4 Low Temperature	7	6	5	4	3	2	1	0	81
3Ah	R/W	Zone 4 High Temperature	7	6	5	4	3	2	1	0	00

If an external temperature input or the internal temperature sensor either exceeds the value set in the corresponding high limit register or falls below the value set in the corresponding low limit register, the corresponding bit will be set automatically by the aSC7621 in the Interrupt Status Register 1 (41h). For example, if the temperature read from the Remote - and Remote + inputs exceeds the Zone 1 High Temp register limit setting, Interrupt Status Register 1 ZN1 bit will be set. The temperature limits in these registers are represented as 8 bit 2's complement, signed numbers in Celsius, as shown below in Table 20. Setting the Ready/Lock/Start/Override register Lock bit has no effect on these registers.

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Temperature	Temperature Limit (2's Complement)	
>127°C	0111	1111
+127°C (Default High)	0111	1111
+125°C	0111	1101
+90°C	0101	1010
+50°C	0011	0010
+25°C	0001	1001
0°C	0000	0000
-50°C	1100	1110
-127°C (Default Low)	1000	0001

Table 20 Temperature Zone High- and Low-Limit Registers - 8-Bit Two's Complement

Register 5C-5Eh: Fan Temperature Zone Assignment and Spin-up Mode

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Lock
5Ch	R/W	Fan 1 Configuration	ZON2	ZON1	ZON0	INV	ALT	SPIN2	SPIN1	SPIN0	62	X
5Dh	R/W	Fan 2 Configuration	ZON2	ZON1	ZON0	INV	ALT	SPIN2	SPIN1	SPIN0	62	X
5Eh	R/W	Fan 3 Configuration	ZON2	ZON1	ZON0	INV	ALT	SPIN2	SPIN1	SPIN0	62	X

This register becomes read-only when the Ready/Lock/Start/Override register Lock bit is set. Any further attempts to write to this register shall have no effect.

Bits [7:5] Zone/Mode and Bit [3] Alternate Zone/Mode

Bits [7:5] of the Fan Configuration registers associate each fan with a Temperature Zone. When in Auto Fan Mode the fan will be assigned to a zone, and its PWM duty cycle will be adjusted according to the temperature of that zone. If "Hottest" option is selected (110), the fan will be controlled by the the hottest of zones 1, 2 or 3. To determine the "hottest zone", the PWM level for each zone is calculated then the zone with the higher PWM value (not temperature) is selected. When in manual control mode, the Current PWM duty register (30-32h) become Read/Write. It is then possible to control the PWM outputs with software by writing to these registers. When the fan is disabled (100) the corresponding PWM output should be driven low (or high, if inverted).

Bit-3 enables an alternate set of definitions for the ZON[2:0] Zone/Mode bits described in Table 21.

Fan Configuration ALT = 0	ZON [2:0]
Fan on zone 1.	000
Fan on zone 2.	001
Fan on zone 3.	010
Fan on full. PWM = 255.	011
Fan disabled. PWM = 0.	100
Fan controlled by hottest of 2, or 3.	101
Fan controlled by hottest of zones 1, 2, and 3.	110
Fan Manually controlled (Test Mode)	111

Fan Configuration ALT = 1	ZON[2:0]
Fan on zone 4.	000
Fan controlled by hottest of zones 1, 2, 3, and 4.	001
Reserved. (Fan on full. PWM = 255.)	010
Reserved. (Fan on full. PWM = 255.)	011
Vendor specific. (Fan on full. PWM = 255.)	100
Vendor specific. (Fan on full. PWM = 255.)	101
Vendor specific. (Fan on full. PWM = 255.)	110
Vendor specific. (Fan on full. PWM = 255.)	111

Table 21 Fan Zone Setting

Bit [4] PWM Invert

Bit [4] inverts the PWM output. If set to 0, 100% duty cycle will yield an output that is always high. If set to 1, 100% duty cycle will yield an output that is always low.

Bit [2:0] Spin Up

Bits [2:0] specify the 'spin up' time for the fan. When a fan is being started from a stationary state, the PWM output is held at 100% duty cycle for the time specified in the table below before scaling to a lower speed.

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Spin Up Time	SPIN[2:0]
0 ms	000
100 ms	001
250 ms	010
400 ms	011
700 ms	100
1000 ms	101
2000 ms	110
4000 ms	111

Table 22 Fan Spin-Up Register

Register 00h: Zone Status

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Lock
00h	R	Fan Zone Status	Fan 3 Zone #		Fan 2 Zone #		Fan 1 Zone #		RES	RES	N/A	
			1	0	1	0	1	0				

The Fan Zone Status register reports the current Temperature Zone assignment to a fan. It reveals the actual assignment when the user has selected a mode in which the hottest of multiple zones to determine fan speed. Zone 1 = 01b, Zone 2 = 10b, Zone 3 = 11b and Zone 4 = 00b. If a fixed assignment or manual fan speed control is used these Zone #s will return 00b. This is a read-only register, a write has no effect.

Register 62h, 63h, 3Ch: Min/Off, Spike Smoothing

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Lock
62h	R/W	Min/Off, Zone1 Spike Smoothing	OFF3	OFF2	OFF1	RES	ZN1E	ZN1-2	ZN1-1	ZN1-0	00	X
63h	R/W	Zone2 Spike Smoothing	ZN2E	ZN2-2	ZN2-1	ZN2-0	ZN3E	ZN3-2	ZN3-1	ZN3-0	00	X
3Ch	R/W	Zone 4 Range, Spike Smoothing	RAN3	RAN2	RAN1	RAN0	ZN4E	ZN4-2	ZN4-1	ZN4-0	C3h	X

The OFF1-OFF3 (Bits 7 to 5) specify whether the duty cycle will be 0% or Minimum Fan Duty when the measured temperature falls below the Temperature LIMIT register setting (see Table 24 below).

If the Remote pins are connected to a processor or chipset, instantaneous temperature spikes may be sampled by the aSC7621. Temperature readings are first passed through a user-programmable filter described above in the Temperature Measurement Filter section and then assigned to a Temperature Zone for fan speed control.

If these spikes are not filtered, the CPU fan (if connected to aSC7621) may turn on prematurely or produce unpleasant noise. For this reason, any zone that is connected to a chipset or processor should have spike smoothing enabled. Individual system characteristics will determine how large this coefficient should be.

When spike smoothing is enabled, the temperature reading registers will contain a value that is the result of the first filter. A second filter acts on the assigned Temperature Zone and is “smoothed out” for fan speed control. Table 23 shows the approximate filter response time to a step function in Temperature Zone reading.

ZN1E, ZN2E, ZN3E and ZN4E enable temperature smoothing for zones 1, 2, 3 and 4 respectively.

ZN1-2, ZN1-1 and ZN1-0 control smoothing time for Zone 1.

ZN2-2, ZN2-1 and ZN2-0 control smoothing time for Zone 2.

ZN3-2, ZN3-1 and ZN3-0 control smoothing time for Zone 3.

ZN4-2, ZN4-1 and ZN4-0 control smoothing time for Zone 4.

These registers become read-only when the Ready/Lock/Start/Override register Lock bit is set. Any further attempts to write to these registers shall have no effect.

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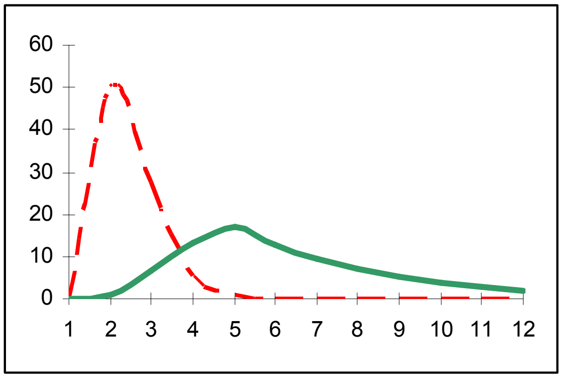

Figure 11 Representation of What Temperature Is Passed to the aSC7621 Auto Fan Control with (green) and without (red dashed) Spike Smoothing

Spike Smoothing Time	ZNn-[2:0]
35 seconds	000
17.6 seconds	001
11.8 seconds	010
7.0 seconds	011
4.4 seconds	100
3.0 seconds	101
1.6 seconds	110
0.8 seconds	111

Table 23 Spike Smoothing for ZN1 to ZN4

PWM Action	Off/Min Bit
At 0% duty below LIMIT	0
At Min PWM Duty below LIMIT	1

Table 24 PWM Output Below Limit Depending on Value of Off/Min

Register 64-66h: Minimum PWM Duty Cycle

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Lock
64h	R/W	Fan 1 PWM Minimum	7	6	5	4	3	2	1	0	80	X
65h	R/W	Fan 2 PWM Minimum	7	6	5	4	3	2	1	0	80	X
66h	R/W	Fan 3 PWM Minimum	7	6	5	4	3	2	1	0	80	X

This register specifies the minimum duty cycle that the PWM will output when the measured temperature reaches the Temperature LIMIT register setting.

This register becomes Read-only when the Ready/Lock/Start/Override register Lock bit is set. Any further attempts to write to this register shall have no effect.

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Minimum PWM %	Register Value		
	Binary		Hex
0%	0000	0000	00
~25%	0100	0000	40
~50% (Default)	1000	0000	80
~75%	1100	0000	C0
100%	1111	1111	FF

Table 25 Minimum PWM Duty Cycle Setting

Register 38-3Ah: Maximum PWM Duty Cycle

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Lock
38h	R/W	Fan 1 Max Duty Cycle	7	6	5	4	3	2	1	0	FF	X
39h	R/W	Fan 2 Max Duty Cycle	7	6	5	4	3	2	1	0	FF	X
3Ah	R/W	Fan 3 Max Duty Cycle	7	6	5	4	3	2	1	0	FF	X

The Maximum PWM Duty registers store the maximum duty cycle that may be commanded at each PWM output under automatic fan control. This value is overridden to 100% when the assigned zone's temperature has exceeded the Absolute Maximum Temperature setting. When temperature falls below Absolute Maximum, PWM command will resume the linear ramp only after it has fallen by the Thermal Zone Hysteresis value (Registers 6D-6Eh). Values follow the representation in Table 19.

This register becomes read-only when the Ready/Lock/Start/Override register Lock bit is set. Any further attempts to write to this register shall have no effect.

Register 67-69h: Temperature Limit

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Lock
67h	R/W	Zone 1 Fan Temp Limit	7	6	5	4	3	2	1	0	5A	X
68h	R/W	Zone 2 Fan Temp Limit	7	6	5	4	3	2	1	0	5A	X
69h	R/W	Zone 3 Fan Temp Limit	7	6	5	4	3	2	1	0	5A	X
3Bh	R/W	Zone 4 Fan Temp Limit	7	6	5	4	3	2	1	0	E0	X

These are the temperature limits for the individual zones. When the current temperature equals this limit, the fan will be turned on if it is not already. When the temperature exceeds this limit, the fan speed will be increased according to the algorithm set forth in the Auto Fan Range, PWM Frequency register description, Default = 90°C = 5Ah

This register becomes read-only when the Ready/Lock/Start/Override register Lock bit is set. Any further attempts to write to this register shall have no effect.

Temperature	Fan Temp Limit (2's Complement)	
>127°C	0111	1111
+127°C	0111	1111
+125°C	0111	1101
+90°C (default)	0101	1010

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Temperature	Fan Temp Limit (2's Complement)	
+50°C	0011	0010
+25°C	0001	1001
0°C	0000	0000
-50°C	1100	1110
-127°C	1000	0001

Table 26 Fan Temperature Limit Register - 8-Bit Two's Complement

Register 6A-6Ch: Temperature Limit

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Lock
6Ah	R/W	Zone 1 Temp Absolute Limit	7	6	5	4	3	2	1	0	64	X
6Bh	R/W	Zone 2 Temp Absolute Limit	7	6	5	4	3	2	1	0	64	X
6Ch	R/W	Zone 3 Temp Absolute Limit	7	6	5	4	3	2	1	0	64	X
3Dh	R/W	Zone 4 Temp Absolute Limit	7	6	5	4	3	2	1	0	00	X

In the Auto Fan mode, if a zone exceeds the temperature set in the Absolute Temperature Limit register, all of the PWM outputs will increase its duty cycle to 100%. This is a safety feature that attempts to cool the system if there is a potentially catastrophic thermal event. If set to 80h (-128°C), the feature is disabled. Default = 100 C = 64h. The PWM will remain at 100% until the assigned Temperature Zone falls below the Absolute Temp Limit for that zone by an amount equal to the hysteresis value for that zone.

These registers become read-only when the Ready/Lock/Start/Override register Lock bit is set. Any further attempts to write to these registers shall have no effect.

Temperature	Absolute Limit (2's Complement)	
>127°C	0111	1111
+127°C	0111	1111
+125°C	0111	1101
+100°C (default)	0110	0100
+50°C	0011	0010
+25°C	0001	1001
0°C	0000	0000
-50°C	1100	1110
-127°C	1000	0001
-128°C (Disable)	1000	0000

Table 27 Absolute Temperature Limit Register - 8-Bit Two's Complement

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Register 6D-6Eh: Thermal Zone Hysteresis

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Lock
6Dh	R/W	Zone 1 and Zone 2 Hysteresis	H1-3	H1-2	H1-1	H1-0	H2-3	H2-2	H2-1	H2-0	44	X
6Eh	R/W	Zone 3 and Zone 4 Hysteresis	H3-3	H3-2	H3-1	H3-0	H4-3	H4-2	H4-1	H4-0	44	X

If the temperature is above Fan Temp Limit, then drops below Fan Temp Limit, the following will occur:

- The fan will remain on, at Fan PWM Minimum, until the temperature goes a certain amount below Fan Temp Limit.
- The Hysteresis registers control this amount. See below table for details, all values from 0°C to 15°C are possible.

This register becomes read-only when the Ready/Lock/Start/Override register Lock bit is set. Any further attempts to write to these registers shall have no effect.

Temperature	Zone Hysteresis Hn-[3:0]
0°C	0000
1°C	0001
4°C (default)	0100
10°C	1010
15°C	1111

Table 28 Zone Hysteresis Register Format

Register 75h: Fan Spin-Up Mode

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Lock
75h	R/W	Fan Spin-Up Mode	Tach4 Disable	Tach3/4 Disable	Tach2 Disable	Tach1 Disable	RES	PWM3 SU	PWM2 SU	PWM1 SU	00	X

The PWM SU bit configures the PWM spin-up mode. If PWM SU is cleared the spin-up time will terminate after time programmed by the Fan Configuration register has elapsed. When set to 1, the spin-up time will terminate early if the TACH reading interpreted as RPM exceeds the Tach Minimum RPM value or after the time programmed by the Fan Configuration register has elapsed, which ever occurs first. Note that the magnitudes of the tach readings and the limits in the registers represent a time period that is inversely proportional to RPM.

This register becomes Read-only when the Ready/Lock/Start/Override register Lock bit is set. Any further attempts to write to this register shall have no effect.

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Miscellaneous Registers

Registers 19h and 1Ah: GPIO Configuration

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Lock
19h	R/W	GPIO 1 Configuration	RES	RES	Alert Assignment		GPIO 1 bit	GPIO 1 Function			00	X
					1	0		2	1	0		
1Ah	R/W	GPIO 2 Configuration	GPIO 2 bit	GPIO 2 Function			GPIO 3 bit	GPIO 3 Function			00	X
				2	1	0		2	1	0		

GPIO pins are multi-function and may be used as input, output, bi-directional or may serve as an alarm pin with ALERT or THERM behavior. This is an open-drain output and a read returns the state of the pin, a write drives the pin based on the GPIO bit.

This register becomes Read-only when the Ready/Lock/Start/Override register Lock bit is set. Any further attempts to write to this register shall have no effect.

GPIO Configuration 1 contains two controls. The 1st is the ALERT Assignment and the 2nd is GPIO 1 pin definitions.

1. The Alert assignment defines which one of the GPIO pins that will source the Alert. The Alert assignment supersedes any GPIO pin configuration.
2. The GPIO 1 Function defines the configuration of the GPIO 1 pin. The default is to configure the pin as an input. Any zone Fan Temp Limit status can be sent to the pin or the written value of bit 3 can be sent to GPIO 1 pin. The read value of bit 3 indicates the level of the GPIO 1 pin not the state of the GPIO Register bit.

Bit	Field	GPIO Configuration 1 [19h]	
2:0	GPIO 1 Function	**Value**	**Function**
		000 (Default)	GPIO PIN Read only, Output drive always set high.
		001	Zone 1 Therm Status, pin = 0, Zone 1 exceeds Fan Temp Limit
		010	Zone 2 Therm Status, pin = 0, Zone 2 exceeds Fan Temp Limit
		011	Zone 3 Therm Status, pin = 0, Zone 3 exceeds Fan Temp Limit
		100	Zone 4 Therm Status, pin = 0, Zone 4 exceeds Fan Temp Limit
		101	Any Zone Therm Status, pin = 0, Any Zone exceeds Fan Temp Limit
		110	GPIO PIN Read only, Output drive always set high.
		111	GPIO PIN IO Mode, Output drive set to GPIO Reg.Bit 3.
3	GPIO 1 Bit	Read of this bit always returns value of GPIO 1 IO Pin. Write to this function sends value to GPIO 1 Pin when Function is IO mode.	
5:4	Alert Assignment	**Value**	**Function**
		00 (Default)	No ALERT Function ALERT disabled
		01	ALERT function sent to GPIO 1, pin = 0, ALERT Active
		10	ALERT function sent to GPIO 2, pin = 0, ALERT Active
		11	ALERT function sent to GPIO 3, pin = 0, ALERT Active
7:6	RES	Reserved	

Table 29 GPIO Configuration 1 [19h]

GPIO Configuration 2 contains two controls. The 1st is GPIO 2 pin definition and the 2nd is GPIO 3 pin definition.

1. The GPIO 2 Function defines the configuration of the GPIO 2 pin. The default is to configure the pin as an input. Any zone therm status can be sent to the pin or the written value of bit 7 can be sent to GPIO 2 pin. The read value of bit 7 indicates the level of the GPIO 2 pin not the state of bit 7 register.
2. The GPIO 3 Function defines the configuration of the GPIO 3 pin. The default is to configure the pin as an input. Any zone therm status can be sent to the pin or the written value of bit 3 can be sent to GPIO 3 pin. The read value of bit 3 indicates the level of the GPIO 3 pin not the state of bit 3 register

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Bit	Field	GPIO Configuration 2 [1Ah]	
2-0	GPIO 3 Function	**Value**	**Function**
		000 (Default)	GPIO PIN Read only Output drive always set high.
		001	Zone 1 Therm Status, pin = 0, Zone 1 exceeds Fan Temp Limit
		010	Zone 2 Therm Status, pin = 0, Zone 2 exceeds Fan Temp Limit
		011	Zone 3 Therm Status, pin = 0, Zone 3 exceeds Fan Temp Limit
		100	Zone 4 Therm Status, pin = 0, Zone 4 exceeds Fan Temp Limit
		101	Any Zone Therm Status, pin = 0, Any Zone exceeds Fan Temp Limit
		110	GPIO PIN Read only, Output drive always set high.
		111	GPIO PIN IO Mode, Output drive set to GPIO Reg.Bit 3.
3	GPIO 3 Bit	Read of this bit always returns value of GPIO 3 IO Pin. Write to this function sends value to GPIO 3 Pin when Function is IO mode.	
7:4	Alert Assignment	**Value**	**Function**
		000 (Default)	GPIO PIN Read only Output drive always set high.
		001	Zone 1 Therm Status, pin = 0, Zone 1 exceeds Fan Temp Limit
		010	Zone 2 Therm Status, pin = 0, Zone 2 exceeds Fan Temp Limit
		011	Zone 3 Therm Status, pin = 0, Zone 3 exceeds Fan Temp Limit
		100	Zone 4 Therm Status, pin = 0, Zone 4 exceeds Fan Temp Limit
		101	Any Zone Therm Status, pin = 0, Any Zone exceeds Fan Temp Limit
		110	GPIO PIN Read only Output drive always set high.
		111	GPIO PIN IO Mode Output drive set to GPIO Reg.Bit 7.
7	GPIO 2 Bit	Read of this bit always returns value of GPIO 2 IO Pin. Write to this function sends value to GPIO 2 Pin when Function is IO mode.	

Table 30 GPIO Configuration 2 [1Ah]

Register 3Eh: Company ID

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
3Eh	R	Company ID	7	6	5	4	3	2	1	0	61

The company ID register contains the company identification number. For Andigilog this is 61h. This number is assigned by Intel and is a method for uniquely identifying the part manufacturer. This register is read-only – a write to this register has no effect.

Register 3Fh: Version/Stepping

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
3Fh	R	Version/Stepping	VER3	VER2	VER1	VER0	4WIRE	PECI	STP1	STP0	6C

The two least significant bits of the Version/Stepping register [1:0] contain the current stepping of the aSC7621 silicon. The four most significant bits [7:4] reflect the aSC7621 base device number when set to a value of 0110b. For the aSC7621, this register will read 01101100b (6Ch).

The register is used by application software to identify which device in the hardware monitor family has been implemented in the given system. Based on this information, software can determine which registers to read from and write to. Further, application software may use the current stepping to implement work-around for bugs found in a specific silicon stepping.

This register is read-only – a write to this register has no effect.

Register 6Fh: Test Register

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Lock
6Fh	R/W	Test Register	RES	RES	RES	RES	RES	RES	RES	XEN	00h	X

XOR Tree Test

The aSC7621 incorporates a XOR tree test mode. When the test mode is enabled by setting the "XEN" bit high in the Test Register at address 6Fh via the SMBus, the part will enter XOR test mode.

Since the test mode an XOR tree, the order of the signals in the tree is not important. SMBDAT and SMBCLK are not included in the test tree. Connections to the XOR tree are shown in Figure 12.

This register becomes Read-Only when the Ready/Lock/Start/Override register Lock bit is set. Any further attempts to write to this registers shall have no effect.

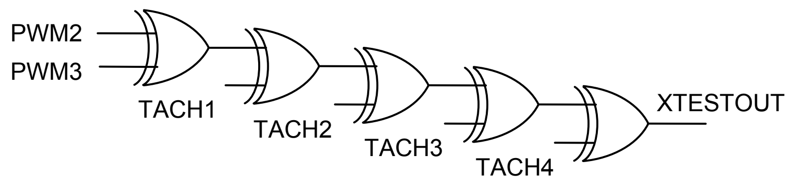

Figure 12 XOR Test Tree

Register 70-7Fh: Vendor Specific Registers

These registers are for vendor specific features, including test registers. They will not default to a specific value on power up.

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Applications Information

Remote Diodes

The aSC7621 is designed to work with a variety of remote sensors in the form of the substrate thermal diode of a CPU or graphics controller or a diode-connected transistor. Actual diodes are not suited for these measurements.

There is some variation in the performance of these diodes, described in terms of its departure from the ideal diode equation. This factor is called diode non-ideality, nf.

The equation relating diode temperature to a change in thermal diode voltage with two driving currents is:

$$\Delta V_{BE} = (nf)\frac{KT}{q}\ln(N)$$

where:

nf = diode non-ideality factor, (nominal 1.009).
K = Boltzman's constant, (1.38×10^{-23}).
T = diode junction temperature in Kelvins.
q = electron charge (1.6×10^{-19} Coulombs).
N = ratio of the two driving currents (16).

The aSC7621 is designed and trimmed for an expected nf value of 1.009, based on the typical value for the Intel Pentium™ III and AMD Athlon™. There is also a tolerance on the value provided. The values for other CPUs and the 2N3904 may have different nominal values and tolerances. Consult the CPU or GPU manufacturer's data sheet for the nf factor. Table 31 gives a representative sample of what one may expect in the range of non-ideality. The trend with CPUs is for a lower value with a larger spread.

When thermal diode has a non-ideality factor other than 1.009 the difference in temperature reading at a particular temperature may be interpreted with the following equation:

$$T_{actual} = T_{reported}\left(\frac{1.009}{n_{actual}}\right)$$

where:

$T_{reported}$ = reported temperature in temperature register.
T_{actual} = actual remote diode temperature.
n_{actual} = selected diode's non-ideality factor, nf .
Temperatures are in Kelvins or °C + 273.15.

This equation assumes that the series resistance of the remote diode is the same for each. This resistance is given in the data sheet for the CPU and may vary from 2.5Ω to 4.5Ω.

Although the temperature error caused by non-ideality difference is directly proportional to the difference from 1.008, but a small difference in non-ideality results in a relatively large difference in temperature reading. For example, if there were a ±1% tolerance in the non-Ideality of a diode it would result in a ±2.7 degree difference (at 0°C) in the result (0.01 x 273.15).

This difference varies with temperature such that a fixed offset value may only be used over a very narrow range. Typical correction method required when measuring a wide range of temperature values is to scale the temperature reading in the host firmware.

Part	nf Min	nf Nom	nf Max	Series Res
Pentium™ III (CPUID 68h)	1.0057	1.008	1.0125	
Pentium 4, 130nM	1.001	1.002	1.003	3.64
Pentium 4, 90nM		1.011		3.33
Pentium 4, 65nM		1.009		4.52
Intel Pentium M	1.0015	1.0022	1.0029	3.06
AMD Athlon™ Model 6	1.002	1.008	1.016	
AMD Duron™ Models 7 and 8	1.002	1.008	1.016	
AMD Athlon Models 8 and 10	1.0000	1.0037	1.0090	
2N3904	1.003	1.0046	1.005	

Table 31 Representative CPU Thermal Diode and Transistor Non-Ideality Factors

CPU or ASIC Substrate Remote Diodes

A substrate diode is a parasitic PNP transistor that has its collector tied to ground through the substrate and the base (Remote -) and emitter (Remote +) brought out to pins. Connection to these pins is shown in Figure 13. The non-ideality figures in Table 31 include the effects of any package resistance and represent the value seen from the CPU socket. The temperature indicated will need to be compensated for the departure from a non-ideality of 1.008.

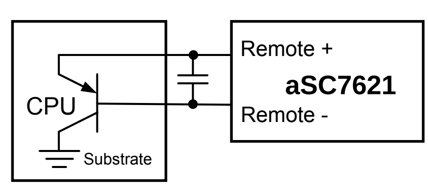

Figure 13 CPU Remote Diode Connection

Series Resistance

Any external series resistance in the connections from the aSC7621 to the CPU pins should be accounted for in interpreting the results of a measurement.

The impact of series resistance on the measured temperature is a result of measurement currents developing offset voltages that add to the diode voltage. This is relatively constant with temperature and may be corrected with a fixed value in the offset register. To determine the temperature impact of resistance is as follows:

$$\Delta T_R = R_S \times \Delta I_D / T_V$$

$$or,$$

$$\Delta T_R = R_S \times \frac{90\mu A}{230\mu V/°C} = R_S \times 0.391°C/\Omega$$

where:

ΔT_R = difference in the temperature reading from actual.

R_S = total series resistance of interconnect (both leads).

ΔI_D = difference in the two diode current levels (90µA).

T_V = scale of temperature vs. V_{BE} (230µV/°C).

For example, a total series resistance of 10Ω would give an offset of +3.9°C.

Discrete Remote Diodes

When sensing temperatures other than the CPU or GPU substrate, an NPN or PNP transistor may be used. Most commonly used are the 2N3904 and 2N3906. These have characteristics similar to the CPU substrate diode with non-ideality around 1.0046. They are connected with base to collector shorted as shown in Figure 14.

While it is important to minimize the distance to the remote diode to reduce high-frequency noise pickup, they may be located many feet away with proper shielding. Shielded, twisted-pair cable is recommended, with the shield connected only at the aSC7621 end as close as possible to the ground pin of the device.

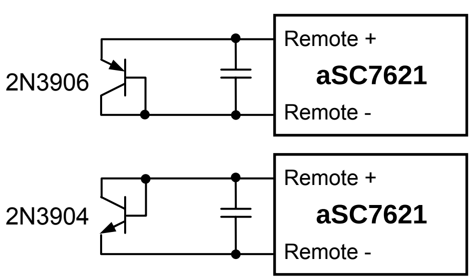

Figure 14 Discrete Remote Diode Connection

As with the CPU substrate diode, the temperature reported will be subject to the same errors due to non-ideality variation and series resistance. However, the transistor's die temperature is usually not the temperature of interest and care must be taken to minimize the thermal resistance and physical distance between that temperature and the remote diode. The offset and response time will need to be characterized by the user.

Board Layout Considerations

The distance between the remote sensor and the aSC7621 should be minimized. All wiring should be defended from high frequency noise sources and a balanced differential layout maintained on Remote + and Remote -.

Any noise, both common-mode and differential, induced in the remote diode interconnect may result in an offset in the temperature reported. Circuit board layout should follow the recommendation of Figure 15. Basically, use 10-mil lines and spaces with grounds on each side of the differential pair. Closer spacing may also be used if required by layout, but the priority is balance of diode path and minimum vias. Choose the ground plane closest to the CPU when using the CPU's remote diode.

Figure 15 Recommended Remote Diode Circuit Board Interconnect

Noise filtering is accomplished by using a bypass capacitor placed as close as possible to the two pairs of aSC7621 Remote + and Remote - pins. A 1.0nF ceramic capacitor is recommended, but up to 3.3nF may be used. Additional filtering takes place within the aSC7621.

It is recommended that the following guidelines be used to minimize noise and achieve highest accuracy:

1. Place a 0.1µF bypass capacitor to digital ground as close as possible to the power pin of the aSC7621.
2. Match the trace routing of the Remote + and Remote - leads and use a 1.0nF filter capacitor close to the aSC7621. Use ground runs along side the pair to minimize differential coupling as in Figure 15.
3. Place the aSC7621 as close to the CPU or GPU remote diode leads as possible to minimize noise and series resistance.
4. Avoid running diode connections close to or in parallel with high-speed busses or 12V, staying at least 2cm away.

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5. Avoid running diode connections close to on-board switching power supply inductors.
6. PC board leakage should be minimized by maintaining minimum trace spacing and covering traces over their full length with solder mask.

Thermal Considerations

The temperature of the aSC7621 will be close to that of the PC board on which it is mounted. Conduction through the leads is the primary path for heat flow. The reported local sensor is very close to the circuit board temperature and typically between the board and ambient.

In order to measure PC board temperature in an area of interest, such as the area around the CPU where voltage regulator components generate significant heat, a remote diode-connected transistor should be used. A surface-mount SOT-23 or SOT-223 is recommended. The small size is advantageous in minimizing response time because of its low thermal mass, but at the same time it has low surface area and a high thermal resistance to ambient air. A compromise must be achieved between minimizing thermal mass and increasing the surface area to lower the junction-to-ambient thermal resistance.

In order to sense temperature of air-flows near board-mounted heat sources, such as memory modules, the sensor should be mounted above the PC board. A TO-92 packaged transistor is recommended.

The power consumption of the aSC7621 is relatively low and should have little self-heating effect on the local sensor reading. At the highest measurement rate the dissipation is less than 2mW, resulting in only a few tenths of a degree rise.

Evaluation Board

The Andigilog SMBus EVB provides a platform for evaluation of the operational characteristics of the aSC7511, aSC7512 and aSC7621. The board features a graphical user interface (GUI) to control and monitor all activities and readings of these parts. The provided software will run on a Windows XP™-based desktop or laptop PC with a USB port.

In addition to being a self-contained fan speed control demonstration, it may be connected into an operating PC's fan and CPU diode to evaluate various settings under real operating conditions without the need to adjust BIOS code. After optimization, the settings may be programmed into the system.

Features:

- Interactive GUI for setting limits and operational configuration
- aSC7512 and aSC7621 Automatic Fan Control
- Powered and operated from the USB port
- Support for reading or writing to any register
- User-defined, time-stamped logging of any registers, saved in spreadsheet-compatible format
- Graphical readouts:
    - Temperature and alarms
    - Fan RPM
    - Automatic fan control state
    - Voltage
- Selectable on-board 2N3904 or wired remote diode
- Headers for 2-, 3- and 4-wire fans with PWM for aSC7512
- Headers for 3 4-wire fans for aSC7621
- Saving of register setting configurations
- LED indicators of pin alarm states
- Optional use of external 12V fan power for higher current fans
- Optional connection to off-board SMBus clients

Application Diagrams

The aSC7621 may be easily adapted to 2-, 3- or 4-wire fans for precise, wider-range fan speed control when compared to variable DC drive. Up to four fans may be controlled. Fans 1 and 2 are independent. Fan 3 is independent and may be tied to fan 4 for speed control. Separate tachometer readings may be reported for all four.

Application diagram in Figure 16 shows connections to four 4-wire fans. External FETs may be added to the PWM output to drive 3-wire fans.

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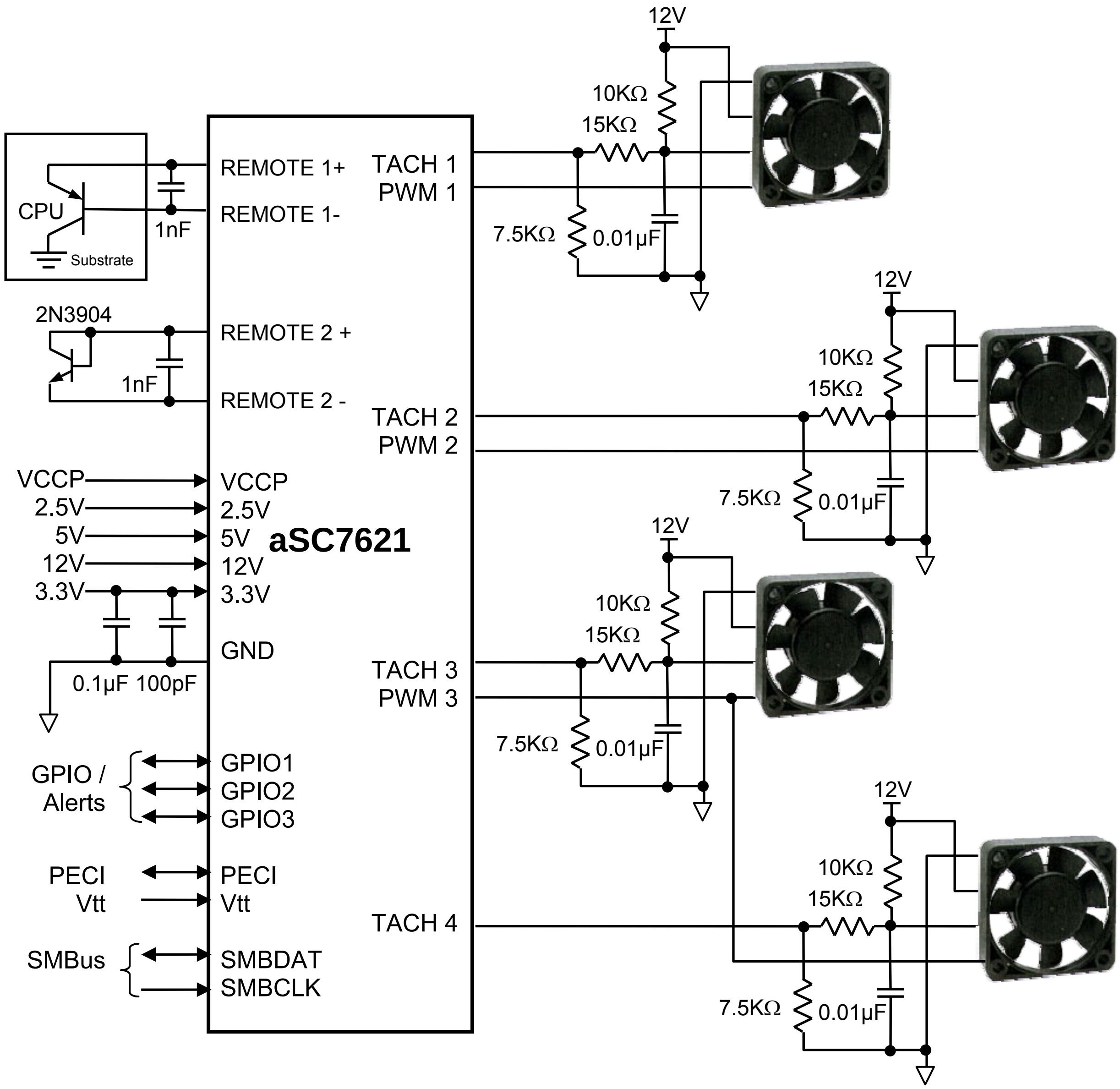

Figure 16 Application Diagram

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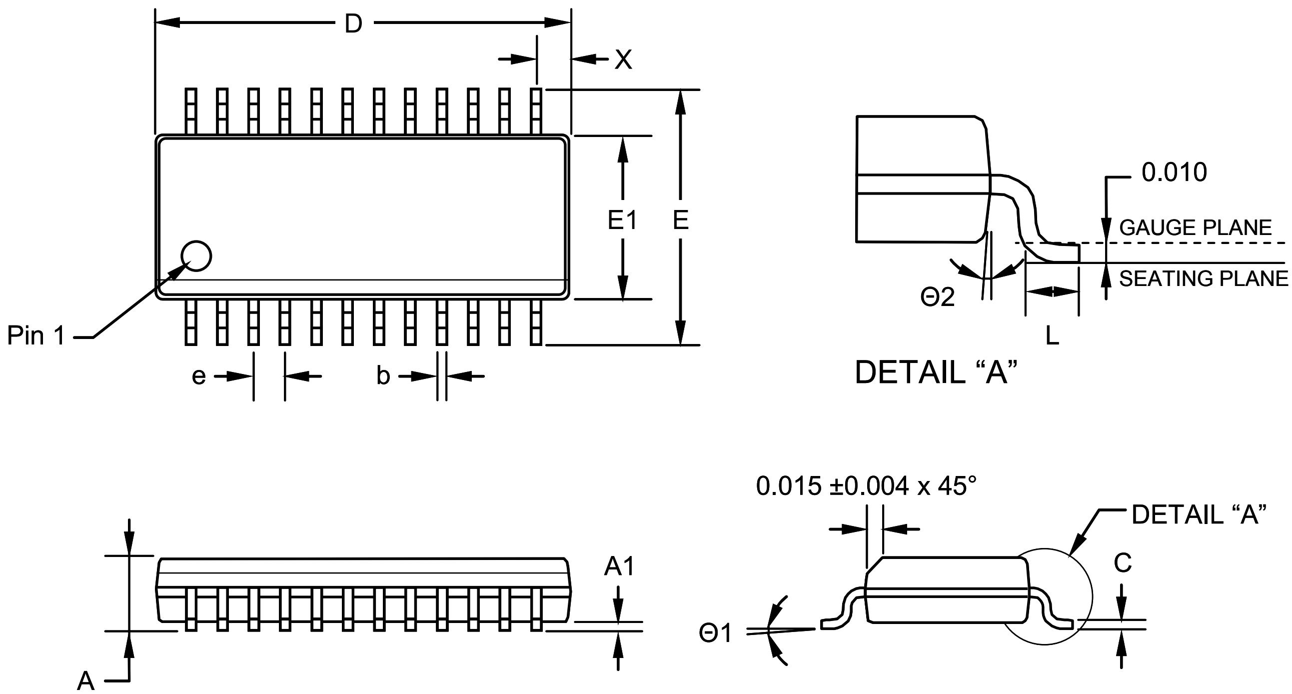
Physical Dimensions inches unless otherwise noted

24-Lead Molded QSOP Package



Notes:

1. Pb-Free
2. Co-planarity is 0 to 0.004" MAX
3. Package surface finish – Matte (VDI #24~27)
4. All dimensions exclude mold flash
5. The lead width, B, to be determined at 0.0075" from the lead tip

Symbol	MIN	MAX
A	0.054	0.068
A1	0.004	0.0098
B	0.008	0.012
D	0.337	0.344
E1	0.150	0.157
E	0.229	0.244
E	0.025 BSC	
C	0.0075	0.0098
L	0.016	0.034
X	0.0325 REF	
Θ1	0°	8°
Θ2	7° BSC	

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Data Sheet Classifications

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This classification is shown on the heading of each page of a specification for products that are either under development (design and qualification), or in the formative planning stages. Andigilog reserves the right to change or discontinue these products without notice.

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