

# MOS INTEGRATED CIRCUIT

# $\mu$ PD16304

## 40 bit VACUUM FLUORESCENT DISPLAY DRIVER

### CMOS LSI

#### DESCRIPTION

The  $\mu$ PD16304 is high voltage driver utilized high voltage CMOS process for Vacuum Fluorescent Display. The  $\mu$ PD16304 consists of a 40 bit shift register (20 bit shift register x 2), 40 bit latch, and high voltage CMOS drivers. All inputs are CMOS-compatible.

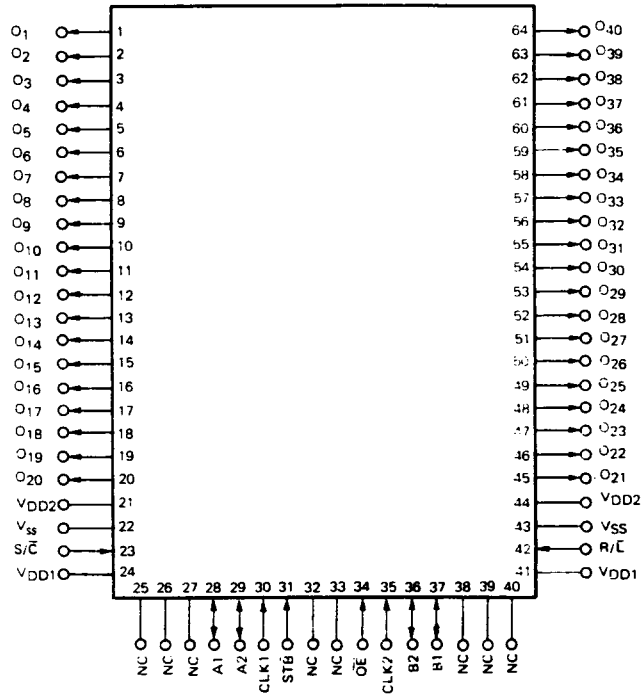
#### FEATURES

- 20 bit shift register by two construction
- Capable of selecting serial data or 2 bit parallel data input
- High voltage output capability 200 V
- High current output capability 20 mA
- Full CMOS construction both logic and driver
- Wide operating temperature range  $-40$  to  $+85^{\circ}\text{C}$
- 80 pin plastic QFP (3 Direction Lead)

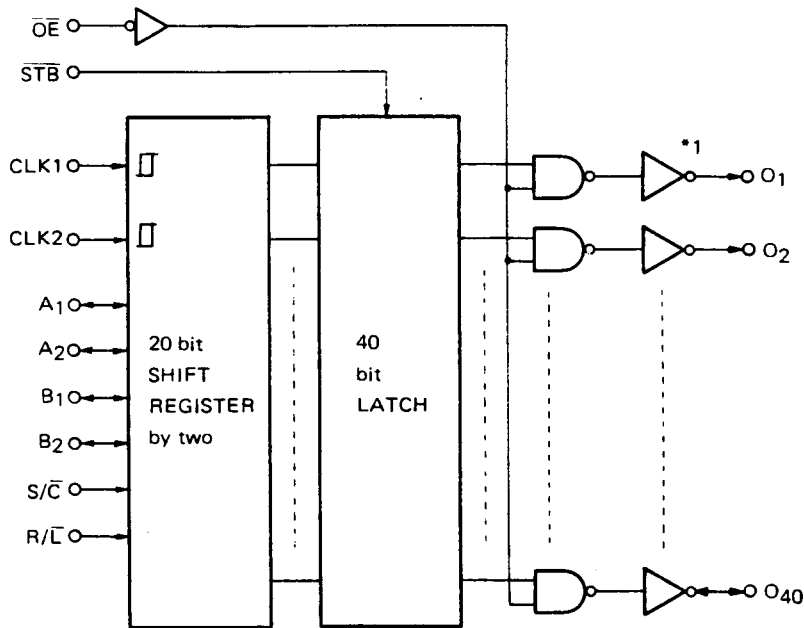
#### Ordering Information

ORDERING CODE	PACKAGE
$\mu$ PD16304GF-3L9	80 pin plastic QFP (3 Direction Lead)

# PIN CONFIGURATION (TOP VIEW)



# BLOCK DIAGRAM



\*1 HIGH VOLTAGE CMOS DRIVER

## PIN FUNCTION

SYMBOL	PIN NAME	PIN No.	FUNCTION
$\overline{OE}$	Output Enable Input	34	Data is output while this pin is low. All outputs are low while this pin is high.
$\overline{STB}$	Latch Strobe Input	31	New data enter the latches while this pin is low. These data are stored while this pin is high.
A <sub>1</sub>	Data Input/Output of right shift	28	When $S/\overline{C}$ is high, A <sub>1</sub> and B <sub>1</sub> are input/output terminal. A <sub>2</sub> and B <sub>2</sub> outputs low.
A <sub>2</sub>		29	
B <sub>1</sub>		37	
B <sub>2</sub>		36	
CLK1	Data Input/Output of left shift	30	Data is entered to the shift register on the low-to-high transition of clock input. When $S/\overline{C}$ is high, CLK1 is enable, CLK2 is irrelevant. When $S/\overline{C}$ is low, both CLK1 and CLK2 are enable.
CLK2		35	
$R/\overline{L}$	Data shift direction control Input	42	While this pin is high, data is shifted to the right, and A terminals are data input, B terminals are data output. While this pin is low, data is shifted to the left, and A terminals are data output, B terminals are data input.
$S/\overline{C}$	Data Input Selection control Input	23	While this pin is high, data input mode is serial. While this pin is low, data input mode is 2 bit parallel.
O <sub>1</sub> thru O <sub>40</sub>	High Voltage Output	1 thru 20 45 thru 64	Each output will be able to output 200 V, 20 mA.
V <sub>DD1</sub>	Power Supply for logic	24, 41	5 V ± 10 %
V <sub>DD2</sub>	Power Supply for driver	21, 44	30 V to 150 V
V <sub>SS</sub>	Ground	22, 23	
N.C.	No Connection	25, 26, 27, 32, 38, 39, 40	
I.C.	Internally connection	33	This pin should be open. Don't connect any pin.

**TRUTH TABLE 1 (SHIFT REGISTER)**

INPUTS				DATA I/O				SHIFT REGISTER	
S/C	R/L	CLK 1	CLK 2	A1	A2	B1	B2		
H	H	↑	X	SIN	L*1	SO	L*1	A <sub>1</sub> → O <sub>1</sub> → O <sub>2</sub> . . . . . → O <sub>39</sub> → O <sub>40</sub>	
		H or L	X					No Change	
		↓	X					Data of O <sub>40</sub> is output from B <sub>1</sub> (SO).	
	L	H or L	↑	X	SO	L*1	SIN	L*1	B <sub>1</sub> → O <sub>40</sub> → O <sub>39</sub> . . . . . → O <sub>2</sub> → O <sub>1</sub>
			H or L	X					No Change
			↓	X					Data of O <sub>1</sub> is output from A <sub>1</sub> (SO).
L	H	↑*2	↑*2	SIN 1	SIN 2	SO 1	SO 2	A <sub>1</sub> → O <sub>1</sub> → O <sub>3</sub> . . . . . → O <sub>37</sub> → O <sub>39</sub> CLK 1 : Odd bit Shift A <sub>2</sub> → O <sub>2</sub> → O <sub>4</sub> . . . . . → O <sub>38</sub> → O <sub>40</sub> CLK 2 : Even bit Shift	
		H or L	H or L					No Change	
		↓*2	↓*2					Data of O <sub>39</sub> is output from B <sub>1</sub> . Data of O <sub>40</sub> is output from B <sub>2</sub> .	
	L	H or L	↑*2	↑*2	SO 1	SO 2	SIN 1	SIN 2	B <sub>1</sub> → O <sub>39</sub> → O <sub>37</sub> . . . . . → O <sub>3</sub> → O <sub>1</sub> CLK 2 : Odd bit Shift B <sub>2</sub> → O <sub>40</sub> → O <sub>38</sub> . . . . . → O <sub>4</sub> → O <sub>2</sub> CLK 1 : Even bit Shift
			H or L	H or L					No Change
			↓*2	↓*2					Data of O <sub>1</sub> is output from A <sub>1</sub> . Data of O <sub>2</sub> is output from A <sub>2</sub> .

H: High level    L: Low level    X: H or L

SIN: Serial Input/SO: Serial Output

- \*1 A<sub>2</sub> and B<sub>2</sub> outputs are low because of fixing to low internally.  
These pin should be open or connected to ground externally.
- \*2 CLK 1 and CLK 2 operate independently.

**TRUTH TABLE 2 (Driver)**

OE	STB	FUNCTION (O <sub>1</sub> Thru O <sub>40</sub> )
L	L	Outputs data of shift register.
	H	Latches data of shift register before the transition of STB.
H	L	All outputs are low. But latch circuit operates with state of data through.
	H	All outputs are low. But latch circuit operates with state of data latch.

H: High level    L: Low level

### ABSOLUTE MAXIMUM RATINGS ( $T_a = 25\text{ }^\circ\text{C}$ , $V_{SS} = 0\text{ V}$ )

Supply Voltage (Logic)	$V_{DD1}$	-0.5 to +7.0	V
Input Voltage	$V_I$	-0.5 to $V_{DD1} + 0.5$	V
Output Voltage (Logic)	$V_{O1}$	-0.5 to $V_{DD1} + 0.5$	V
Output Voltage (Driver)	$V_{DD2}$	-0.5 to 200	V
Output Voltage (Driver)	$V_{O2}$	-0.5 to $V_{DD2} + 0.5$	V
Output Current (Driver)	$I_{O2}$	$\pm 20$	mA
Power Dissipation	$P_D$	1 000	mW
Operating Temperature	$T_{opt}$	-40 to +85	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-65 to +150	$^\circ\text{C}$

### RECOMMENDED OPERATING CONDITIONS

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage (Logic)	$V_{DD1}$	4.5	5	5.5	V
High Level Input Voltage	$V_{IH}$	$0.7 \cdot V_{DD1}$		$V_{DD1}$	V
Low Level Input Voltage	$V_{IL}$	0		$0.2 \cdot V_{DD1}$	V
Supply Voltage (Driver)	$V_{DD2}$	30		150	V
Driver Output Current	$I_{OH2(A)}$			-2.5	mA
	$I_{OH2(G)}$			-15	mA

$I_{OH2(A)}$  : Anode Drive Current

$I_{OH2(G)}$  : Grid Drive Current

**ELECTRICAL CHARACTERISTICS ( $T_a=25^\circ\text{C}$ ,  $V_{DD1}=4.5$  to  $5.5$  V,  $V_{DD2}=150$  V,  $V_{SS}=0$  V)**

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
High Level Output Voltage	$V_{OH1}$	Logic $I_{OH1}=-1$ mA	$0.9 \cdot V_{DD1}$			V
Low Level Output Voltage	$V_{OL1}$	Logic $I_{OL1}=1$ mA			$0.1 \cdot V_{DD1}$	V
High Level Output Voltage	$V_{OH21}$	$O_1$ thru $O_{40}$ , $I_{OH2}=-1$ mA	148	149.5		V
	$V_{OH22}$	$O_1$ thru $O_{40}$ , $I_{OH2}=-10$ mA	135	145		V
Low Level Output Voltage	$V_{OL21}$	$O_1$ thru $O_{40}$ , $I_{OL2}=1$ mA		1.2	3	V
	$V_{OL22}$	$O_1$ thru $O_{40}$ , $I_{OL2}=5$ mA		10	25	V
High Level Input Current	$I_{IH}$	$V_I=V_{DD1}$			1	$\mu\text{A}$
Low Level Input Current	$I_{IL}$	$V_I=0$ V			-1	$\mu\text{A}$
High Level Input Voltage	$V_{IH}$		$0.7 \cdot V_{DD1}$			V
Low Level Input Voltage	$V_{IL}$				$0.2 \cdot V_{DD1}$	V
Supply Current	$I_{DD1}$	Logic Power Supply $T_a=85^\circ\text{C}$			1.0	mA
	$I_{DD2}$	Driver Power Supply $T_a=85^\circ\text{C}$			1.0	mA

**SWITCHING CHARACTERISTICS**

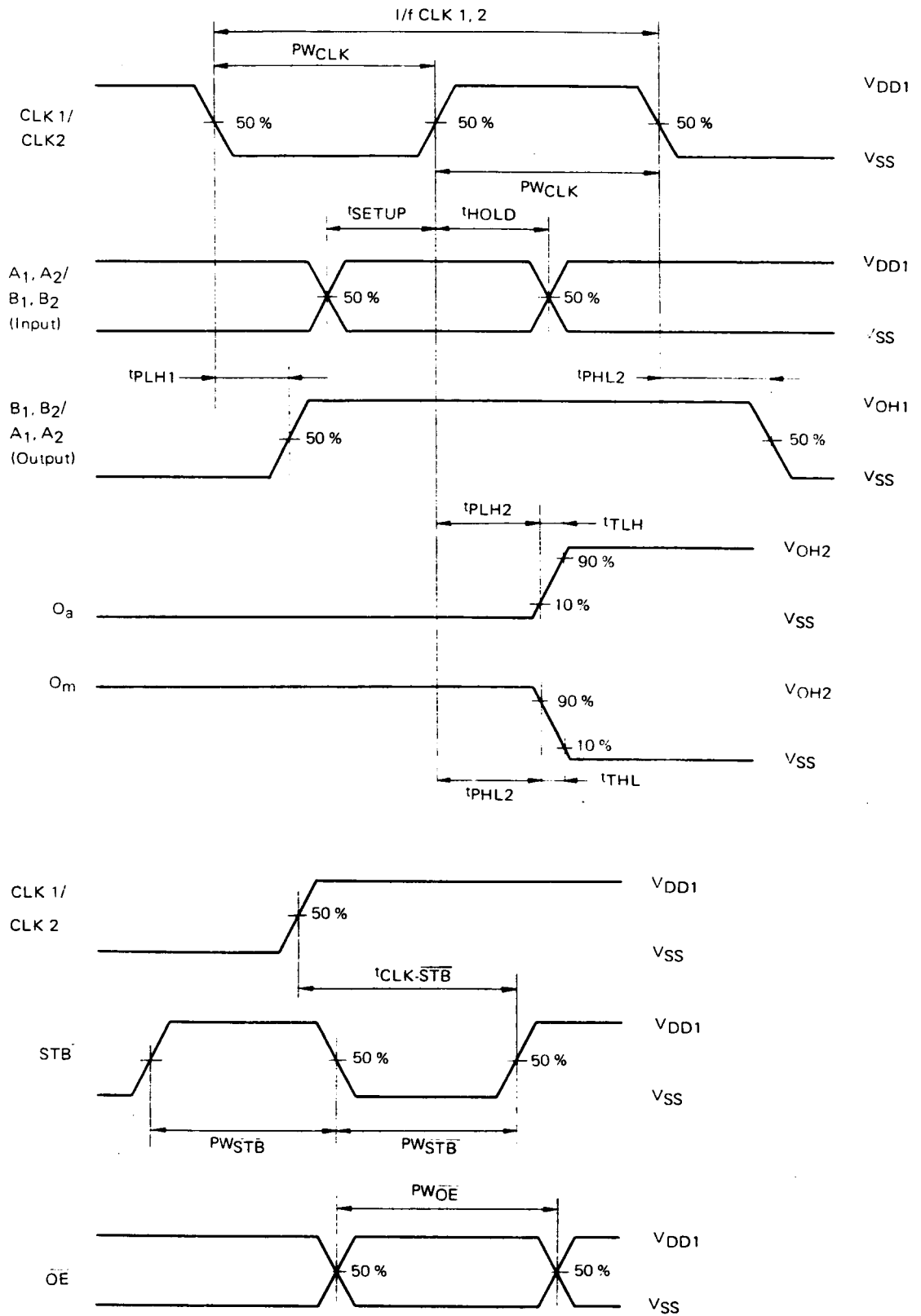
( $T_a=25^\circ\text{C}$ ,  $V_{DD1}=5$  V,  $V_{SS}=0$  V, Logic  $C_L=15$  pF, Driver  $C_L=30$  pF)

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time	$t_{PHL1}$	CLK1, 2— $A_1$ , $B_1$ or $A_2$ , $B_2$			100	ns
	$t_{PLH1}$				100	ns
	$t_{PHL2}$	CLK1, 2— $O_1$ thru $O_{40}$			650	ns
	$t_{PLH2}$				450	ns
Output Transient Time	$t_{THL}$	$O_1$ thru $O_{40}$			2.0	$\mu\text{s}$
	$t_{TLH}$	$O_1$ thru $O_{40}$			0.4	$\mu\text{s}$
Maximum Frequency	$f_{max.}$	Duty=50 %	6.25	12		MHz
Input Capacitance	$C_i$			10	15	pF

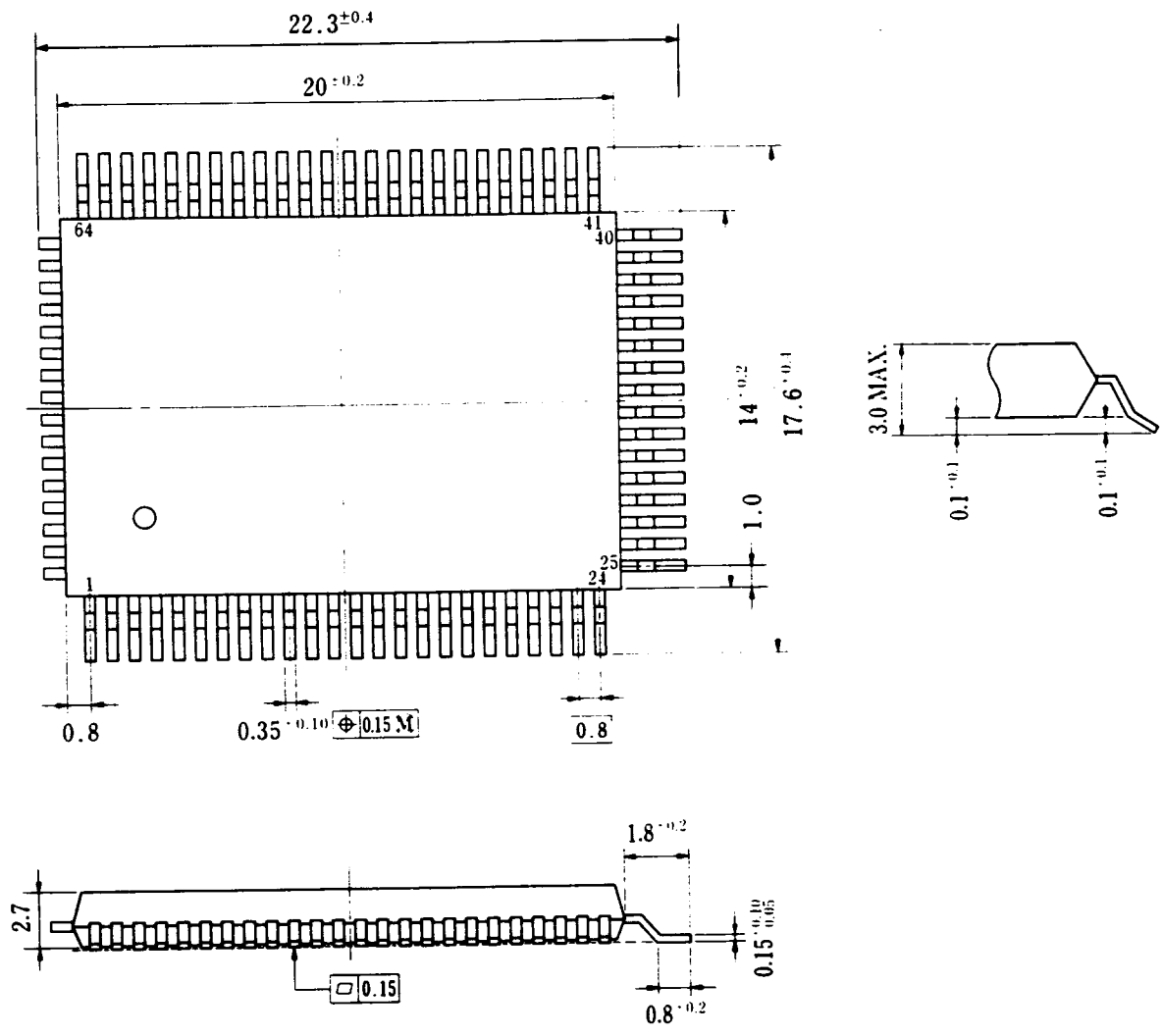
**TIMING REQUIREMENT ( $T_a=-40$  to  $+85^\circ\text{C}$ ,  $V_{DD1}=4.5$  to  $5.5$  V,  $V_{SS}=0$  V)**

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Clock Pulse Width	$PW_{CLK}$	80			ns	
Strobe Pulse Width	$PW_{STB}$	80			ns	
OE Pulse Width	$PW_{OE}$	4			$\mu\text{s}$	
Data Setup Time	$t_{SETUP}$	80			ns	
Data Hold Time	$t_{HOLD}$	80			ns	
Setup Time (CLK—STB)	$t_{CLK-STB}$	160			ns	

# SWITCHING WAVE CHART



80 PIN plastic QFP (3 Direction Lead) (Unit mm)



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