STE101P

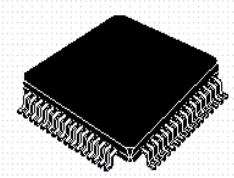
10/100 Fast ethernet 3.3 V transceiver

Features

- IEEE802.3u 100Base-TX and IEEE802.3 and 10Base-T transceiver
- Support for IEEE802.3x flow control
- MII /RMII / SMII interface
- Auto MDIX supported
- Provides Full-duplex operation on both 100Mbps and 10Mbps modes
- Provides MLT-3 transceiver with DC restoration for Base-line wander compensation
- Provides loop-back modes for diagnostics
- Supports external transformer with turn ratio 1.414:1 on Tx/Rx side.
- Five LED display for operating mode and functionality signalling
- Operation from single 3.3V supply
- High Cable ESD tolerance
- Standard 64-pin QFP package pinout
- Industrial temperature compliant
- Self termination transceiver for external components and power saving
- Power dissipation < 200mW

Applications

- Switches/routers/hubs
- NIC adapters
- Game consoles
- VoIP gateways/phones
- Network printers
- DTVs/DVD-Rs



TQFP64 10 x 10

Description

The STE101P is a high performance Fast Ethernet physical layer interface for 10Base-T and 100Base-TX application.

It was designed with advanced CMOS technology to provide MII, RMII and SMII interfaces for easy attachment to 10/100 Media Access Controllers 100Base-TX of IEEE802.3u and 10Base-T of IEEE802.3

The STE101P supports both half-duplex and full-duplex operation at 10 and 100 Mbps operation. Its operating mode can be set using auto negotiation, parallel detection or manual control. It also allows for the support of auto-negotiation functions for speed and duplex detection. The Automatic MDI / MDIX feature compensates for using a cross over cable. With Auto MDIX, the STE101P automatically detects what is on the other end of the network cable and switches the TX & RX pins accordingly.

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1 System and block diagrams

Figure 1. System diagram of the STE101P application

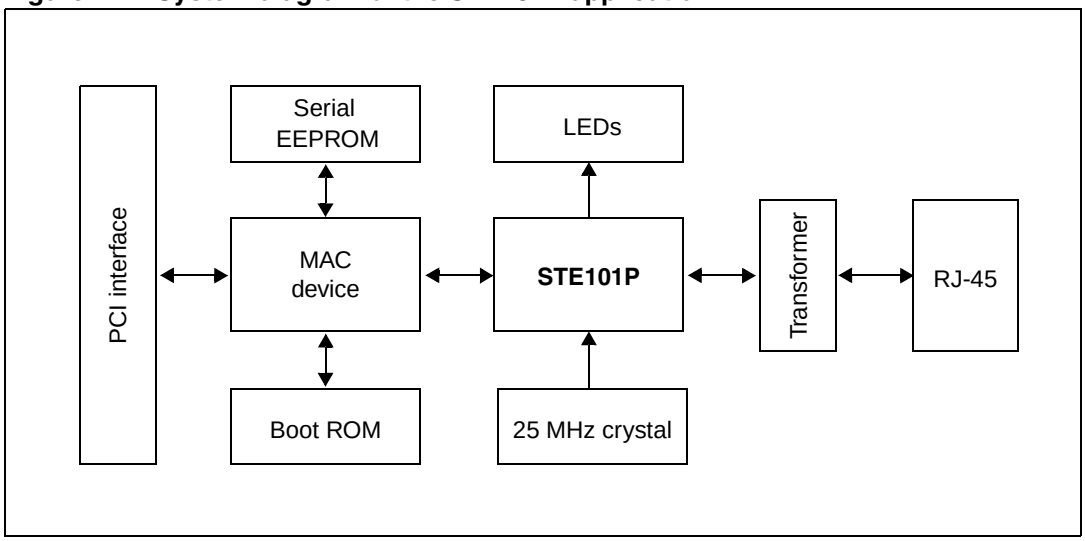
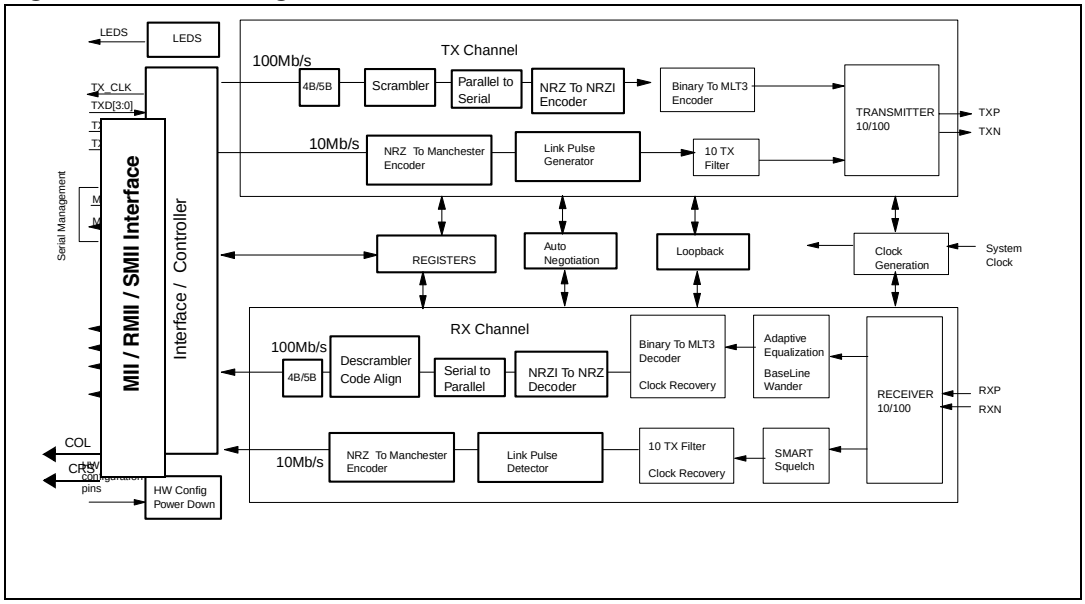


Figure 2. Block diagram



2 Features

2.1 Physical layer

- Integrates the whole physical layer functions of 100Base-TX and 10Base-T
- Provides full-duplex operation on both 100Mbps and 10Mbps modes
- Provides auto-negotiation (NWAY) function of full/half duplex operation for both 10 and 100 Mbps
- Provides MLT-3 transceiver with DC restoration for base-line wander compensation
- Provides transmit wave-shaper, receive filters, and adaptive equalizer
- Provides loop-back modes for diagnostic
- Builds in stream cipher scrambler/ de-scrambler and 4B/5B encoder/decoder
- Supports external transmit transformer with turn ratio 1.414:1
- Supports external receive transformer with turn ratio 1.414:1

2.2 LED display

The LED display, consists of five LEDs having the following characteristics:

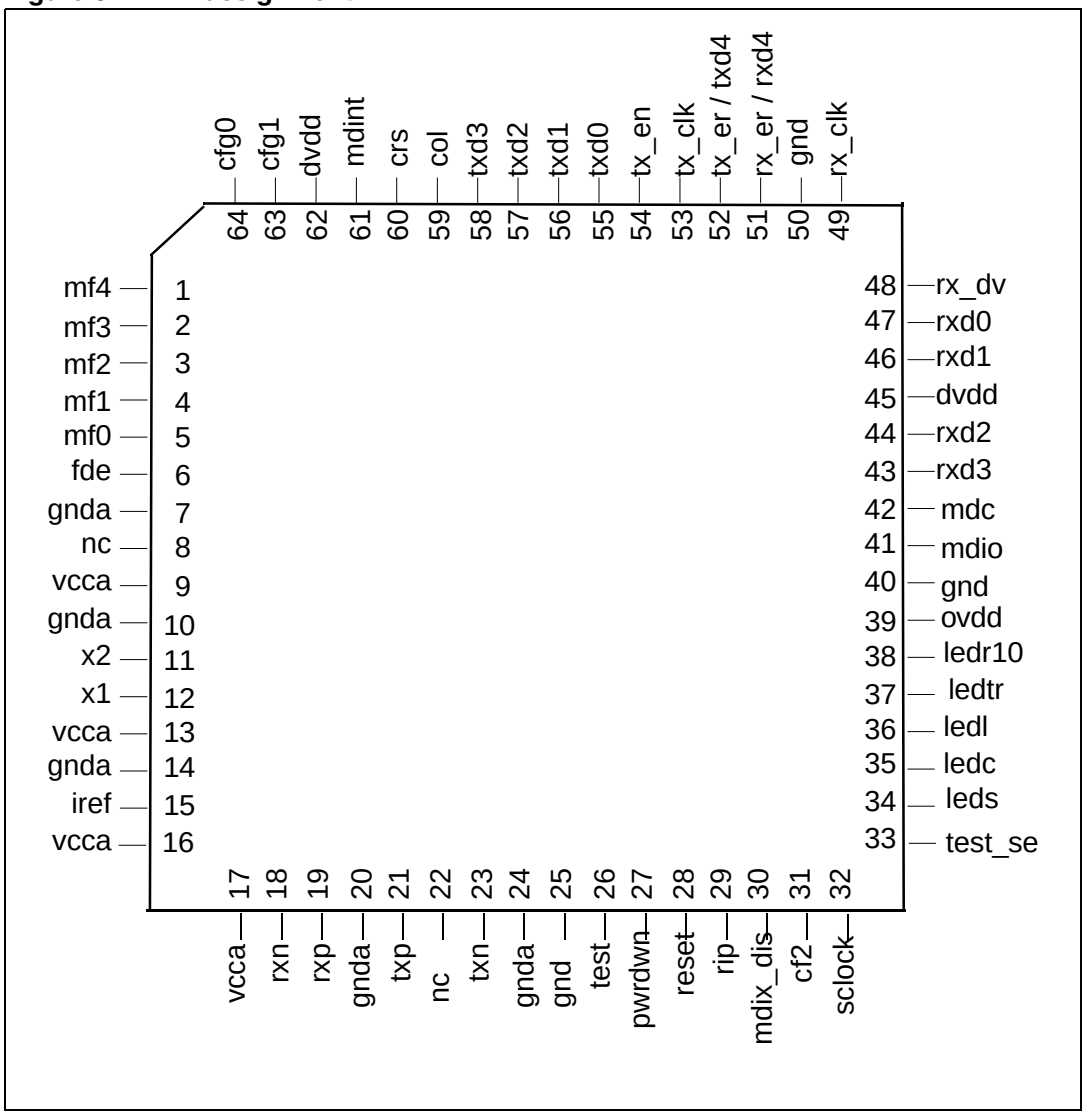
- 10 Mbps speed LED: 10Mbps(on) or 100Mbps(off)
- 100 Mbps speed LED: 100Mbps(on) or 10Mbps(off)
- TX/RX activity LED: Blinks at 10Hz when receiving, but not colliding
- Link LED: On when a good link is detected, blinks when there is TX or RX activity
- Full duplex / collision LED: ON during full duplex operation. Blinks at 20Hz to indicate a collision

2.3 Package

- Standard 64-pin QFP package pinout

3 Pin assignment

Figure 3. Pin assignment



4 Pin description

Table 1. Pin description

Pin No.	Name	Type	Description
Data interface			
52	tx_er	I	**Transmit Coding Error**. The MAC asserts this input when an error has occurred in the transmit data stream. When the STE101P is operating at 100 Mbps, the STE101P responds by sending invalid code symbols on the line. In Symbol (5B) Mode this pin functions as txd4.
52 58 57 56 55	txd4 txd3 txd2 txd1 txd0	I	**Transmit Data**. The Media Access Controller (MAC) drives data to the STE101P using these inputs. txd4 is monitored only in Symbol (5B) Mode. These signals must be synchronized to the tx_clk. *txd0 = MII/RMII/SMII tx data *txd1 = MII/RMII tx data *txd2/txd3 = MII tx data
54	tx_en	I	**MII Transmit Enable (or SMII =ssync)**. The MAC asserts this signal when it drives valid data on the txd inputs. This signal must be synchronized to the tx_clk.
53	tx_clk	I/O	**MII Transmit Clock**. Normally the STE101P drives tx_clk. 25 MHz for 100 Mbps operation. 2.5 MHz for 10 Mbps operation.
51	rx_er	O	**Receive Error**. The STE101P asserts this output when it receives invalid symbols from the network. This signal is synchronous to rx_clk. In Symbol (5B) Mode this pin functions as rxd4.
51 43 44 46 47	rxd4 rxd3 rxd2 rxd1 rxd0	O	**Receive Data**. The STE101P drives received data on these outputs, synchronous to rx_clk. rxd4 is driven only in Symbol (5B) Mode. *rxd0 = MII/RMII/SMII rx data *rxd1 = MII/RMII rx data *rxd2/rxd3 = MII rx data
48	rx_dv	O	**Receive Data Valid**. MII RXDV (or RMII = CRSDV). The STE101P asserts This signal when it drives valid data on rxd. This output is synchronous to rx_clk.
49	rx_clk	O	**MII Receive Clock**: This continuous clock provides reference for rxd, rx_dv, and rx_er signals. 25 MHz for 100 Mbps operation. 2.5 MHz for 10 Mbps operation.
59	col	O	**MII Collision Detection:** The STE101P asserts this output when detecting a collision. This output remains High for the duration of the collision. This signal is asynchronous and inactive during full-duplex operation.
60	crs	O	**MII Carrier Sense**: During half-duplex operation (PR0:8=0), the STE101P asserts this output when either transmit or receive medium is non idle. During full duplex operation (PR0:8=1), crs is asserted only when the receive medium is non-idle.

Table 1. Pin description (continued)

Pin No.	Name	Type	Description
MII control interface			
42	mdc	I	**Management Data Clock**. Clock for the mdio serial data channel. One MDC transition is also required to complete a device reset. Maximum frequency is 2.5 MHz.
41	mdio	I/O	**Management Data Input/Output**, Bi-directional serial data channel for PHY communication.
61	mdint	OD	**Management Data Interrupt.** When any bit in PR18 = 1, an active High output on this pin indicates status change in the corresponding bits in PR17. Interrupt is cleared by reading Register PR17
Physical (twisted pair) interface			
12	x1	I	25 MHz reference clock input. When an external 25 MHz crystal is used, this pin will be connected to one terminal of it. If an external 25 MHz clock source of oscillator is used, then this pin will be the input pin of it.
11	x2	O	25 MHz reference clock output. When an external 25MHz crystal is used, this pin will be connected to another terminal of if. If an external clock source is used, then this pin should be left open.
21 23	txp txn	O	The differential Transmit outputs of 100Base-TX or 10Base-T, these pins directly output to the transformer.
19 18	rxp rxn	I	The differential Receive inputs of 100Base-TX or 10Base-T, these pins directly input from the transformer.
15	iref	O	Reference resistor/DC regulator output. Reference Resistor connecting pin for reference current, directly connect a 5KΩ ± 1% resistor to Vss.
38	ledr10	I/O	LED display for 10Ms/s link status. This pin will be driven on continually when 10Mb/s network operating speed is detected. The pull-up/pull-down status of this pin is latched into the PR14 bit 7 during power up/reset.
37	ledtr		LED display for TX/RX Activity status. This pin will be driven on at a 10 Hz blinking frequency when either effective receiving or transmitting is detected. The status of this pin is latched into the PR14 bit 6 during power up/reset.
36	ledl	I/O	LED display for Link Status. This pin will be driven on continually when a good Link test is detected, and Blink during TX or RX activity if PR1B bit 9 = 0. The status of this pin is latched into the PR14 bit 5 during power up/reset.
35	ledc	I/O	LED display for Full Duplex or Collision status. This pin will be driven on continually when a full duplex configuration is detected. This pin will be driven on at a 20 Hz blinking frequency when a collision status is detected in the half duplex configuration. The status of this pin is latched into the PR14 bit 4 during power up/reset.
34	leds	I/O	LED display for 100Ms/s link status. This pin will be driven on continually when 100Mb/s network operating speed is detected. The status of this pin is latched into the PR14 bit 3 during power up/reset.

Table 1. Pin description (continued)

<table>
<tr><th>Pin No.</th><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>64</td><td>cfg0</td><td>I</td><td>Configuration Control 0.
When A/N is enabled, cfg0 determines operating mode advertisement capabilities in combination with cfg1 when mf0/ PR00:12 =1. (See Table 2)
When A/N is disabled, cfg1 disables mlt3 and directly affects PR13:0
When cfg0 is Low, mlt3 encoder/decoder is enabled and PR13:1 =0.
When cfg0 is High, mlt3 encoder/decoder is bypassed and PR13:1 = 1.</td></tr>
<tr><td>63</td><td>cfg1</td><td>I</td><td>Configuration Control 1.
When A/N is enabled, cfg1 determines operating mode advertisement capabilities in combination with cfg1 when mf0/ PR00:12 =1. (See Table 2)
When A/N is disabled, CFG1 enables Loopback mode and directly affects PR00 bit 14.
When cfg1 is Low, Loopback mode is disabled and PR00:14 = 0.
When cfg1 is High, Loopback mode is enabled and PR00:14 = 1.</td></tr>
<tr><td>28</td><td>reset</td><td>I</td><td>Reset (Active-Low). This input must be held low for a minimum of 1 ms to reset the STE101P. During Power-up, the STE101P will be reset regardless of the state of this pin. Reset will not be complete until >1ms plus an MDC transition.</td></tr>
<tr><td>29</td><td>rip</td><td>O</td><td>Reset In Progress. This output is used to indicate when the device has completed power-up/reset and the registers and functions can be accessed.
When rip is High, power-up/reset has been successful and the device can be used normally
When rip is Low, device reset is not complete.</td></tr>
<tr><td>30</td><td>mdix_dis</td><td></td><td>Auto MDI/MDIX disable</td></tr>
<tr><td>31</td><td>cf2</td><td></td><td>NC for MII operation. Should be tied high for RMII/SMII operation. See Table 2.</td></tr>
<tr><td>32</td><td>sclk</td><td></td><td>NC for MII operation. System clock for RMII (50MHz) and SMII (125MHz)</td></tr>
<tr><td>26, 33</td><td>test,
test_se</td><td></td><td>Test pins. Should be tied to ground for normal operation</td></tr>
<tr><td>27</td><td>pwrdwn</td><td>I</td><td>Power Down. When High, forces STE101P into Power Down mode. This pin is OR’ed with the Power Down bit (PR00:11). During the Power Down mode, txp/txn outputs and all LED outputs are 3-stated, and the MII interface is isolated.</td></tr>
<tr><td>5
4
3
2
1</td><td>mf0
mf1
mf2
mf3
mf4</td><td>I</td><td>Multi-function pins. Each mf pin internally drives different configuration functions. The functions of the five mf inputs are as shown in the table below.
<table>
<tr><th>Pin</th><th>Function</th><th>Reg. & Bit affected</th></tr>
<tr><td>mfo</td><td>Auto negotiation</td><td>PR00:12</td></tr>
<tr><td>mf1</td><td>Enable NRZ, NRZI conversion</td><td>PR13:7</td></tr>
<tr><td>mf2</td><td>4B/5B coding enable</td><td>PR13:6</td></tr>
<tr><td>mf3</td><td>Scrambler operation disable</td><td>PR13:0</td></tr>
<tr><td>mf4</td><td>10/100Mbps speed select</td><td>PR00:13</td></tr>
</table>
The logic level of mf0-4 will determine the value that the affected bits will have upon reset of the STE101P. The operating functions of cfg0, cfg1, and fde change depending on the state of mf0 (Auto-Negotiation enabled or disabled). Table shows the relationship between cfg0, cfg1 and fde.</td></tr>
</table>

Table 1. Pin description (continued)

Pin No.	Name	Type	Description
6	fde	I	**Full-duplex enable**. **When A/N is enabled**, fde determines full-duplex advertisement capability in combination with cfg0 and cfg1. (See Table 2) **When A/N is disabled**, fde directly affects full-duplex operation and determines the value of PR00 bit 8 (Full/Half Duplex Mode Select). When fde is High, full-duplex is enabled and PR00:8 = 1. When fde is Low, full-duplex is disabled and PR00:8 = 0.
8, 22	nc		nc (No Connection) - Should be left floating or pulled low for normal operation.
Digital power pins			
39	ovdd	I	IO ring power supply (3.3V)
45, 62	dvdd	I	Digital power (3.3V)
25, 40, 50	gnd	I	Ground
Analog power pins			
9, 13, 16, 17			vcca
7, 10, 14, 20, 24			gnda

5 Hardware control interface

5.1 Operating configurations

The hardware control interface consists of the MF0, CFG <2:0> and FDE input pins. This interface is used to configure operating characteristics of the STE101P. The hardware control interface provides initial values for the MDIO registers, and then passes control to the MDIO Interface. Table 2 shows how to set up the desired operating configurations using the hardware control interface.

Table 2. CFG decode

Function	MF0	FDE	CFG0	CFG1	CF2	Reg:Bit
MII mode / MLT3 enabled	0	x	0	x	0	PR13:1
MII mode / MLT3 disabled	0	x	1	x	0	PR13:1
MII mode/ local loopback disabled	0	x	x	0	0	PR00:14
MII mode/ local loopback enabled	0	x	x	1	0	PR00:14
MII mode / advertise 10HD	1	0	0	1	0	PR04:8,7,6,5
MII mode / advertise 10HD /FD	1	1	0	1	0	PR04:8,7,6,5
MII mode / advertise 100HD	1	0	1	0	0	PR04:8,7,6,5
MII mode / advertise 100HD / FD	1	1	1	0	0	PR04:8,7,6,5
MII mode / advertise 10/100 HD	1	0	1	1	0	PR04:8,7,6,5
MII mode / advertise all	1	1	1	1	0	PR04:8,7,6,5
SMII mode	x	x	0	0	1	RS1C:12
RMII mode	x	x	0	1	1	RS1C:11

Note: When MF0 = 0, PR04 is configured to advertise all (i.e 8:5 = 4'b1111).
When MF0=1, MLT3 is enabled and Loopback is disabled by default

5.2 LED / PHY address interface

The LED output pins can be used to drive LED's directly, or can be used to provide status information to a network management device. The active state of each LED output driver is dependent on the logic level sampled by the corresponding PHY address input upon power-up/reset. For example, if a given PAD input is resistively pulled low then the corresponding LED output will be configured as an active high driver. Conversely, if a given PAD input is resistively pulled high then the corresponding LED output will be configured as an active low driver. These outputs are standard CMOS drivers and not open-drain.

The STE101P PAD[4:0] inputs provide up to 32 unique PHY address options. An address selection of all zeros (00000) will result in a PHY isolation condition as a result of power-on/reset, as documented for Register PR00 bit 10. (See Section 7 for more detailed descriptions of device operation.)

6 Registers and descriptors description

All of the *management data control* and *status* registers in the STE101P's register set are accessed via a Write or Read operation on the serial MDIO Port. This access requires a protocol described in the MII management Interface section.

6.1 Register list

Table 3. List of registers

Address	Reg. Index	Name	Def.(1)	Register description
00h - 0d	PR00	CNTRL	0x0000	MII control register (*Table 4*)
01h - 1d	PR01	STATS	0x7809	MII status register (*Table 5*)
02h - 2d	PR02	PHYID	0x0006	PHY identifier (HI) register (*Table 6*)
03h - 3d	PR03	PHYID	0x1c52	PHY identifier (LO) register (*Table 7*)
04h - 4d	PR04	LDADV	0x01e1	Auto negotiation advertisement register (*Table 8*)
05h - 5d	PR05	LPADV	0x0000	Auto negotiation link partner ability register (*Table 9*)
06h - 6d	PR06	ANEGX	0x0004	Auto negotiation expansion register (*Table 10*)
07h - 7d	PR07	LDNPG	0x2001	Auto negotiation next page transmit register (*Table 11*)
08h - 8d	PR08	LPNPG	0x0000	Auto negotiation link partner next page transmit register (*Table 12*)
10h - 16d	PR10	XCNTL	0x0000	100BaseTX auxiliary control register (*Table 13*)
11h - 17d	PR11	XCIIS	0x0000	Configuration information interrupt & status register (*Table 14*)
12h - 18d	PR12	XIE	0x0000	Interrupt enable register (*Table 15*)
13h - 19d	PR13	100CTR	0x01c0	100BaseTX control register (*Table 16*)
14h - 20d	PR14	XMC	0x0002	Mode control register (*Table 17*)
18h - 24d	PR18	AUXCS	0x0030	Auxiliary control/status register (*Table 18*)
19h - 25d	PR19	AUXSS	0x0000	Auxiliary status summary register (*Table 19*)
1ah - 26d	PR1A	INRPT	0x1f00	Interrupt register (*Table 20*)
1bh - 27d	PR1B	AUXM2	0x000a	Auxiliary mode 2 register (*Table 21*)
1ch - 28d	PR1C	TSTAT	0x0820	Auxiliary error and general status register (*Table 22*)
1dh - 29d	PR1D	AUXMD	0x0000	Auxiliary mode register (*Table 23*)
1eh - 30d	PR1E	AMPHY	0x0000	Auxiliary PHY register (*Table 24*)
1fh - 31d	PR1F	BTEST	0x000b	Shadow register enable (*Table 25*)
18h - 24d	RS18	XDCNT	0x0000	100BaseTX disconnect counter register (*Table 26*)
1bh - 27d	RS1B	MISC	0x0000	Misc/status/test/error register (*Table 27*)
1ch - 28d	RS1C	AUX S3	0x0000	FIFO status (*Table 28*)

Table 3. List of registers (continued)

Address	Reg. Index	Name	Def.(1)	Register description
1dh - 29d	RS1D	AUX M3	0x0004	FIFO control (*Table 29*)
1eh - 30d	RS1E	AUX S4	0x0000	Packet/IPG length counter (*Table 30*)

1. Default value

6.2 Register description

Table 4. PR00 [0d00, 0x00]: MII control register

Bit #	Name	Description	Reset value	RW type	Type
15	Soft reset	1 = Requires approx. 1 micro second to complete soft reset sequence	0	R/W	SC
14	Local loop back	1 = Local Loop-back passes data from TX-> RX serial conversion analog logic	0	R/W	-
13	Force 100	1= Forced 100Mb speed selection. Ignored if Auto Negotiation is enabled	P	R/W	-
12	Auto negotiation enable	1 = Software Auto Negotiation enable. Ignored if hardware pin strap enables Auto Negotiation	P	R/W	-
11	Power down	1= Channel is powered down. If this bit is set for all channels then the IO pad directions are forced and the device is in power down state.	0	R/W	-
10	Isolate	1= Isolation mode. Related Pad outputs are forced to tri-state, inputs are ignored.	0	R/W	-
9	Restart auto negotiation	1= Restart Auto Negotiation. Auto Negotiation must be enabled for any effect.	0	R/W	SC
8	Full duplex	1= Full Duplex. Only applies if auto negotiation is disabled	P	R/W	-
7	Collision test	1= Collision test	0	R/W	-
6~0	---	Reserved	0	R/W	-
SC = Self clear (Clear following action), P=Pinstrap (Read at reset), R/W = Read/Write able					

Soft reset: In order to reset the STE101P by software control, a “1” must be written to the bit 15 of the Control Register using an MII write operation. The bit clears itself after the reset process is complete, and does not need to be cleared using a second MII write. Writes to other Control Register bits will have no effect until the reset process is completed, which requires approximately 1 microsecond. Writing a “0” to this bit has no effect. Since this bit is self-clearing, after a few cycles from a write operation, it will return a “0” when read.

Local loopback: The STE101P may be placed into loop back mode by writing a “1” to bit 14 of the Control Register. The loop back mode may be cleared by writing a “0” to bit 14 of the Control Register, or by resetting the chip. When this bit is read, it will return a “1” when the chip is in software-controlled loop back mode, otherwise it will return a “0”.

Force 100: If Auto Negotiation is enabled, this bit has no effect on the speed selection. However, if Auto Negotiation is disabled by software control, the operating speed of the STE101P can be forced by writing the appropriate value to bit 13 of the Control Register. Writing a “1” to this bit forces 100BASETX operation, while writing a “0” forces 10BASE-T operation. When this bit is read, it returns the value of the software-controlled forced speed selection only. In order to read the overall state of forced speed selection, including both hardware and software control, use bit 8 of the Auxiliary Control Register.

Auto negotiation enable: Auto negotiation can be disabled by one of two methods: hardware or software control. If the ANEN input pin is driven to a logic “0”, auto negotiation is disabled by hardware control. If bit 12 of the Control Register is written with a value of “0”, auto negotiation is disabled by software control. When auto negotiation is disabled in this manner, writing a “1” to the same bit of the Control Register or resetting the chip will re-enable Auto Negotiation. Writing to this bit has no effect when Auto Negotiation has been disabled by hardware control. When read, this bit will return the value most recently written to this location, or “1” if it has not been written since the last chip reset.

Power down: 1 = Channel is powered down. If this bit is set for all channels, then the IO pad directions are forced and the device is in power down state.

Isolate: The PHY may be isolated from its Media Independent Interface by writing a “1” to bit 10 of the Control Register. All MII outputs will be tri-stated, except tx_clk, and all MII inputs will be ignored. Since the MII management interface is still active, the isolate mode may be cleared by writing a “0” to bit 10 of the Control Register, or by resetting the chip. When this bit is read, it will return a “1” when the chip is in isolate mode, otherwise it will return a “0”.

Restart auto negotiation: Bit 9 of the Control Register is a self-clearing bit that allows the Auto Negotiation process to be restarted, regardless of the current status of the Auto Negotiation state machine. In order for this bit to have an effect, Auto Negotiation must be enabled. Writing a “1” to this bit restarts the Auto Negotiation, while writing a “0” to this bit has no effect. Since the bit is self-clearing after only a few cycles, it always returns a “0” when read. The operation of this bit is identical to bit 9 of the Auxiliary PHY Register.

Full duplex: By default, the STE101P powers up in half-duplex mode. The chip can be forced into full-duplex mode by writing a “1” to bit 8 of the Control Register while Auto Negotiation is disabled. Half-duplex mode can be resumed by writing a “0” to bit 8 of the Control Register, or by resetting the chip.

Collision test: The COL pin may be tested during loop back by activating the collision test mode. While in this mode, asserting TXEN will cause the COL output to go high within 512 bit times. Deasserting TXEN will cause the COL output to go low within 4 bit times. Writing a “1“to bit 7 of the Control Register enables the collision test mode. Writing a “0” to this bit or resetting the chip disables the Collision Test mode. When this bit is read, it will return a “1”

when the *collision test* mode has been enabled, otherwise it will return a “0”. This bit should only be set while in loop back test mode.

Reserved bits: All reserved MII register bits must be written as “0” at all times. Ignore the STE101P output when these bits are read.

Table 5. PR01 [0d01, 0x01]: MII status register

Bit #	Name	Description	Reset value	RW type	Type
15	100Base T4 ability	Tied to 0. Not supported	0	RO	
14	100BaseTX FDX ability	Tied to 1. Device is always 100BaseTX and Full Duplex capable	1	RO	
13	100BaseTX ability	Tied to 1. Device is always 100BaseTX Half Duplex capable.	1	RO	
12	10BaseT FDX ability	Tied to 1. Device is always 10BaseT and Full Duplex capable	1	RO	
11	10BaseT ability	Tied to 1. Device is always 10BaseT Half Duplex capable	1	RO	
10~7	Reserved	---	0	RO	
6	Preamble suppression	1= MII management frames can be accepted without the standard preamble	0	R/W	
5	Auto Negotiation complete	1 = Auto Negotiation Completed and registers 4,5,6 are now valid	0	RO	
4	Remote fault	1= Link Partner has signalled a far end fault condition	0	RO	LH
3	Auto negotiation ability	Tied to 1. Device is always capable of Auto Negotiation	1	RO	
2	Link status	1=Link pass state established. 0=Link fail state “latched” after link pass state	0	RO	LL
1	Jabber detect	1= Jabber condition detected. Transmission exceeded max number of bytes.	0	RO	LH
0	Extended register ability	Tied to 1. Device always supports the extended register set.	1	RO	

100Base T4 ability: The STE101P is not capable of T4 operation, and will return a “0” when bit 15 of the s*tatus* register is read.

100BaseTX FDX ability The STE101P is capable of 100BaseTX full-duplex operation, and will return a “1” when bit 14 of the *status* register is read.

100BaseTX ability: The STE101P is capable of 100BaseTX half-duplex operation, and will return a “1” when bit 13 of the *status* register is read.

10BaseT FDX ability: The STE101P is capable of 10BASE T full-duplex operation, and will return a “1” when bit 12 of the *status* register is read.

10BaseT ability: The STE101P is capable of 10BASE T half-duplex operation, and will return a “1” when bit 11 of the *status* register is read.

Reserved bits: Ignore STE101P output when these bits are read.

Preamble suppression: This bit is the only writable bit in the *status* register. Writing this bit to a “1” allows subsequent MII management frames to be accepted with or without the standard preamble pattern. When preamble suppression is enabled, only 2 preamble bits are required between successive Management Commands, instead of the normal 32.

Auto negotiation complete: Bit 5 of the *status* register will return a “1” if the auto negotiation process has been completed, and the contents of registers 4, 5, and 6 are valid.

Auto Negotiation ability: The STE101P is capable of performing IEEE Auto Negotiation, and will return a “1” when bit 4 of the *status* register is read, regardless of whether or not the Auto Negotiation function has been disabled

Link status: The STE101P will return a “1” on bit 2 of the *status* register when the link state machine is in link pass, indicating that a valid link has been established. Otherwise, it will return a “0”. When a link failure occurs after the *link pass* state has been entered, the *link status* bit will be latched at “0” and will remain so until the bit is read. After the bit is read, it becomes “1” if the *link pass* state has been entered again.

Jabber detect: 10BASE-T operation only. The STE101P will return a “1” on bit 1 of the s*tatus* register if a jabber condition has been detected. After the bit is read, of if the chip is reset, it reverts to “0”.

Extended register ability The STE101P supports extended capability registers, and will return a “1” when bit 0 of the Status Register is read. Several extended registers have been implemented in the STE101P, and their bit functions are defined later in this section.

Table 6. PR02 [0d02, 0x02]: PHY Identifier (HI) register

Bit #	Name	Description	Default value	RW type
15~0	PHYID1	Part one of PHY Identifier. Assigned to the 3rd to 18th bits of the Organizationality Unique Identifier (OUI). 5the ST OUI is 0080E1 hex)	0006h	R

Table 7. PR03 [0d03, 0x03]: PHY Identifier (LO) register

Bit #	Name	Description	Default value	RW type
15-10	PHYID2	Part two of PHY Identifier. Assigned to the 19th to 24th bits of the Organizationality Unique Identifier (OUI). 5the ST OUI is 0080E1 hex)	000111b	R
9-4	MODEL	Model number of STE101P. Six-bit manufacture’s model number	000101b	R
3-0		Revision number of STE101P. Four-bit manufacture’s revision number	0010b	R

The STE101P Revision A for this register has a value of 0x1c51

The STE101P Revision B for this register has a value of 0x1c52.

This allows identification of the revision of the device via software reading of this register.

Table 8. PR04 [0d04, 0x04]: Auto negotiation advertisement register

Bit #	Name	Description	Reset value	RW type	Type
15	Nxt page	1= Supports next page function	0	R/W	-
14	Reserved	---	0		-
13	Remote fault	Remote fault indicator to be sent to the link partner during auto negotiation	0	R/W	-
12,11	Reserved	---	0		-
10	Pause	1 = Supports PAUSE operation of flow control for full duplex link	1	R/W	-
9	100Base T4 advertise	Advertise T4. Not supported	0	R/W	-
8	100BaseTX FDX advertise	Advertise 100MB Full duplex	1	R/W	-
7	100BaseTX advertise	Advertise 100MB	1	R/W	-
6	10BaseT FDX advertise	Advertise 10MB Full duplex	1	R/W	-
5	10BaseT advertise	Advertise 10MB	1	R/W	-
4~0	Advertised selector field[4:0]	Advertise 802.3 class of PHY transceivers.	00001 [4:0]	R/W	-

Nxt Page: The STE101P supports next page capability.

Reserved: Ignore output when read

Remote fault: Writing a “1” to bit 13 of the Advertisement register causes a Remote Fault indicator to be sent to the Link Partner during Auto Negotiation. Writing a “0” to this bit or resetting the chip clears the Remote Fault transmission bit. This bit returns the value last written to it, or else “0” if no write has been completed since the last chip reset.

Pause: The use of this bit is independent of the negotiated data rate, medium, or link technology. The setting of this bit indicates the availability of additional DTE capability when full-duplex operation is in use. This bit is used by one MAC to communicate Pause Capability to its Link Partner, and has no effect on PHY operation.

Advertisement bits: Bits 9:5 of the Advertisement register allow the user to customize the ability information transmitted to the Link Partner. The default value for each bit reflects the abilities of the STE101P. By writing a “1” to any of the bits, the corresponding ability will be transmitted to the Link Partner. Writing a “0” to any bit causes the corresponding ability to be suppressed from transmission. Resetting the chip restores the default bit values. Reading the register returns the values last written to the corresponding bits, or else the default values if no write has been completed since the last chip reset. Even though that bit 9, Advertise 100BASE-T4 is writable, it should never be set since the STE101P is incapable of the T4 operation.

Advertised selector: Bits 4:0 of the Advertisement register contain the fixed value “00001”, indicating that the chip belongs to the 802.3 class of PHY transceivers.

Table 9. PR05 [0d05, 0x05]: Auto negotiation link partner ability register

Bit #	Name	Description	Reset value	RW type	Type
15	LP nxt page	1= Link Partner supports next Page function	0	RO	-
14	LP ack	1= Successful Reception of Link Partner’s link control word	0	RO	-
13	LP remote fault	1 = Link Partner is signalling a remote fault	0	RO	-
12,11	Reserved	----	0	RO	-
10	LP pause	Used by MAC in full duplex to allow additional DTE ability	0	RO	-
9	LP 100Base T4	Link Partner 100Base T4 ability	0	RO	-
8	LP 100BaseTX FDX	Link Partner 100MB Full duplex ability	0	RO	-
7	LP 100BaseTX	Link Partner 100MB ability	0	RO	-
6	LP 10BaseT FDX	Link Partner 10MB Full duplex ability	0	RO	-
5	LP 10BaseT	Link Partner 10MB ability	0	RO	-
4~0	LP selector field[4:0]	Link partner class of PHY transceivers	0	RO	-

LP nxt page: Bit 15 of the *link partner ability* register returns a value of “1” when the Link Partner implements the Next Page function and has Next Page information that it wants to transmit.

LP ack: Bit 14 of the *link partner ability* register is used by Auto Negotiation to indicate that a device has successfully received its Link Partner’s Link Code Word.

LP remote fault: Bit 13 of the *link partner ability* register returns a value of “1” when the Link Partner signals that a remote fault has occurred. The STE101P simply copies the value to this register and does not act upon it.

Reserved: ignore when read.

LP pause: Indicates that the link partner pause bit is set.

LP selector field: Bits 4:0 of the *link partner ability* register reflect the value of the Link Partner’s selector field. These bits are cleared any time Auto Negotiation is restarted or the chip is reset.

Advertisement bits: Bits 9: 5 of the *link partner ability* register reflect the abilities of the Link Partner. A “1” on any of these bits indicates that the Link Partner is capable of performing the corresponding mode of operation. Bits 9:5 are cleared any time Auto Negotiation is restarted or the STE101P is reset.

Table 10. PR06 [0d06, 0x06]: Auto negotiation expansion register

Bit #	Name	Description	Reset value	RW type	Type
15~5	---	Reserved	0	RO	-
4	Parallel detection fault	Parallel detection fault detected by the Auto Negotiation FSM	0	RO	-
3	LP next page able	1= Link Partner is Next Page capable	0	RO	-
2	LD next page able	Tied to 1. Device is always next page capable	1	RO	-
1	Page received	1= New link control work received from the link partner	0	RO	-
0	LP auto negotiation able	1 = Link Partner has Auto Negotiation capability	0	RO	-

Reserved: Ignore when read.

Parallel detection fault: Bit 4 of the Auto Negotiation Expansion Register is a read-only bit that gets latched high when a parallel detection fault occurs in the Auto Negotiation state machine. For further details, please consult the IEEE standard. The bit is reset to “0” after the register is read, or when the chip is reset.

LP next page able: Bit 3 of the Auto Negotiation Expansion Register returns a “1” when the Link Partner has Next Page capabilities. It has the same value as bit 15 of the Link Partner Ability Register.

Page received: Bit 1 of the Auto Negotiation Expansion Register is latched high when a new Link Code Word is received from the Link Partner, checked, and acknowledged. It remains high until the register is read, or until the chip is reset.

LP auto negotiation able: Bit 0 of the Auto Negotiation Expansion Register returns a “1” when the Link Partner is known to have Auto Negotiation capability. Before any Auto Negotiation information is exchanged, or if the Link Partner does not comply with IEEE Auto Negotiation, the bit returns a value of “0”.

Table 11. PR07 (0d07, 0x07): Auto negotiation next page transmit register

Bit #	Name	Description	Reset value	RW type	Type
15	Next page	Identifies this as the last page to be transmitted 1 = Additional Next Page(s) will follow.	0	R/W	-
14	Ack	Acknowledge	0	R/W	-
13	Msg page	0 = Unformatted Page. 1 = Message page.	1	R/W	-
12	Ack2	1 = Device can comply with message	0	R/W	-
11	Toggle	Arbitration control used to manage next page exchange.	0	RO	-
10~0	Message/ Unformatted code field	Code Field	00000000001	R/W	-

Next page: Indicates whether this is the last Next Page to be transmitted.

Msg page: Differentiates a Message Page from an Unformatted Page.

Ack2: Indicates that a device has the ability to comply with the message.

Toggle: Used by the Arbitration function to ensure synchronization with the Link Partner during Next Page exchange.

Message code field: An eleven-bit wide field, encoding 2048 possible messages.

Unformatted code field: An eleven-bit wide field, which may contain an arbitrary value.

Table 12. PR08 [0d08, 0x08]: Auto negotiation link partner next page transmit reg.

Bit #	Name	Descriptions	Reset Val	RW Type	Type
15	Next page	Identifies this as the last page to be transmitted 1 = Additional Next Page(s) will follow.	0	RO	-
14	Ack	Acknowledge	0	RO	-
13	Msg page	0 = Unformatted Page. 1 = Message page.	0	RO	-
12	Ack2	1 = Device can comply with message	0	RO	-
11	Toggle	Arbitration control used to manage next page exchange.	0	RO	-
10~0	Message/ Unformatted code field	Code Field	0	RO	-

Next page: Indicates whether this is the last Next Page.

Msg page: Differentiates a Message Page from an Unformatted Page.

Ack2: Indicates that Link Partner has the ability to comply with the message.

Toggle: Used by the Arbitration function to ensure synchronization with the Link Partner during Next Page exchange.

Message code field: An eleven-bit wide field, encoding 2048 possible messages.

Unformatted code field: An eleven-bit wide field, which may contain an arbitrary value.

Table 13. PR10 [0d16, 0x10]: 100BaseTX auxiliary control register

Bit #	Name	Descriptions	Reset Val	RW Type	Type
15~8	Reserved	---	0	R/W	-
7	Bypass symbol	1= Bypass the Symbol alignment. Used in conjunction with bit[10] to place 5B codes directly onto MII and RXER pins	0	R/W	-
6	Reserved	---	0	R/W	-
5	FEF enable	1 = Enable Far-End fault detection	0	R/W	-
4~3	Reserved	---	0	R/W	-

Table 13. PR10 [0d16, 0x10]: 100BaseTX auxiliary control register

Bit #	Name	Descriptions	Reset Val	RW Type	Type
2	Extended FIFO	1 = Enable Extended FIFO feature. FIFO fills and empties according to LP speed.	0	R/W	-
1	RMII_OOBS	1 = Enable RMII Out of Band signalling	0	R/W	-
0	Reserved	---	0	R/W	-

Reserved: Write as “0”, Ignore when read.

Bypass symbol: Receive symbol alignment may be bypassed by writing a “1” to bit 7 of MII Register 10h. When used in conjunction with the bypass 4B/5B encoder/decoder bit, unaligned 5B codes will be placed directly on the RXER and RXD [3:0] pins.

Reserved: The Reserved bits of the 100BaseTX Auxiliary Control Register must be written as “0” at all times. Ignore the STE101P outputs when these bits are read.

Table 14. PR11 [0d17, 0x11]: 100BaseTX Auxiliary Status Register

Bit #	Name	Description	Reset value	RW type	Type
15~12	Reserved	---	0	R/W	-
11	FIFO over run	1=FIFO over run occurred. PHY speeds or packet length may be too extreme	0	RO	LH
10	Reserved	---	0	RO	-
9	Speed	1=100Mbps 0=10Mbps	P	RO	-
8	Duplex	1=Full Duplex 0=Half Duplex	P	RO	-
7	Pause function	1=Pause Function Enabled 0= Pause Function Disabled	0	RO	-
6	Auto neg interrupt	1=Interrupt if Auto Neg completed	0	RO	-
5	Remote fault interrupt	1= Interrupt if Remote Fault detected	0	RO	LH
4	Link down interrupt	1=Interrupt if Link down (following link up condition)	0	RO	LH
3	Link code word recd interrupt	0=No Link Code Word detected 1=Interrupt if Link Code Word received	0	RO	LH
2	Parallel detection fault	1= Interrupt if Parallel Detection fault	0	RO	LH
1	Auto neg page recd.	1=Interrupt if Auto negotiation page received	0	RO	LH
0	Ref interrupt	1=Interrupt if 64K errant packets received	0	RO	LH
LH = Latched High (Clear after read), LL = Latched Low (Clear after read)					

Table 15. PR12 [0d18, 0x12]: Interrupt enable register

Bit #	Name	Description	Reset value	RW type	Type
15~7	Reserved	---	0	RO	-
6	Auto Neg Complete Int Enable	1=Enable Auto Negotiation completed Interrupt	0	R/W	-
5	RF Int Enable	1=Enable Remote Fault Interrupt	0	R/W	_
4	LD Int Enable	1=Enable Link Down Interrupt	0	R/W	-
3	Auto Neg Ack Int Enable	1=Enable Auto Negotiation Acknowledge Interrupt	0	R/W	_
2	Par Det Int Enable	1=Enable Parallel Detection Fault Interrupt	0	R/W	-
1	Auto Neg Page Recd Int enable	1=Enable Auto negotiation Page Received Interrupt	0	R/W	_
0	RX Error Buffer Int Enable	1=Enable RX error Buffer full Interrupt	0	R/W	-

Table 16. PR13 [0d19, 0x13]: 100BaseTX control register

Bit #	Name	Descriptions	Reset Val	RW Type	Type
15~14	Reserved	---	0	RO	-
13	Disable RX err counter	1=Disable receive error counter	0	R/W	-
12	Auto Neg Complete	1=Auto Negotiation process completed	0	RO	-
11	RX Voltage peak-peak	1=Receive voltage peak-to-peak 1.4VPP	0	R/W	-
10	Reserved	---	0	R/W	-
9	Enable Loop back	1=Enable remote loop back	0	R/W	-
8	Enable DC rest (Baseline wander)	1=Enable DC restoration (Baseline wander)	1	R/W	-
7	Enable NRZI to NRZ	1=Enable NRZI to NRZ data conversion	P	R/W	-
6	Enable 4B/5B	1=Enable 4B/5B encoder and decoder	P	R/W	-
5	Transmit Isolation	1=Transmit Isolation (Isolate MII and TX +/-). PHY address = <00000> at reset	0	R/W	-

Table 16. PR13 [0d19, 0x13]: 100BaseTX control register (continued)

Bit #	Name	Descriptions	Reset Val	RW Type	Type
4~2	CMode	000: In auto negotiation 001: 10Base-T Half Duplex 010: 100Base-TX Half Duplex 011: Reserved 100: Reserved 101: 10Base-T Full Duplex 110: 100Base-TX Full Duplex 111: Isolation, Auto Neg Disable	0	RO	-
1	MLT3 Disable	1=MLT3 Disabled	P	R/W	-
0	Scrambler/descrambler disable	1=Scrambler and descrambler logic is disabled	P	R/W	-

Table 17. PR14 [0d20, 0x14]: XCVR Mode control register

Bit #	Name	Descriptions	Reset Val	RW Type	Type
15~12	Reserved	---	0	RO	-
11	Link Detect	1=Reduces 10Base-T squelch level to increase cable length	0	R/W	-
10~8	Reserved	---	0	RO	-
7~3	PHY address	Phy Address[4:0] value of <00000> latched during reset = isolation mode	P	R/W	-
2	Reserved	---	0	RO	-
1	Preamble suppression	1=Accept management MDIO frames with the Preamble suppressed	1	R/W	-
0	Reserved	---	0	RO	-

Table 18. PR18 [0d24, 0x18]: Auxiliary control register

Bit #	Name	Description	Reset value	RW type	Type
15	Jabber disable	1= Disable Jabber detection, which will shut off the transmit when the packet length exceeds IEEE defined length	0	R/W	
14	Force link	1= Disable link integrity FSM checking and force the device to link pass state	0	R/W	
13~8	Reserved	---	0	RO	
7	HSQ	Increase HSQ or decrease LSQ squelch levels of incoming 10 BaseT packets	0	R/W	
6	LSQ				
5	Edge rate[1]	Program DAC output (Not supported)	1	R/W	
4	Edge rate[0]				
3	Auto Negotiation enable	1 = Auto negotiation enabled	P	RO	

Table 18. PR18 [0d24, 0x18]: Auxiliary control register (continued)

Bit #	Name	Description	Reset value	RW type	Type
2	Force 100	1 =Speed forced to 100MB	P	RO	
1	Speed 100 indicate	1 = Speed is 100MB	0	RO	
0	FDX indicate	1 = Full duplex mode selected	P	RO	
P = Pin Strap (Read at reset)					

Jabber disable: 10BASE-T operation only. Bit 15 of the Auxiliary Control Register allows the user to disable the Jabber Detect function, defined in the IEEE standard. This function shuts off the transmitter when a transmission request has exceeded a maximum time limit. By writing a “1” to bit 15 of the Auxiliary Control Register, the Jabber Detect function is disabled. Writing a “0” to this bit or resetting the chip restores normal operation. Reading this bit returns the value of Jabber Detect Disable.

Force link: Writing a “1” to bit 14 of the Auxiliary Control Register allows the user to disable the Link integrity state machines, and place the STE101P into forced Link Pass status. Writing a “0” to this bit or resetting the chip restores the Link Integrity functions. Reading this bit returns the value of Link Integrity Disable.

HSQ and LSQ: Extend or decrease the squelch levels for detection of incoming 10BASE-T data packets. The default squelch levels implemented are those defined in the IEEE standard. The high and low squelch levels are useful for situations where the IEEE-prescribed levels are inadequate. The squelch levels are used by the CRS/LINK block to filter out noise and recognize only valid packet preambles and link integrity pulses. Extending the squelch levels allows the STE101P to operate properly over long range cable lengths. Decreasing the squelch levels may be useful in situations where there is a high level of noise present on the cables. Reading these two bits returns the value of the squelch levels.

Edge rate: Control bits used to program the transmit DAC output edge rate in 100BASE-TX mode. These bits are logically AND’ed with the ER[1:0] input pins to produce the internal edge-rate controls (Edge_Rate[1] AND ER[1], Edge_Rate[0] AND ER[0]).

Auto negotiation enable: A read-only bit that indicates whether Auto Negotiation has been enabled or disabled on the STE101P. A combination of a “1” in bit 12 of the *control* register and a logic “1” on the ANEN input pin is required to enable Auto Negotiation. When Auto Negotiation is disabled, bit 3 of the Auxiliary Control Register returns a “0”. At all other times, it returns a “1”.

Force 100: A read-only bit that returns a value of ‘0” when one of the following two cases is true:

1. The ANEN pin is low AND the F100 pin is low.
2. Bit 12 of the *control* register has been written “0” AND bit 13 of the *control* register has been written “0”. When bit 8 of the Auxiliary Control Register is “0”, the speed of the chip will be 10BASE-T. In all other cases, either the speed is not forced (Auto Negotiation is enabled), or the speed is forced to 100BaseTX.

Speed 100 indicate: Bit 1 of the Auxiliary Control Register is a read-only bit that shows the true current operation speed of the STE101P. A “1” bit indicates 100BaseTX operation, while a “0” indicates 10BASE-T. Note that while the Auto Negotiation exchange is performed, the STE101P is always operating at 10BASE-T speed.

FDX Indicate: Bit 0 of the Auxiliary Control Register is a read-only bit that returns a “1” when the STE101P is in full-duplex mode. In all other modes, it returns a “0”.

Table 19. PR19 [0d25, 0x19]: Auxiliary status register

Bit #	Name	Description	Reset value	RW type	Type
15	Auto negotiation complete	1 = Auto Negotiation completed	0	RO	-
14	Auto negotiation ack	1= Auto Negotiation completed acknowledge state	0	RO	LH
13	Auto negotiation detect	1= Auto Negotiation entered acknowledge state	0	RO	LH
12	LP auto negotiation ability	1 = Auto Negotiation Link Partner ability detect	0	RO	LH
11	Auto negotiation pause	1=LD and LP pause bits set during Auto Negotiation	0	RO	-
10~8	Auto negotiation HCD	Highest Common Denominator determined by Auto Negotiation: 000= NO common denominator 001=10BaseT 010=10BaseT / Full Duplex 011=100BaseTX 100=100BaseT4 (Not Supported) 101=100BaseTX / Full Duplex 11x=Not defined	0	RO	
7	Parallel detection fault	1=Parallel detection fault detected	0	RO	LH
6	LP remote far end fault	1=Link Partner signalled far-end fault condition	0	RO	LH
5	LP page received	1=New page received from LP	0	RO	LH
4	LP Auto Negotiation ability	1=Link Partner is capable of Auto Negotiation	0	RO	LH
3	SP100 indicate	1=100 Mbps	0	RO	-
2	Link status	1=Link pass state	0	RO	LL
1	Auto negotiation enable	1=Auto Negotiation enabled	0	RO	-
0	Jabber detect	1=Jabber condition detected	0	RO	LH
LH = Latched High (Clear after reset)					

Table 20. PR1A[0d26, 0x1A]: Interrupt register

Bit #	Name	Description	Reset value	RW type	Type
15	FDX enable	Full duplex LED Enable. Affects which status signals are sent out on the serial LED data.	0	R/W	-
14	Interrupt enable	Interrupt enable. effects which status signals are sent out on the serial LED data. Note: bits [15:14} are mutually exclusive	0	R/W	-
13~12	Reserved	---	0	R/W	-
11	FDX Mask	1= Changes in full-duplex will not generate an interrupt	1	R/W	-
10	SPD Mask	1 = Speed will not generate an interrupt	1	R/W	-
9	Link Mask	1 = Changes in link status will not generate an interrupt	1	R/W	-
8	INTR Mask	1= None of the interrupts above will generate an Interrupt. Master enable	1	R/W	-
7~5	Reserved	---	0	RO	-
4	Global Interrupt	1=Any interrupt was detected	0	RO	-
3	FDX Interrupt	1 = Half / Full duplex change	0	RO	LH
2	Speed Interrupt	1= 10/100 Speed change	0	RO	LH
1	Link Interrupt	1 = Link status change	0	RO	LH
0	Interrupt status	Status of the INTR# pin	0	RO	LH
LH = Latched High (Clear after reset)					

FDX enable: Setting this bit enables the FDX LED mode. Bits 14 and 15 of this register are mutually exclusive. Only one may be set at a time. When FDXLED mode is enabled, XMTLED# becomes FDXLED# and RCVLED# becomes ACTLED#.

INTR enable: Setting this bit enables Interrupt Mode. Bits 14 and 15 of this register are mutually exclusive. Only one may be set at a time. When Interrupt Mode is enabled, XMTLED# becomes INTR# and RCVLED# becomes ACTLED#. Side Note: if both bits 14 and 15 are set at the same time, the FDXLED# will override the INTR# output, even though the interrupt's FDX, SPD, and LINK change status bits will behave as in normal interrupt operation.

FDX mask: When this bit is set, changes in Duplex mode will not generate an interrupt.

SPD mask: When this bit is set, changes in operating speed will not generate an interrupt.

LINK mask: When this bit is set, changes in Link Status will not generate an interrupt.

INTR mask: Master Interrupt Mask. When this bit is set, no interrupts will be generated, regardless of the state of the other MASK bits.

FDX interrupt: A "1" indicates a change of the Duplex status since last register read. Register read clears the bit.

Speed interrupt: A “1” indicates a change of the Speed status since last register read. Register read clears the bit.

Link interrupt: A “1” indicates a change of the Link status since last register read. Register read clears the bit.

Interrupt status: Represents status of the INTR# pin. A “1” indicates that the interrupt mask is off and that one or more of the change bits are set. Register read clears the bit.

Table 21. PR1B [0d27, 0x1B]: Auxiliary mode 2 register

Bit #	Name	Description	Reset value	RW type	Type
15~10	Reserved	---	0	RO	-
11~10	Reserved	---	0	R/W	-
9	LED no flash	1= Link LED will not blink for Tx/Rx 0= Link LED blinks with Tx/Rx activity	0	R/W	-
8	Reserved		0	RO	-
7	Block 10Base-T echo	1=Block 10Base-T echo data	1	R/W	-
6	Traffic meter LED	1=Traffic Meter LED Mode On 0=Traffic Meter LED Mode Off	1	R/W	-
5	Activity LED force	1=Activity LEDs forced on 0=Activity LEDs not forced	0	R/W	-
4	Serial LED enable	1=Serial LED Mode enabled 0=Serial LED Mode disabled	0	R/W	-
3	SQE disable	1=SQE not transmitted in 10Base-T half-duplex 0=SQE transmitted in 10Base-T half-duplex	1	R/W	-
2	Activity LED enable	Not supported	0	R/W	-
1	Qualified parallel detect	Not supported	1	R/W	-
0	Reserved	---	0	RO	-

LED no flash: Default 0. When set = 1, this bit will cause the Link LED (ledl, pin 36) to not blink when there is Tx/Rx activity, but be driven on continually when a good link is detected. In the default state (LED_No_Flash=0), the Link LED will be driven on when a good link is detected, and momentarily blink off and on at a 10Hz rate during Tx/RX activity.

Block 10BaseT echo: Default 0. When enabled during 10BASE-T half-duplex transmit operation, the TXEN signal will not echo onto the RXDV pin. The TXEN will echo onto the CRS pin, and the CRS deassertion directly follows the TXEN deassertion

Traffic meter LED: Default 0. When asserted, the Receive and Transmit (Activity) LED’s (XMTLED# and RCVLED# pins) will not blink based on the internal LED-CLK (approximately 80ms ON time). Instead, they will blink based on the rate of Receive and Transmit activity. Each time a Receive or Transmit operation occurs, the respective LED will

turn on for a minimum of 5ms. With light traffic, the LED's will blink at a low rate. During medium to heavy traffic (packets within 5ms of each other), the LED's will remain on.

Activity LED force: Default 0. When asserted, the Receive and Transmit (Activity) LED's (XMTLED# and RCVLED# pins) will be turned on. When 0, will have no affect on the Activity LED's. The Activity Force ON bit has a higher priority than Activity LED Force Inactive, bit 4, Register 1Dh.

Serial LED enable: Default 0. When asserted, the 4 slices' LED outputs will be serially shifted out on the 2nd slices' LED outputs. The sequence of outputs for the different Serial modes are: FDX, '1', Speed, Link, FDX, Activity when the FDXLED mode is set and, FDX, '1', Speed, Link, Transmit, Receive, when neither interrupt nor FDXLED modes are selected. When this bit is 0, the four LED outputs per slice will be operated in parallel.

SQE disable: Default 0. When asserted, will disable SQE pulses when operating in 10BASE-T half-duplex mode

Qualified parallel detect: This bit allows the Auto Negotiation /Parallel Detection process to be qualified with information in the Advertisement register. Default value is 0.

Table 22. PR1C[0d28, 0x1C]: 10Base-T error and general status register

Bit #	Name	Description	Reset value	RW type	Type
15~14	Reserved	---	0	RO	-
13	MDIX status	1=MDIX is used 0=MDI configuration is used	0	RO	-
12	MDIX swap	1=Force MDIX 0=MDI or MDIX if MDIX is enabled	0	R/W	-
11	MDIX disable	1=Disable MDIX 0=Autodetect and set MDI or MDIX	P	R/W	-
10	Manchester code error	Not supported	0	RO	-
9	EOF error	1=End of Frame detection error (Jabber detection - 10BaseT)	0	RO	-
8~4	Reserved	---	0	RO	-
3	Auto negotiation enable	1=Auto Negotiation enable	P	RO	-
2	Force 100	1=100Mbs mode forced	P	RO	-
1	SP100	1=100Mbps speed selected	0	RO	-
0	FDX indicate	1=Full duplex mode selected	0	RO	-
P=Pin strap (Read at reset)					

MDIX status: This bit indicates whether MDI or MDIX is in use.

MDIX swap: Setting this bit forces the device to MDIX. When this bit is 0, the MDIX status will be determined by Auto-Negotiation if Auto-MDIX is enabled.

MDIX disable: Setting this bit disables Auto detection and negotiation of MDIX. Clearing this bit enables Auto MDIX

Manchester code error: Indicates that a Manchester code violation was received. This bit is only valid during 10BASE-T operation.

EOF error: Indicates the EOF (end of frame) sequence was improperly received, or not received at all. This error bit is only valid during 10BASE-T operation.

Auto negotiation enable: A read-only bit that indicates whether Auto Negotiation has been enabled or disabled on the STE101P. A combination of a “1” in bit 12 of the Control *register* and a logic “1” on the ANEN input pin is required to enable Auto Negotiation.

Force 100: A read-only bit that returns a value of “0” when one of the following two cases is true:

1. The ANEN pin is low AND the F100 pin is low.
2. Bit 12 of the Control register has been written “0” AND bit 13 of Control Register has been written “0”.

When bit 8 of the Auxiliary Control Register is “0”, the speed of the chip will be 10BASE-T. In all other cases, either the speed is not forced (Auto Negotiation is enabled), or speed is forced to 100 BASE-X.

SP 100: A read-only bit that shows the true current operation speed of the STE101P. A “1” bit indicates 100BaseTX operation, while a “0” indicates 10BASE-T. Note that while the Auto Negotiation exchange is performed, the STE101P is always operating at 10BASE-T speed.

FDX indicate: A read-only bit that returns a “1” when the STE101P is in full-duplex mode. In all other modes, it returns a “0”.

Table 23. PR1D[0d29, 0x1D]: control register

Bit #	Name	Description	Reset value	RW type	Type
15~5	Reserved	---	0	RO	-
4	Force activity LED	1=Disables the Activity LED output pin	0	R/W	-
3	Force Link LED	1=Disables the Link LED output pin	0	R/W	-
2	Reserved	---	0	R/W	-
1	Block TXEN	1=Short IPG’s <(4) TXC cycles will insert (2) IDLE cycles prior to next packet	0	R/W	-
0	Reserved	---	0	R/W	-

Reserved: Write as “000h”, ignore when Read.

Force activity LED: When set to “1”, the XMTLED# and RCVLED# output pins are forced into their inactive state, regardless of the mode (normal, FDX, Interrupt, or Serial) these outputs are configured to. When “0”, XMTLED# and RCVLED# output pins are enabled.

Force link LED: When set to “1”, the Link LED output pin if forced into its inactive state. When “0”, Link LED output is enabled.

Block TXEN: When this mode is enabled, short IPG’s of 1, 2, 3, or 4 TXC cycles will all result in the insertion of two IDLE’s before the beginning of the next packet’s JK symbols.

Table 24. PR1E[0d30, 0x1E]: Auxiliary PHY register

Bit #	Name	Description	Reset value	RW type	Type
15	HCD 100Base-TX FDX	1=Auto Negotiation selected 100Base-TX full-duplex	0	RO	-
14	HCD 100Base-T4	1=Auto Negotiation selected 100 BaseT4 (Not supported)	0	RO	-
13	HCD 100Base-TX	1=Auto Negotiation selected to 100BaseTX	0	RO	-
12	HCD 10Base-T FDX	1=Auto Negotiation selected to 10BaseT full-duplex	0	RO	-
11	HCD 10Base-T	1=Auto Negotiation selected to 10BaseT	0	RO	-
10~9	Reserved	---	0	RO	-
8	Restart Auto negotiation	1=Restart Auto Negotiation. Auto Negotiation must be enabled for any effect	0	R/W	SC
7	Auto negotiation complete	1=Auto Negotiation process Completed	0	RO	-
6	Reserved	---	0	RO	-
5	Auto negotiation ack	1=Auto Negotiation Acknowledge completed	0	RO	-
4	Auto negotiation ability	1=Auto Negotiation waiting for LP Ability	0	RO	-
3	Super isolate	1=Super Isolate Mode 0=Normal Operation	0	R/W	-
2	Reserved	---	0	RO	-
1	Reserved	---	0	R/W	-
0	RXER code	Reserved	0	R/W	-
SC= Self Clear (Clear following action)					

HCD 10BaseT: Bits 15: 11 of the Auxiliary PHY Register are five read-only bits that report the Highest Common Denominator (HCD) result of the Auto Negotiation process. Immediately upon entering the Link Pass state after each reset or Restart Auto Negotiation, only one of these five bits will be a “1”. The Link Pass state is identified by a “1” in bit 6 or 7 of this register. The HCD bits are reset to “0” every time Auto Negotiation is restarted or the STE101P is reset. Note that for their intended application, these bits will uniquely identify the HCD only after the first Link Pass after reset or restart of Auto Negotiation. On later Link Fault and subsequent re-negotiations, if the ability of the Link Partner is different, more than one of the above bits may be active. These bits are only set for full Auto Negotiation hand-shake, and not for Parallel Detection of Forced speed modes. Note that bit 14, HCD_T4, will never be set in the STE101P.

Reserved: Ignore when read

Restart auto negotiation: A self-clearing bit that allows the Auto Negotiation process to be restarted, regardless of the current status of the state machine. For this bit to work, Auto Negotiation must be enabled. Writing a “1” to this bit restarts Auto Negotiation. Since the bit is self-clearing, it always returns a “0” when read. The operation of this bit is identical to bit 9 of the Control Register.

Auto negotiation complete: This read-only bit returns a “1” after the Auto Negotiation process has been completed. It remains “1” until the Auto Negotiation is restarted, a Link Fault, occurs, or the chip is reset. If Auto Negotiation is disabled, or the process is still in progress, the bit returns a “0”.

Auto negotiation ack: This read-only bit is set to “1” when the Arbitrator state machine exits the Acknowledged Detect state. It remains high until the Auto Negotiation process is restarted, or the STE101P is reset.

Auto negotiation ability: This read-only bit returns a “1” when the Auto Negotiation state machine is in the Ability Detect state. It enters this state a specified time period after the Auto Negotiation process begins, and exits after the first FLP burst or link pulses are detected from the Link Partner. This bit returns a “0” any time the Auto Negotiation state machine is not in the Ability Detect state.

Super isolate: Writing a “1” to this bit places the STE101P into the Super Isolate mode. Similar to the Isolate mode, all MII inputs are ignored, and all MII outputs are tri-stated. Additionally, all link pulses are suppressed. This allows the STE101P to coexist with another PHY on the same adapter card, with only one being activated at any time.

RXER code: Writing a “1” to bit 0 of the Auxiliary Mode Register enables the RXER Code mode during 10BASE-T operation. In this mode, when a receive data error occurs, indicated by pins RXDV=1 and RXER=1, the RXD[3:0] bus will contain a non-zero 4-bit encoded value indicating the type of error. This feature provides the user with more detailed information regarding the status of the system. Writing a “0” to this bit or resetting the chip restores normal operation. Note that this mode does not disrupt normal communication with the MAC layer, and can safely be used at all times. Also, note that the RXER Code mode is not available in 10BASE-T Serial mode. In 100BaseTX operation, the RXER code mode is always active.

Table 25. PR1F[0d31, 0x1F]: Shadow register enable

Bit #	Name	Description	Reset value	RW type	Type
15~8	Reserved	---		RO	
7	Shadow enable	1= Enable Shadow registers	0	R/W	-
6~0	Reserved	---		RO	-

Table 26. RS18 [0d24, 0x18]: 100BaseTX Disconnect Counter Register

Bit #	Name	Description	Reset value	RW type	Type
15	LP fast	1=Link Partner recovered clock is faster than the local reference clock	0	RO	-
14	LP slow	1=Link Partner recovered clock is slower than the local reference clock	0	RO	-
13~0	Reserved	---	0	R/W	-

Table 27. RS1B [0d27, 0x1B]: MISC Status/error/test register

Bit #	Name	Description	Reset value	RW type	Type
15	MLT3 detect	1= MLT3 signalling is enabled with no errors detected	0	RO	-
14~12	TX cable length	Cable length (meters) decode as follows: 000 <= 20 001 = 20-40 010 = 40-60 011 = 60-80 100 =80-100 101 =100-120 110 = 120-140 111 = >140	0	RO	-
11	Reserved	---	0	RO	-
10	LED test cntrl	LED Test controls. Speed up clock for simulation	0	R/W	-
9	Descrambler Locked	1=Descrambler is locked on RX stream	0	RO	-
8	False carrier detect	1=False carrier detected	0	RO	LH
7	Bad ESD detect	1=Bad ESD detected	0	RO	LH
6	RXER detect	1=RX(100) error detected	0	RO	LH
5	TXER detect	1=TX(100) error detected	0	RO	LH
4	Lock error detect	1=Lock error detected	0	RO	LH
3	MLT3 error detected	1=MLT3 error detected	0	RO	LH
2~0	Reserved	---	0	R/W	-

Table 28. RS1C[0d28, 0x1C]: Auxiliary status 3 - FIFO status register

Bit #	Name	Description	Reset value	RW type	Type
15~13	Reserved	---	0	RO	-
12	SMII mode	1 = SMII mode	P	RO	-
11	RMII mode	1 = RMII mode	P	RO	-
10	MII mode	1 = MII mode	P	RO	-
9~8	Reserved	---	0	RO	-
7	FLP detect	1=Fast Link Pulse detection	0	RO	LH
6	NLP detect	1=Normal Link Pulse detection	0	RO	-
5	Link Break	1=Link Break timer expired	0	RO	-
4	Link Fail	1=Link fail timer expired	0	RO	-
3~0	FIFO consumption	Current FIFO consumption	0	RO	-

Table 29. RS1D [0d29, 0x1D]: FIFO control register

Bit #	Name	Description	Reset value	RW type	Type
15~4	Reserved	---	0	R/W	
3~0	FIFO size select	Configure the size of the FIFO. Sizes in # of bits: 0000 = 12 1000 = 44 0001 = 16 1001 = 48 0010 = 20 1010 = 52 0011 = 24 1011 = 56 0100 = 28 1100 = 60 0101 = 32 1101 = 64 0110 = 36 0111 = 40	0	R/W	

Table 30. RS1E [0d30, 0x1E]: Packet counter register

Bit #	Name	Description	Reset value	RW type	Type
15~0	Packet length counter	Number of bytes in the last packet received	0	RO	

7 Device operation

The STE101P includes a 10/100 Base-T Ethernet Transceiver with MII, RMII, and SMII interfaces for data and control from/to the Station Management Entity (STE). The STE101P integrates the IEEE802.3u compliant functions of PCS (Physical Coding Sub-layer), PMA (Physical Medium Attachment), and PMD (Physical Medium Dependent) for 100Base-TX, and the IEEE802.3 compliant functions of Manchester encoding/decoding and transceiver for 10Base-T. IEEE standard auto-negotiation functions are also supported. Media Independent Interface (MII) is a 4-bit interface transferring 10Mbit data using a 2.5MHz clock and 100Mbit data using a 25MHz clock. RMII (Reduced Media Independent Interface) is a low pin count alternative capable of transferring 10 and 100 Mbit dibits data using a 50MHz reference clock. A further alternative called SMII (Serial Media Independent Interface) is also possible allowing a further reduction in the number of pins required to connect the PHY to the MAC. SMII is capable of transferring 10 and 100 Mbit serial data using a 125MHz reference clock. All the functions and operation schemes are described in the following sections.

7.1 100Base-TX transmit operation

In the 100Base-TX transmission, the device provides the transmission functions of PCS, PMA, and PMD for encoding of MII data nibbles to five-bit code-groups (4B/5B), scrambling, serialization of scrambled code-groups, converting the serial NRZ code into NRZI code, converting the NRZI code into MLT3 code, and then driving the MLT3 code into the category 5 Unshielded Twisted Pair cable through an isolation transformer with the turns ratio of 1.414:1.

Data code-groups encoder: In normal MII mode application, the device receives nibble type 4B data via the TxD0~3 inputs of the MII. These inputs are sampled by the device on the rising edge of Tx-clk and passed to the 4B/5B encoder to generate the 5B code-group used by 100Base-TX.

Idle code-groups: In order to establish and maintain the clock synchronization, the device needs to keep transmitting signals to the medium. The device will generate Idle code-groups for transmission when there is no real data want to be sent by MAC.

Start-of-stream delimiter-SSD (/J/K/): In a transmission stream, the first 16 nibbles are MAC preamble. In order to let partner delineate the boundary of a data transmission sequence and to authenticate carrier events, the device will replace the first 2 nibbles of the MAC preamble with /J/K/ code-groups.

End-of-stream delimiter-ESD (/T/R/): In order to indicate the termination of the normal data transmissions, the device will insert 2 nibbles of /T/R/ code-group after the last nibble of FCS.

Scrambling: All the encoded data (including the idle, SSD, and ESD code-groups) is passed to the data scrambler to reduce the EMI and spread the power spectrum using a 10-bit scrambler seed loaded at the beginning.

Data conversion of parallel to serial, NRZ to NRZI, NRZI to MLT3: After scrambled, the transmission data with 5B type in 25MHz will be converted to serial bit stream in 125MHz by the parallel to serial function. After serialized, the transmission serial bit stream will be further converted from NRZ to NRZI format. This NRZI conversion function can be bypassed, if the bit 7 of PR13 register is cleared as 0. After NRZI converted, the NRZI bit stream is passed through MLT3 encoder to generate the TP-PMD specified MLT3 code. With this MLT3 code, it lowers the frequency and reduces the energy of the transmission signal in the UTP cable and also makes the system easily to meet the FCC specification of EMI.

Wave-shaper and media signal driver: In order to reduce the energy of the harmonic frequency of transmission signals, the device provides the wave-shaper prior to the line driver to smooth but keep symmetric the rising/falling edge of transmission signals. The wave-shaped signals include the 100Base-TX and 10Base-T both are passed to the same media signal driver. This design can simplify the external magnetic connection with single one.

RMII mode: Uses a reference clock (SCLK) of 50MHz. For RMII mode, CRS and RX_DV pins combine their functionality into the CRS_DV pin (pin 48). The CRS_DV pin will toggle at the end of a frame to indicate that the data is being emptied from the internal FIFO's.

SMII mode: Uses a reference clock (SCLK) of 125 MHz. Serial data is passed while operating in SMII mode. Only Bit 0 of the txd bus is used to pass the serial frames. The first bit of the frames is identified by the sync pulse. A FIFO is not needed for the transmit data path as the internal 25MHz clock used for the encoding is synchronized with the 125MHz reference clock.

7.2 100Base-TX receive operation

In the 100Base-TX receiving operation, the device provides the receiving functions of PMD, PMA, and PCS for receiving incoming data signals through category 5 UTP cable and an isolation transformer with 1.414:1 turns ratio. It includes the adaptive equalizer and baseline wander, data conversions of MLT3 to NRZI, NRZI to NRZ and serial to parallel, the PLL for clock and data recovery, the de-scrambler, and the decoder of 5B/4B.

Adaptive equalizer and baseline wander: Since the high speed signals over the unshielded (or shielded) twisted Pair cable will induce the amplitude attenuation and phase shifting. Furthermore, these effects are depends on the signal frequency, cable type, cable length and the connectors of the cabling. So a reliable adaptive equalizer and baseline wander to compensate all the amplitude attenuation and phase shifting are necessary. In the transceiver, it provides the robust circuits to perform these functions.

MLT3 to NRZI decoder and PLL for data recovery: After receiving the proper MLT3 signals, the device converts the MLT3 to NRZI code for further processing. After adaptive equalizer, baseline wander, and MLT3 to NRZI decoder, the compensated signals with NRZI type in 125MHz are passed to the Phase Lock Loop circuits to extract out the original data and synchronous clock.

Data conversions of NRZI to NRZ and serial to parallel: After data is recovered, the signals will be passed to the NRZI to NRZ converter to generate the 125 MHz serial bit stream. This serial bit stream will be packed to parallel 5B type for further processing. The NRZI to NRZ conversion can be bypassed, if the bit 7 of PR13 register is cleared as 0.

De-scrambling and decoding of 5B/4B: The parallel 5B type data is passed to de-scrambler and 5B/4B decoder to return their original MII nibble type data.

Carrier sensing: Carrier Sense (CRS) signal is asserted when the STE101P detects any 2 non-contiguous zeros within any 10 bit boundary of the receiving bit stream. CRS is de-asserted when ESD code-group or Idle code-group is detected. In half duplex mode, CRS is asserted during packet transmission or receive. But in full duplex mode, CRS is asserted only during packet reception.

RMII mode: 5B code group are converted to 4bit nibbles and the data is sent through a FIFO to the RMII receive data pins as dibits. In case of invalid code group in the data stream, REXER signal is asserted and the 4 bits of the receive data pins will be driven with a specific code signalling the type of error detected.

SMII mode: Receive data is buffered in a FIFO to bridge differences between the recovered and reference clocks. Control information and data nibbles are encapsulated into segments of 10 bit SMII frames. Each frame represents a byte of data. The RXER pin is asserted relevant to errant packet data entering the FIFO.

7.3 10Base-T transmit operation

In the 10Base-T, the device's TX channel includes the parallel to serial converter, NRZ to Manchester Encoder, Link pulse generation, and an internal Physical Ethernet Wire Interface (Phy). It also provides Collision detection and SQE test for half duplex application.

RMII mode: Uses a reference clock (SCLK) of 50 MHz. The value on txd[1:0] must be valid such that txd[1:0] may be sampled every 10th cycle yielding the correct frame data. To achieve this, the dibits should be repeated 10 times.

SMII mode: Uses a reference clock (SCLK) of 125MHz. The MII nibbles must be extracted from the SMI frame for sampling on a 2.5MHz clock. To achieve this, the serial txd frame should be repeated 10 times.

7.4 10Base-T receive operation

The 10Base-T RX channel contains the Phy, SMART Squelch circuits, clock recovery circuits, Link pulse detector, Manchester-to-NRZ decoder and serial-to-parallel converter. Manchester decoding is performed on the data stream.

RMII mode: Dibits are repeated 10 times so that any repeated dibit may be sampled on the 10Mb clock edge.

SMII mode: The MII nibbles are extracted from the SMI frame and ready for sampling on a 2.5MHz clock. To allow for this, the serial txd frame is repeated 10 times.

7.5 Loop-back operation

The STE101P provides internal loop-back option for both the 100Base-TX and 10Base-T operations. Setting bit 14 of PR00 register to 1 can enable the loop-back option. In this loop-back operation, the txp/txn and rxp/rxn lines are isolated from the media. The STE101P also provides remote loop-back operation for 100Base-TX operation. Setting bit 9 of PR13 register to 1 enables the remote loop-back operation.

In the 100Base-TX internal loop-back operation, the data comes from the transmit output of NRZ to NRZI converter then loop-back to the receive path into the input of NRZI to NRZ converter.

In the 100Base-TX remote loop-back operation, the data is received from rxp/rxn pins through receive path to the output of data and clock recover and then loop-back to the input of NRZI to MLT3 converter of transmit path then transmit out to the medium via the transmit line drivers.

In the 10Base-T loop-back operation, the data is through transmit path and loop-back from the output of the Manchester encoder into the input of Phase Lock Loop circuit of receive path.

7.6 Full duplex and half duplex operation

The STE101P can operate for either full duplex or half duplex network application. In full duplex, both transmit and receive can be operated simultaneously. Under full duplex mode, collision (COL) signal is ignored and carrier sense (CRS) signal is asserted only when the STE101P is receiving.

In half duplex mode, either transmit or receive can be operated at one time. Under half duplex mode, collision signal is asserted when transmit and receive signals collided and carrier sense asserted during transmission and reception.

7.7 Auto-negotiation operation

The Auto-Negotiation function is designed to provide the means to exchange information between the STE101P and the network partner to automatically configure both to take maximum advantage of their abilities, and both are setup accordingly. The Auto-Negotiation function can be controlled through ANE, bit 12 of the PR00 register, or the MF0 pin 5.

Auto-Negotiation exchanges information with the network partner using the Fast Link Pulses (FLPs) - a burst of link pulses. There are 16 bits of signaling information contained in the burst pulses to advertise all remote partner's capabilities which are determined by the register of PR04. According to this information they find out their highest common capability by following the priority sequence as below:

1. 100Base-TX full duplex
2. 100Base-TX half duplex
3. 10Base-T full duplex
4. 10Base-T half duplex

During power-up or reset, if Auto-Negotiation is found enabled then FLPs will be transmitted and the Auto-Negotiation function will proceed. Otherwise, the Auto-Negotiation will not occur until the bit 12 of PR0 register is set to 1. When Auto-Negotiation is disabled, then the Network Speed and Duplex Mode are selected by programming PR00 register.

7.8 Power down operation

To reduce the power consumption, the STE101P is designed with a power down feature, which can save the power consumption significantly. Since the power supply of the 100Base-TX and 10Base-T circuits are separated, the STE101P can turn off the circuit of either the 100Base-TX or 10Base-T when the other one of them is operating. There is also a Power Down mode which can be selected by PDEN in register PR00 bit 11. During the Power Down mode, TXP/TXN outputs and all LED outputs are 3-stated, and the MII

interface is isolated. During Power Down mode the MII management interface is still available for reading and writing device registers. Power Down mode can be exited by clearing bit 11 of register PR00 or by a hardware or software reset (setting PR00:15=1).

7.9 LED display operation

The STE101P provides 5 LED pins, the detail descriptions about the operation are described in the PIN Description section, and as follows.

- Speed LED: 100Mbps(on) or 10Mbps(off)
- Receive LED: Blinks at 10Hz when receiving, but not colliding
- Transmit LED: Blinks at 10Hz when transmitting, but not colliding
- Link LED: On when 100M or 10M link is active. It will also blink at 10Hz for Transmit and Receive Activity if bit 9 of register PR1B (0x1b) is 0 (default). It will not blink if register PR1B bit 9 = 1.
- Collision LED: Blinks at 20Hz to indicate a collision

7.10 Reset operation

There are two ways to reset the STE101P.

First, for hardware reset, the STE101P can be reset via RESET pin (pin 28). The active low Reset input signal is required for at least 1 ms, and at least one transition is required on MDC (pin 42) to ensure proper reset operation. The RIP output pin 29 goes to a logic 1 to indicate that reset has completed.

Second, for software reset, when bit 15 of register PR00 is set to 1, the STE101P resets the entire circuits and registers to their default values, then clear the bit 15 of PR00 to 0, and set the RIP output pin 29 to logic 1.

Both hardware and software reset operations initialize all registers to their default values. This process includes re-evaluation of all hardware-configurable registers. Logic levels on several I/O pins are detected during hardware reset period to determine the initial functionality of STE101P. Some of these pins are used as outputs after the reset operation. Care must be taken to ensure that the configuration setup will not interfere with normal operation. Dedicated configuration pins can be tied to the Vcc or ground directly. Configuration pins multiplexed with LED outputs should be weakly pulled up or weakly pulled down through resistors as shown in the following circuits.

Figure 4. LED connection for Logic level 0

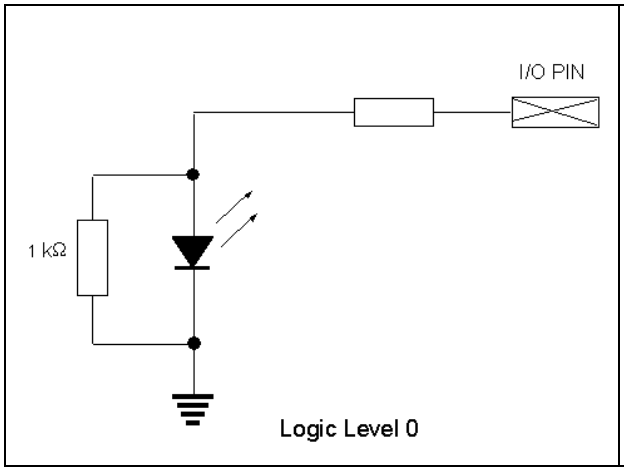
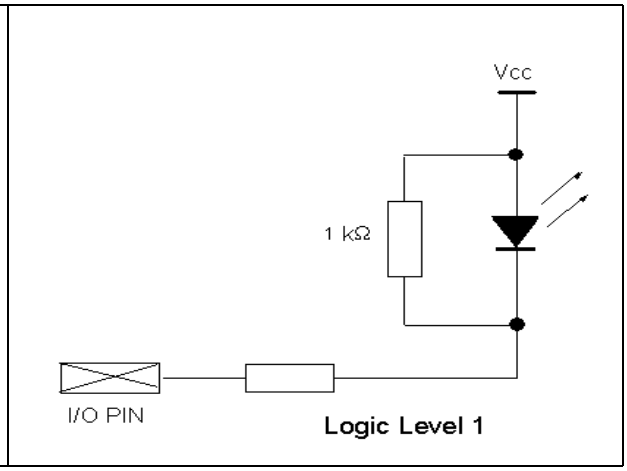


Figure 5. LED connection for Logic level 1



Note: The above LED connections are recommended for setting a Logic Level 1 or Logic Level 0 on the STE101P LED/PHY address pins, for determining PHY address.

7.11 Preamble suppression

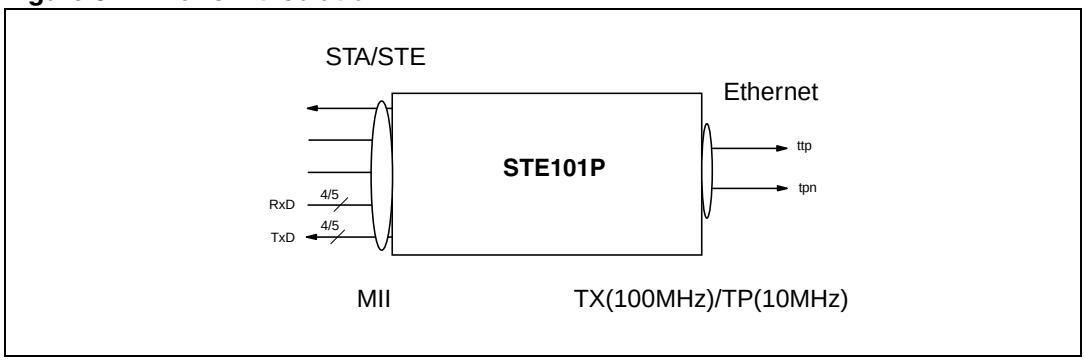
Preamble suppression mode in the STE101P is indicated by a one in bit six of the PR1 Register. If it is determined that all PHY devices in the system support preamble suppression, then a preamble is not necessary for each management transaction. The first transaction following power-up/hardware reset requires 32 bits of preamble. The full 32 bit preamble is not required for each additional transaction. The STE101P will respond to management accesses without preamble, but a minimum of one idle bit between management transactions is required as specified in IEEE 802.3u.

7.12 Remote fault

The remote fault function indicates to a link partner that a fault condition has occurred by using the Remote Fault bit, which is encoded in bit 13 of the Link Code Word. A local device indicates to its link partner that it has found a fault by setting the Remote Fault bit in the Auto-Negotiation register to logic one and renegotiating with the link partner. The Remote Fault bit remains at logic one until successful negotiation with the Link Code Word occurs. The bit will then return to 0. When the message is sent that the Remote Fault bit is set to logic one, the device will set the Remote Fault bit in the MII to logic one if the management function is present.

7.13 Transmit isolation

Figure 6. Transmit isolation



The transmit isolation isolates the PHY from MII and Tx +/- interface. As in the Isolate mode, all MII inputs are ignored and all MII outputs are tri-stated. Additionally, all link pulses are suppressed.

7.14 Automatic MDI / MDIX feature

The automatic MDI / MDIX feature compensates for using a cross over cable. With Auto MDIX, the STE101P automatically detects what the other device is and switches the TX & RX pins accordingly. The state machine basically controls switching the tdp/tdn and the rdp/rdn signals prior to the auto-negotiation communication. The swapping occurs to allow FLP/NLP to be transmitted and received in the event that the external cable connections have been swapped.

7.15 RMII interface

The Reduced Media Independent Interface (RMII) provides a low cost alternative to the IEEE 802.3u MII interface. It can support 10 and 100 Mbit data rates with a single clock, using independent 2 bit wide transmit and receive paths. A single synchronous reference clock (SCLK pin 32) of 50 MHz is used as a timing reference for all transmitters and receivers. By doubling the clock frequency relative to the MII, four pins are saved in the data path, which uses two lines into each transmitter and two lines out of each receiver relative to 4 lines in each direction in the MII interface. Since Start of Packet and End of Packet timing information is preserved across the interface, the MAC is able to derive the COL signal from the receive and transmit data delimiters, saving another pin.

7.16 SMII interface

The Serial MII Interface is an alternative to the MII and RMII interfaces to further reduce the number of pins required for the interface from the MAC to the PHY. SMII uses on one data pin (TXD0/RXD0), a SYNC pin, and encodes signals TXER, TXEN, CRS, and RX_DV into the data stream. In SMII mode, the TX_EN pin (54) is used as the SYNC pin for the SMII interface, and a pin 32 (SCLK) requires a reference clock of 125MHz.

8 Electrical specifications and timings

Table 31. Absolute maximum ratings

Parameter	Value	Unit
Supply Voltage(Vcc)	-0.5 V to 5.5 V	V
Input Voltage	-0.5 V to VCC + 0.5 V	V
Output Voltage	-0.5 V to VCC + 0.5 V	V
Storage Temperature	-65 °C to 150 °C (-85 °F to 302 °F)	°C (°F)
Ambient Temperature	-40 °C to +85 °C	°C
ESD Protection	2000	V

Table 32. General DC specifications

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Units
General DC						
Vcc	Supply voltage		3.15	3.3	3.45	V
10Base-T voltage/current characteristics						
Vida10	Input differential accept peak voltage	5MHz ~ 10MHz	585		3100	mV
Vidr10	Input differential reject peak voltage	5MHz ~ 10MHz	0		585	mV
Vod10	Output differential peak voltage		2200		2800	mV
Icct10	Line driver supply			17		mA
Idd10	Digital current consumption	Link active		18		mA
IddA10	Analog current consumption	Link active, transmitting 100%		77		mA
100Base-TX voltage/current characteristics						
Vida100	Input differential accept peak voltage		200		1000	mV
Vidr100	Input differential reject peak voltage		0		200	mV
Vod100	Output differential peak voltage		950		1050	mV
Icct100	Line driver supply			12		mA
Idd100	Digital current consumption	Link active		25		mA
IddA100	Analog current consumption	Link active, transmitting 100%		70		mA

Table 33. X1 and NLP timing specifications

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
X1 specifications						
TX1d	X1 duty cycle		45	50	55	%
TX1p	X1 period			30		ns
TX1t	X1 tolerance			+/- 50		PPM
$TX1C_L$	X1 load capacitance				18	pF
10Base-T normal link pulse (NLP)						
TNPW	NLP width	10Mbps		100		ns
TNPC	NLP period	10Mbps	8		24	ms

Figure 7. Normal link pulse timings

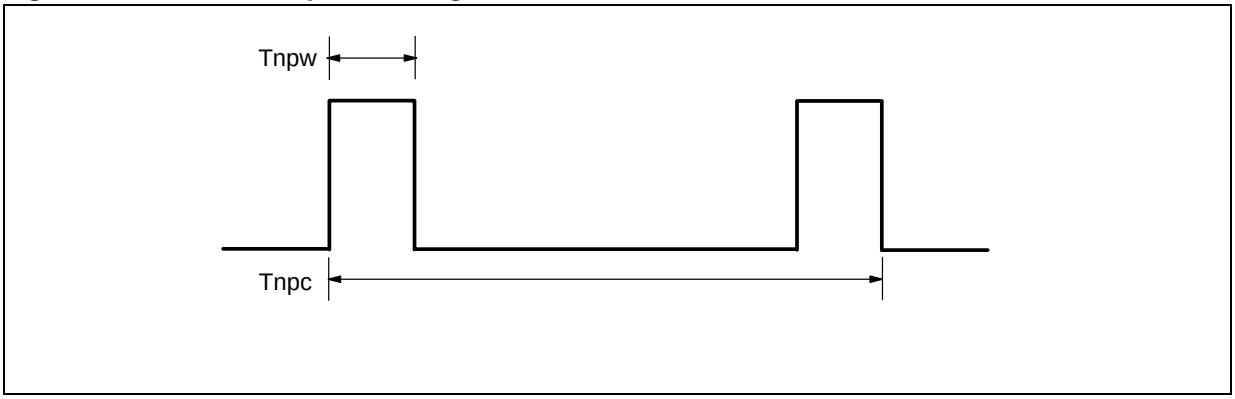


Figure 8. Fast link pulse timing

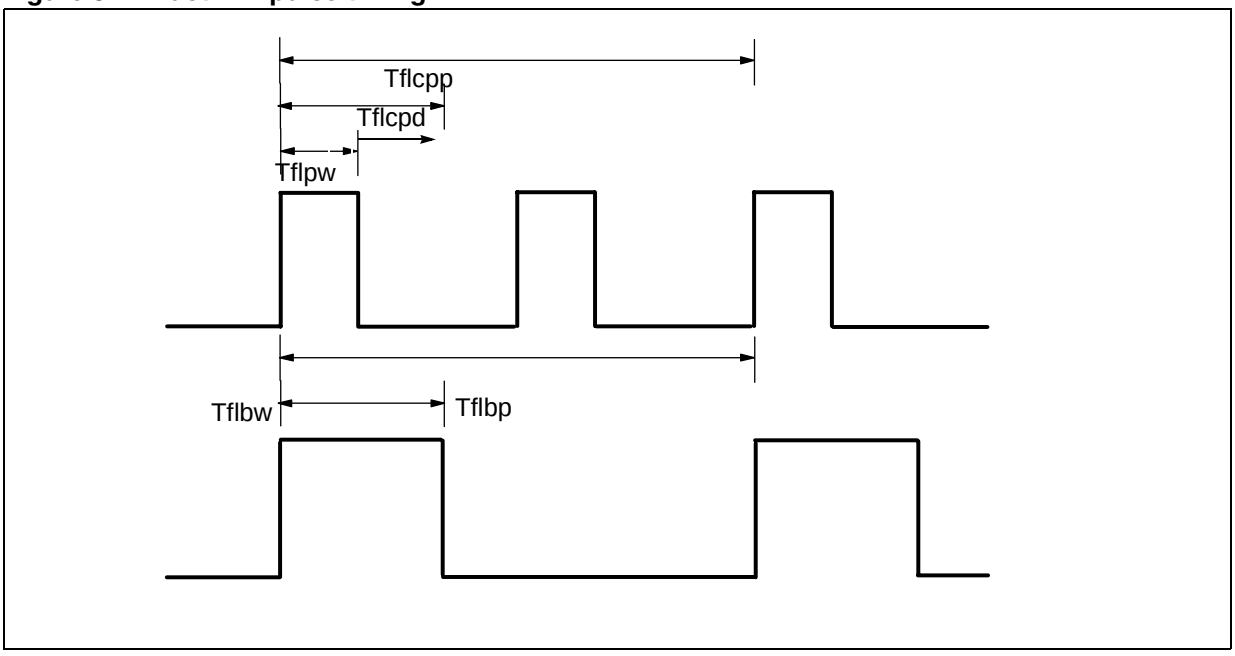


Table 34. Fast link pulse (FLP) AC timing specifications

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Units
Tflpw	FLP width			100		ns
Tflcpp	Clock pulse to clock pulse period		111	125	139	µs
Tflcpd	Clock pulse to data pulse period		55.5	62.5	69.5	µs
-	Number of pulses in one burst		17		33	pulse
Tflbw	Burst width			2		ms
Tflbp	FLP burst period		8	16	24	ms

Figure 9. MII management clock timing

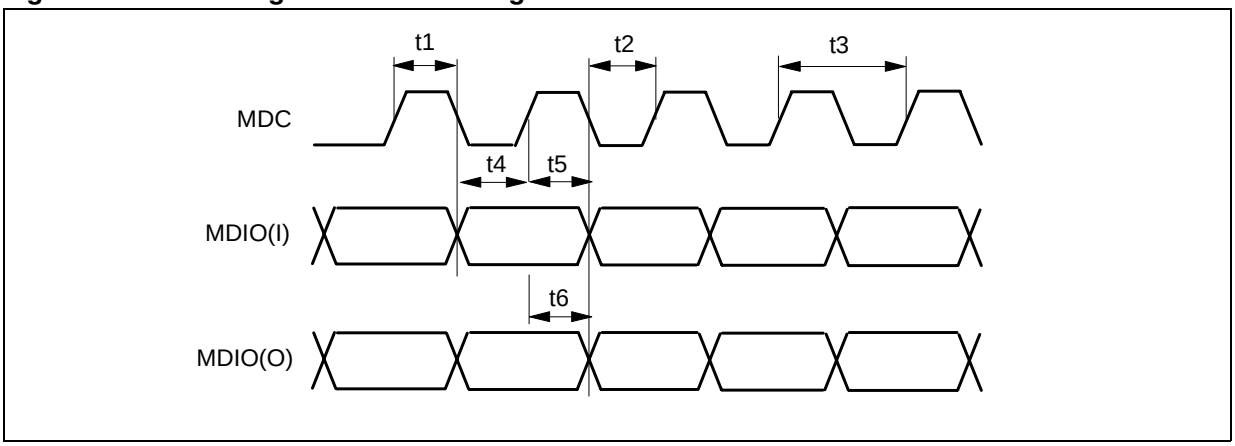


Table 35. MII management and 100Base-TX transmitter AC timing specifications

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Units
MII management clock						
t1	MDC low pulse width		200		—	ns
t2	MDC high pulse width		200		—	ns
t3	MDC period		400		—	ns
t4	MDIO(I) setup to MDC rising edge		10		—	ns
t5	MDIO(O) hold time from MDC rising edge		10		—	ns
t6	MDIO(O) valid from MDC rising edge		0		300	ns
100Base-TX transmitter						
Tjit	TDP-TDN differential output peak jitter				1.4	ns
T_{TLAT}	Transmit latency - Data on txp/txn after txen asserted			225		ns

Figure 10. MII receive timing

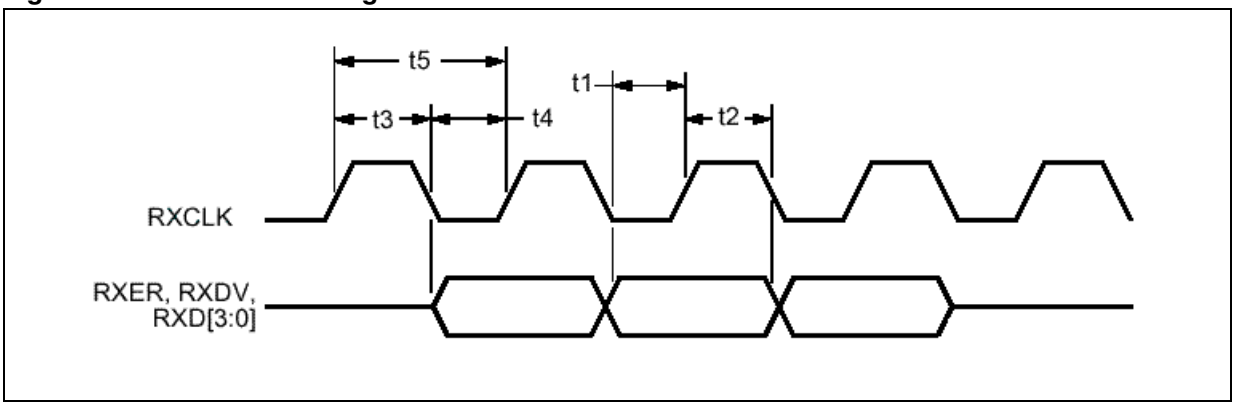


Table 36. MII receive and 100Base-TX AC timing specifications

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
MII receive						
t1	RX-ER, RX-DV, RXD[3:0] setup to RX-CLK		10		—	ns
t2	RX-ER, RX-DV, RXD[3:0] hold after RX-CLK		10		—	ns
t3	RX-CLK high pulse width (100 Mbits/s)		14		26	ns
	RX-CLK high pulse width (10 Mbits/s)			200		ns
t4	RX-CLK low pulse width (100 Mbits/s)		14		26	ns
	RX-CLK low pulse width (10 Mbits/s)			200		ns
t5	RX-CLK period (100 Mbits/s)			40		ns
	RX-CLK period (10 Mbits/s)			400		ns
100Base-TX receiver						
T_{RLAT}	Receive latency -RXDV asserted after valid data on rxp/rxn			225		ns

Figure 11. MII transmit timing

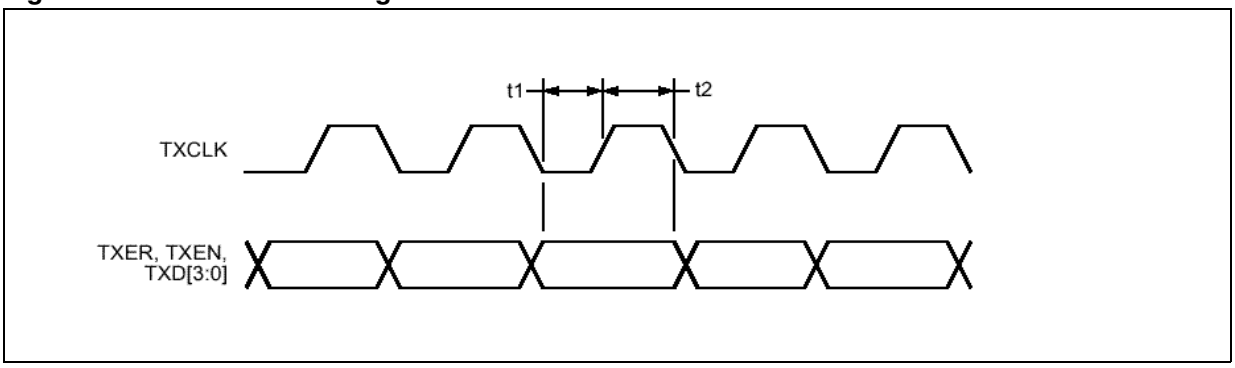


Table 37. MII transmit and 100Base-TX transmitter AC timing specifications

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
MII Transmit						
t1	TX-ER,TX-EN,TXD[3:0] Setup to TX-CLK Rise		10		—	ns
t2	TX-ER,TX-EN,TXD[3:0] Hold After TX-CLK Rise		0		25	ns
100Base-TX transmitter						
Tjit	TDP-TDN Differential Output Peak-to-Peak Jitter				1.4	ns
T_{TLAT}	Transmit latency - Data on txp/txn after txen asserted			225		ns

Table 38. RMII AC timing specifications

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
T_{SCLK}	SCLK Frequency			50		MHz
T_{SCLK}	SCLK Cycle Time			20		ns
Tsu	TXD[1:0], TX_EN, TX_ER Setup to SCLK rising edge		4			ns
T_{HOLD}	TXD[1:0], TX_EN, TX_ER Hold after SCLK rising edge		2			ns
T_{OUT}	RXD[1:0], CRSDV, RX_ER output delay from SCLK rising edge		2		16	ns
T_{RLAT}	Receive Latency -RXDV asserted after valid data on rxp/rxn			200		ns
T_{TLAT}	Transmit latency - Data on txp/txn after txen asserted			300		ns

Figure 12. RMII transmit timing

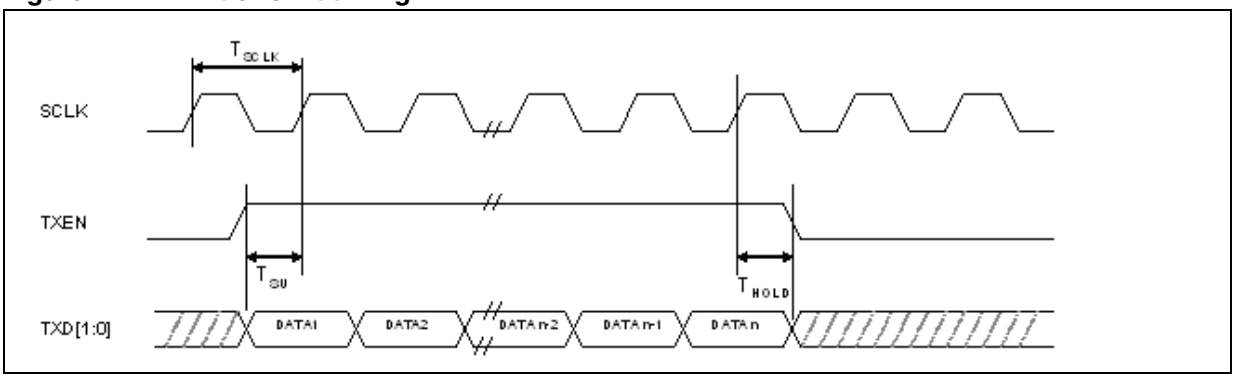


Figure 13. RMII receive timing

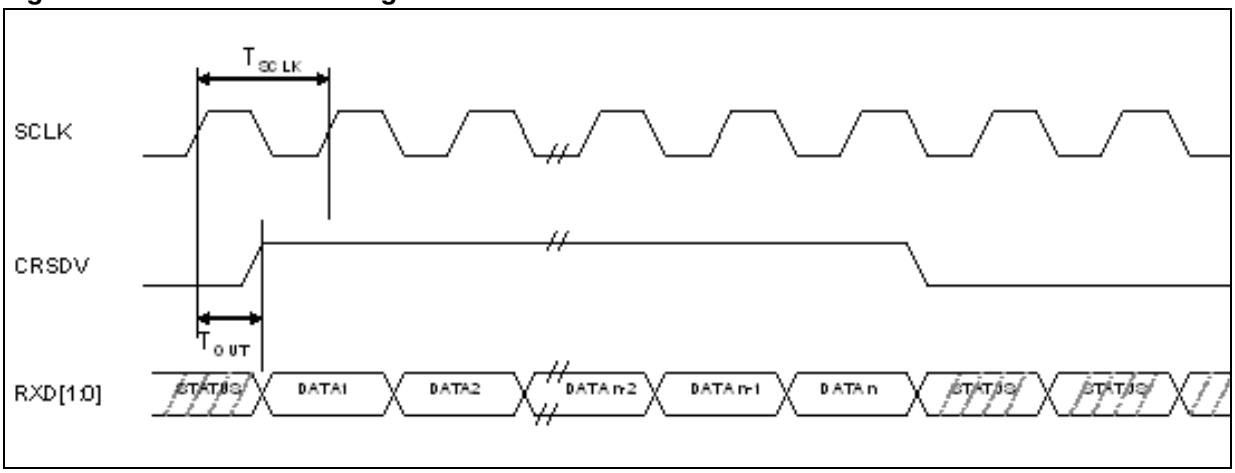


Table 39. SMII AC timing specifications(1)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
T_{SCLK}	SCLK Frequency			125		MHz
T_{SCLK}	SCLK Cycle Time			8		ns
Tsu	TXD0, SYNC Setup to SCLK rising edge		1.5			ns
T_{HOLD}	TXD0, SYNC Hold after SCLK rising edge		1			ns
T_{OUT}	RXD0 output delay from SCLK rising edge		1.5		5	ns
T_{RLAT}	Receive Latency - CRS after valid data on rxp/rxn			250		ns
T_{TLAT}	Transmit latency - Data on txp/txn after txs/syc			250		ns

1. The MAC should continuously generate a pulse on SYNC every 10 clocks.
Transmit and receive data and control information are provided in ten bit segments. In 10MBit mode, each segment is repeated ten times, so every ten segments represent a new byte of data. Therefore in receive mode the MAC can sample any one of every 10 segments in 10Mbps mode. However in transmit mode the MAC must repeat the data for each of the repeated 10 segments in 10Mbps mode.
In SMII mode, the TX_EN pin (54) is used as the SYNC pin for the SMII interface. SLCK is pin 32.
For SMII mode the configuration pin setting must be CF2 = 1, CFG1 = 0, CFG0 = 0

Figure 14. SMII transmit timing

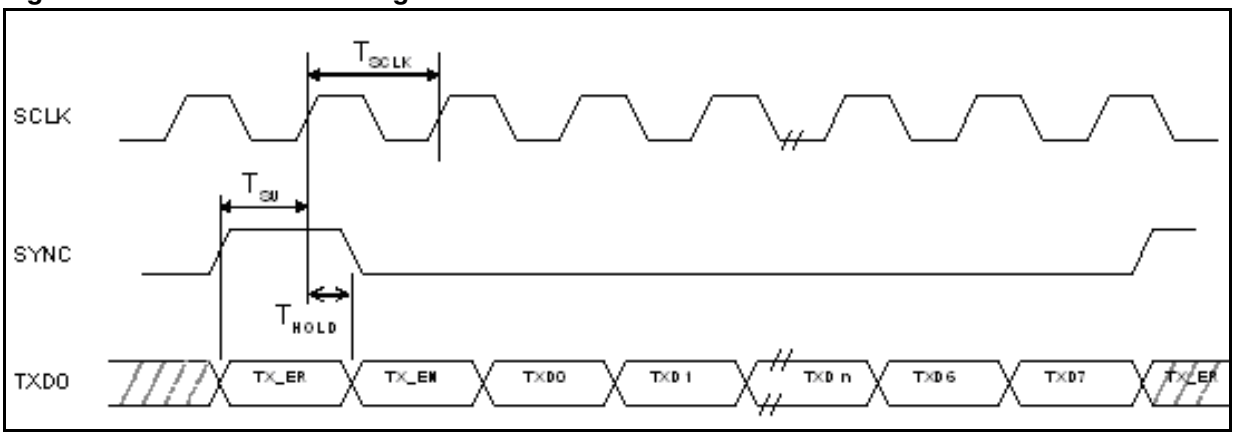
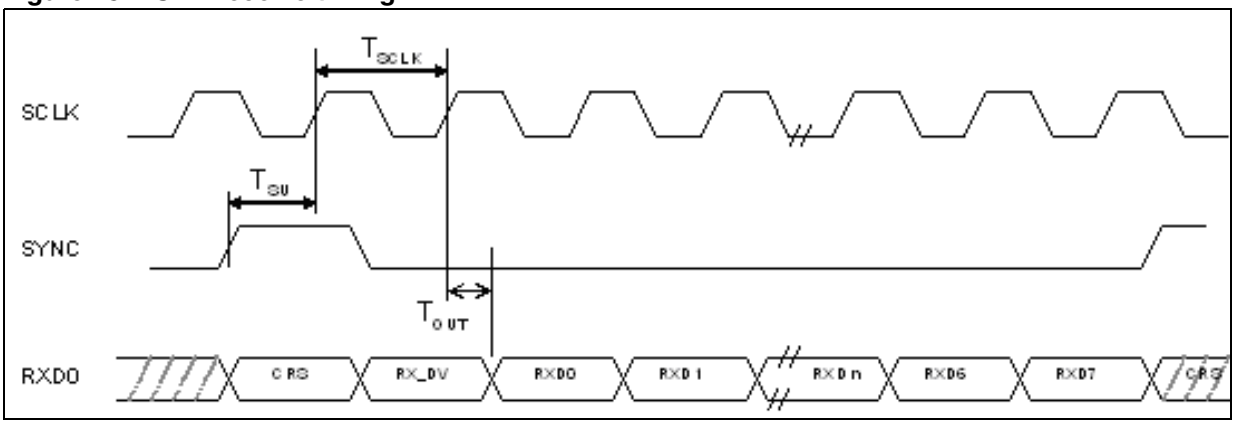


Figure 15. SMII receive timing



9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 16. TQFP 64 package mechanical drawing

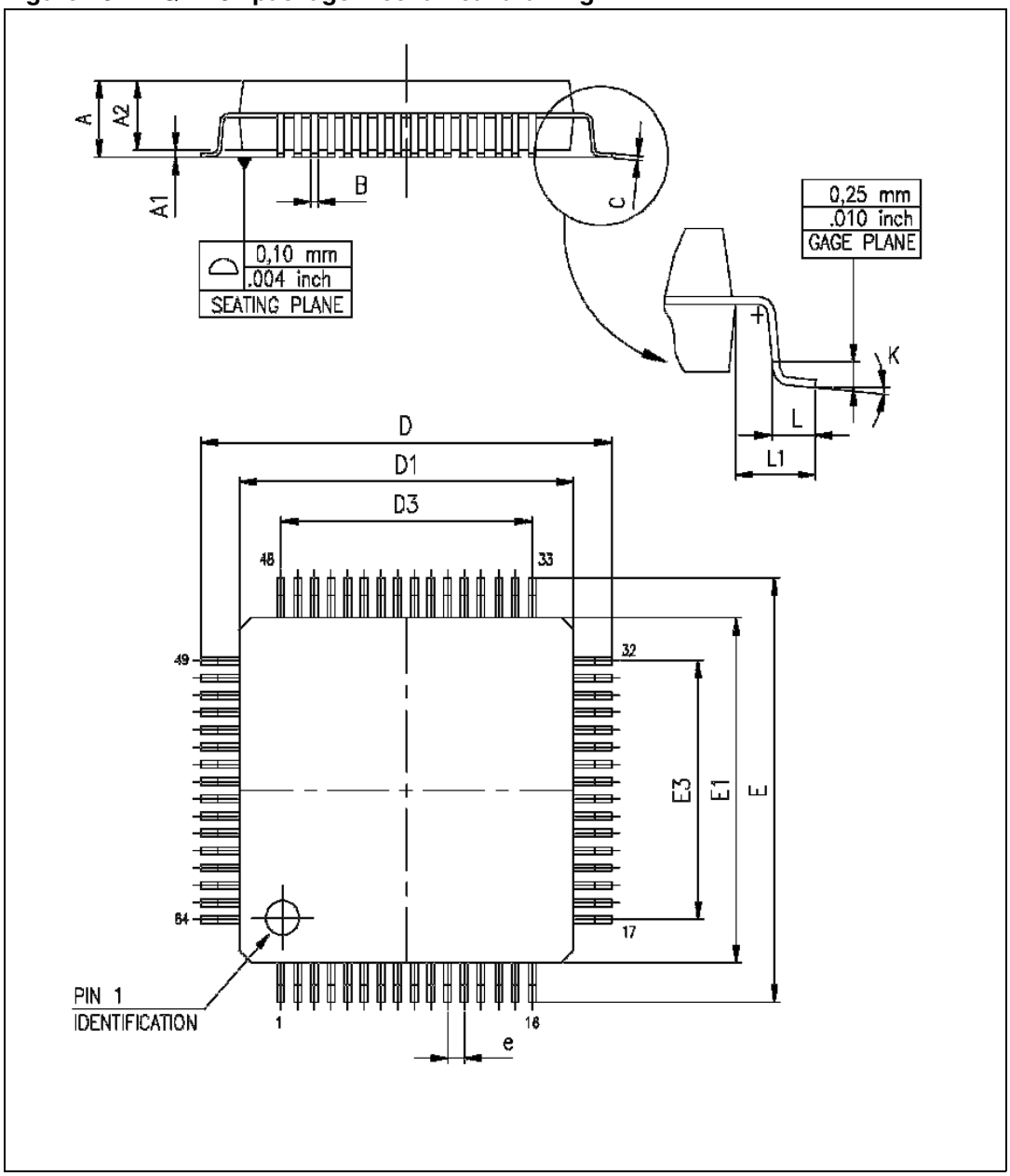


Table 40. TQFP 64L/Body 10 x 10 x 1.40 mm / footprint 1.00 mm

Reference	Dimensions (mm)			Dimensions (inch)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.420		1.540	0.056		0.061
A1	0.065	0.100	0.135	0.003	0.004	0.005
A2	1.360	1.400	1.440	0.054	0.055	0.057
B	0.175	0.200	0.225	0.007	0.008	0.009
c			0.165			0.006
D	11.90	12.00	12.10	0.469	0.472	0.476
D1	9.975	10.00	10.025	0.393	0.394	0.395
D3	7.450	7.500	7.550	0.293	0.295	0.297
e	0.450	0.500	0.550	0.018	0.020	0.022
E	11.90	12.00	12.10	0.469	0.472	0.476
E1	9.975	10.00	10.025	0.393	0.394	0.395
E3	7.450	7.500	7.550	0.293	0.295	0.297
L	0.450			0.018		
L1	0.938	1.000	1.063	0.037	0.039	0.042
K	1.5d	3.5d	5.5d	1.5d	3.5d	5.5d

10 Ordering information

Table 41. Order codes

Part number	Temp range, °C	Package	Packing
E-STE101P(1)	-40 to 85	TQFP64 (14x14x1.4mm)	Tube

1. E-: ECOPACK®

11 Revision history

Table 42. Document revision history

Date	Revision	Changes
15-Sep-2006	1	Initial release.

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