

# NTD2955

## Power MOSFET

### -60 V, -12 A, P-Channel DPAK

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. Designed for low-voltage, high-speed switching applications in power supplies, converters, and power motor controls. These devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer an additional safety margin against unexpected voltage transients.

#### Features

- Avalanche Energy Specified
- $I_{DSS}$  and  $V_{DS(on)}$  Specified at Elevated Temperature
- Designed for Low-Voltage, High-Speed Switching Applications and to Withstand High Energy in the Avalanche and Commutation Modes
- Pb-Free Packages are Available

#### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	-60	Vdc
Gate-to-Source Voltage	$V_{GS}$	$\pm 20$	Vdc
- Continuous	$V_{GSM}$	$\pm 25$	Vpk
- Non-repetitive ( $t_p \leq 10$ ms)			
Drain Current	$I_D$	-12	Adc
- Continuous @ $T_a = 25^\circ\text{C}$	$I_{DM}$	-36	Apk
- Single Pulse ( $t_p \leq 10$ ms)			
Total Power Dissipation @ $T_a = 25^\circ\text{C}$	$P_D$	55	W
Operating and Storage Temperature Range	$T_J, T_{stg}$	-55 to 175	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy - Starting $T_J = 25^\circ\text{C}$ ( $V_{DD} = 25$ Vdc, $V_{GS} = 10$ Vdc, Peak $I_L = 12$ Apk, $L = 3.0$ mH, $R_G = 25$ $\Omega$ )	$E_{AS}$	216	mJ
Thermal Resistance	$R_{\theta JC}$	2.73	$^\circ\text{C/W}$
- Junction-to-Case	$R_{\theta JA}$	71.4	
- Junction-to-Ambient (Note 1)	$R_{\theta JA}$	100	
- Junction-to-Ambient (Note 2)			
Maximum Lead Temperature for Soldering Purposes, 1/8 in. from case for 10 seconds	$T_L$	260	$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

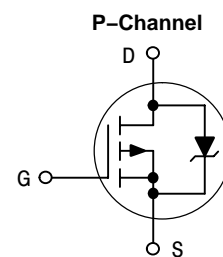
1. When surface mounted to an FR4 board using 1 in pad size (Cu area = 1.127 in<sup>2</sup>).
2. When surface mounted to an FR4 board using the minimum recommended pad size (Cu area = 0.412 in<sup>2</sup>).



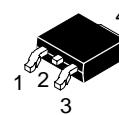
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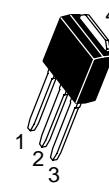
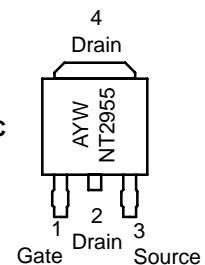
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	$I_D$ MAX
-60 V	155 m $\Omega$ @ -10 V, 6 A	-12 A



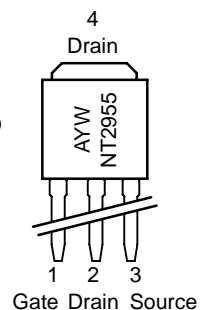
#### MARKING DIAGRAMS



**DPAK  
CASE 369C  
STYLE 2**



**DPAK-3  
CASE 369D  
STYLE 2**



NT2955 Device Code  
A = Assembly Location  
Y = Year  
W = Work Week

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

**ELECTRICAL CHARACTERISTICS** ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Drain-to-Source Breakdown Voltage (Note 3) ( $V_{GS} = 0\text{ Vdc}$ , $I_D = -0.25\text{ mA}$ ) (Positive Temperature Coefficient)	$V_{(BR)DSS}$	-60 -	- 67	- -	Vdc mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current ( $V_{GS} = 0\text{ Vdc}$ , $V_{DS} = -60\text{ Vdc}$ , $T_J = 25^\circ\text{C}$ ) ( $V_{GS} = 0\text{ Vdc}$ , $V_{DS} = -60\text{ Vdc}$ , $T_J = 150^\circ\text{C}$ )	$I_{DSS}$	- -	- -	-10 -100	$\mu\text{Adc}$
Gate-Body Leakage Current ( $V_{GS} = \pm 20\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )	$I_{GSS}$	-	-	-100	nAdc

**ON CHARACTERISTICS** (Note 3)

Gate Threshold Voltage ( $V_{DS} = V_{GS}$ , $I_D = -250\ \mu\text{Adc}$ ) (Negative Temperature Coefficient)	$V_{GS(th)}$	-2.0 -	-2.8 4.5	-4.0 -	Vdc mV/ $^\circ\text{C}$
Static Drain-Source On-State Resistance ( $V_{GS} = -10\text{ Vdc}$ , $I_D = -6.0\text{ Adc}$ )	$R_{DS(on)}$	-	0.155	0.180	$\Omega$
Drain-to-Source On-Voltage ( $V_{GS} = -10\text{ Vdc}$ , $I_D = -12\text{ Adc}$ ) ( $V_{GS} = -10\text{ Vdc}$ , $I_D = -6.0\text{ Adc}$ , $T_J = 150^\circ\text{C}$ )	$V_{DS(on)}$		-1.86 -	-2.6 -2.0	Vdc
Forward Transconductance ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 6.0\text{ Adc}$ )	gFS		8.0	-	Mhos

**DYNAMIC CHARACTERISTICS**

Input Capacitance	$(V_{DS} = -25\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ , $F = 1.0\text{ MHz}$ )	$C_{iss}$	-	500	750	pF
Output Capacitance		$C_{oss}$	-	150	250	
Reverse Transfer Capacitance		$C_{rss}$	-	50	100	

**SWITCHING CHARACTERISTICS** (Notes 3 and 4)

Turn-On Delay Time	$(V_{DD} = -30\text{ Vdc}$ , $I_D = -12\text{ A}$ , $V_{GS} = -10\text{ V}$ , $R_G = 9.1\ \Omega$ )	$t_{d(on)}$	-	10	20	ns
Rise Time		$t_r$	-	45	85	
Turn-Off Delay Time		$t_{d(off)}$	-	26	40	
Fall Time		$t_f$	-	48	90	
Gate Charge	$(V_{DS} = -48\text{ Vdc}$ , $V_{GS} = -10\text{ Vdc}$ , $I_D = -12\text{ A}$ )	$Q_T$	-	15	30	nC
		$Q_{GS}$	-	4.0	-	
		$Q_{GD}$	-	7.0	-	

**DRAIN-SOURCE DIODE CHARACTERISTICS** (Note 3)

Diode Forward On-Voltage ( $I_S = 12\text{ Adc}$ , $V_{GS} = 0\text{ V}$ ) ( $I_S = 12\text{ Adc}$ , $V_{GS} = 0\text{ V}$ , $T_J = 150^\circ\text{C}$ )	$V_{SD}$	- -	-1.6 -1.3	-2.5 -	Vdc
Reverse Recovery Time ( $I_S = 12\text{ A}$ , $dI_S/dt = 100\text{ A}/\mu\text{s}$ , $V_{GS} = 0\text{ V}$ )	$t_{rr}$	-	50		ns
	$t_a$	-	40	-	
	$t_b$	-	10	-	
Reverse Recovery Stored Charge	$Q_{RR}$	-	0.10	-	$\mu\text{C}$

3. Indicates Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

4. Switching characteristics are independent of operating junction temperature.

TYPICAL PERFORMANCE CURVES ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

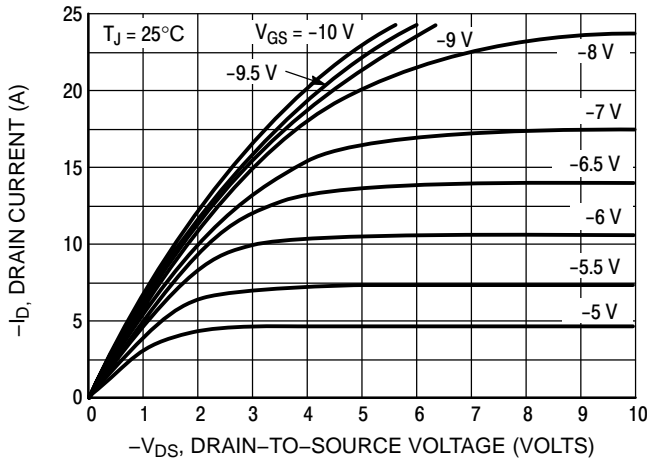


Figure 1. On-Region Characteristics

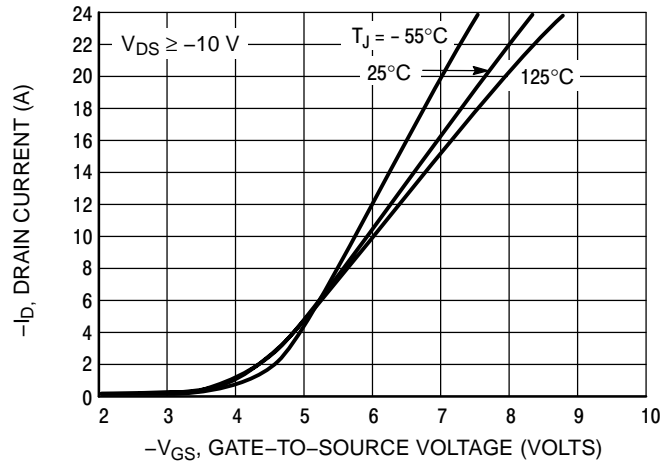


Figure 2. Transfer Characteristics

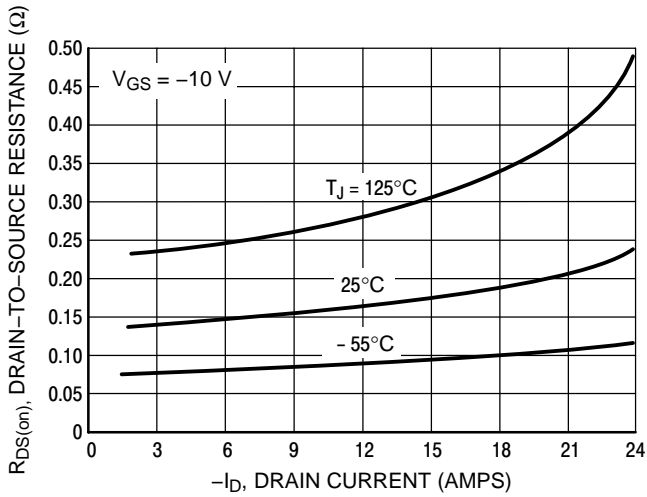


Figure 3. On-Resistance versus Drain Current and Temperature

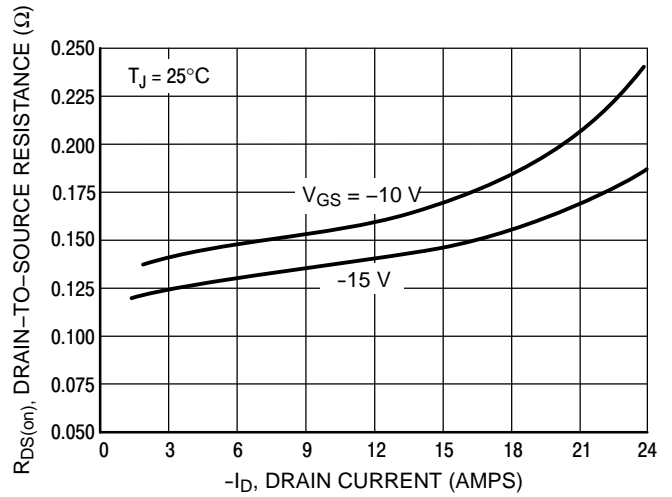


Figure 4. On-Resistance versus Drain Current and Gate Voltage

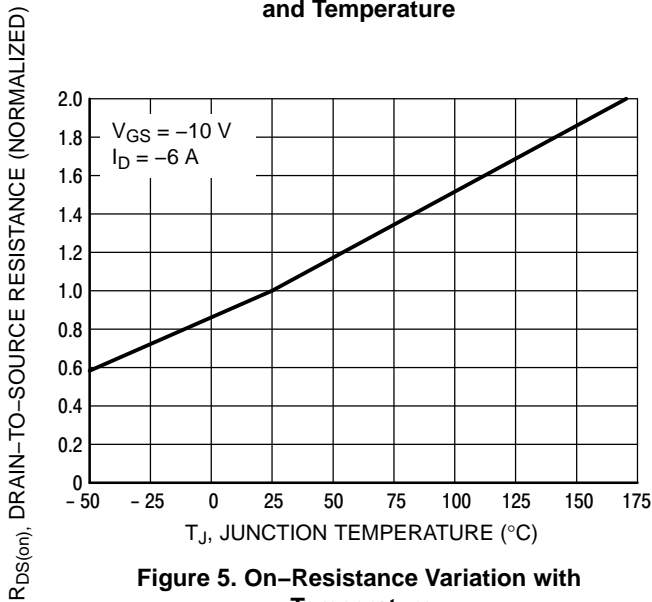


Figure 5. On-Resistance Variation with Temperature

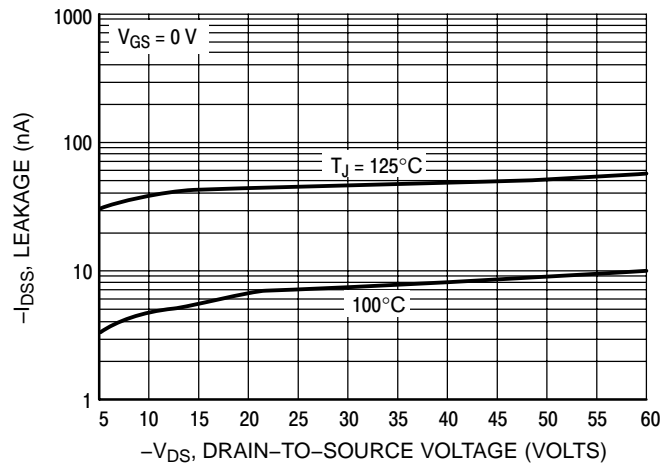


Figure 6. Drain-To-Source Leakage Current versus Voltage

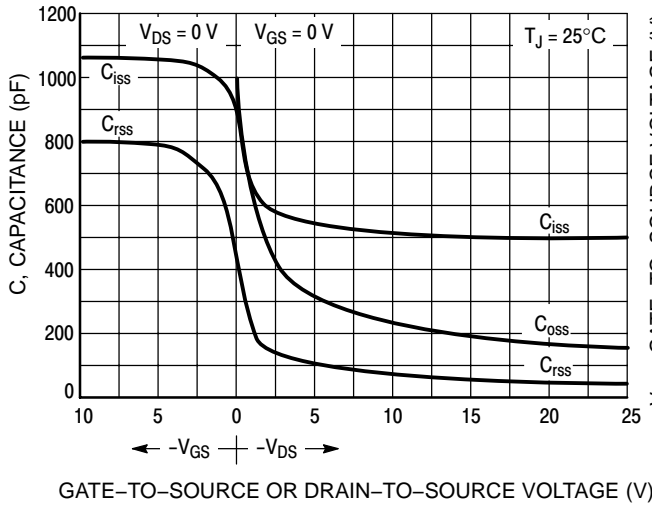


Figure 7. Capacitance Variation

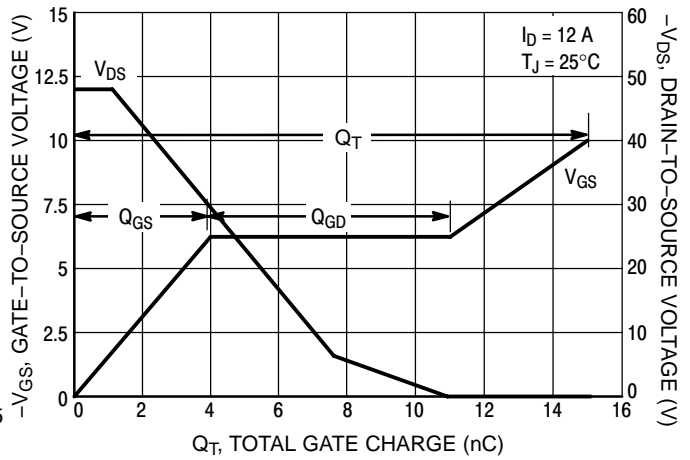


Figure 8. Gate-To-Source and Drain-To-Source Voltage versus Total Charge

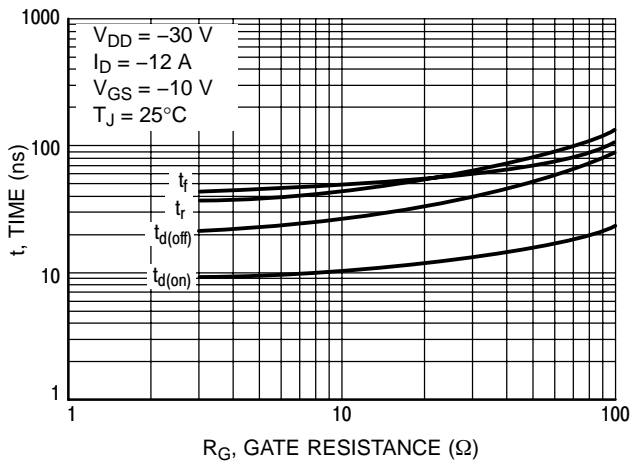


Figure 9. Resistive Switching Time Variation versus Gate Resistance

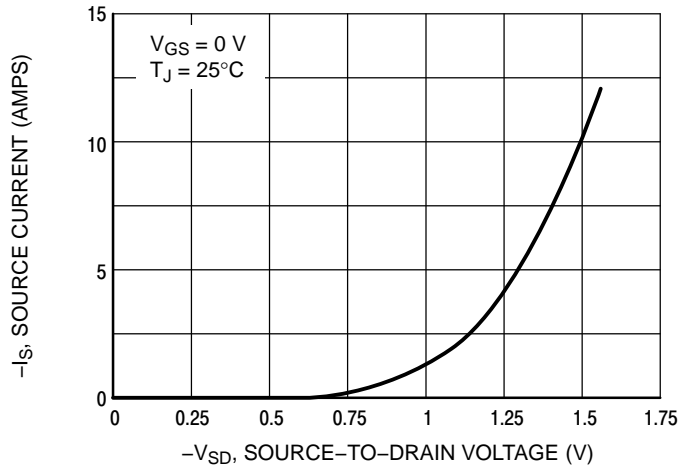


Figure 10. Diode Forward Voltage versus Current

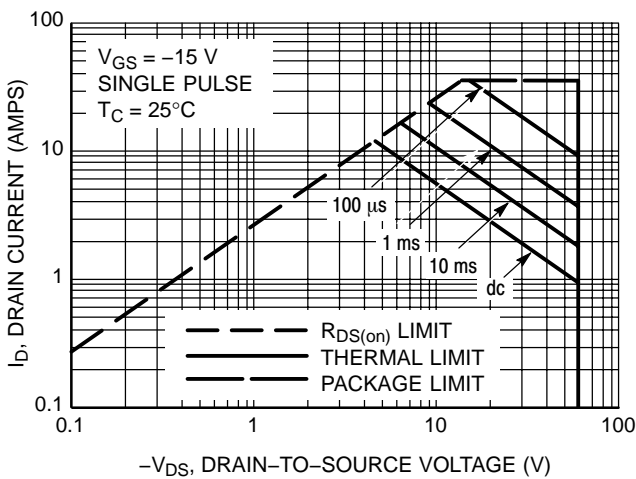


Figure 11. Maximum Rated Forward Biased Safe Operating Area

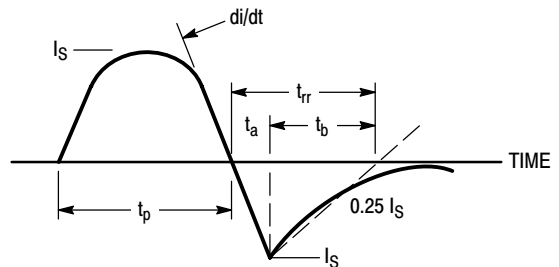


Figure 12. Diode Reverse Recovery Waveform

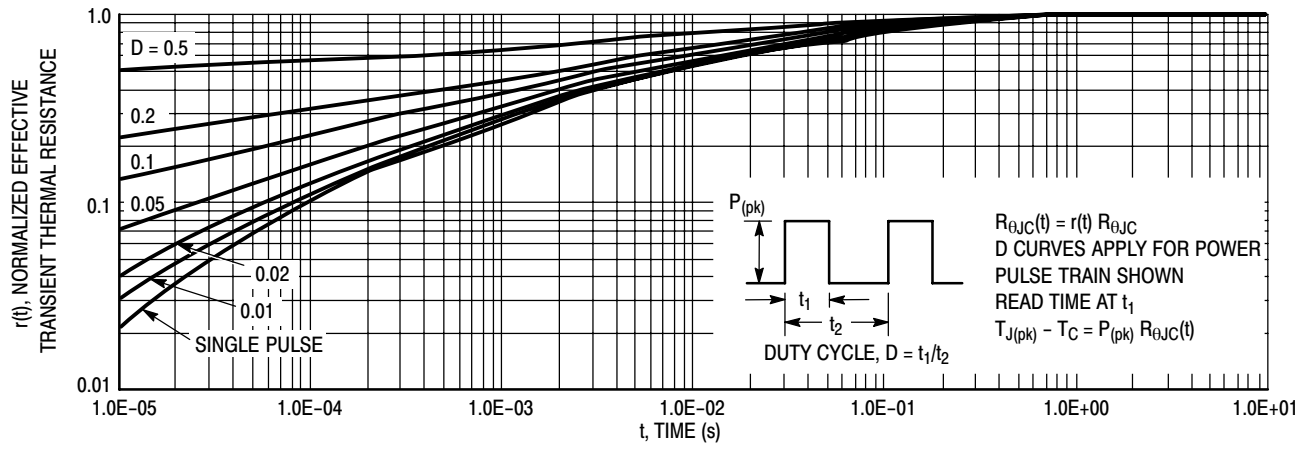


Figure 13. Thermal Response

**ORDERING INFORMATION**

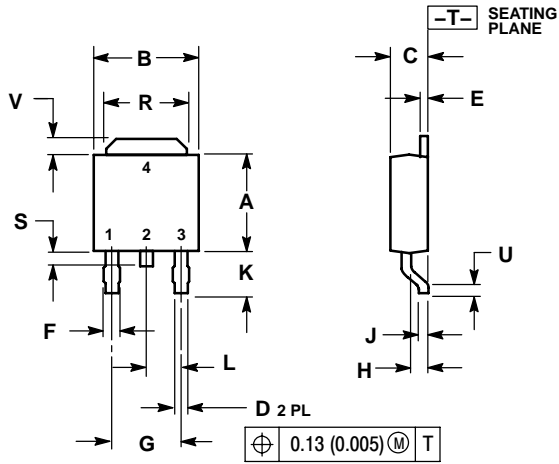
<b>Device</b>	<b>Package</b>	<b>Shipping†</b>
NTD2955	DPAK	75 Units / Rail
NTD2955G	DPAK (Pb-Free)	
NTD2955-001	DPAK-3	75 Units / Rail
NTD2955-1G	DPAK-3 (Pb-Free)	
NTD2955T4	DPAK	2500 / Tape & Reel
NTD2955T4G	DPAK (Pb-Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NTD2955

## PACKAGE DIMENSIONS

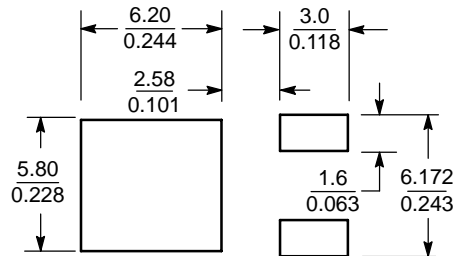
DPAK  
CASE 369C-01  
ISSUE O



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

STYLE 2:  
PIN 1. GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN

### SOLDERING FOOTPRINT\*



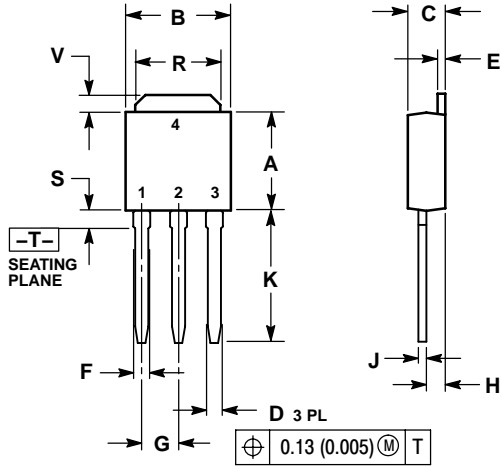
SCALE 3:1  $\left( \frac{\text{mm}}{\text{inches}} \right)$

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NTD2955

## PACKAGE DIMENSIONS

DPAK-3  
CASE 369D-01  
ISSUE B



NOTES:

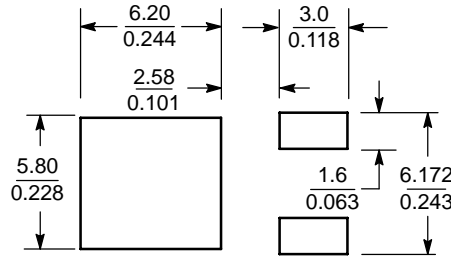
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

STYLE 2:

- PIN 1. GATE
- DRAIN
- SOURCE
- DRAIN

### SOLDERING FOOTPRINT\*



SCALE 3:1 (mm/inches)

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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