FAIRCHILD
A Schlumberger Company

F3851/F3856
Program Storage Unit

Microprocessor Product

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Description

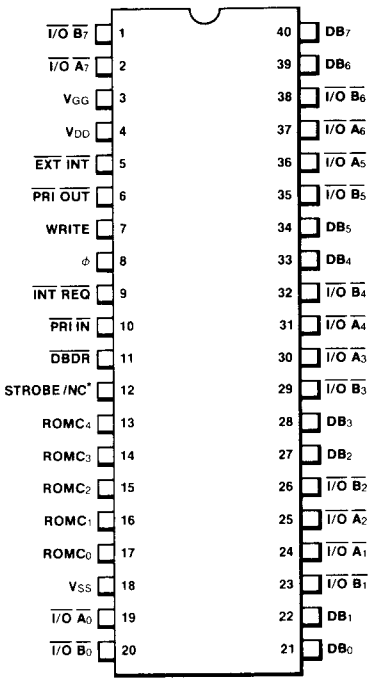
The Fairchild F3851 and F3856 are the principal program storage devices for the F8 microcomputer system. The F3851 provides 1024 bytes of ROM; the F3856 provides 2048 bytes. The program storage unit (PSU) is customized with programs and permanent data tables, which are specified as ROM masks.

The PSU devices have two 8-bit, bidirectional I/O ports, interrupt logic, a programmable timer, and a pulse width measurement circuit. They also contain memory addressing logic with data counters and program counters. The interrupt logic responds to requests from an external device and internally from the timer. The pulse width measurement circuit (F3856) is a combination of these two capabilities.

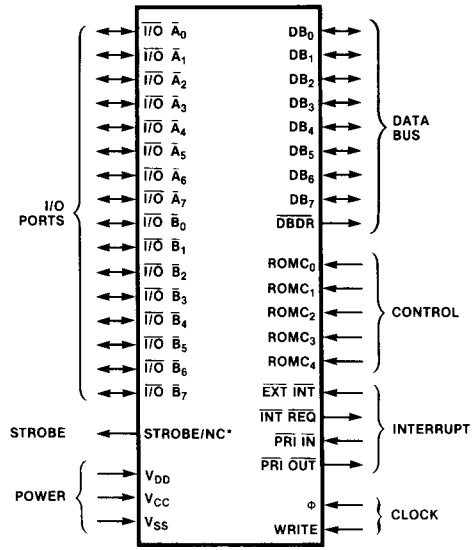
The PSU devices are manufactured using N-channel, isoplanar MOS technology; therefore, power dissipation is very low, typically less than 275 mW.

- **1024/2048 Bytes of Program Storage**
- **Internal Memory Addressing Logic**
- **16 Bidirectional, Individually Controlled I/O Lines, Organized as Two 8-Bit Ports**
- **Programmable Timer (F3856) — Preset, Start, Stop, and Read-Back Ability; Four Selectable Timer Count Rates, and Pulse Width Measurement**
- **Full Interrupt Level — Daisy-Chain Expandable, Independent Interrupt Address Vectors for Timer and External Interrupt**
- **2 MHz Operation**
- **TTL and LSTTL Compatible**
- **Low Power Dissipation, Typically Less Than 275 mW**
- **+5 V and +12 V Power Supplies**

Connection Diagram



Signal Functions



*NC for F3851 only.

Device Organization

The PSU is more than a read-only memory unit: every memory device within the F8 system contains its own memory addressing logic along with associated address registers. Refer to figure 1 for a simplified block diagram of the PSU. A single 8-bit data bus provides all necessary communication between a PSU (or any other memory device) and an F3850 CPU.

The PSU has an elementary arithmetic unit that can increment and add 16-bit data units; for memory addressing logic, these two operations are sufficient. The PSU is functionally illustrated in figure 2. These devices also contain a control unit that decodes the five read-only memory control (ROMC) lines, generated by the CPU, as though they were a 5-bit instruction code. Similar to the CPU, the PSU generates internal signals to control data flow and arithmetic logic within itself. One control output, data bus drive (DBDR), is generated to coincide with data being output by the PSU.

System Clock Timing

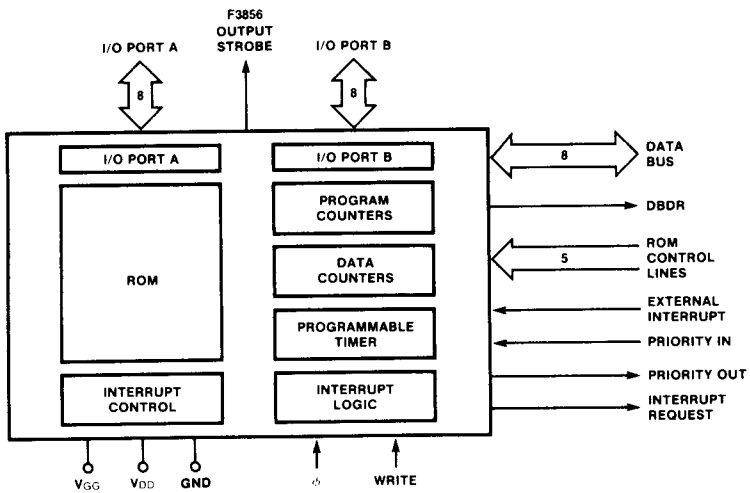
All timing within the F3851/F3856 PSU is controlled by the ϕ and WRITE signals, which are generated from the F3850 CPU. Refer to the F3850 data sheet for a description of these clock signals, The WRITE clock refreshes and updates PSU address registers, which are dynamic. The ϕ clock drives sequencing logic to precharge the ROM matrix; it also drives the programmable timer.

I/O Ports

The unit contains four preassigned I/O port addresses: the two lowest are assigned to I/O ports A and B and are used to transfer data to and from external devices. The other two I/O addresses are assigned to the programmable timer and the interrupt control register and are treated as I/O ports. Associated with the I/O ports is an I/O port address select register (ASR). This is a 6-bit register for the F3851 and a 5-bit register for the F3856. The contents are a mask option, which must be specified at the time the PSU is created. The ports are addressed as follows:

XXXXXX00	I/O port A
XXXXXX01	I/O port B
XXXXXX10	Interrupt control register
XXXXXX11	Programmable timer

Figure 1 PSU Simplified Block Diagram



For example, if the six binary digits are 000010, the four I/O port addresses are H'08', H'09', H'0A', and H'0B'.

When a logic 1 is output to I/O port A or B, it places a 0 V level on the output pin. This same inverted logic applies to input.

The F3851 I/O ports, timer, and interrupt control register are not initialized during the power-on reset cycle. The F3856 I/O ports and interrupt control register are initialized during both the power-on or external reset cycle; the timer register is not initialized during power-on or external reset cycles.

ROM Addressing

The F3851 8K PSU has 1024 bytes of read-only memory; the F3856 16K PSU has 2048 bytes. This ROM array may contain object program code and/or tables of nonvarying data. Every PSU is implemented using a custom mask that specifies the state of every ROM bit and certain address mask options that are external to the ROM array.

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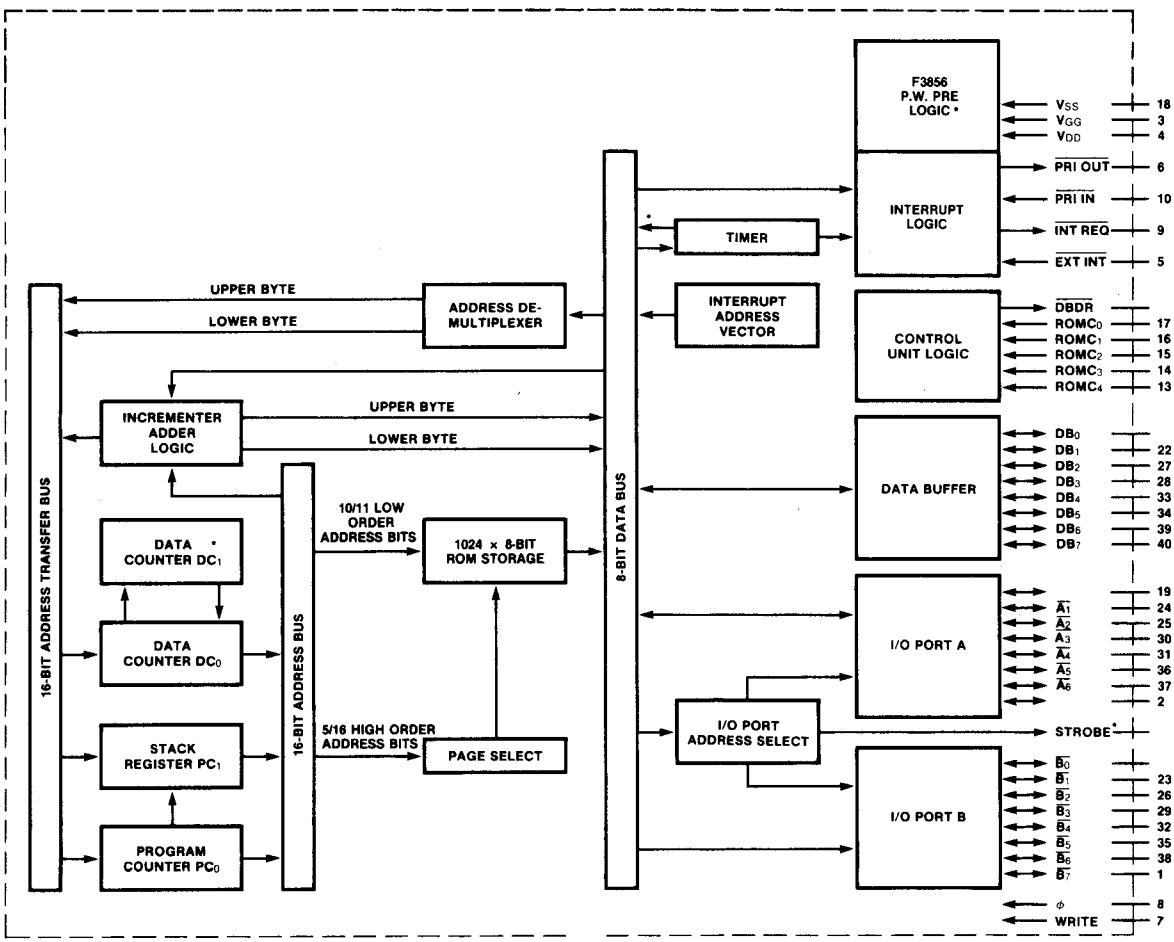
Figure 2 PSU Functional Diagram



The ROM addressing logic consists of 16-bit registers: program counter PC_0, stack register PC_1, and data counter DC_0. Data counter DC_1 is provided on the F3856 as an additional buffer for DC_0.

A 6-bit page select register and 10-bit address select register provide decode logic for the F3851. The F3856 uses a 5-bit page select register and an 11-bit address select register.

Program Counter, Data Counter, and Stack Registers
Program counter PC_0 always addresses the memory location out of which the next program instruction byte is read. If the instruction requires data (i.e., an operand) to be accessed, data counter DC_0 must address memory for this purpose; PC_0 cannot be used to address data, since it is saving the address of the next instruction code. By using the exchange DC instruction in the F3856 program, the two data counter contents of DC_0 and DC_1 can be exchanged.

The provision of two address registers, PC_0 and DC_0, is a convenience to the F3850 CPU and is not a necessary part of the memory addressing logic sequence within a PSU. Address decoding is identical, whether originating in PC_0 or DC_0.

The PC_0, PC_1, and DC_0 are loaded from two consecutive single-byte inputs on the data bus; PC_1 and DC_0 are transmitted as two single-byte outputs on the data bus. The contents of DC_0 and DC_1 of F3856 can be exchanged in one instruction.

Stack register PC_1 is a buffer for program counter PC_0; the contents of PC_1 are never used directly to address memory. When an interrupt is acknowledged, the contents of PC_0 are saved in PC_1.

Page Select and Address Select Registers
All memory addresses are 16 bits wide, whether originating in the program counter or in the data counter. Address decode logic within the PSU separates the 16-bit address into two portions: the low order addresses the ROM storage bytes; the high order addresses the page.

	High-Order Byte Address	Low-Order Page Address
F3851	1024 Byte Select 6 Bits	64 Page Options 10 Bits
F3856	2048 Byte Select 5 Bits	32 Page Options 11 Bits

If the high-order bits of the address coincide exactly with the page select mask, an enable signal is generated, causing the PSU logic to respond to a memory access request. If the high-order bits of the address do not coincide exactly with the page select, no enabling signal is generated and the PSU does not respond to memory access requests.

The page select register identifies the memory addressing space of the individual PSU device. Each of the 32 (or 64) page select options allowed by the 5-bit (or 6-bit) page select register identifies a single address space consisting of 2048 (or 1024) continguous memory addresses.

Incrementer Adder Logic
There are only two arithmetic operations that memory devices need to perform on the contents of memory address registers:

1. Increment by 1 the 16-bit value stored in address PC_0 or DC_0.

2. Add an 8-bit value, treated as a signed binary number (subject to twos complement arithmetic) to the 16-bit value stored in an address register. If the 8-bit value is being treated as a signed binary number, the high-order bit of the 8-bit value is the sign bit; the sign bit must be propagated through the missing high-order eight bits.

The PSU control unit implements the incrementer adder logic through control signals internal to PSU device logic.

Addressing Consistency in Multiple Memory Devices
When an ROMC state specifies a memory access, only one memory device responds to the memory access operation itself. However, every memory device responds to ROMC states that call for modifying the contents of a program counter or data counter register. Providing every memory device that is connected to the 8-bit data bus of an F3850 CPU is also connected to the ROMC control lines of the same CPU, address contentions cannot arise. Every memory device simultaneously receives the same ROMC state signals from the CPU; every memory device responds to ROMC states by identically modifying the contents of memory address registers, if such modifications are specified. Therefore, every PC_0 register on every memory device always contains identical information; the same is true for DC_0 and PC_1 registers.

Only one memory device (the one whose address space includes the specified memory address) actually responds to any memory access request. To avoid addressing conflicts, it is only necessary to ensure that the following conditions exist:

Signal Descriptions
The PSU input and output signals are described in table 1.

Table 1 PSU Signal Descriptions

Mnemonic	Pin No.	Name	Description
Clock			
ϕ	8	Clock	The two clock input signals that originate at the F3850 CPU.
WRITE	7		
I/O Ports			
$\overline{I/O\ A_0}$-$\overline{I/O\ A_7}$	19, 24, 25, 30, 31, 36, 37, 2	I/O Ports A	Bidirectional ports through which the PIO communicates with logic external to the microprocessor system.
$\overline{I/O\ B_0}$-$\overline{I/O\ B_7}$	20, 23, 26, 29, 31, 35, 38, 1	I/O Ports B	
Control			
$ROMC_0$-$ROMC_4$	17, 16, 15, 14, 13	Read-Only Memory Control	Input signals that originate at the F3850 CPU control internal functions of the PSU.
Data Bus			
DB_0-DB_7	21, 22, 27, 28, 33, 34, 39, 40	Data Bus	Bidirectional 3-state lines that link the PSU to all other devices within the microprocessor system.
$\overline{DBDR}$	11	Data Bus Drive	A low output, open-drain signal that indicates the data bus currently contains data flowing from the PSU.
Strobe			
STROBE	12	Strobe	This output signal provides a positive pulse whenI/O port A is being read by an input instruction or is being updated by an output instruction (F3856).
Interrupt			
$\overline{EXT\ INT}$	5	External Interrupt	A high-to-low transition on this input signal is interpreted as an interrupt request from an external device.
$\overline{INT\ REQ}$	9	Interrupt Request	This output signal is the $\overline{INT\ REQ}$ input to the F3850 CPU; it must be output low to interrupt the CPU, which occurs only if $\overline{PRI\ IN}$ is low and PSU interrupt control logic is requesting an interrupt.
$\overline{PRI\ IN}$	10	Priority In	Unless this input signal is low, the PSU does not set the $\overline{INT\ REQ}$ signal low in response to an interrupt.
$\overline{PRI\ OUT}$	6	Priority Out	This output signal becomes the $\overline{PRI\ IN}$ signal to the next device in the interrupt-priority daisy chain; it is output high unless the $\overline{PRI\ IN}$ signal is entering the PSU low and the PSU is not requesting an interrupt
Power			
V_{DD}	4	Power Supply	+5 V ±5%
V_{GG}	3	Power Supply	+12 V ±5%
V_{SS}	18	Ground	System ground — 0 V; V_{DD} and V_{GG} are referenced to V_{SS}.

1. All memory devices must receive the same ROMC state signals from one CPU and must contain identical information.

2. Page select masks must not be duplicated—more than one memory device cannot have the same memory space.

3. The memory address contained in the specified register (PC_0 or DC_0) must be within the memory space of at least one memory device.

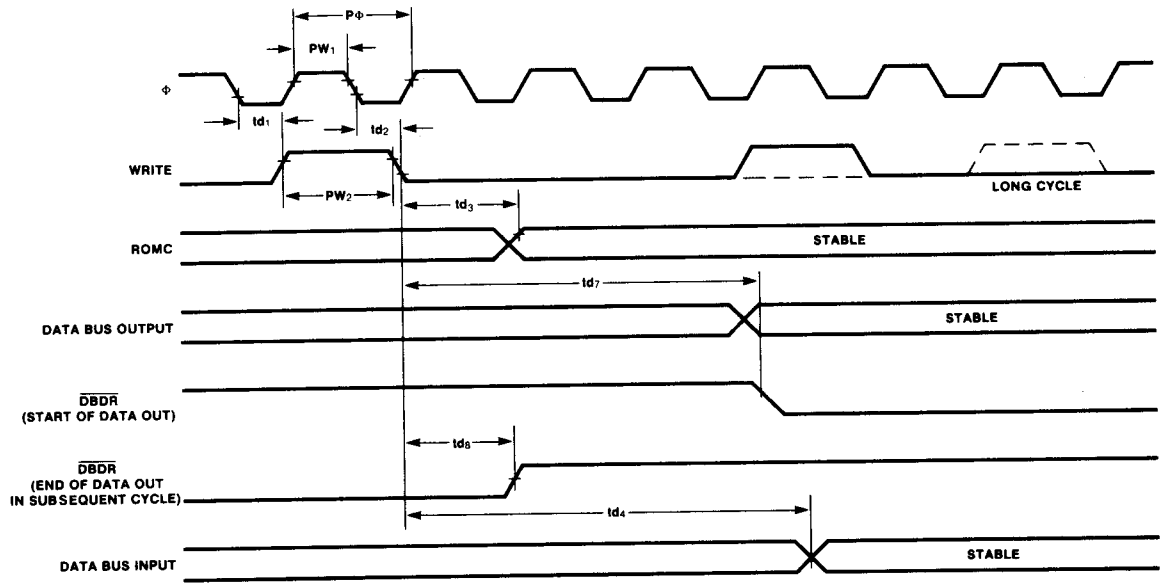
ROMC States
Table 2 lists the data bus contents as a function of ROMC states.

Instruction Execution

The PSU responds to signals that are output by the F3850 CPU in the course of implementing instruction cycles. Refer to table 2 for a summary of the data bus response to the ROMC states generated by the CPU.

Data Output by the PSU
Figure 3 provides timing when the PSU outputs data on the

Figure 3 Data Bus Timing



data bus. This timing applies whenever a PSU is the data source. The PSU places data on the data bus, even in the worst case, in time for the setup required by any F3850 CPU destination (refer to the F3850 CPU data sheet).

Table 2 Data Bus Contents as a Function of the ROMC State

ROMC State (Hex)	If F3851/F3856 PSU is the Source*		If F3850 CPU is the Source
	Description of Data	Address**	Description of Data
00	Instruction	PC_0	
01	Offset for branch	PC_0	
02	Operand	DC_0	
03	Operand	PC_0	
04			
05			Byte to be stored
06	Upper byte, DC_0		
07	Upper byte, PC_1		
08			= 00 for PC_0
09	Lower byte, DC_0		
0A			Offset for DC_0
0B	Lower byte, PC_1		
0C	Byte for PC_0, lower	PC_0	
0D			
0E	Byte for DC_0, lower	PC_0	
0F	Lower byte of interrupt vector if it is source of the interrupt		
10			
11	Byte for DC_0, upper	PC_0	
12			Byte for PC_0, lower
13	Upper byte of interrupt vector if it is source of the interrupt		
14			Byte for PC_0, upper
15			Byte for PC_1, upper
16			Byte for DC_0, upper
17			Byte for PC_0, lower
18			Byte for PC_1, lower
19			Byte for DC_0, lower
1A			Byte for selected I/O port
1B	Byte from I/O register, if selected		
1C			(Note 1)
1D			
1E	Lower byte, PC_0		
1F	Upper byte, PC_0		

*Only drives the data bus within the segment of address space that belongs to the PSU.
**An entry in this column specifies the register from which a memory address was obtained.

Note 1
During INS or OUTS instruction for port 0 or 1: I/O byte
During INS or OUTS instruction for port 4-F: I/O address
During all other instructions, F3850 does not drive.

The data bus drive signal ($\overline{DBDR}$) is low, while data output by the PSU is stable on the data bus. Thus, a $\overline{DBDR}$ low signal indicates that the data bus currently contains data flowing from a PSU. For systems with more than one PSU, the $\overline{DBDR}$ outputs can be wire-ORed and the result used as a bus data flow direction indicator. The $\overline{DBDR}$ signal remains low until timing delay td_8 into the instruction cycle following the one in which $\overline{DBDR}$ was set low.

Data Input to the PSU

When the PSU receives data off the data bus, in the worst case, the data must be added to a 16-bit number within the PSU adder/incrementer. This worst case corresponds to data coming from the accumulator of the CPU for an ADC instruction or from a memory device for a BR instruction. For this worst case, arriving data must allow sufficient time for 16-bit adder logic (time delay td_4 in figure 3 identifies this worst-case timing).

PSU Input/Output Interfacing

The I/O ports with addresses XXXXXX00 and XXXXXX01 (XXXXXX is the 6-bit I/O port address select) are used to transmit data between the PSU and external devices. The IN and INS instructions cause data at the I/O ports to be transmitted to the CPU; the OUT and OUTS instructions cause data in the CPU accumulator to be loaded into an I/O port. Each I/O pin has an output latch that holds the pin DC data.

Input and output operations using the two PSU I/O ports execute in three instruction cycles. During the first cycle, the port address is transmitted to the data bus. During the second cycle, data is either sent from the accumulator to the I/O latch or enabled from the I/O pin to the accumulator, depending on whether the instruction is an output or an input. At the falling edge of the WRITE signal (marking the end of the second cycle and beginning of the third cycle), the data is strobed into either the latch (OUTS) or the accumulator (INS), respectively. The third cycle is then used by the CPU for its next instruction fetch.

I/O Port Options

Data bus timing associated with the execution of I/O instructions does not differ from data bus timing associated with any other data transfer to or from the PSU. However, timing at the I/O port itself depends on which port option is being used. Figures 4, 5, and 6 illustrate the three port options; figure 7 illustrates timing for the three cases.

Standard Pull-Up Configuration (Figure 4)— All I/O port bits should be set for a high level, before data input, to prevent incoming logic 0s from being masked by logic 1s preset at the port from previous outputs. In some instances, the ability to mask bits of a port to logic 1 is useful. (Note that logic 1 becomes a 0 V electrical level at the I/O pin; logic 0 corresponds to a high electrical level.)

Each I/O port pin is a wire-AND structure between an internal latch and an external signal, if any. The latch is always loaded directly from the accumulator. Each I/O pin is set high or low under program control. If a 1 (high) is presented at the latch, gate (b) turns on and gate (a) turns off, so that P is at V_{SS} (low). If a 0 (low) is presented at the latch, gate (a) turns on and gate (b) turns off, so that P is at V_{DD} (high).

When data is output through an I/O port, the pin is connected directly to a standard TTL gate input. Data is input to the pin from a TTL output. In normal operation, high or low levels at P drive the external TTL device input transistor (d). If a low level is set at P, transistor (d) conducts current through the path J, I, P, and FET (b). This is transferred as a low level to the rest of the circuits in the TTL device and results in a high or low level at the output of the device, depending on its characteristics. If the level at P is set high, transistor (d) cuts off and a high level is transferred by (d). When data is input to the I/O pin, a high or low signal at the pin transfers a logic 1 or 0 to the accumulator.

Since the I/O pin and the TTL device output at 0 are wire-ANDed, it is possible for the state of one to affect the transfer of data out from the I/O pin or in from the TTL device output. For example, if the latch in the I/O port is set so that the pin is clamped low by (b), the level at 0 cannot pull P high. Conversely, if P is clamped to a low level by (c), setting the latch for a high level has no effect.

Open-Drain Configuration (Figure 5)— When the I/O port is configured as shown in figure 5, the drain connection of FET (a) is open, i.e., not connected to V_{DD} through a pull-up transistor. This option is most useful in applications where several signals (possibly several I/O port lines) are to be wire-ORed together. A common external pull-up, R_L, is used to establish the logic 1 levels. Another advantage of this option is that the output (point Y) can be tied through a pull-up resistor to a voltage higher than V_{DD} (clear up to V_{GG}) for interfacing to external circuits requiring a higher logic 1 level than V_{DD} provides.

If a high level is present at point X (coming from the port latch), FET (a) will conduct and pull point Y to a low level by current flow through R_L. This low level at Y causes transistor (b) to turn on and present a low level to the input TTL circuit.

If a low level is present at X, FET (a) turns off and point Y is pulled toward V_{DD} by R_L. This causes transistor (b) to turn off and present a high level to the internal TTL circuits.

When data is input, a high level at the base of transistor (c) causes (c) to conduct and pull point Y low, with current flow through T_L. This transfers a high level to the internal I/O port logic through inverting action by the hysteresis circuit. If a

Figure 4 Standard Pull-Up Configuration

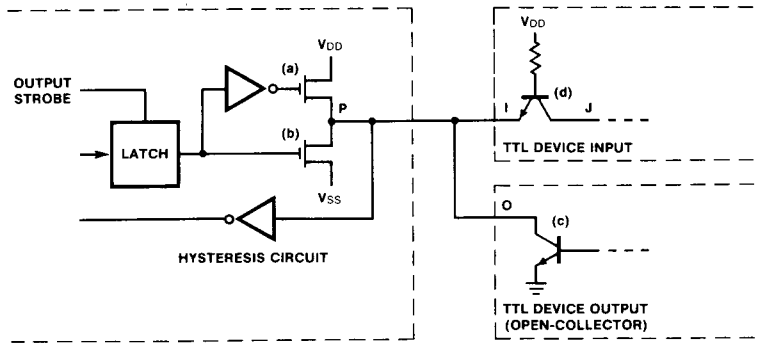


Figure 5 Open-Drain Configuration

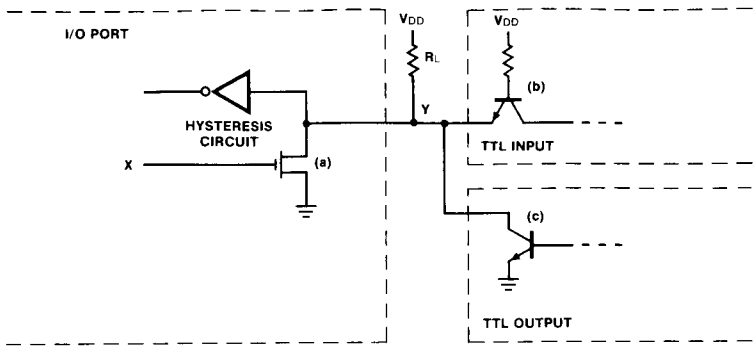
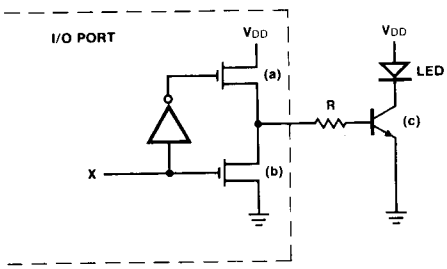


Figure 6 Driver Pull-Up Configuration



low level is present at the base of (c), conduction stops and point Y is pulled toward V_{DD} by R_L. This is then transferred as a low level to internal I/O port logic through the hysteresis circuit.

Driver Pull-Up Configuration (Figure 6)— Figure 6 shows the I/O port driver pull-up option used to drive an LED indicator. This application is typical of a front-panel address or data display, where a row of LED indicators shows the logic state at each pin of an I/O port.

A high level at X turns FET (b) on and (a) off, providing a path for current through resistor R from the base of transistor (c). This stops (c) from conducting and the LED does not light. If a low level is present at X, (b) turns off and (a) turns

on, providing a path for current from V_{DD} through (a) to R. This current through R turns on (c), which causes the LED to conduct and be lighted.

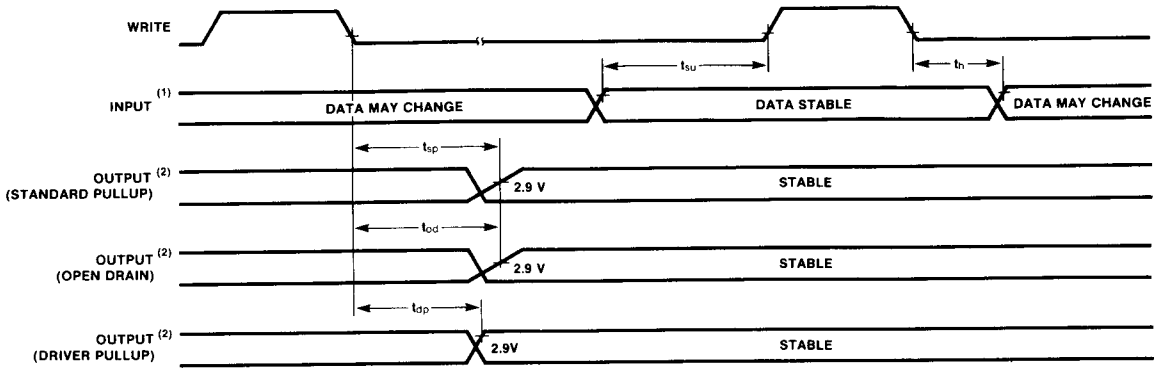
The three options for I/O port output configurations described above are provided to aid the designer in optimizing (minimizing) the system hardware for a particular application. The choice in configuration is specified as a mask option by the designer.

During input instrucions, the trailing edge of the STROBE signal is used to indicate to the external device that the current data on the I/O port is read and new data can be changed. For example, if a shift register is connected to the I/O port, the trailing edge of the STROBE signal is used to advance the shift register.

During output instruction, the trailing edge of this STROBE signal indicates that the new data on the I/O port latches is being changed. The output on the latches becomes true after typically 500 ns of the trailing edge of this signal.

Figure 7 PSU I/O Port Timing

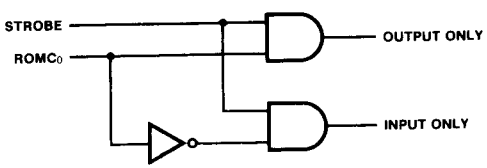
Refer to the "Timing Characteristics" section for all signal characteristics.



F3856 I/O Strobe

An additional output strobe signal is provided on the F3856 to indicate the execution of an input or output instruction for the low address I/O port on the PSU circuit. (This is port 4 of the PSU circuit with the 4-7 address.) A pulse of the duration of the WRITE clock on the STROBE pin is provided at the end of the second cycle of the I/O instruction for this port. Figure 8 shows the timing relationship of this output with respect to the execution being performed.

Although this pulse appears for both input and output instructions for this port, two different signals for input only are derived from the external gating of the STROBE and $ROMC_0$ signals, as shown below.



F3851 Programmable Timer

The F3851 PSU has an 8-bit shift register, addressable as I/O port XXXXXX11, that can be used as a programmable timer (XXXXXX is the 6-bit I/O port address select, a PSU mask option). Figure 9 illustrates the shift register logic and the exclusive-OR feedback path.

Based on the logic illustrated in figure 9, binary values in the range 0 through 254, when loaded into the timer, are converted into "timer counts." As shown in table 3, "timer contents" is the actual binary value loaded into a timer, and "timer counts" is the corresponding number of time intervals the timer takes to time out. Data cannot be read out of the programmable timer I/O port.

As described in the *Guide to Programming the F8 Microcomputer,* an assembly-language program specifies timer counts, and the assembler converts timer counts into the binary value that must be loaded into the programmable timer. This is the value given under "Contents" in table 3. To

Figure 8 I/O Instruction Fetch and Strobe Timing

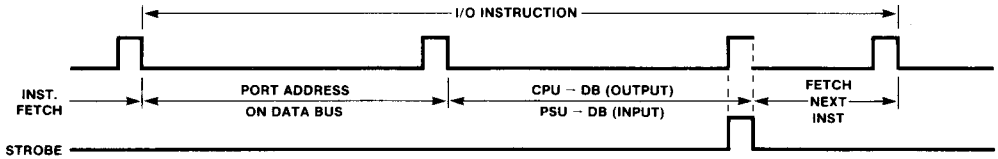
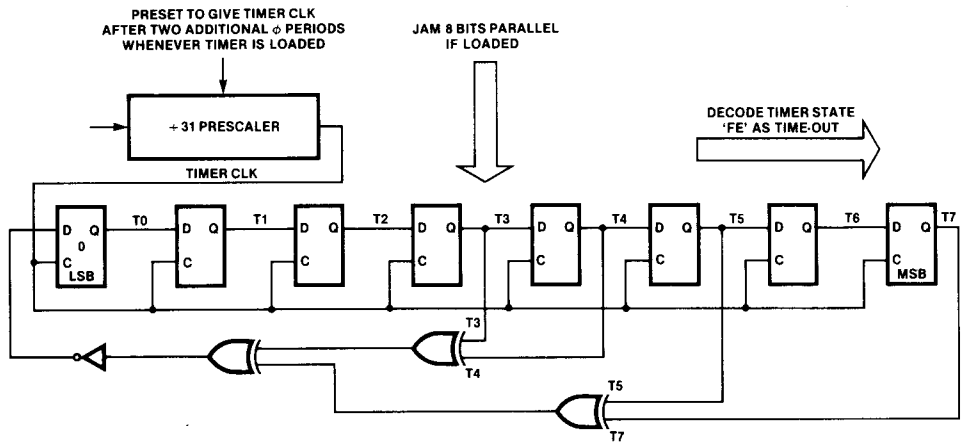


Figure 9 F3851 Timer Block Diagram



use a programmable timer, bypassing assembly-language programming, load the programmable timer with the value given under "Contents" in table 3 to time out after the number of intervals given under "Counts."

It is also possible to write small subroutines that calculate time values one count faster or slower than a given value. Such subroutines would be used if programmed delays are required.

The OUT or OUTS instruction is used to load timer counts into the programmable timer. The contents of the programmable timer cannot be read using an IN or INS instruction. The timer times out after a time interval given by the product (period of ϕ clock × (timer counts) × 31). For example, a value of 200 (11001000, or H'C8') loaded into the programmable timer becomes 215 timer counts. The timer, therefore, times out in 3.33 ms, if the period of clock signal ϕ is 500 ns.

A value of 255 (H'FF') loaded into a programmable timer stops the timer.

All timers run continuously, unless they have been stopped by loading H'FF' into the timer. Upon timing out, the timer transmits an interrupt request to the interrupt logic. If proper interrupt logic conditions exist, the timer interrupt request is passed on to the CPU through the $\overline{INT\ REQ}$ signal.

After a programmable timer has timed out, it again times out after 255 timer counts; therefore, if the programmable timer is left running, it times out every 7905 ϕ clock periods, or every 3.953 ms for a 500 ns clock.

If the timer is actually loaded with a zero value, it times out in 24 counts, whereas, once it has timed out, it next times out in 255 counts; i.e., a time-out is not the same thing as counting down to zero.

When the timer and timer interrupt are being set to time a new interval, the timer is always loaded before enabling the timer interrupt. Loading the timer clears any pending timer interrupts. When the timer interrupt is enabled, any pending

timer interrupt is acknowledged and forwarded to the CPU. Since the timer runs continuously, unless stopped under program control, enabling the timer before loading a time count can cause errors. Prior time-outs of the timer are latched in the interrupt logic of the PSU, even while timer interrupts are disabled. When the timer is enabled, an immediate interrupt acknowledge occurs if, by chance, the continuous-running timer happens to time out while timer interrupts are disabled.

If the timer is loaded just before enabling timer interrupts, loading the timer clears pending timer interrupts. Now a spurious interrupt request does not exist when the timer interrupt is enabled.

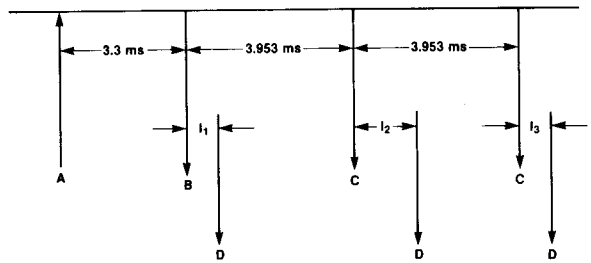
Figure 10 illustrates a possible signal sequence for a timer that is initially loaded with 200, then allowed to run continuously.

F3851 Interrupt Control Register

The interrupt control register (ICR) has the I/O port address XXXXXX10 (where XXXXXX is the 6-bit I/O port address select). Data is loaded into this register (I/O port) using an OUT or OUTS instruction. Data cannot be read out of this register. The contents of the ICR are interpreted as follows:

Contents of I/O Port	Interpretation
B'XXXXXX00'	Disable all interrupts
B'XXXXXX01'	Enable external interrupt, disable timer interrupt
B'XXXXXX10'	Disable all interrupts
B'XXXXXX11'	Disable external interrupt, enable timer interrupt

Figure 10 Time-Out and Interrupt Request Timing



A — 200 LOADED INTO TIMER
B — FIRST TIME OUT
C — SECOND AND SUBSEQUENT TIME-OUTS
D — INTERRUPT SERVICE ROUTINES BEING ENTERED BY CPU
I_1, I_2, I_3 — INTERVALS BETWEEN TIME-OUT INTERRUPT REQUEST REACHING INTERRUPT LOGIC AND SERVICE ROUTINES BEING ENTERED BY CPU

Table 3 F3851 Timer Counts

Contents of Counter	Counts to Interrupt	Contents of Counter	Counts to Interrupt	Contents of Counter	Counts to Interrupt	Contents of Counter	Counts to Interrupt
FE	254	4D	189	D2	124	9F	59
FD	253	9A	188	A5	123	3D	58
FB	252	34	187	4B	122	7C	57
F7	251	69	186	96	121	F8	56
EE	250	D3	185	2D	120	F1	55
DC	249	A7	184	5B	119	E2	54
B8	248	4F	183	B7	118	C5	53
71	247	9E	182	6E	117	8A	52
E3	246	3C	181	DD	116	15	51
C7	245	78	180	BA	115	2A	50

Table 3 F3851 Timer Counts

8E	244	F0	179	75	114	55	49
1D	243	E0	178	EB	113	AA	48
3B	242	C1	177	D6	112	54	47
76	241	82	176	AD	111	A8	46
ED	240	04	175	5A	110	50	45
DA	239	06	174	85	109	A0	44
B4	238	12	173	6A	108	41	43
68	237	24	172	D5	107	83	42
D1	236	48	171	AB	106	06	41
A3	235	90	170	56	105	0D	40
47	234	21	169	AC	104	1A	39
8F	233	42	168	58	103	35	38
1F	232	84	167	B1	102	6B	37
3F	231	°A	166	62	101	D7	36
7E	230	14	165	C4	100	AF	35
FC	229	28	164	88	99	5E	34
F9	228	51	163	11	98	BD	33
F3	227	A2	162	22	97	7B	32
E6	226	45	161	44	96	F6	31
CD	225	8B	160	89	95	EC	30
9B	224	17	159	13	94	D8	29
36	223	2E	158	26	93	B0	28
6D	222	5D	157	4C	92	60	27
DB	221	BB	156	98	91	C0	26
B6	220	77	155	30	90	80	25
6C	219	EF	154	61	89	00	24
D9	218	DE	153	C2	88	01	23
B2	217	BC	152	84	87	03	22
64	216	79	151	03	86	07	21
C8	215	F2	150	10	85	0F	20
91	214	E4	149	20	84	1E	19
23	213	C9	148	40	83	3D	18
46	212	93	147	81	82	7A	17
8D	211	27	146	02	81	F4	16
1B	210	4E	145	05	80	E8	15
37	209	9C	144	0B	79	D0	14
6F	208	38	143	16	78	A1	13
DF	207	70	142	2C	77	43	12
BE	206	E1	141	59	76	87	11
7D	205	C3	140	B3	75	0E	10
FA	204	86	139	66	74	1C	9
F5	203	0C	138	CC	73	39	8
EA	202	18	137	99	72	72	7
D4	201	31	136	32	71	E5	6
A9	200	63	135	65	70	CB	5
52	199	C6	134	CA	69	97	4
A4	198	8C	133	95	68	2F	3
49	197	19	132	2B	67	5F	2
92	196	33	131	57	66	BF	1
25	195	67	130	AE	65	7F	0
4A	194	CE	129	5C	64	FE	254
94	193	9D	128	B9	63		
29	192	3A	127	73	62		
53	191	74	126	E7	61		
A6	190	E9	125	CF	60		

In these I/O port contents definitions, X represents "don't care" binary digits.

F3856 Timer and Interrupt Control Registers

The F3856 logic responds to an interrupt request that can originate internally from the timer logic or from input by an external device, or from the pulse width measurement circuits. Interrupt functions present in the F3856 include the ability to program the active transition of the external interrupt, the ability to have both the timer and the external interrupts active at the same time, and the ability to measure pulse width of an external signal.

The timer is an 8-bit binary count-down register that is used in conjunction with interrupt logic to generate real-time intervals, to measure elapsed time between two events, or to measure a pulse width appearing on the $\overline{EXT}$ $\overline{INT}$ signal. The timer is selected to run in one of four values provided by the prescaler and can be made to start counting or stop counting under program control. Also, the timer contents can be read back under program control.

A zero-detect circuit in the timer detects transitions from a one-count to a zero-count and provides a signal to the interrupt circuits. If all other conditions are satisfied, interrupt circuits, after receiving this signal, request an interrupt service from the CPU.

An external interrupt can be selected under program control to detect the falling or rising edge of the signal. The active edge is determined by the contents in a bit in the interrupt control register.

Both interrupts can be enabled at the same time. When both interrupts are enabled, they are serviced on a first-come, first-served basis. For example, if the timer interrupt arrives later than the unserviced external interrupt, the external interrupt is serviced first, and the timer interrupt remains stored until it is serviced or cleared. If both interrupts arrive at the same cycle, the timer interrupt is handled first.

The internal timer register (TR) and interrupt control register (ICR) are associated with the two high address ports. The TR, depending on various functions, is in one of two modes: stationary or run. In the stationary mode, the contents of the TR remain unaffected. In the run mode, the TR is a binary count-down register, which decrements every 2, 8, 32, or 128 ϕ clock time, depending on the value of the two prescaler bits on the ICR. A circuit detects the one-count-to-zero-count transition of the register and stores it in a flip-flop for interrupt purposes. This flip-flop is cleared any time a new value is loaded into TR.

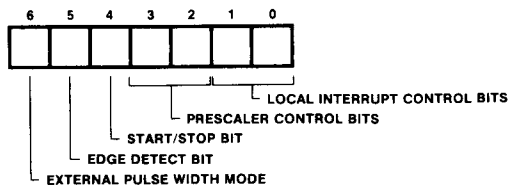
The flip-flop is not cleared by a loading of ICR. While counting, the timer jumps from all-zero value to all-one value and, depending on prescaler values, provides an interrupt period of every 512, 2048, 8192, or 32768 ϕ clocks.

If the timer is in the run mode and the ICR is set for a prescaler value of 2 at the time a value of 2 or 1 is loaded into the TR, the next transition from a one-count to a zero-count is not detected.

F3856 Interrupt Control Register Configuration
The ICR is a 7-bit register used to define various modes of interrupt, the value of the prescaler, and external pulse width measurement. This register is loaded by output instructions; no provision is made to read the contents of this register. The ICR, along with the I/O ports on the F3856, is reset to zero during the reset sequence.

The configuration of this register is shown in figure 11.

Figure 11 F3856 ICR Configuration



Local Interrupt Control (Bits 0-1)—These modes define the interrupt state of the timer and external interrupts (see table 4).

Table 4 F3856 Timer and External Interrupt Modes

Bit 1	Bit 0	Function
0	0	No Interrupt
0	1	Enable External Interrupt Only
1	0	Enable Both External and Timer Interrupts
1	1	Enable Timer Interrupt Only

Prescaler Control (Bits 2-3)—These bits define one of the four different prescalers for the timer (refer to table 5).

Table 5 F3856 Timer Prescaler Modes

Bit 3	Bit 2	Prescaler Value	Timer Resolution at 2 MHz	Timer Period at 2 MHz
1	1	2	1 μs	256 μs
1	0	8	4 μs	1.024 ms
0	0	32	16 μs	4.095 ms
0	1	128	64 μs	16.384 ms

Start-Stop Timer (Bit 4)—This bit controls the TR. When at 0, the TR is in the run mode; when at 1, the TR is in the stationary mode.

Edge Detect Control (Bit 5)—This bit defines the active edge of the $\overline{EXT}$ $\overline{INT}$ input signal as the source during external interrupts. When this bit is at 0, the falling edge is active; when it is at 1, the rising edge is active.

External Pulse Width Mode (Bit 6)—When this bit is at 0, no special function is performed and the interrupts and timer circuits are controlled by bits 0 through 5 of the ICR. However, when this bit is at 1, the special function of pulse width measurement is performed.

Pulse Width Measurement
The following procedure is used to measure pulse width for the F3856 PSU (refer to figure 12).

1. Before the pulse arrives, set the ICR as follows:
   a. Set the external pulse width mode bit to 1.
   b. Set the edge detect bit to 1 for a negative pulse or to 0 for a positive pulse.
   c. Set the start/stop bit to 1 (stop mode).
   d. Set the prescaler bits to the value of prescaler desired.
   e. Set the interrupt bits to turn on both interrupts.
2. Load TR with an initial value.
3. As soon as the pulse arrives, the timer starts counting and provides the timer interrupts at zero crossing.
4. At the end of the pulse, the timer stops counting and provides an external interrupt, indicating the end of the pulse. The timer contents can now be read under program control for calculating the pulse width.

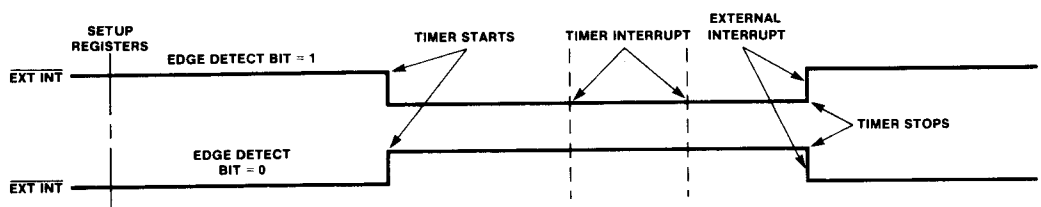
In this procedure, both interrupts are enabled. It is possible to disable one or both interrupts. If the external interrupt is not enabled, the timer stops at the end of the pulse. However, some means of indication are necessary to detect the end of the pulse to the main program. If the timer interrupt is not enabled, the timer zero crossing is not detected. If the pulse duration is always short, such that the timer is stopped before reaching zero, it is not necessary to enable the timer interrupt.

When the timer is loaded with a zero count, the timer interrupt does not occur immediately, although the timer is a zero-count. The timer interrupt occurs only after the one-to-zero transition during the countdown. Hence, when the timer is loaded with a zero count, the timer interrupt occurs after 256 timer counts.

This feature of being able to load a zero count in the timer without getting interrupted allows the programmer to have complete control over the timer count and is also useful during the pulse width measurement mode.

During reset procedures, the ICR is loaded with zero, which disables the local interrupt controls and establishes the trailing edge of the $\overline{EXT}$ $\overline{REQ}$ input signal as the active edge for the external interrupt. The active edge of the external signal can be changed by bit 5 of the ICR. However, when this bit is changed, and the level appearing on the external signals is of the same level as the one obtained after the new active edge, an external interrupt is generated. For example, when changing the active edge of the external signal from trailing edge to rising edge under program control, if the external signal is already at a high level, an interrupt is generated.

Figure 12 F3856 Pulse Width Measurement



If such interrupts are undesirable, an additional step is necessary to disable the local external interrupt control during the change of ICR bit 5. For example, when loading the ICR for the change of direction, the external interrupt control can be disabled with the same instruction, and the next instruction can then enable it.

Note that the feature of generating an interrupt by changing bit 5 of the ICR can be used for software (program-generated) interrupts.

PSU Interrupt Handling

A typical F8 system interrupt interconnection is shown in figure 13. Each PSU and PIO has a $\overline{\text{PRI}}$ $\overline{\text{IN}}$ and a $\overline{\text{PRI}}$ $\overline{\text{OUT}}$ line so that they can be daisy-chained together in any order to form a priority level of interrupts. Depending on the contents of the ICR, the interrupt control logic can be accepting timer interrupts or external interrupts, or neither, but never both.

Figure 14 is a diagram of the PSU interrupt logic. Between the $\overline{\text{EXT}}$ $\overline{\text{INT}}$ input signal or the time-out input and the $\overline{\text{INT}}$ $\overline{\text{REQ}}$ output signal, there are three flip-flops. The $\overline{\text{EXT}}$ $\overline{\text{INT}}$ signal and the time-out interrupt input each have a synchronizing flip-flop and edge detect logic.

Each edge detect clock is followed by its own interrupt flip-flop that latches the true condition.

The outputs of the timer interrupt flip-flop and the external interrupt flip-flop are ORed to set the service request flip-flop, providing that an interrupt from some other PSU is not being acknowledged.

The $\overline{\text{INT}}$ $\overline{\text{REQ}}$ signal is the NAND of priority input and service request. This is an open-drain signal. The $\overline{\text{INT}}$ $\overline{\text{REQ}}$ signal of several PSUs can be tied together so that any one can force the line to 0 V if it is requesting interrupt service; a pull-up to V_{DD} is provided by the F3850 CPU to the $\overline{\text{INT}}$ $\overline{\text{REQ}}$ input pin.

The $\overline{\text{PRI}}$ $\overline{\text{IN}}$ signal is part of the interrupt priority chain. The chain begins by a strap to V_{SS}. Each device in the chain has a $\overline{\text{PRI}}$ $\overline{\text{IN}}$ input signal and a $\overline{\text{PRI}}$ $\overline{\text{OUT}}$ output signal. The $\overline{\text{PRI}}$ $\overline{\text{OUT}}$ signal of the PSU is active (0 V) only if the $\overline{\text{PRI}}$ $\overline{\text{IN}}$ signal is active (0 V) and service request is inactive This means that the $\overline{\text{PRI}}$ $\overline{\text{OUT}}$ and $\overline{\text{INT}}$ $\overline{\text{REQ}}$ signals are always at opposite levels. The $\overline{\text{PRI}}$ $\overline{\text{OUT}}$ signal becomes the $\overline{\text{PRI}}$ $\overline{\text{IN}}$ signal for the next device in the interrupt priority daisy chain, if there is one. The function of the priority daisy chain is to ensure that just one device at a time is requesting interrupt service.

The service request flip-flop cannot become set if another interrupt request is being acknowledged anywhere in the system. Rather, if an interrupt request has been latched into the timer interrupt flip-flop or the external interrupt flip-flop, the PSU logic waits until after the process of acknowledging the other interrupt has been completed before setting the service request. This precaution is necessary to ensure that the priority chain is not altered during acknowledgement; an error would occur if one half of the interrupt vector came from one device and the second half from some other device.

The service request flip-flop is cleared after an interrupt from the PSU has been acknowledged. It is also cleared whenever the interrupt control register for the PSU is accessed by an output instruction.

The conditions for setting the timer interrupt flip-flop and the external interrupt flip-flop differ slightly. External interrupts must be enabled before the external interrupt flip-flop can be set by a negative-going transition of the $\overline{\text{EXT}}$ $\overline{\text{INT}}$ signal. However, the timer interrupt flip-flop is set by a timer time-out independent of the timer interrupt enable bit. This means that the PSU can detect a time-out interrupt that is requested while the PSU was checking for external interrupts.

The timer interrupt flip-flop is cleared whenever the PSU device timer is loaded or when its timer interrupt has been acknowledged. The external interrupt flip-flop is cleared whenever the device interrupt control register is accessed by an output instruction or when its external interrupt has been acknowledged.

Interrupt Acknowledge Sequence

Upon receiving an interrupt request, whether from an external source through the $\overline{\text{EXT}}$ $\overline{\text{INT}}$ signal or from the internal timer, the PSU and CPU go through an interrupt sequence that ultimately results in the execution of an interrupt service routine located at the memory address indicated by the interrupt address vector. Figures 15 and 16 illustrate the interrupt sequences for the two cases. Events occurring in these sequences are labeled A through H.

Event A—The initial interrupt request arrives. The falling edge of the $\overline{\text{EXT}}$ $\overline{\text{INT}}$ pin identifies an external interrupt. The rising edge of the interval timer output indicates a time-out.

Event B—The synchronizing flip-flop in the PSU control logic changes state.

Event C—The timer or external interrupt flip-flop goes true, indicating the local interrupt logic acknowledgement of the interrupt. The timer interrupt flip-flop always responds and saves the time-out occurrence, whereas the external inter-

Figure 13 F8 System Interrupt Interconnection

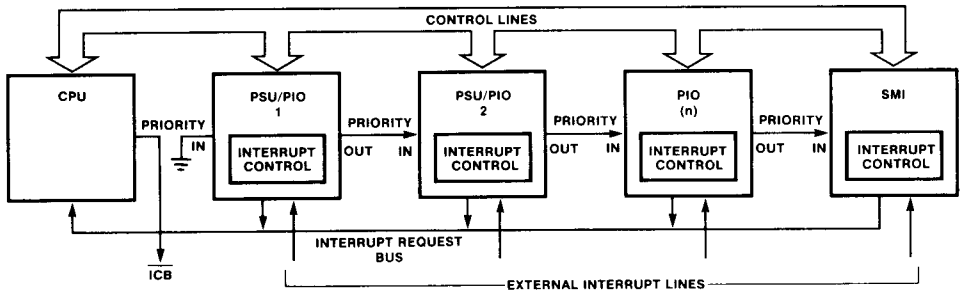
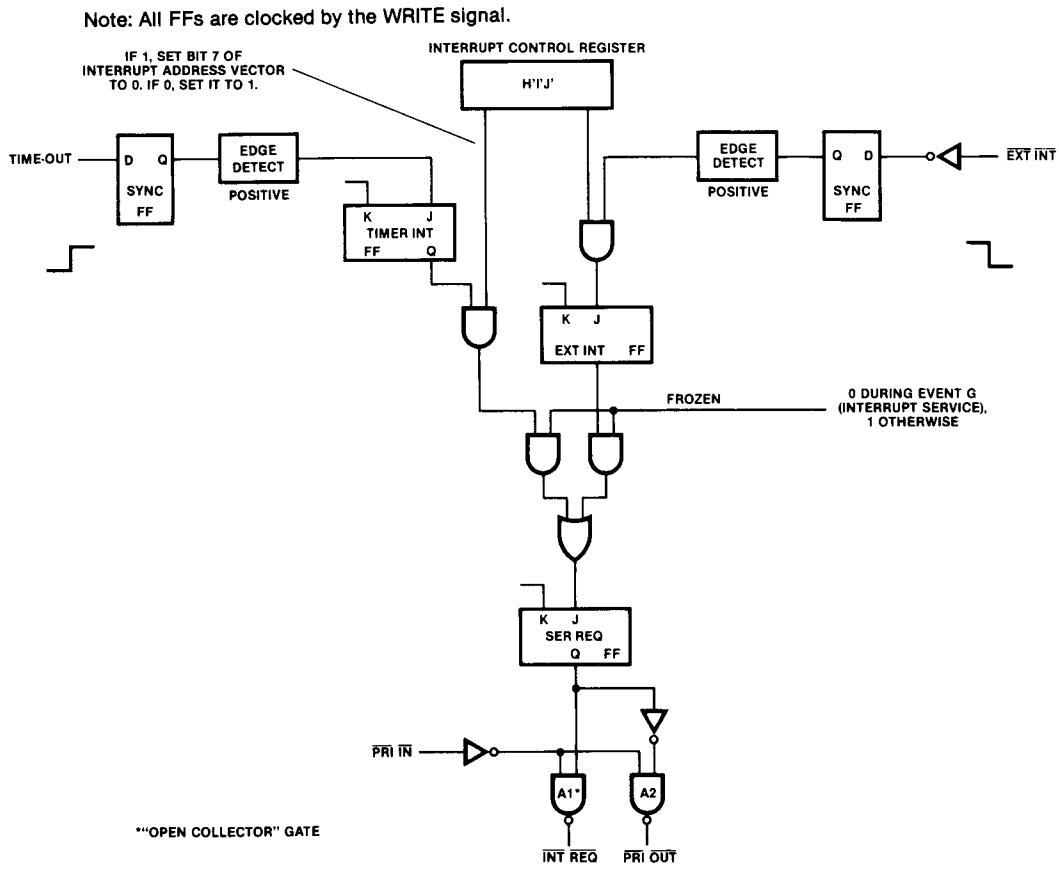


Figure 14 Conceptual Illustration of F3851 PSU Interrupt Logic



rupt flip-flop is set at this time only if the external interrupt mode is enabled within the local control logic.

Event D—The INT REQ line is pulled low by the PSU, passing the request for servicing on to the CPU. The following conditions must be present for this to occur:

1. The PRI IN pin must be low.
2. The proper enable state must exist in the local control logic for the type of interrupt (timer or external).
3. The system is not already into Event F because of servicing some other interrupt.

Event E—The CPU now begins its response to the $\overline{INT}$ $\overline{REQ}$ line by transmitting the unique ROMC state H'10'.

This occurs only when the following conditions are satisfied:

1. The CPU is executing the last cycle of an instruction (beginning an instruction fetch).
2. The ICB is enabled (ICB = 0).
3. The current instruction fetch is not protected.

Event F—The CPU generates the interrupt acknowledge sequence of ROMC states.

Event G—At this point, the CPU begins fetching the first instruction of the interrupt service routine. In the PSU interrupt logic, the service request flip-flop and the appropriate interrupt request flip-flop have been cleared.

Event H—The CPU begins executing the first instruction of the interrupt service routine.

Interrupt Address Vector

During the interrupt acknowledge, the interrupting PSU provides a 16-bit interrupt address vector (refer to figure 17). The CPU causes this vector to be loaded into PC_0 so that program execution can branch to the routine that handles this particular interrupt. Fifteen bits of the interrupt vector are specified as a mask option. Bit 7 cannot be masked; it is set by the interrupt control logic to 0 if the timer interrupt is enabled or to 1 if the external interrupt is enabled.

Figure 15 Timer Interrupt Sequence

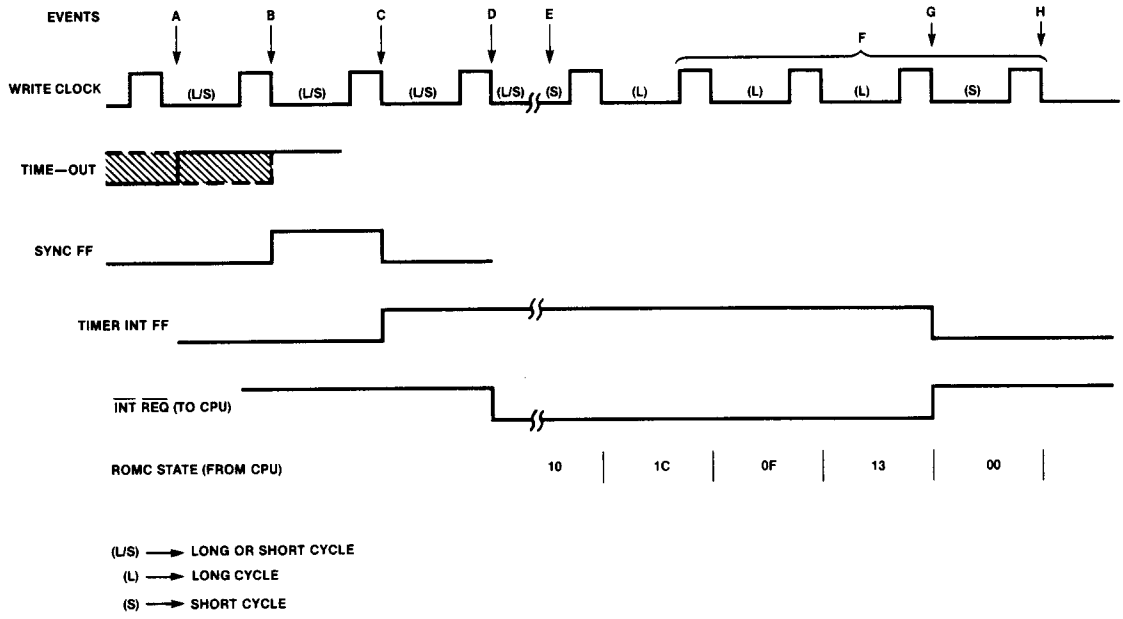


Figure 16 External Interrupt Sequence

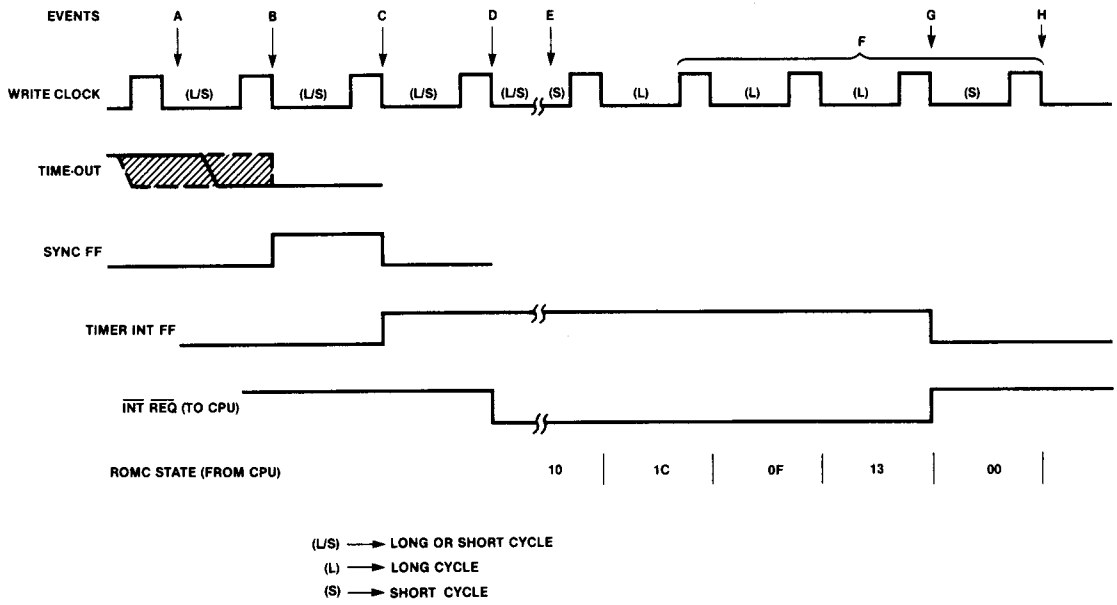
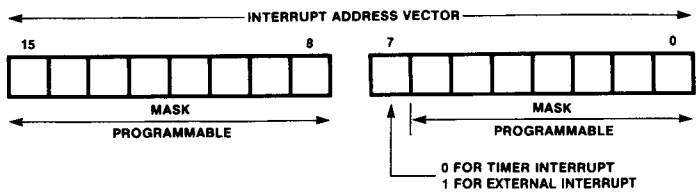


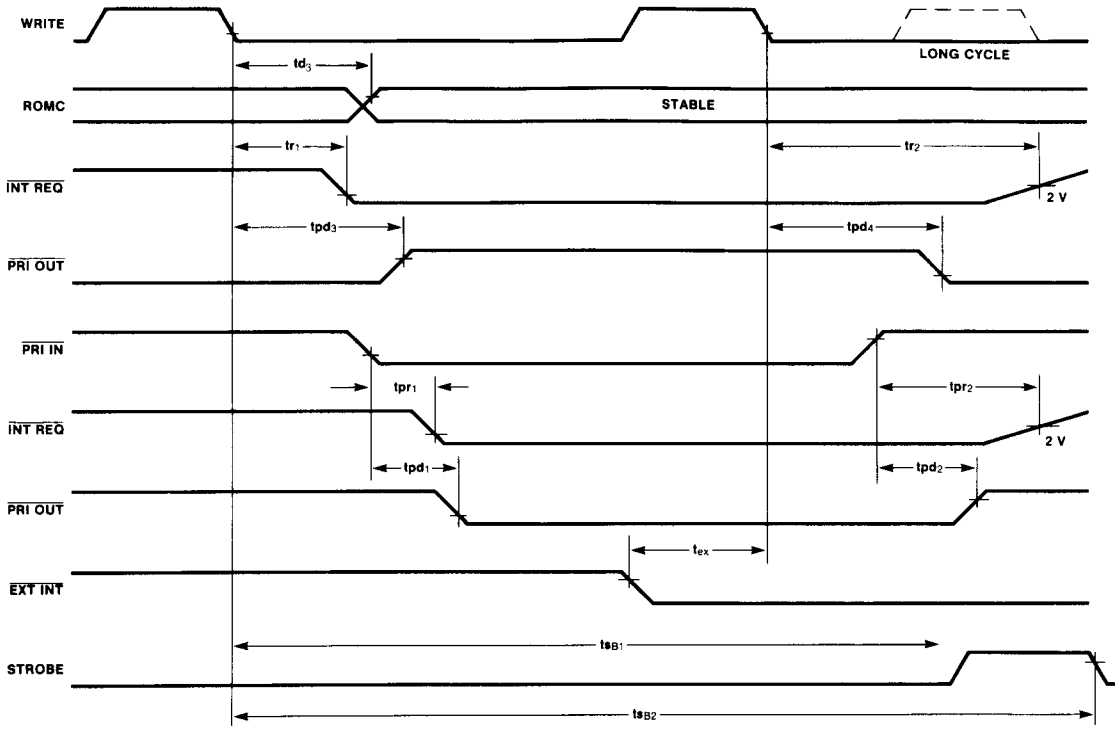
Figure 17 Interrupt Address Vector



Interrupt Signal Timing
Timing for signals associated with the PSU interrupt logic is shown in figure 18. All signal characteristics are given in the timing characteristics section of this data sheet.

Note: Timing measurements are made at valid logic level to valid logic level of the signals referenced unless otherwise noted.

Figure 18 PSU Interrupt Timing



Timing Characteristics

The timing characteristics of the PSU devices are described in table 6. The ac characteristics are $V_{SS} = 0$ V, $V_{DD} = +5.0$ V ±5%, $V_{GG} = +12$ V ±5%, $T_A = 0°C$ to $+70°C$, unless otherwise specified.

Table 6 PSU Signal Timing Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$P\phi$	ϕ Period	0.5		10	μs	
PW_1	ϕ Pulse Width	180		$P\phi-180$	ns	$t_r, t_f = 50$ ns typ.
td_1, td_2	ϕ to Write + Delay			250	ns	$C_L = 100$ pF
td_4	WRITE to DB Input Delay			$2P\phi+1.0$	μs	
PW_2	WRITE Pulse Width	$P\phi-100$		$P\phi$	ns	$t_r, t_f = 50$ ns typ.
PW_S	WRITE Period; Short		$4P\phi$			
PW_L	WRITE Period; Long				ns	
td_3	WRITE to ROMC Delay			550	ns	
td_7	WRITE to DB Output Delay	$2P\phi+100-td_2$	$2P\phi+200$	$2P\phi+850-td_2$	ns	$C_l = 100$ pF
	WRITE to $\overline{DBDR}$ – Delay					
td_8	WRITE to $\overline{DBDR}$ + Delay		200		ns	Open drain
tr_1	WRITE to $\overline{INT}$ $\overline{REQ}$ – Delay			430	ns	$C_L = 100$ pF(1)
tr_2	WRITE to $\overline{INT}$ $\overline{REQ}$ + Delay			430	ns	$C_l = 100$ pF(3)
tpr_1	$\overline{PRI}$ $\overline{IN}$ to INT $\overline{REQ}$ – Delay		200		ns	$C_L = 100$ pF(2)
tpd_1, tpd_2	$\overline{PRI}$ $\overline{IN}$ to $\overline{PRI}$ $\overline{OUT}$ Delay		800		ns	$C_L = 50$ pF
tpd_3, tpd_4	WRITE to $\overline{PRI}$ $\overline{OUT}$ Delay		600		ns	$C_L = 50$ pF
t_{sp}	WRITE to Output Stable			1.0	μs	$C_L = 50$ pF, standard pull-up(3)
t_{od}	WRITE to Output Stable			2.5	μs	$C_L = 50$ pF, $R_L = 12.5$ kΩ, open drain(5)
t_{dp}	WRITE to Output Stable		200	400	ns	$C_L = 50$ pF, driver pull-up
t_{su}	I/O Set-up Time	1.3			μs	
t_h	I/O Hold Time	0			ns	
t_{ex}	$\overline{EXT}$ $\overline{INT}$ Set-up Time	400			ns	
t_sB_1	WRITE to STROBE + Delay			$5P\phi+300$	ns	$C_L = 50$ pF
t_sB_2	WRITE to STROBE – Delay			$6P\phi+410$	ns	$C_L = 50$ pF

Notes
1. Assume priority in was enabled ($\overline{PRI}$ $\overline{IN} = 0$) in the previous F8 cycle, before the interrupt is detected in the PSU.
2. The PSU has an interrupt pending before priority in is enabled.
3. Assume pin tied to $\overline{INT}$ $\overline{REQ}$ input of the F3850 CPU.
4. Input and output capacitance is 3 to 5 pF, typical, on all pins except V_{DD}, V_{GG}, and V_{SS}.

DC Characteristics

The dc characteristics of the PSU devices are provided in tables 7 and 8.

Supply Currents $V_{SS} = 0$ V, $V_{DD} = +5$ V ±5%, $V_{GG} = +12$ V ±5%, $T_A = 0°C$, $+70°C$

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_{DD}	V_{DD} Current		28	60	mA	f = 2 MHz, outputs unloaded
I_{GG}	V_{GG} Current		10	30	mA	f = 2 MHz, outputs unloaded

Table 7 F3851 PSU DC Characteristics

Symbol	Parameter	Signal	Min.	Max.	Units	Test Conditions
V_{IH}	Input High Voltage	Data Bus (DB_0 -DB_7)	2.9	V_{DD}	V	
V_{IL}	Input Low Voltage		V_{SS}	0.8	V	
V_{OH}	Output High Voltage		3.9	V_{DD}	V	$I_{OH} = -100\ \mu A$
V_{OL}	Output Low Voltage		V_{SS}	0.4	V	$I_{OL} = 1.6$ mA
I_{IH}	Input High Current			1.0	μA	$V_{IN} = V_{DD}$, 3-state mode
I_{OL}	Input Low Current			−1.0	μA	$V_{IN} = V_{SS}$, 3-state mode
V_{IH}	Input High Voltage	Clock Lines (ϕ, WRITE)	4.0	V_{DD}	V	
V_{IL}	Input Low Voltage		V_{SS}	0.8	V	
I_L	Leakage Current			3.0	μA	$V_{IN} = V_{DD}$
V_{IH}	Input High Voltage	Priority In and Control	3.5	V_{DD}	V	
V_{IL}	Input Low Voltage	Lines ($\overline{PRI\ IN}$, $ROMC_0$ -	V_{SS}	0.8	V	
I_L	Leakage Current	$ROMC_4$)		3.0	μA	$V_{IN} = V_{DD}$
V_{OH}	Output High Voltage	Priority out ($\overline{PRI\ OUT}$)	3.9	V_{DD}	V	$I_{OH} = -100\ \mu A$
V_{OL}	Output Low Voltage		V_{SS}	0.4	V	$I_{OL} = 100\ \mu A$
V_{OH}	Output High Voltage	Interrupt Request			V	Open-drain output[1]
V_{OL}	Output Low Voltage	($\overline{INT\ REQ}$)	V_{SS}	0.4	V	$I_{OL} = 1$ mA
I_L	Leakage Current			3.0	μA	$V_{IN} = V_{DD}$
V_{OH}	Output High Voltage	Data Bus Drive ($\overline{DBDR}$)				External pull-up
V_{OL}	Output Low Voltage		V_{SS}	0.4	V	$I_{OL} = 2$ mA
I_L	Leakage Current			3.0	μA	$V_{IN} = V_{DD}$
V_{IH}	Input High Voltage	External Interrupt	3.5		V	
V_{IL}	Input Low Voltage	($\overline{EXT\ INT}$)		0.8	V	
V_{IC}	Input Clamp Voltage			15	V	$I_{IH} = 185\ \mu A$
I_{IH}	Input High Current			10	μA	$V_{IN} = V_{DD}$
I_{IL}	Input Low Current			−225	μA	$V_{IN} = 2$ V
I_{IL}	Input Low Current		−150	−500	μA	$V_{IN} = V_{SS}$
V_{OH}	Output High Voltage	I/O Port Option A	3.9[5]	V_{DD}	V	$I_{OH} = -30\ \mu A$
V_{OH}	Output High Voltage	(Standard Pull-up)	2.9	V_{DD}	V	$I_{OH} = -150\ \mu A$
V_{OL}	Output Low Voltage		V_{SS}	0.4	V	$I_{OL} = 1.6$ mA
V_{IH}	Input High Voltage		2.9[3]	V_{DD}	V	Internal pull-up to V_{DD}[3]
V_{IL}	Input Low Voltage		V_{SS}	0.8	V	
I_L	Leakage Current			1.0	μA	$V_{IN} = V_{DD}$
I_{IL}	Input Low Current			−1.6	mA	$V_{IN} = 0.4$ V[4]
V_{OH}	Output High Voltage	I/O Port Option B				External pull-up
V_{OL}	Output Low Voltage	(Open Drain)	V_{SS}	0.4	V	$I_{OL} = 2$ mA
V_{IH}	Input High Voltage		2.9[3]	V_{DD}	V	[3]
V_{IL}	Input Low Voltage		V_{SS}	0.8	V	
I_{IL}	Leakage Current			2.0	μA	$V_{IN} = +12$ V
V_{OH}	Output High Voltage	I/O Port Option C	3.75	V_{DD}	V	$I_{OH} = -1$ mA
V_{OL}	Output Low Voltage	(Driver Pull-up)	V_{SS}	0.4	V	$I_{OL} = 1.6$ mA

Notes

1. Pull-up resistor to V_{DD} on CPU.
2. Positive current is defined as conventional current flowing into the pin referenced.
3. Hysteresis input circuit provides additional 0.3 V noise immunity while internal/external pull-up provides TTL compatibility.
4. Measured while I/O port is outputting a high level.
5. Guaranteed but not tested.

Table 8 F3856 PSU DC Characteristics

Symbol	Parameter	Signal	Min.	Max.	Units	Test Conditions
V_{IH}	Input High Voltage	Data Bus (DB_0 -DB_7)	2.9	V_{DD}	V	
V_{IL}	Input Low Voltage		V_{SS}	0.8	V	
V_{OH}	Output High Voltage		3.9	V_{DD}	V	$I_{OH} = -100\ \mu A$
V_{OL}	Output Low Voltage		V_{SS}	0.4	V	$I_{OL} = 1.6$ mA
I_{IH}	Input High Current			3.0	μA	$V_{IN} = V_{DD}$, 3-state mode
I_{OL}	Input Low Current			−3.0	μA	$V_{IN} = V_{SS}$, 3-state mode
V_{IH}	Input High Voltage	Clock Lines (ϕ, WRITE)	4.0	V_{DD}	V	
V_{IL}	Input Low Voltage		V_{SS}	0.8	V	
I_L	Leakage Current			3.0	μA	$V_{IN} = V_{DD}$
V_{IH}	Input High Voltage	Priority In and Control	3.5	V_{DD}	V	
V_{IL}	Input Low Voltage	Lines ($\overline{PRI}$ $\overline{IN}$, $ROMC_0$ -	V_{SS}	0.8	V	
I_L	Leakage Current	$ROMC_4$)		3.0	μA	$V_{IN} = V_{DD}$
V_{OH}	Output High Voltage	Priority out ($\overline{PRI}$ $\overline{OUT}$)	3.9	V_{DD}	V	$I_{OH} = -100\ \mu A$
V_{OL}	Output Low Voltage		V_{SS}	0.4	V	$I_{OL} = 100\ \mu A$
V_{OH}	Output High Voltage	Interrupt Request			V	Open-drain output[1]
V_{OL}	Output Low Voltage	($\overline{INT}$ $\overline{REQ}$)	V_{SS}	0.4	V	$I_{OL} = 1.0$ mA
I_L	Leakage Current			3.0	μA	$V_{IN} = V_{DD}$
V_{OH}	Output High Voltage	Data Bus Drive ($\overline{DBDR}$)				External pull-up
V_{OL}	Output Low Voltage		V_{SS}	0.4	V	$I_{OL} = 2.0$ mA
I_L	Leakage Current			3.0	μA	$V_{IN} = V_{DD}$
V_{OH}	Input High Voltage	Strobe	3.9	V_{DD}	V	$I_{OH} = -1.0$ mA
V_{OL}	Output Low Voltage		V_{SS}	0.4	V	$I_{OL} = 2.0$ mA
V_{IH}	Input High Voltage	External Interrupt	2.9	V_{DD}	V	$I_{IN} = -130\ \mu A$ (internal pull-up)
V_{IL}	Input Low Voltage	($\overline{EXT}$ $\overline{INT}$)	V_{SS}	0.8	V	
I_{IL}	Input Low Current			−1.6	mA	$V_{IN} = 0.4$ V
V_{OH}	Output High Voltage	I/O Port Option A	3.9	V_{DD}	V	$I_{OH} = -30\ \mu A$[5]
V_{OH}	Output High Voltage	(Standard Pull-up)	2.9	V_{DD}	V	$I_{OH} = -150\ \mu A$
V_{OL}	Output Low Voltage		V_{SS}	0.4	V	$I_{OL} = 1.6$ mA
V_{IH}	Input High Voltage		2.9	V_{DD}	V	Internal pull-up to V_{DD}[3]
V_{IL}	Input Low Voltage		V_{SS}	0.8	V	
I_{IL}	Input Low Current			−1.6	mA	$V_{IN} = 0.4$ V[4]
V_{OH}	Output High Voltage	I/O Port Option B				External pull-up
V_{OL}	Output Low Voltage	(Open Drain)	V_{SS}	0.4	V	$I_{OL} = 2$ mA[3]
V_{IH}	Input High Voltage		2.9	V_{DD}	V	
V_{IL}	Input Low Voltage		V_{SS}	0.8	V	
V_{OH}	Output High Voltage	I/O Port Option C	4.0	V_{DD}	V	$I_{OH} = -1.0$ mA
V_{OL}	Output Low Voltage	(Driver Pull-up)	V_{SS}	0.4	V	$I_{OL} = 2.0$ mA

Notes
1. Pull-up resistor to V_{DD} on CPU.
2. Positive current is defined as conventional current flowing into the pin referenced.
3. Hysteresis input circuit provides additional 0.3 V noise immunity while internal/external pull-up provides TTL compatibility.
4. Measured while I/O port is outputting a high level.
5. Guaranteed but not tested.

Mask Options

The ROM array may contain object program code, tables of nonvarying data, or both. Every PSU is implemented using a custom mask that specifies the state of every ROM bit, as well as certain address mask options that are external to the ROM array. The following mask options are specified:

1. The 1024 or 2048 bytes of ROM storage. This reflects programs and permanent data table stored in the PSU memory.
2. The 5-bit or 6-bit page select. This defines the PSU address space.
3. The 6-bit I/O port address select. This defines the four PSU I/O port addresses.
4. The 16-bit interrupt address vector, excluding bit 7.
5. The I/O port output option. The choices are the standard pull-up (option A), the open-drain (option B), and the driver pull-up (option C).

PSU Mask Option Formats

The format for mask options must be submitted to Fairchild Microprocessor Division before device manufacture. The data to be stored in permanent memory may be submitted in the form of an EPROM or HP2644/HP2645 cartridge (Formulator format only). Other options must be specified on the Fairchild ROM Code Entry Form, available from a Fairchild representative.

Absolute Maximum Ratings

These are stress ratings only, and functional operation at these ratings, or under any conditions above those indicated in this data sheet, is not implied. Exposure to the absolute maximum rating conditions for extended periods of time may affect device reliability, and exposure to stresses greater than those listed may cause permanent damage to the device.

Supply Voltage V_{GG}	−0.3 V, +15 V
Supply Voltage V_{DD}	−0.3 V, +7 V
I/O Port Open Drain Option	−0.3 V, +15 V
External Interrupt Input (F3851)	−600 μA, +225 μA
Other I/O Port Options	−0.3 V, +7 V
All Inputs and Outputs	−0.3 V, +7 V
Storage Temperature	−55°C, +150°C
Operating Temperature	0°C, +70°C

Thermal Resistance Values

Plastic

θ_{JA} (Junction to Ambient) = 60°C/W (Still Air)
θ_{JC} (Junction to Case) = 42°C/W

Ceramic

θ_{JA} (Junction to Ambient) = 48°C/W (Still Air)
θ_{JC} (Junction to Case) = 33°C/W

Recommended Operating Ranges

The recommended operating ranges of the PIO devices are shown below.

Symbol	Parameter	Min.	Typ.	Max.
V_{DD}	Supply Voltage	+4.75 V	+5 V	+5.25 V
V_{GG}	Supply Voltage	+11.4 V	+12 V	+12.6 V
V_{SS}	Ground		0 V	

Ordering Information

Part Number	Package	Temperature Range*
F3851DC	Ceramic	C
F3851DM	Ceramic	M
F3851PC	Plastic	C
F3856DC	Ceramic	C
F3856DM	Ceramic	M
F3856PC	Plastic	C

*C = Commercial Temperature Range 0° to +70°C
L = Limited Temperature Range −40°C to +85°C
M = Military Temperature Range −55°C to +125°C