

Applications

- SONET/SDH-based transmission systems, test equipment and modules
- OC-3 fibre optic modules and line termination
- ATM and FDDI optical receivers

Features

- Single +5 V power supply
- Input noise current = 12 nA rms when used with a 0.5 pF detector
- Transimpedance gain = 15 kΩ into a 50 Ω load (single-ended)
- On-chip automatic gain control gives input current overload of 2.6 mA pk and max output voltage swing of 300 mV pk-pk
- 50 Ω single-ended or 100 Ω differential wire bond selectable outputs
- Bandwidth (-3 dB) = 150 MHz (min)
- Wide data rate range = 10 Mb/s to 155 Mb/s
- High input bias level = 2 V
- Minimal external components, supply decoupling only
- Operating junction temperature range = -40°C to +95°C
- Equivalent to Nortel Networks AB52

Product Description

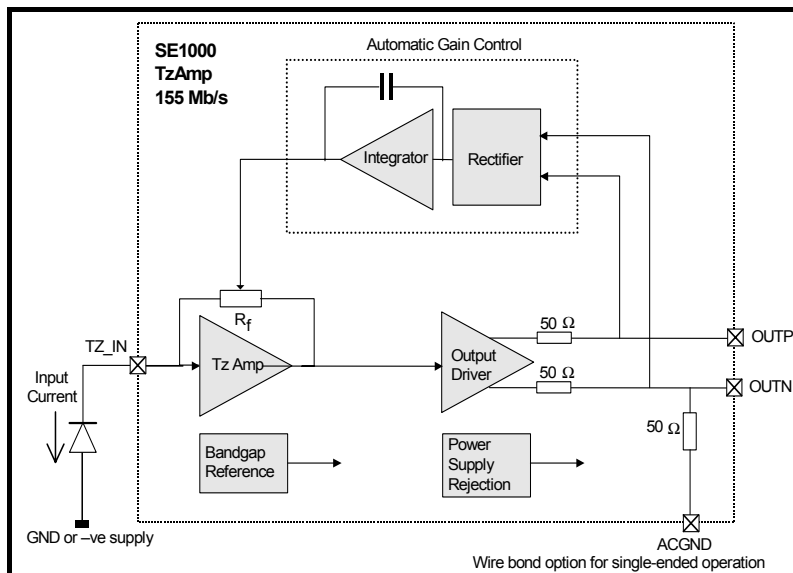
SiGe Semiconductor offers a portfolio of optical networking ICs for use in high-performance optical transmitter and receiver functions, from 155 Mb/s up to 12.5 Gb/s.

SiGe Semiconductor's SE1000W is a fully integrated, silicon bipolar transimpedance amplifier; providing wideband, low noise preamplification of signal current from a photodetector. It features single-ended or differential outputs, selectable by wire bond options, and incorporates an automatic gain control mechanism to increase dynamic range, allowing input signals up to 2.6 mA peak. For differential outputs, a decoupling capacitor on the supply is the only external circuitry required.

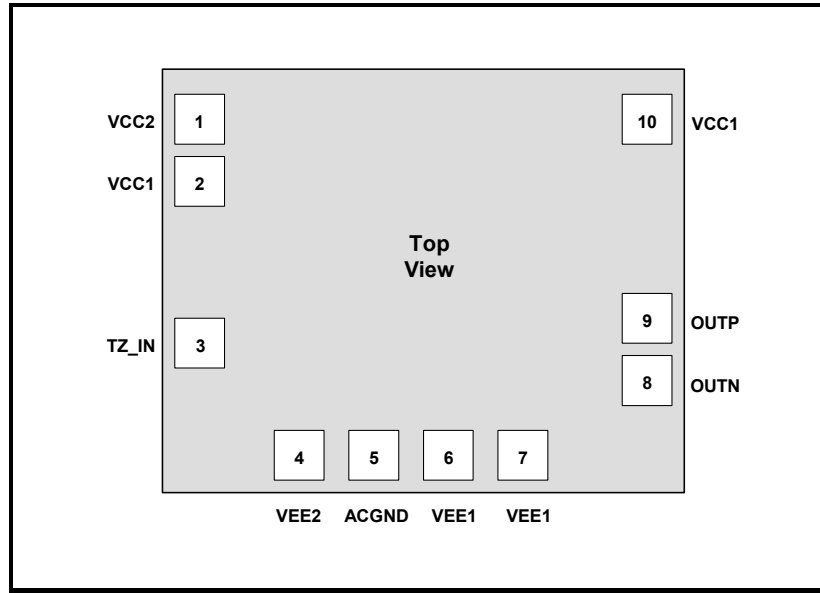
Ordering Information

Type	Package	Remark
SE1000W	Bare Die	Shipped in Waffle Pack

Functional Block Diagram



Bondpad Diagram



Bondpad Description

Pad No.	Name	Description
1	VCC2	Positive supply (+5.0 V), front end circuitry only.
2	VCC1	Positive supply (+5.0 V), pads 2 & 10 are connected on chip. Only one pad needs to be bonded.
3	TZ_IN	Input pad (connect to photodetector cathode).
4	VEE2	Negative supply (0V) – Note this is separate ground for the input stage, which is AC coupled on chip. There is no DC current through this pad.
5	ACGND	Bond option: Connected to external capacitor to ground for single-ended operation (recommended 1 nF); unconnected for differential operation.
6	VEE1	Negative supply (0V), pads 6 & 7 are connected on chip. Only one pad needs to be bonded.
7	VEE1	Negative supply (0V), pads 6 & 7 are connected on chip. Only one pad needs to be bonded.
8	OUTN	Negative differential voltage output; leave unconnected for single-ended operation.
9	OUTP	Positive differential or single-ended voltage output.
10	VCC1	Positive supply (+5.0 V), pads 2 & 10 are connected on chip. Only one pad needs to be bonded.

Functional Description

Amplifier Front-End

The transimpedance front-end amplifies an input current from a photodetector, at pin TZ_IN, to produce an output voltage with the feedback resistor R_f determining the level of amplification (see the functional block diagram on page 1). An automatic gain control loop varies this resistor, to ensure that the output from the front-end does not saturate the output driver stage that follows. This gain control allows input signals of up to 2.6 mA peak.

The input pin TZ_IN is biased at 3 V below the supply voltage VCC, allowing a photodetector to easily be reverse biased by connecting the anode to ground, and hence enabling single rail operation.

The front-end stage has its own supply pins, VCC2 (+5 V) and VEE2 (0 V), to achieve optimum noise performance and maintain integrity of the high-speed signal path. The remainder of the circuitry uses the supply pins VCC1 (+5 V) and VEE1 (0 V).

Output driver stage

The output driver acts as a buffer stage, capable of swinging up to 150 mVpk-pk into a 50 Ω load (or 300 mVpk-pk differential into a 100 Ω load). The small output swings allow ease of use with low voltage post amplifiers (e.g. 3.3 V parts).

The output can be configured in a differential or single-ended mode. For differential operation, the pad ACGND is not wire bonded and the circuit provides a fully balanced 100 Ω output, on the pins OUTP and OUTN. For single-ended operation, the ACGND pad is required to be wire bonded to an external capacitor

to ground (recommend 1 nF). Under these circumstances, OUTP operates as a single-ended 50 Ω output. In both cases, increasing optical input level gives a positive-going output signal on the OUTP pin.

Automatic Gain Control (AGC)

The AGC circuit monitors the voltages from the output driver and compares them to an internal reference level produced via the on-chip bandgap reference circuit. When this level is exceeded, the gain of the front-end is reduced by controlling the feedback resistor R_f .

A long time-constant integrator is used within the control loop of the AGC with a typical low frequency cut-off of 5 kHz.

Power Supply Rejection

An on-chip power supply rejection circuit is used to achieve both single-ended and differential rejection from the +5 V VCC rail.

This stable DC reference minimizes the variation in the noise and bandwidth performance of the circuit due to power supply variation of +4.7 V to +5.3 V.

The AC rejection ensures that performance is not degraded by noise on the power supply. The circuit achieves a power supply rejection on the outputs of 40 dB for both single-ended and differential operation, up to 100 kHz. The use of external decoupling will help to remove any unwanted signals at higher frequencies.

Absolute Maximum Ratings

These are stress ratings only. Exposure to stresses beyond these maximum ratings may cause permanent damage to, or affect the reliability of the device. Avoid operating the device outside the recommended operating conditions defined below.

Symbol	Parameter	Min	Max	Unit
VCC	Supply Voltage	-0.7	6.0	V
V _{IO}	Voltage at any input or output	-0.5	VCC+0.5	V
I _{IO}	Current sourced into any input or output except TZ_IN	-20	20	mA
I _{IO}	Current sourced into pin TZ_IN	-5	5	mA
V _{ESD}	Electrostatic Discharge (100 pF, 1.5 kΩ) except TZ_IN	-2	2	kV
V _{ESD}	Electrostatic Discharge (100 pF, 1.5 kΩ) pin TZ_IN	-0.25	0.25	kV
T _{stg}	Storage Temperature	-65	150	°C

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VCC	Supply Voltage	4.7	5.0	5.3	V
T _j	Operating Junction Temperature	-40		95	°C

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
I _{CC}	Supply Current		39	58	mA
I _{agc}	AGC Threshold	4			μA pk-pk
V _{in}	Input Bias Voltage	VCC-3.2	VCC-3.0	VCC-2.7	V
V _{out}	Output Bias Voltage	2.9		3.5	V
R _{out}	Output Resistance	35	50	65	Ω

AC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
BW (3dB)	Small Signal Bandwidth at –3dB point	150			MHz
Tz	Single-ended Transimpedance (50 Ω on output, f = 50 MHz)	11	15	20	kΩ
Dri	Input Data Rate	10		155	Mb/s
Voutmax	Maximum Differential Output Voltage			300	mV pk-pk
Fif	Low Frequency Cut-off		5		kHz
PSRR	Power Supply Rejection Ratio (single-ended or differential) up to 100 kHz		40		dB
I _{oL}	Input Current before overload (155 Mb/s NRZ data)	2600			μA pk-pk
Pol	Optical Overload	+1.4			dBm
Nrms	Input Noise Current (in 100 MHz)		12	15	nA rms

DC and AC electrical characteristics are specified under the following conditions:

Supply Voltage (VCC) 4.7 V to 5.3 V
 Junction Temperature (Tj) –40°C to 95°C
 Load Resistor (R_L) 50 Ω AC coupled via 220 nF (single-ended)
 Photodetector Capacitance (Cd) 0.5 pF
 Input bond wire inductance 1 nH
 Photodetector responsivity 0.95 A/W
 Transimpedance (Tz) measured with 1 μA mean photocurrent

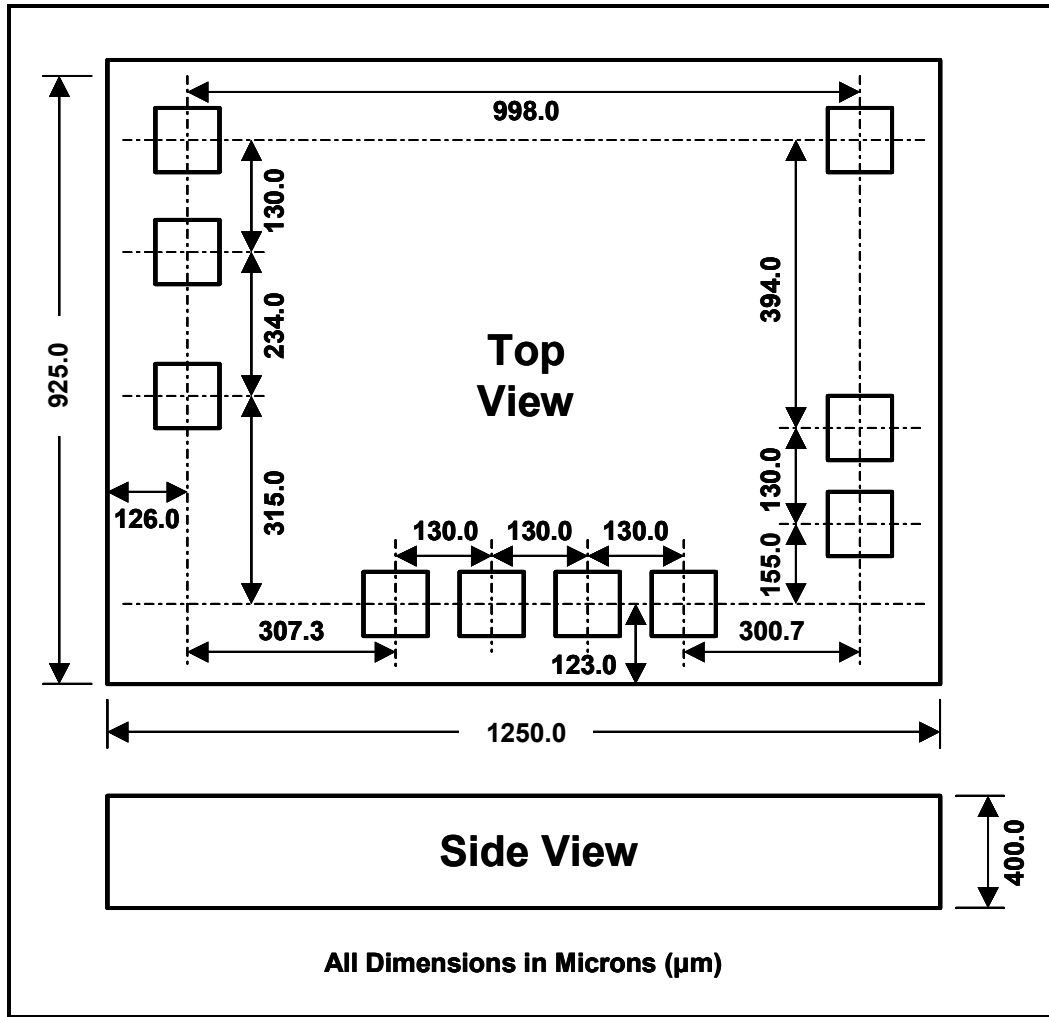
Bondpad Configuration

The bondpad center coordinates are referenced to the center of the lower left pad (pad 4). All dimensions are in microns (μm).

Pad No.	Name	X Coordinate (μm)	Y Coordinate (μm)
1	VCC2	-307.3	679.0
2	VCC1	-307.3	549.0
3	TZ_IN	-307.3	315.0
4	VEE2	0	0
5	ACGND	130.0	0
6	VEE1	260.0	0
7	VEE1	390.0	0
8	OUTN	690.7	155.0
9	OUTP	690.7	285.0
10	VCC1	690.7	679.0

The diagram below shows the bondpad configuration of the SE1000W Transimpedance Amplifier. Note that the diagram is not to scale. All bondpads are 92 μm x 92 μm with a passivation opening of 82 μm x 82 μm. There are two VCC1 and two VEE1 pads for ease of wire bonding; these pad pairs are connected on-chip and only one pad of each type is required to be bonded out.

Mechanical die visual inspection criteria per MIL-STD-883 Method 2010.10 Condition B Class Level B.

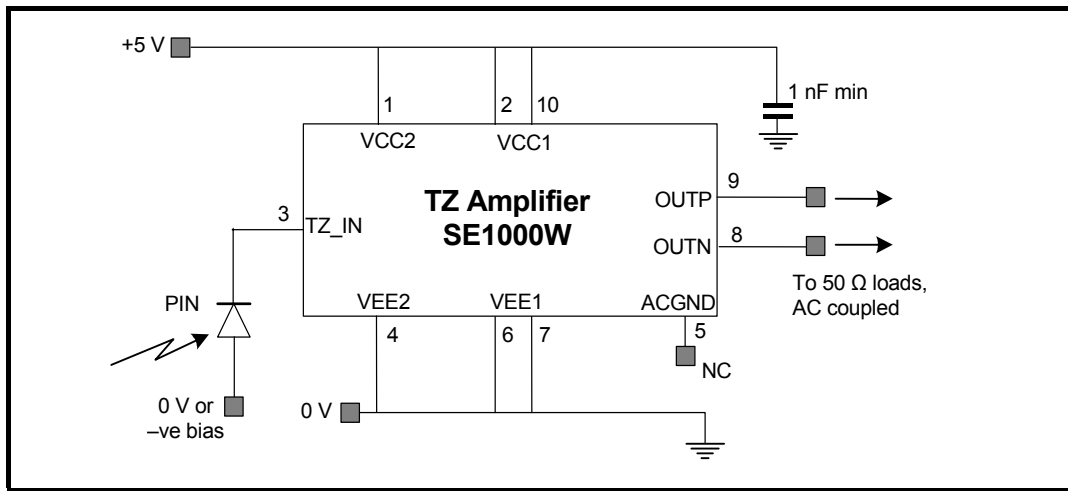


Applications Information

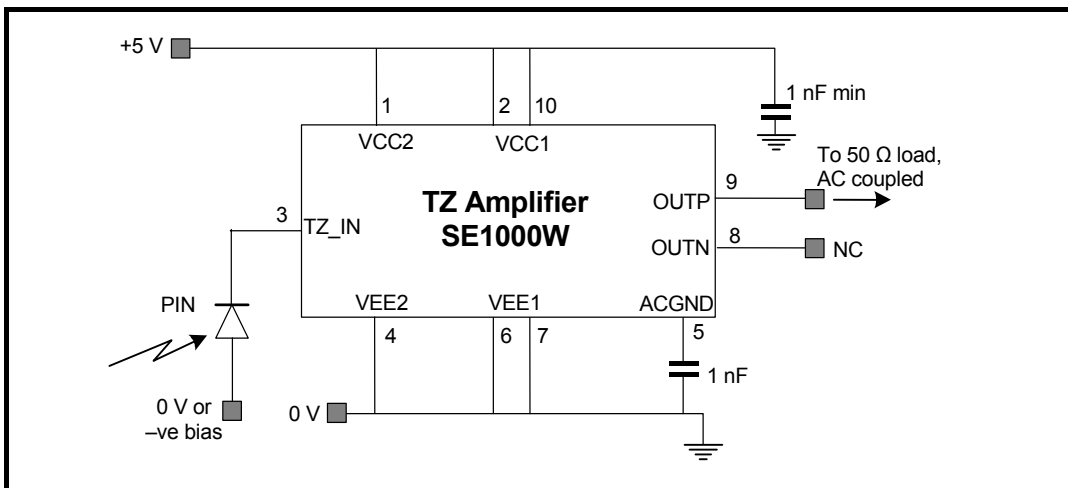
For optimum performance it is recommended that the device be used in differential mode with the circuit shown in the first diagram below.

Note that the two VCC1 pads (2, 10) are connected on-chip, as are the VEE1 pads (6, 7), and only one pad of each type is required to be bonded out. However, in order to minimize inductance for optimum high speed performance, it is recommended that all power pads are wire bonded. The VEE2 and VCC2 pads are not connected on chip to VEE1 and VCC1 respectively, and must be bonded out separately.

Connections for differential operation:



Connections for single-ended operation:



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Product Preview

The datasheet contains information from the product concept specification. SiGe Semiconductor Inc. reserves the right to change information at any time without notification.

Preliminary Information

The datasheet contains information from the design target specification. SiGe Semiconductor Inc. reserves the right to change information at any time without notification.

Final

The datasheet contains information from the final product specification. SiGe Semiconductor Inc. reserves the right to change information at any time without notification. Production testing may not include testing of all parameters.

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