

8259A

Programmable Interrupt Controller
iAPX86 Family
MILITARY INFORMATION

8259A

DISTINCTIVE CHARACTERISTICS

- SMD/DESC qualified
- Eight-level priority controller
- Expandable to 64 levels
- Programmable interrupt modes
- Individual request mask capability
- Single +5-V supply (no clocks)
- 28-pin dual-in-line package

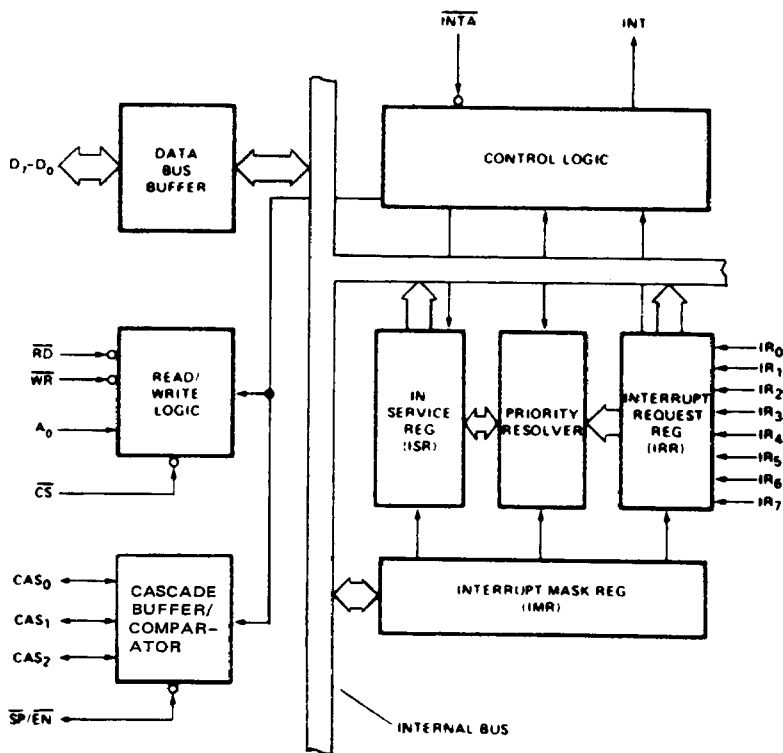
GENERAL DESCRIPTION

The 8259A Programmable Interrupt Controller handles up to eight vectored priority interrupts for the CPU. It is cascadable for up to 64 vectored priority interrupts without additional circuitry. It is packaged in a 28-pin DIP, uses NMOS technology, and requires a single +5-V supply. Circuitry is static, requiring no clock input.

The 8259A is designed to minimize the software and real-time overhead in handling multi-level priority interrupts. It has several modes, permitting optimization for a variety of system requirements.

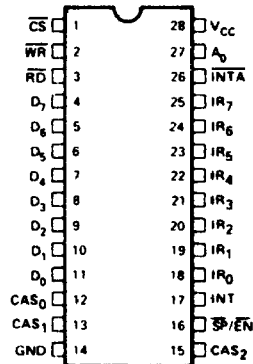
The 8259A is fully upward-compatible with the 8259. Software originally written for the 8259 will operate the 8259A in all 8259-equivalent modes.

BLOCK DIAGRAM



BD003541

CONNECTION DIAGRAM Top View



CD005642

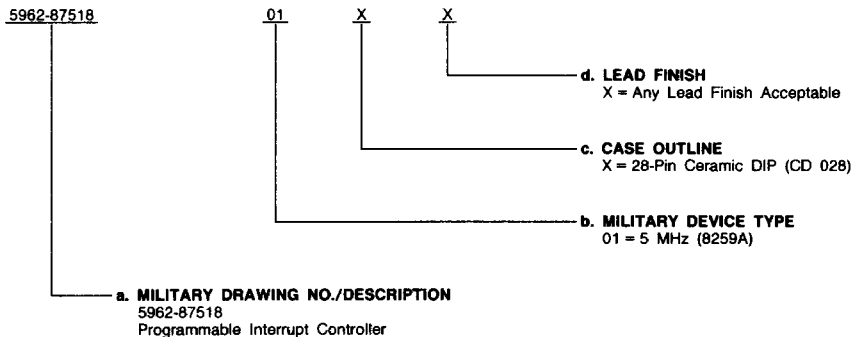
Note: Pin 1 is marked for orientation.

MILITARY ORDERING INFORMATION

Standard Military Drawing (SMD)/DESC Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. Standard Military Drawing (SMD)/DESC products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for SMD/DESC products is formed by a combination of:

- a. Military Drawing Part Number
- b. Device Type
- c. Case Outline
- d. Lead Finish



Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

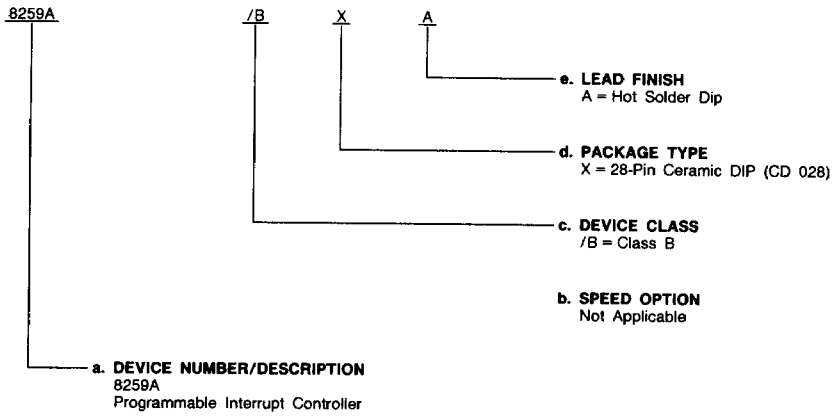
| Valid Combinations | |
|--------------------|----|
| 5962-8751801 | XX |

MILITARY ORDERING INFORMATION (Cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Device Class**
- d. **Package Type**
- e. **Lead Finish**



Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

| Valid Combinations | |
|--------------------|------|
| 8259A | /BXA |

Group A Tests

Group A tests consist of subgroups 1, 2, 3, 7, 8, 9, 10, 11.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature -65 to +150°C
 Voltage on Any Pin
 with Respect to Ground -0.5 V to +7 V
 Power Dissipation 1 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Military (M) Devices
 Temperature (T_C) -55 to 125°C
 Supply Voltage (V_{CC}) 5 V ± 10%

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range (for SMD/DESC and APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

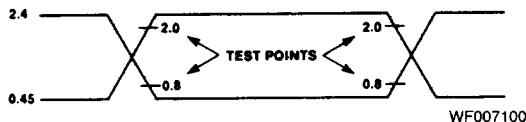
| Parameter Symbol | Parameter Description | Test Conditions | Min. | Max. | Unit |
|-------------------------------------|--------------------------------|------------------------------------------------------------|-------|--------------------------|------|
| V _{IL} | Input LOW Voltage | V _{CC} = 4.5 V to 5.5 V | -0.5* | 0.8 | V |
| V _{IH} | Input HIGH Voltage | V _{CC} = 4.5 V to 5.5 V | 2.3 | V _{CC} + 0.5 V* | V |
| V _{OL} | Output LOW Voltage | I _{OL} = 2.2 mA, V _{CC} = 4.5 V | | 0.45 | V |
| V _{OH} | Output HIGH Voltage | I _{OH} = -400 μA, V _{CC} = 4.5 V | | 2.4 | V |
| V _{OH(INT)} | Interrupt Output HIGH Voltage | I _{OH} = -100 μA, V _{CC} = 4.5 V | | 1.5 | V |
| | | I _{OH} = -400 μA, V _{CC} = 4.5 V | | 2.4 | V |
| I _{LI} | Input Load Current | V _{IN} = 5 V, V _{OUT} = 5.5 V and 0 V | -10 | +10 | μA |
| I _{LOL} , I _{LOH} | Output Leakage Current | V _{CC} = 5 V, V _{OUT} = 5.5 V and 0.45 V | -10 | +10 | μA |
| I _{CC} | V _{CC} Supply Current | V _{CC} = 5 V (Note 1) | | 125 | mA |

Notes: 1. I_{CC} measured in a static condition with output in the worst-case state, having standard I_{OL}/I_{OH} loads applied.

CAPACITANCE (T_C = 25°C, V_{CC} = GND = 0 V)

| Parameter Symbol | Parameter Description | Test Conditions | Min. | Max. | Unit |
|--------------------|-----------------------|---------------------------------------------|------|------|------|
| C _{IN} † | Input Capacitance | f _c = 1 MHz | | 10* | pF |
| C _{I/O} † | I/O Capacitance | Unmeasured pins returned to V _{SS} | | 20* | pF |

*Guaranteed by design; not tested.
 †Not included in Group A tests.

SWITCHING TEST WAVEFORM**Input/Output**

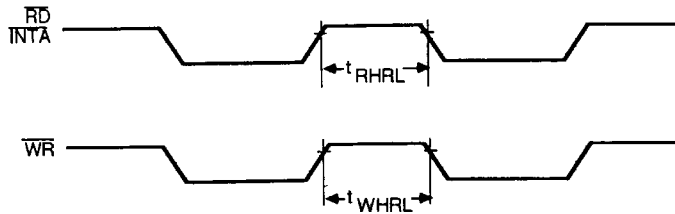
Note: AC testing inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0." Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0."

SWITCHING CHARACTERISTICS over operating range (for SMD/DESC and APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted).

| No. | Parameter Symbol | Parameter Description | Test Conditions | 8259A | | Unit |
|----------------------------|------------------|------------------------------------------------------------------|-----------------|-------|------|------|
| | | | | Min. | Max. | |
| TIMING REQUIREMENTS | | | | | | |
| 1 | t_{AHRL} | A_0/\overline{CS} Setup to $\overline{RD}/\overline{INTA}_1$ | (Note 1) | 0 | | ns |
| 2 | t_{RHAX} | A_0/\overline{CS} Hold after $\overline{RD}/\overline{INTA}_1$ | | 0 | | ns |
| 3 | t_{RLRH} | \overline{RD} Pulse Width | | 235 | | ns |
| 4 | t_{AHWL} | A_0/\overline{CS} Setup to \overline{WR}_1 | | 0 | | ns |
| 5 | t_{WHAX} | A_0/\overline{CS} Hold after \overline{WR}_1 | | 0 | | ns |
| 6 | t_{WLWH} | \overline{WR} Pulse Width | | 290 | | ns |
| 7 | t_{DVWH} | Data Setup to \overline{WR}_1 | | 240 | | ns |
| 8 | t_{WHDX} | Data Hold after \overline{WR}_1 | | 0 | | ns |
| 9 | t_{JLJH} | Interrupt Request Width (LOW) | | 100 | | ns |
| 10 | t_{CVIAL} | Cascade Setup Second or Third \overline{INTA}_1 (Slave Only) | | 55 | | ns |
| 11 | t_{RHRL} | End of \overline{RD} to next Command | | 300 | | ns |
| 12 | t_{WHRL} | End of \overline{WR} to next Command | | 370 | | ns |

| | | | | | | |
|-------------------------|-------------|----------------------------------------------------------------|-----------------|----|-----|----|
| TIMING RESPONSES | | | | | | |
| 13 | t_{RLDV} | Data Valid from $\overline{RD}/\overline{INTA}_1$ | (Notes 1 and 2) | | 200 | ns |
| 14 | t_{RHDX} | Data Float after $\overline{RD}/\overline{INTA}_1$ | | 10 | 100 | ns |
| 15 | t_{JHIH} | Interrupt Output Delay | | | 350 | ns |
| 16 | t_{IALCV} | Cascade Valid from First \overline{INTA}_1 (Master Only) | | | 565 | ns |
| 17 | t_{RLEL} | Cascade Inactive from \overline{RD}_1 or \overline{INTA}_1 | | | 125 | ns |
| 18 | t_{RHEH} | Enable Inactive from \overline{RD}_1 or \overline{INTA}_1 | | | 150 | ns |
| 19 | t_{AHDV} | Data Valid from Stable Address | | | 200 | ns |
| 20 | t_{CVDV} | Cascade Valid to Valid Data | | | 300 | ns |

Notes: 1. Test Conditions: $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$
 $V_{IL} = 0.45 \text{ V}$, $V_{IH} = 2.4 \text{ V}$; $V_{OL} = 0.8 \text{ V}$, $V_{OH} = 2.0 \text{ V}$
 $I_{OL} = 2.2 \text{ mA}$, $I_{OH} = -400 \mu\text{A}$
 2. Test Condition: $C_L = 100 \text{ pF} \pm 20 \text{ pF}$.



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Other Timing (Military)