Attansic® Technology Corporation

AT9173

Bus Termination Regulator

Release Date: Nov. 2004

Revision: V 1.2

1.General Description

The AT9173 is a voltage regulator which could convert the input voltage ringing from 1.6V to 6V to an output voltage that user settled. The regulator can provide sourcing or sinking current.The AT9173, used in conjunction with series termination resistors, provides an excellent voltage source for active termination schemes of high speed transmission lines as those seen in high speed memory buses and distributed backplane designs.

The voltage output of the regulator can be used as a termination voltage for DDR SDRAM. Current limits in both sourcing and sinking mode, plus on-chip thermal shutdown make the circuit tolerant of the output fault conditions.

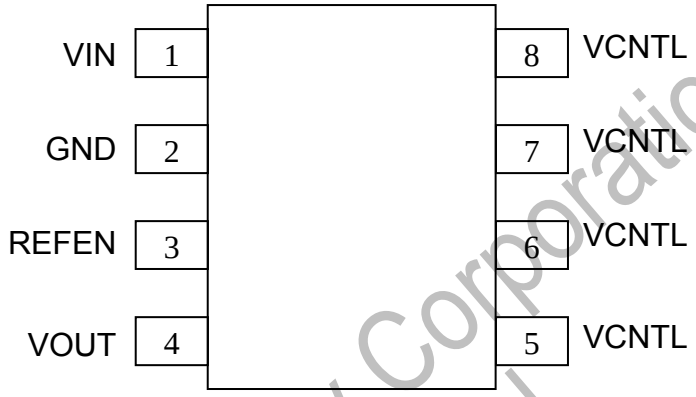
2. Features

- Support Both DDR I (1.25VTT) and DDR II (0.9VTT) Requirements
- Capable of Sourcing and Sinking Current
- Current-limiting Protection
- Thermal Protection
- Integrated Power MOSFETs
- Generates Termination Voltages for SSTL-2
- High Accuracy Output Voltage at Full-Load
- Adjustable VOUT by External Resistors
- Minimum External Components
- Shutdown for Standby or Suspend Mode Operation with High-impedance Output

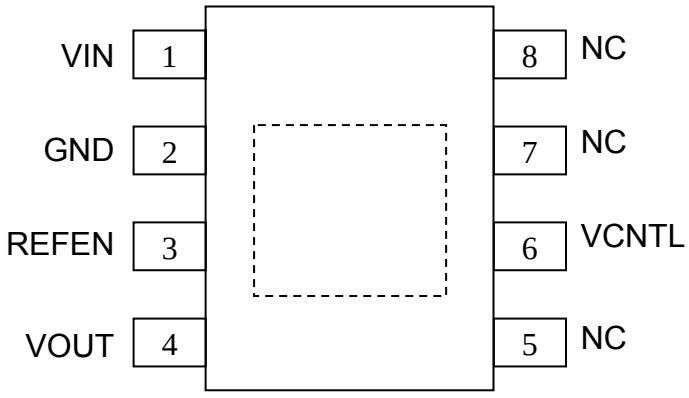
3. Application

- DDR Memory Termination Supply
- Active Termination Buses
- Desktop PC/AGP Graphics
- Supply Splitter
- Set Top Box/IPC

4. Pin Configuration

Part Number	Pin Configurations
AT9173-A (SOP-8) **AT9173-AG (SOP-8, green device)**	

AT9173-A Pin Assignment

Part Number	Pin Configurations
AT9173-C (PSOP-8) **AT9173-CG (PSOP-8, green device)**	 NC= No internal connection = Thermal Pad (Connected to GND plane for better heat dissipation), The Pad of dimension is 0.090 x 0.090 (Inch)

AT9173-C Pin Assignment

5. Pin Description

Pin name	Description
VIN	Power Input
GND	Ground
VCNTL	Driving Voltage
REFEN	Input voltage reference & chip enable
VOUT	Output Voltage

6. Block Diagram

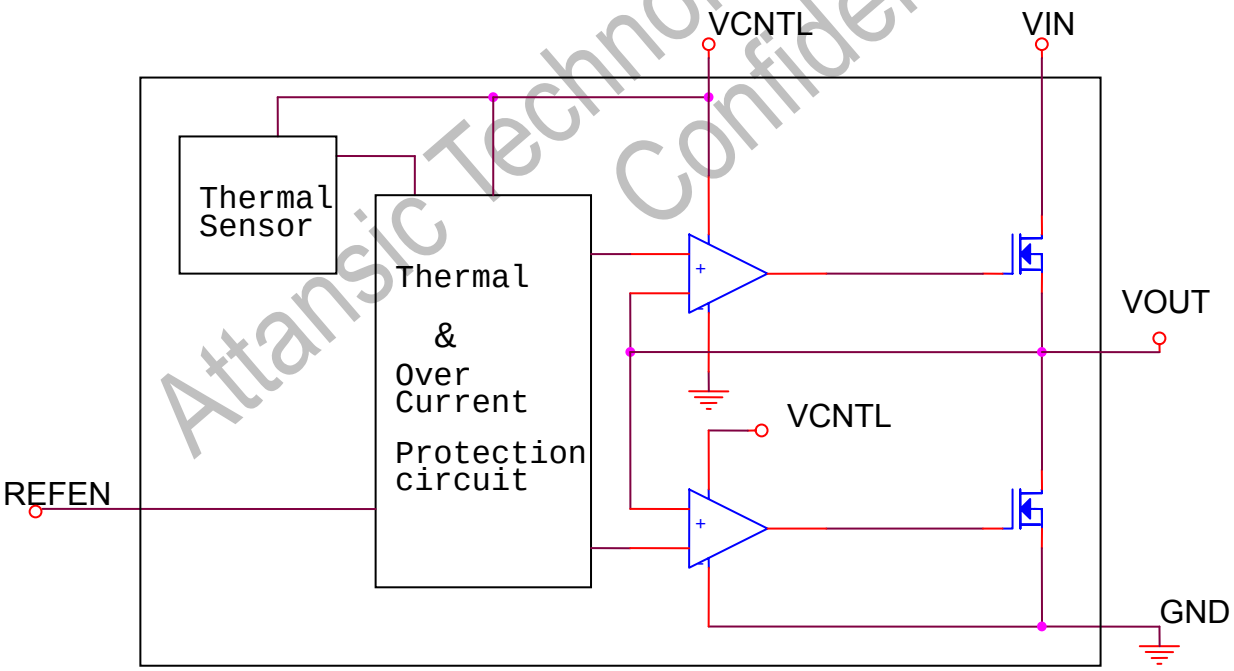


Fig 1 : Block Diagram

7. Application Circuit

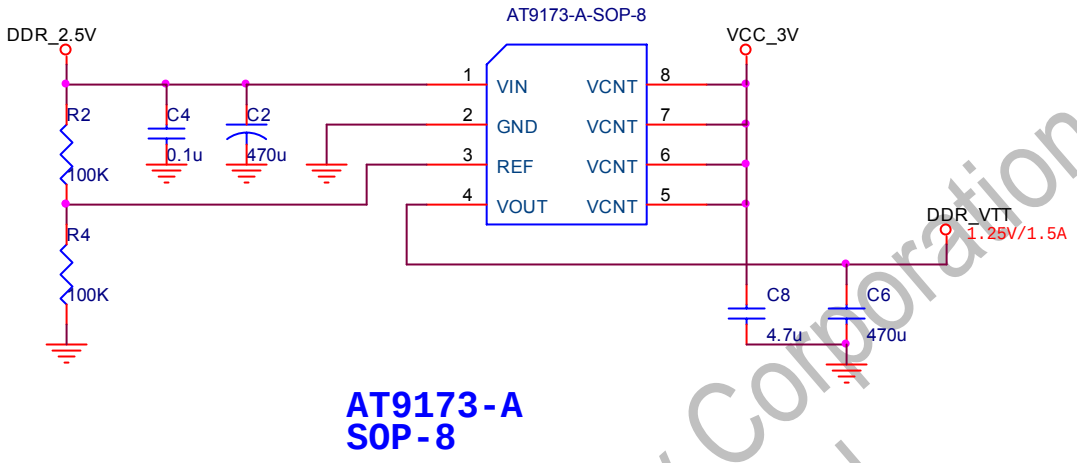


Fig 2 : Application Circuit AT9173-A

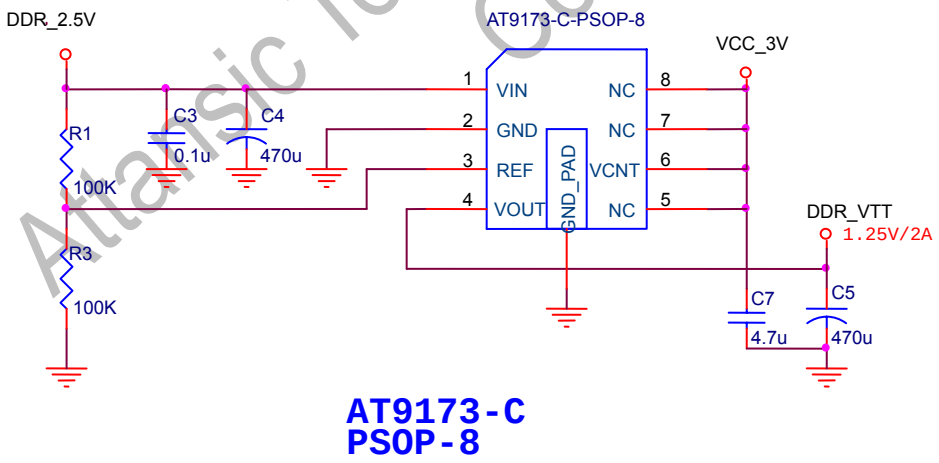


Fig 3 : Application Circuit AT9173-C

8-1. Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
VIN	Input Voltage, VIN to GND	6	V
PD	Power Dissipation	Internally Limit	W
VESD	ESD Rating (Human Body Mode)	2	KV
TSTG	Storage Temperature	150	℃
TL	Lead Temperature (Soldering, 5 sec)	245	℃

8-2. Thermal Characteristics

Symbol	Parameter	Rating	Unit
θ_{JC}	Thermal Resistance In Case		℃/W
	SOP-8	25.7	
	PSOP-8	12	

8-3. Recommended Operating Conditions

Symbol	Parameter	Rating	Unit
VIN	VIN Supply Voltage	1.8~3.3	V
VCNT	VCNT Supply Voltage	3.3	V
REFEN	Reference Voltage Input	0.9/1.25	V
*I_{OUT}	VOUT Output Current*	-2 ~ +2	A
T_J	Junction Temperature	-25~125	℃

*The symbol “+” means the VOUT sources current to load; the symbol “-” means the VOUT sinks current to GND

8-4. Electrical Characteristics

Limits in standard typeface are for T_A=25℃, unless otherwise specified:
V_{IN}=2.5V, V_{CNTL}=3.3V, V_{REFEN}=0.5V_{IN},

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Output Offset Voltage	V_{OS}	I_{OUT}=0A (Note1)	-20	0	20	mV
Load Regulation (DDR 1/2)	$\lvert \triangle V_{LOAD} \rvert$	I_L=0~1.5A Fig 4	-20	0	20	mV
		I_L=0~-1.5A	-20	0	20	
Input Voltage Range (DDR 1/2)	V_{IN}	KEEP $V_{CNTL} \geqq V_{IN}$ on operation power on and power off	1.6	2.5/1.8	4	V
	V_{CNTL}		2.5	3.3	6	
Operating Current of V_{CNTL}	I_{CNTL}	No Load		1.4		mA
Current In Shutdown Mode	I_{SHDN}	V_{REFEN} ＜ 0.2V, R_L=180Ω Fig 5		25.6		μA
Short Circuit Protection						
SOP-8 Current Limit	I_{LIMIT}	Fig 6,7	2.1			A
PSOP-8 Current Limit	I_{LIMIT}	Fig 6,7	2.4			A
Over Temperature Protection						
Thermal Shutdown Temperature	T_{SD}	3.3V ≦ V_{CNTL} ≦ 5V	125			℃
Thermal Shutdown Hysteresis		Guaranteed by design		30		℃

Note1: V_{OS} offset is the voltage measurement defined as V_{OUT} subtracted from V_{REFEN}.

8-5. Test Circuit

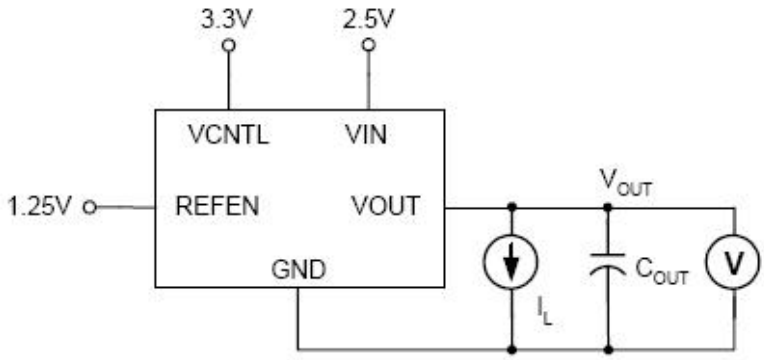


Figure 4: Output Voltage Tolerance, $\triangle V_{OUT}$

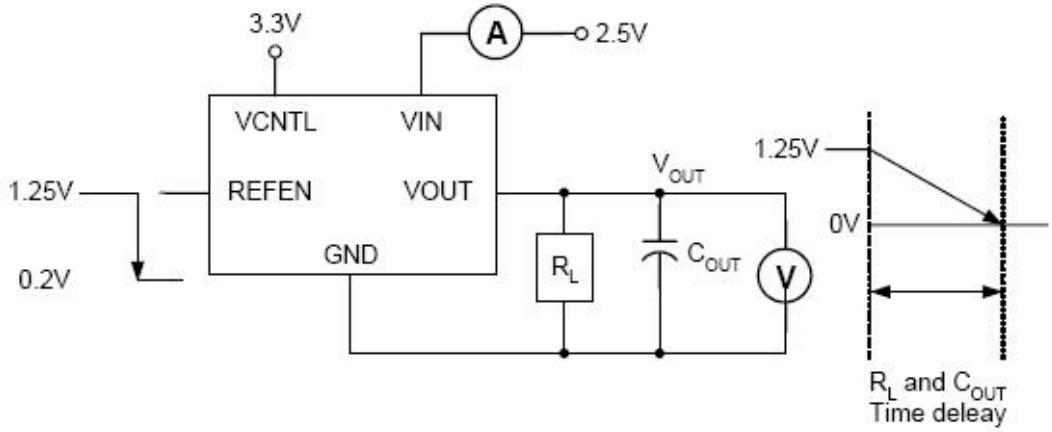


Figure 5: Current in Shutdown Mode, I_{SHCLN}

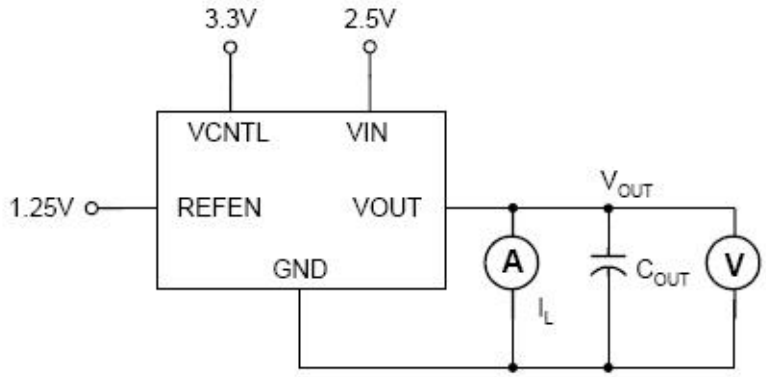


Figure 6: Current Limit for High Side, I_{CLHIGH}

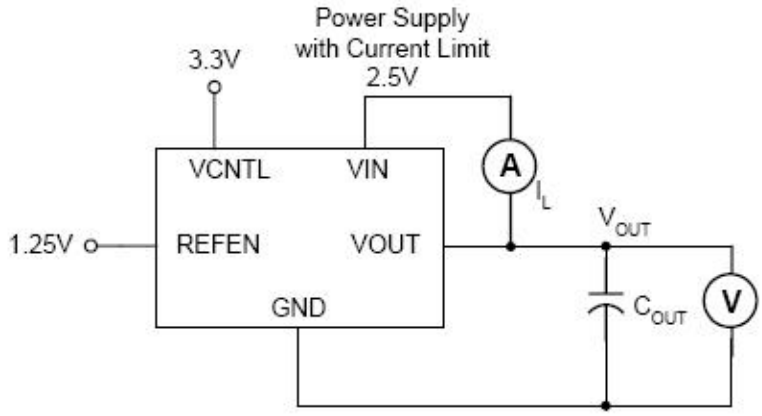
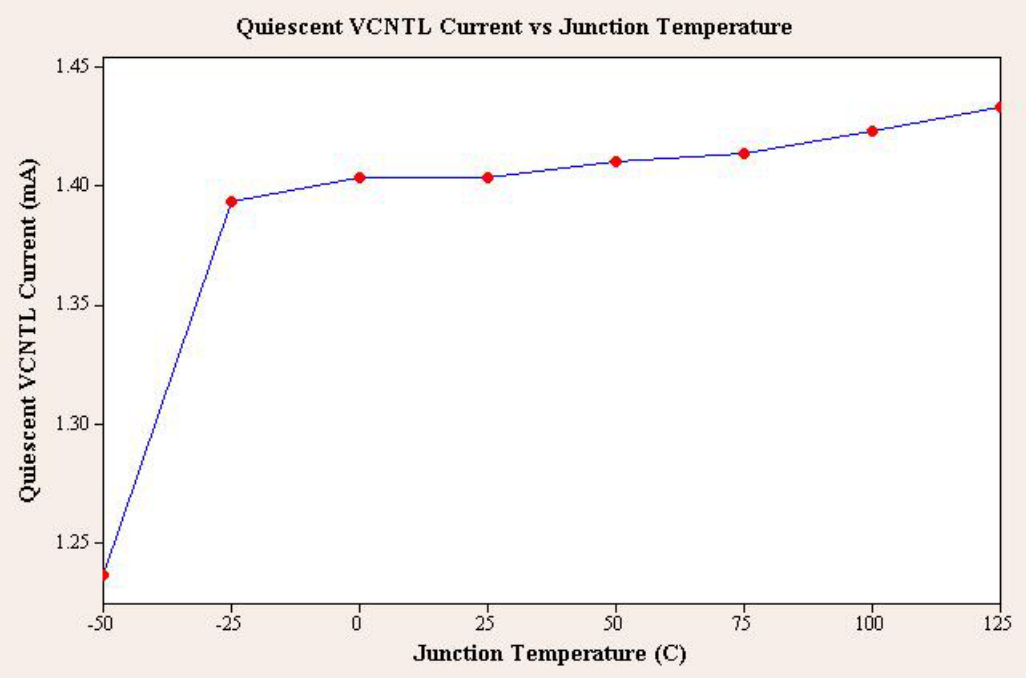
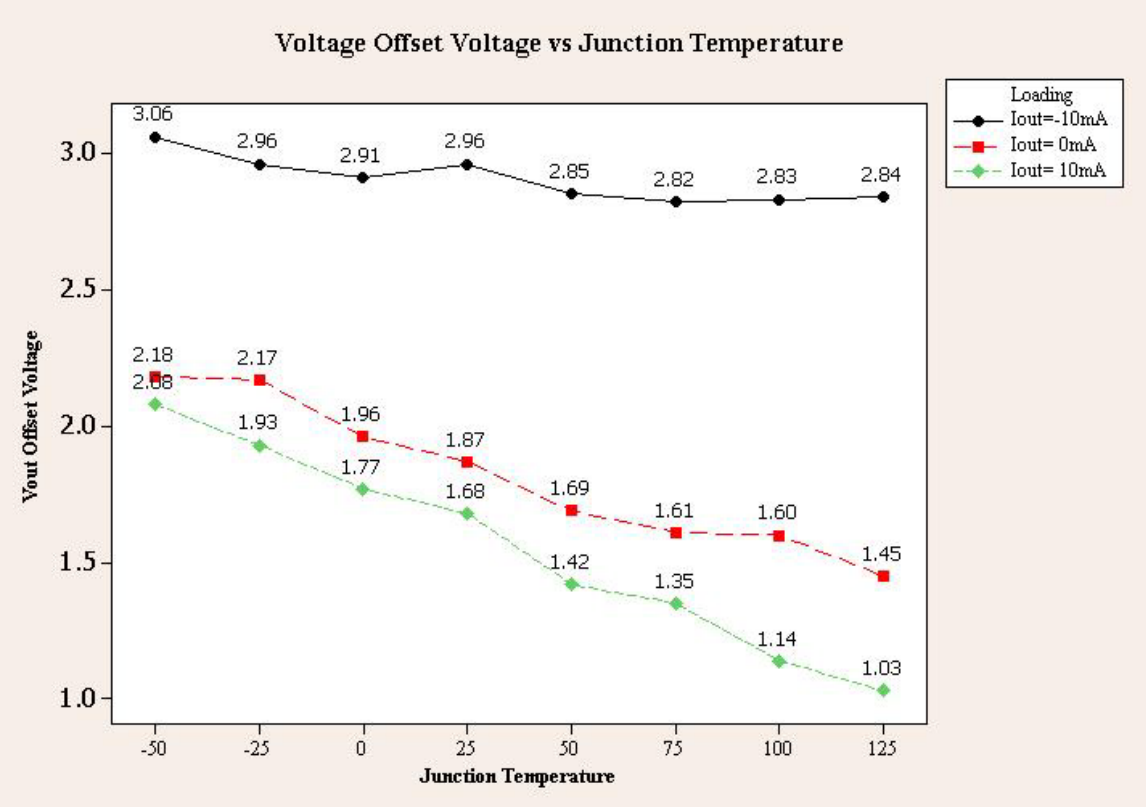


Figure 7: Current Limit for Low Side, I_{CLLOW}

9. Typical Characteristics





10. Operation Waveforms

10-1. Load Transient Response: I_{OUT} = + 0A → +1.5A → +0A

V_{IN}=2.5V, V_{CNTL}=3.3V
V_{REF} is 1.25V supplied by a regulator
C_{OUT}=1000uF/35V
I_{OUT} slew rate = +-0.8A/uS

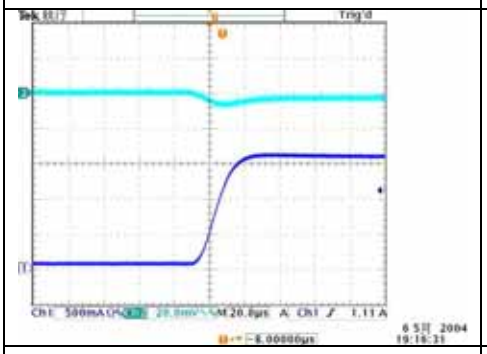
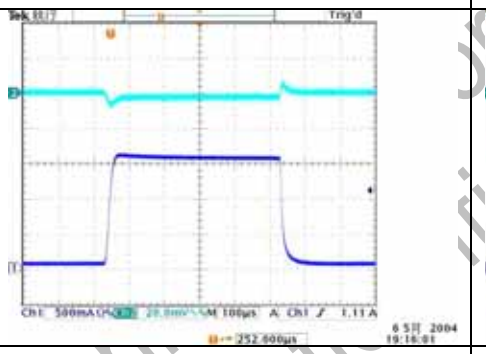
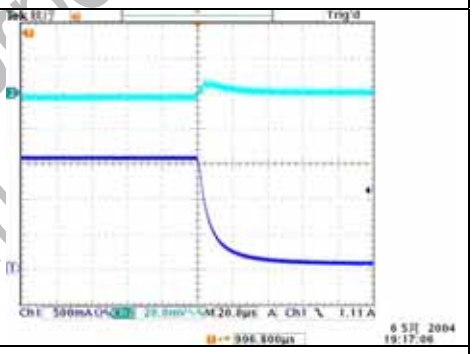
+0A → +1.5A	+0A → +1.5A → +0A	+1.5A → +0A
		
Ch1= I_{OUT} Ch2= V_{OUT}	Ch1= I_{OUT} Ch2= V_{OUT}	Ch1= I_{OUT} Ch2= V_{OUT}

Table 6: Load Transient Response

10-2. Load Transient Response: I_{OUT} = +0A → +2A → +0A

V_{IN}=2.5V, V_{CNTL}=3.3V
V_{REF} is 1.25V supplied by a regulator
C_{OUT}=1000uF/35V
I_{OUT} slew rate = +-0.8A/uS

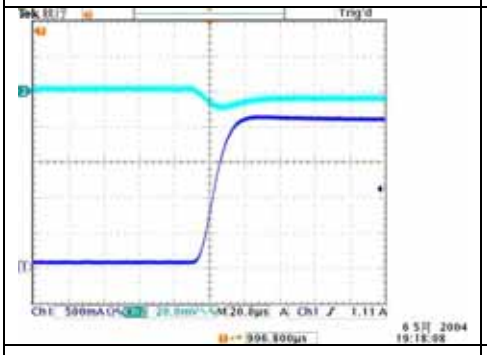
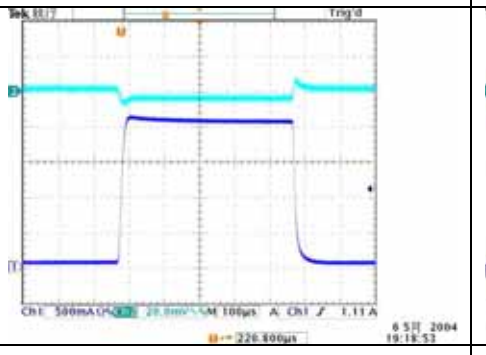
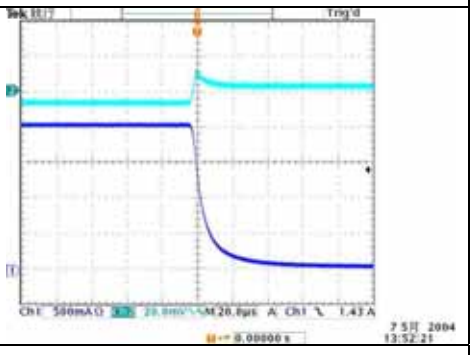
+0A → +2A	+0A → +2A → +0A	+2A → +0A
		
Ch1= I_{OUT} Ch2= V_{OUT}	Ch1= I_{OUT} Ch2= V_{OUT}	Ch1= I_{OUT} Ch2= V_{OUT}

Table 7: Load Transient Response

10-3. Load Transient Response: I_{OUT} = +0A → +3A → +0A

V_{IN}=2.5V, V_{CNTL}=3.3V

V_{REF} is 1.25V supplied by a regulator

C_{OUT}=1000uF/35V

I_{OUT} slew rate = +-0.8A/uS

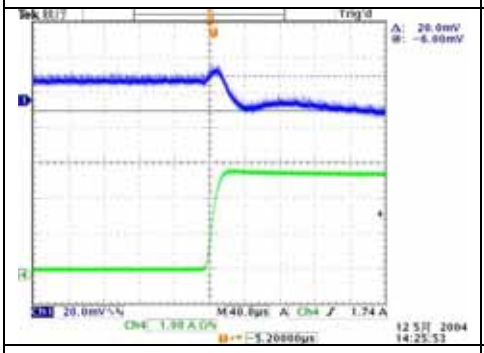
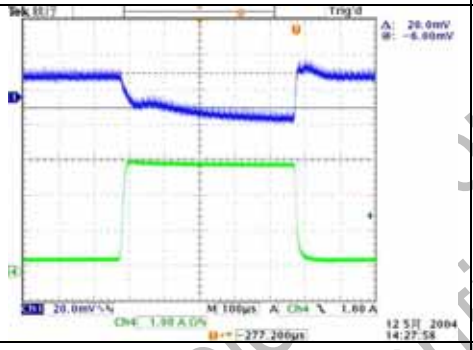
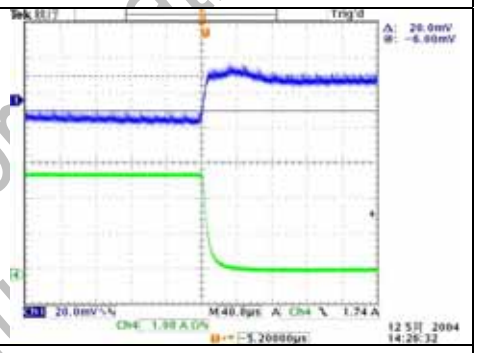
+0A → +3A	+0A → +3A → +0A	+3A → +0A
		
Ch1= I_{OUT} Ch2= V_{OUT}	Ch1= I_{OUT} Ch2= V_{OUT}	Ch1= I_{OUT} Ch2= V_{OUT}

Table 8: Load Transient Response

10-4. Load Transient Response: I_{OUT} = - 0A → -1.5A → -0A

$_{IN}$=2.5V, V_{CNTL}=3.3V

V_{REF} is 1.25V supplied by a regulator

C_{OUT}=1000uF/35V

I_{OUT} slew rate = +-0.8A/uS

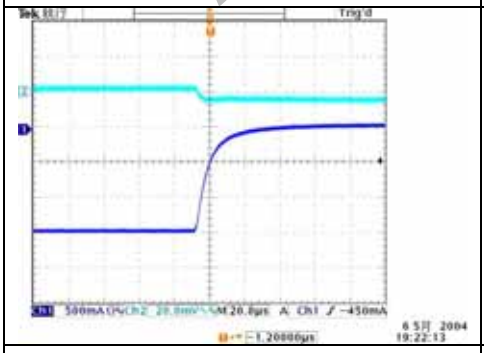
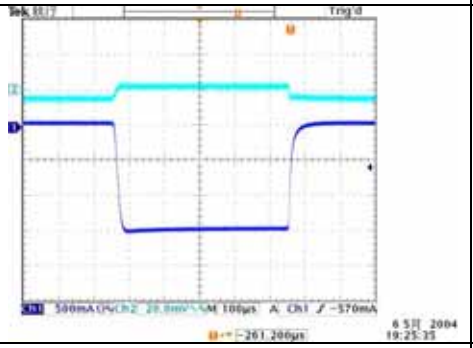
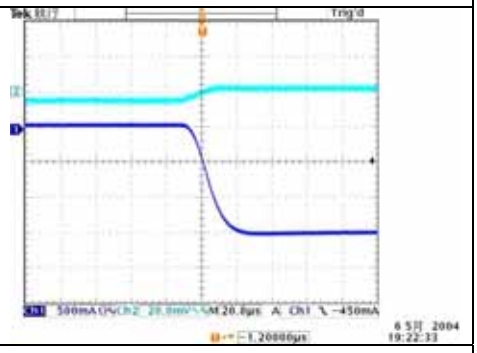
-0A → -1.5A	-0A → -1.5A → -0A	-1.5A → -0A
		
Ch1= I_{OUT} Ch2= V_{OUT}	Ch1= I_{OUT} Ch2= V_{OUT}	Ch1= I_{OUT} Ch2= V_{OUT}

Table 9: Load Transient Response

10-5. Load Transient Response: I_{OUT} = -0A → -2A → -0A

V_{IN}=2.5V, V_{CNTL}=3.3V
V_{REF} is 1.25V supplied by a regulator
C_{OUT}=1000uF/35V
I_{OUT} slew rate = +-0.8A/uS

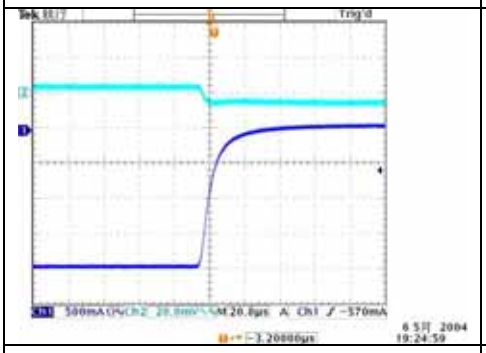
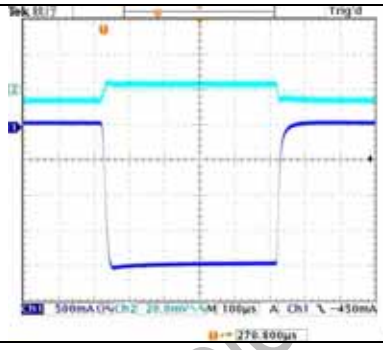
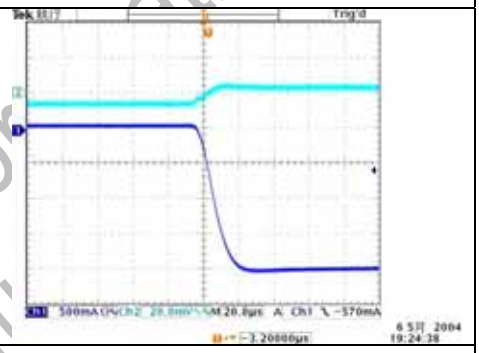
-0A → -2A	-0A → -2A → -0A	-2A → -0A
		
Ch1= I_{OUT} Ch2= V_{OUT}	Ch1= I_{OUT} Ch2= V_{OUT}	Ch1= I_{OUT} Ch2= V_{OUT}

Table 10: Load Transient Response

10-6. Load Transient Response: I_{OUT} = -0A → -3A → -0A

V_{IN}=2.5V, V_{CNTL}=3.3V
V_{REF} is 1.25V supplied by a regulator
C_{OUT}=1000uF/35V
I_{OUT} slew rate = +-0.8A/uS

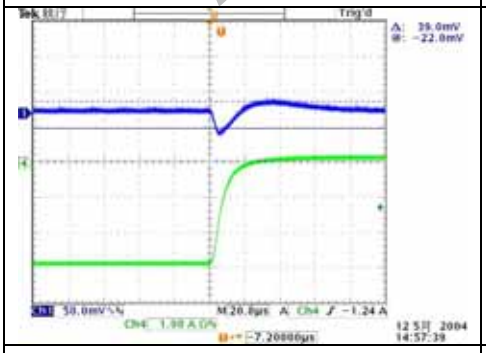
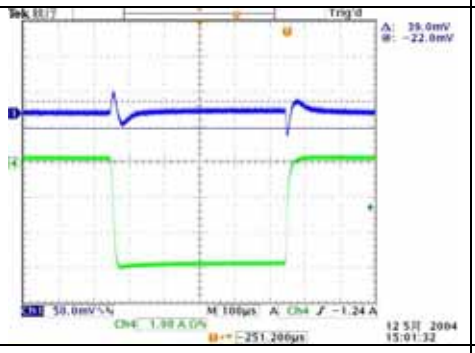
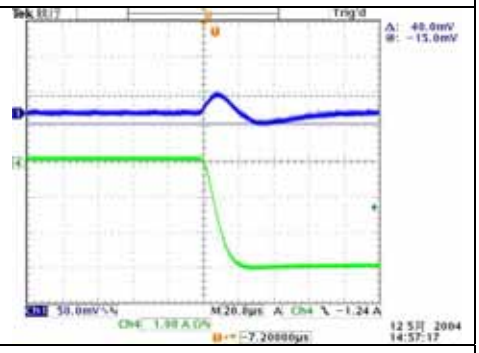
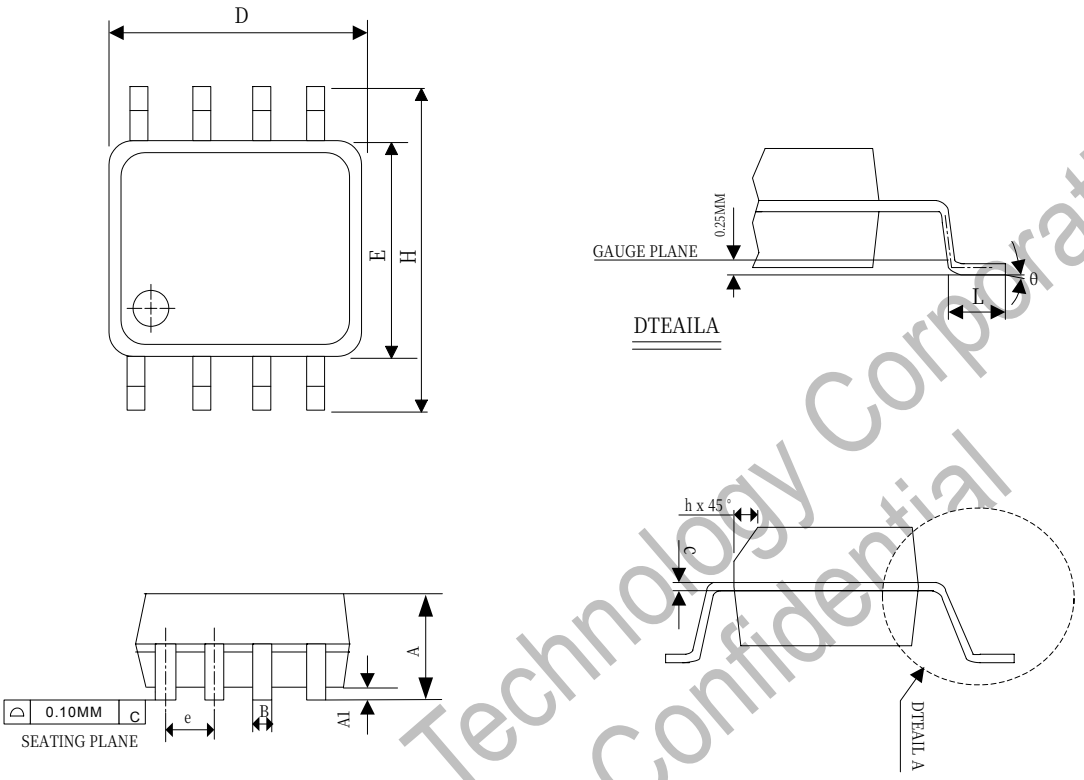
-0A → -3A	-0A → -3A → -0A	-3A → -0A
		
Ch1= I_{OUT} Ch2= V_{OUT}	Ch1= I_{OUT} Ch2= V_{OUT}	Ch1= I_{OUT} Ch2= V_{OUT}

Table 11: Load Transient Response

11-1. SOP-8/PSOP-8 package Information



Symbol	Dimension in mm		Dimension in inch	
	Min	Max	Min	Max
A	1.35	1.75	0.0532	0.0688
A1	0.10	0.25	0.0040	0.0098
B	0.33	0.51	0.013	0.020
C	0.19	0.25	0.0075	0.0098
e	1.27BSC		0.050BSC	
D	4.80	5.00	0.1890	0.1968
H	5.80	6.20	0.2284	0.2440
E	3.80	4.00	0.1497	0.1574
L	0.40	1.27	0.016	0.050
h	0.25	0.50	0.0099	0.0196
θ	0^0	8^0	0^0	8^0
JEDEC	MS-012 (AA)			

*NOTES: DIMENSION “D” DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15 MM (0.006 INCH) PER SIDE.

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