# **MR9710**

T-77-07-0S

# **TELEVIEW DATA ACQUISITION CHIP**

The MR9710 Data Acquisition (DA) chip is one of the set of LSI devices comprising the Plessey Semiconductor Teleview (Teletext/Viewdata) system. It receives data from a TV signal or Telephone Line via an appropriate interface and processes the data accordingly. Under instruction from a control device it acquires the requested data and loads it into the correct location in the preselected page store. Control information extracted from the incoming data is provided to the Teleview system.

The device is fabricated in Plessey Semiconductor Nchannel metal gate MOS process providing direct TTL Interfacing, high speed and good reliability. It is supplied in a 40 lead dual-in-line package.

### **FEATURES**

- Processes Teletext and Viewdata Input Data
- Direct Interface with Teleview Highways
- Direct Interface with Standard UAR/T
- TTL Compatible Serial Teletext Data Input
- Full Checking of Teletext Data including Parity, Hamming and Data Frequency
- 'Don't Care' Digit Facility
- Non-used Viewdata Control Codes made available to Control Processor.
- Addresses Up To Eight Page Stores

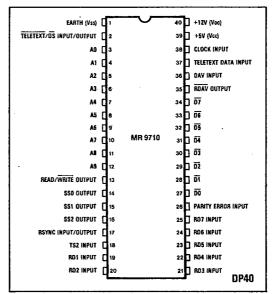


Fig.1 Pin connections - top view

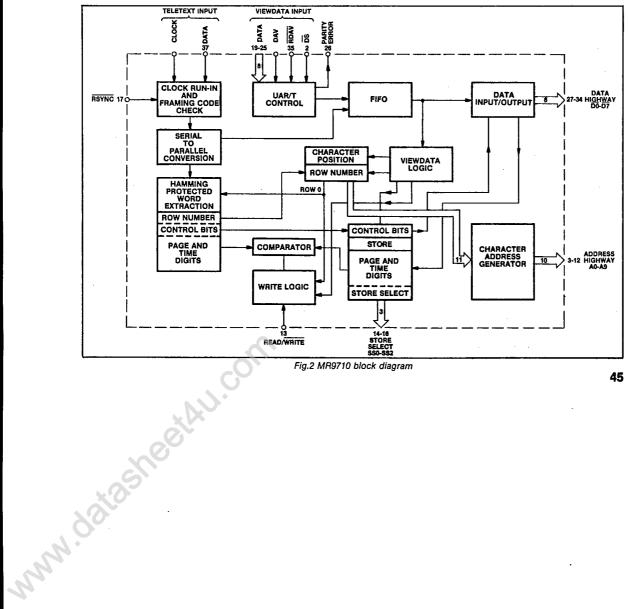


Fig.2 MR9710 block diagram

45

#### **PIN FUNCTIONS**

Pin Number	Name	Function T-77-07-05
1	Vss	This is the negative supply for the device and the reference for all signals and electrical parameters.
2	TELETEXT/DS INPUT/OUTPUT	When strapped to earth (low level), the DA chip will process Teletext. In Viewdata it is the data strobe output to the UAR/T (active low).
3–12	A0 to A9	The 10 bits of address connected to the Address Bus of the Teleview system. As outputs they are tristate and active push pull for high speed driving the store. They are also inputs to enable the device to be addressed.
13	Read/Write Output	The read/write control of the page Stores. The Stores will output data (read) when this signal is high.
1416	SS0-SS2 Outputs	Three bits of Store Select code enabling one of the eight page Stores.
17	RSYNC Input/ Output	A low going pulse indicates to the DA the start of a Teletext line. The DA will output a low going pulse within a few microseconds to re-synchronise the Data Slicer.
18	TS2 Input	The second of the two time slot bits which, when true, indicates that the DA may use the Data and address highways.
19-25	RD1-RD7 Inputs	Received Data taken directly from the UAR/T.
26	Parity Error Input	The Parity error signal from the UAR/T.
27–34	<u>D</u> 0− <u>D</u> 7	Data I/O's for connection directly to the Teleview Data highway. As an output the active state is low and there is a passive pull-up on chip so that the signals on the highway may be 'wire-ored'.
35	RDAV Output	Low active signal to the UAR/T which will reset its data available output.
36	DAV Input	The Data Available signal from the UAR/T to indicate a character is available at the RD1-RD7 pins.
37	Teletext Data Input	Serial data input from a Data Slicer (e.g. SL9100). TTL compatible. If not used this input should be held low.
.38	Clock Input	Normally the Teletext clock running at 6.9375 MHz and synchronised to the Teletext data by RSYNC. In Viewdata only applications a 6MHz clock as used by the Video generator may be input here. TTL compatible.
39 ·	Vcc	Connected to +5V. This has a low current requirement and is used mainly for the output drivers.
40	Vdd	Connected to +12V, the main positive supply for the device.

# **OPERATION**

The Data Acquisition (DA) chip takes data from either the TV (Teletext) or telephone line (Viewdata) via the appropriate interface, processes it accordingly to type and user requests and loads the display data in the correct position in one of eight page Stores.

The processing of Teletext and Viewdata information is described in separate sections as is the interchange of data with the rest of Teleview system.

#### TELETEXT

If pin 2 is held low the DA may receive data via the serial Teletext data input.

While TS2 is true the DA will monitor RSYNC and the address highways. If a pulse appears on RSYNC it will process a Teletext data-line. At other times while TS2 is true it will respond to signals on the address highway and interchange data with a Control Device.

While TS2 is false the DA will do nothing.

#### TELETEXT DATA RECEPTION

Data is extracted from the TV video signal by an external

circuit called the Data Slicer. This circuit provides a serial data signal and a clock to the DA's input.

A 0.5µsec negative pulse generated by the MR9735 Video Generator will appear on the RSYNC line just before the data on a possible Teletext line. This pulse stops the clock in the low state and primes the MR9710 to monitor the Teletext Data Input for clock run-in. The first negative transition restarts the clock which is used as a reference against which to compare the incoming signal. If the frequency is correct the MR9710 outputs a second RSYNC pulse which allows accurate resynchronisation of the clock for the rest of the Teletext line. If the frequency check fails the MR9710 goes back to its idle state waiting for a new RSYNC signal or the Data Interchange time.

After a valid clock run in has been detected Teletext data is clocked into a serial to parallel converter and Framing Code detector. A time out will cause DA to go idle, while the detection of Framing Code will byte synchronise the S-P converter and start the DA receiving the Teletext data as shown in Fig.3.

The first two words following the Framing Code have data protected by Hamming Code and the appropriate

checks and corrections are performed. If the row address indicates that the data is a Page Header (Row 0) then the following 8 words are also processed by the Hamming Code circuit. If any Hamming Code fails such that it cannot be corrected, then that data line is rejected.

Requests for pages of Teletext data are input to the DA during the Data Interchange periods, described later. When a new page is selected the Page and Time store in the DA is loaded with all '1's indicating 'don't care' digits. As keys are pressed by the user of the Teleview system the values are loaded into the DA in the appropriate position.

A comparator in the DA compares Magazine, Page and Time digits one at a time as they are received in the data stream with the digits stored. The comparator will give a true output if the digit compares exactly or if the stored digit is all 1 (value 15). Where an incoming digit has a range less than 4 bits, e.g. time hours tens has the range 0-3 or 2 bits, the unused bits will be made to compare.

Every line of data received is checked for comparison on Magazine number. If this does not compare and the row address indicates that the row is not a Page Header then that row is rejected.

If the Magazine number does not compare and it is a Page Header then, with the exception of Rolling Headers, it is again rejected.

From the time that the DA is told that the P key has been pressed until the selected page has been captured for the first time all Page Headers that compare on Magazine number are loaded into the Store except those with the Interrupted Sequence bit (C9) set. This mode of display is referred to as Rolling Headers and provides an indication to the user that data is being received. During this mode the Magazine Serial bit (C11) will over-ride the Magazine comparison. A page of data may be captured when the page number has been fully enetered, i.e. the 3rd digit has been received or the T key has been pressed, and a Page Header is received whose Magazine, page and time digits compare with those stored in the DA. That header and all subsequent data lines with correct Magazine number will be stored up to and excluding the next Page Header of correct Magazine number. A 'Page being received' indication will be set at this time for transmission to the Control device.

When a Page Header is received that fully compares the Control bits accompanying that Header will be stored for subsequent transmission to the Control.

When the content of a data line is ready to be stored that data is loaded into the appropriate Store as defined by the signal from the Control device. Its position in the Store is defined by the Row Address of that data line, the location of the first character being 40 times the Row Address (with the exception of the Page Header which does not have the first 8 characters), with following characters being stored in the next 39 locations of Store.

Each character is checked for odd parity and if the check fails that character is not written. The write signal is removed to avoid overwriting a possible valid character already existing in Store

The last eight characters of every Page Header contain the current clock time and are always written to Store.

## **VIEWDATA**

With pin 2 connected to the Data Strobe input to a UAR/T and not held to earth the DA will process Viewdata.

While TS2 is true the DA is active as far as the Teleview

highways are concerned and it will monitor RSYNC and the Address highway.

When an RSYNC pulse appears the DA will process any Viewdata character it has available. Whenever it is not processing characters it may receive characters asynchronously from the telephone line, via the exclusive connection to the UAR/T, and store them within the DA. Up to three characters may be received and stored before the next processing period when they may be loaded into the page store. Data Interchange with the Teleview system may occur when TS2 is high.

## ASYNCHRONOUS DATA RECEPTION T-77-07-05

The standard UAR/S (MR1015D) will convert the serial data received via the modem to parallel data for inputting to the DA and indicate a character is ready by the data available (DAV) line. At any time, except when actually processing previously received characters, the DA will read the data and acknowledge on RDAV, a minimum of 3µsec after the DAV signal.

### VIEWDATA CHARACTER PROCESSING

The eight bit input consists of seven bits of data plus a parity fail indication. The codes are shown in Fig.4.

Characters intended for storage are loaded into the Store in a location determined by the Character Address counter which is always arranged to point to the position in Store into which the next character will be written. The counter is manipulated by the Control Characters appearing in Cols. 0 and 1 in the character table.

- 0/8, Back Space, will cause the Character Address counter to be decremented by one.
- 0/9, Horizontal Tab, will cause the Character Address counter to be incremented by one.
- 0/10, Line Feed, will increment by 40.
- 0/11, Vertical Tab, will decrement by 40.
- 0/12, Form Feed, will reset to zero.
- 0/13, Carriage Return, will position the Character Address counter to the beginning of the current block of 40.
- 0/14, Cursor Home, will reset to zero.

A character in columns 2-7 will be written into the appropriate Store at the location indicated by the Character Address counter which will then be incremented by one.

The ESC character (1/11) will cause some modification of the following character as follows:-

If the character is in cols. 4 or 5 it will be written to Store with the most significant bit changed to Zero.

If the character is in col. 3 it will not be written to Store but made ready for transmitting to the Control device.

Any other characters, except NUL, will cancel the ESC sequence and be ignored.

The Form Feed character (0/12) will cause the F bit to be set in the appropriate DA to Control signalling word.

All other control characters in cols. 0 and 1, except NUL, will be sent to the Control at the appropriate time.

If any character has the parity fall indication set then the character 7/15 will be written to Store. At the start of a processing period (i.e. at RSYNC) if a character is available for processing then the DA will erase the Cursor bit by reading the location pointed to by the Character.

# MR9710 PLESSEY SEMICONDUCTORS

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Address counter and re-write it. Since the DA never writes the 8th bit in the Store the cursor will be removed.

**DATA INTERCHANGE** 

During the DA's active period, indicated by TS2, when it is not performing any data processing then it will monitor the Address highway for the following codes:

1111XXXXOX indicates the DA should receive data from the data highway.

1111XXXXXO indicates that the DA should send data to the data highway.

1111X0XXXX indicates that the DA should provide control to the UAR/T.

In the Receive mode the Control device may send data according to the codes in Table 1. The most significant bit of the data acts as a strobe which will cause the other 7 bits to be received and stored in the DA. Magazine, Page and Time digits will be stored in the appropriate location in the digit store, the Store Select number will be stored for use when accessing the Store and the indications of P and T keys being processed will also be latched for use in

the processing period.

T-77-07-05

The receiving of data from the Control is completely asynchronous to the DA's internal clock and is controlled entirely by the Strobe bit.

The Send mode will cause the DA to apply the first code, shown in Table 2, to the data highway. When the code has been read by Control the signal will be acknowledged by Control forcing all 1's (low levels) which will step the DA onto the second word and so on. The Strobe bit is used in this case to indicate that the data is appearing for the first time and once read by Control, is cleared until new data is available. The exception is the first word which always has the Strobe set.

The UAR/T control is recognised by the DA since it has the UAR/T connections and in this mode a Strobe on the data highway will cause the DA to provide a data strobe  $\overline{\text{DS}}$  to the UAR/T.

During the Data Interchange period the DA will monitor the Store Select lines and if they are all taken low it will output the current content of the Character Address counter to the address highway so that the Control may know where to insert the cursor.

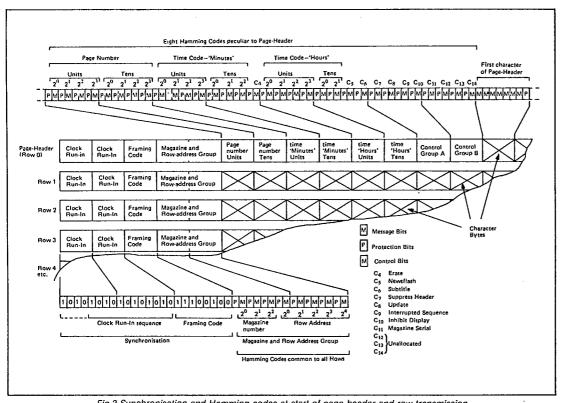


Fig.3 Synchronisation and Hamming codes at start of page-header and row transmission

														T-:	77-0	07-0	)5
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-	8		-	<b>P P</b>	17	-	per :	-	P.			<u></u>			15	771	
<u> </u>	9	┞┸-			U	70	0		<u> </u>	<u>-</u>				<del>-</del>	E		0
0	55		Graphics Red	Graphics <sub>Green</sub>	GraphicsYellow	Graphics Blue	Graphics <sub>Magenta</sub>	Graphics <sub>Cyan</sub>	Graphics <sub>White</sub>	Conceal Display	Contig Graphics	Separated Graphics		Black Background	New Background	Hold Graphics	Release Graphics
<del>-</del>	r,	۵	ø	Œ	v	⊢	<u></u>	>	≥	×	>	Ν	<b></b>	×	<b>↑</b>	<b>←</b>	#
0	4b		Alpha <sup>n</sup> Red	Alpha <sup>n</sup> Green	Alpha <sup>n</sup> Yellow	Alpha Blue	Alpha <sup>n</sup> Magenta	Alpha <sup>n</sup> Cyan	Alpha White	Flash	Steady	End Box	Start Box	Normal Height	Double Height	Special Graphics	Normal Graphics
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	b7b6bsb4b3b2b1	0 0 0 0	0 0 0 1	0 0 1 0	0 0 1 1	0100	0 1 0 1	0110	0111	1000	1001	1010	1 0 1 1	1 1 0 0	1101	1110	1111

Fig.4 Viewdata transmission codes recognised by the MR9710

# MR9710 PLESSEY SEMICONDUCTORS 12E D 7220513 0009370 1

### CONTROL TO DATA ACQUISITION SIGNALLING

Active low signalling, most significant bit is a strobe.

ens nits ens		0000 0000 1000 Dddd 1001 Dddd 1010 Dddd 1011 OSss 1011 10Kk 1011 1100 1011 1110 1011 1111
ens nits ens		1001 Dddd 1010 Dddd 1011 OSss 1011 10Kk 1011 1100 1011 1101 1011 1110
ens		1010 Dddd 1011 OSss 1011 10Kk 1011 1100 1011 1101 1011 1110 1011 1111
		1011 10Kk 1011 1100 1011 1101 1011 1110 1011 1111
		1011 1100 1011 1101 1011 1110 1011 1111
		1011 1101 1011 1110 1011 1111
		1011 1110 1011 1111
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Table 1

Sss is store select number, 000 to 111.

Dddd, Digit key value, initially values 0-9 and 15 used although any value may be sent. For Teletext the magazine range is 0-7, Time hours tens range 0-3, Time minutes tens range 0-7. In addition digit 15 is recognised by the DA as a 'don't care' digit causing automatic comparison.

### DATA ACQUISITION TO CONTROL SIGNALLING

Active low signalling, most significant bit is a strobe, Signals acknowledged by the Control forcing all ones. Control word 1 is sent first and is always sent.

ontrol word 1 is	sent fir	st and is	always	sent.	_	T
Control word	1	1000	T	s	s	s
Where T		is the	Teletex	t bit, 1	= Tel	etext.
S s s			Store Scurrent			er the
Control word Viewdata is be			on wh	ether	Telete	xt or
TELETEXT						
Control word	2	1001	PBR	C4	C6	C5
	3	1010	C10	C9	C8	C7
	4	1011	C14	C13	C12	C11
Sent* only wh	nen Valid	d Heade	r receiv	ed.		
PBR is set whi	ile a pag	e is bein	g receiv	ed.		
C4 to C14 are	the Tel	etext Co	ntrol b	its.		
VIEWDATA		•				
Control word,	, 2	1001	X	F	0	0
	3	1010	b7	0	b6	b5
	4	1011	b4 <sup>-</sup>	b3	b2	b1
Sent* only w	hen a C	ontrol c	haracte	r recei	ved b	y DA.
F is set when	Form Fe	ed chara	acter pr	ocesse	d.	
b1-b7 are the	7 bits c	omprisin	g the V	iewdat	a Chai	acter.

Table 2

\*NOTE: that 'sent' means the Strobe bit is set. The other seven bits are actually put onto the highway at the request of the Control and may be used if appropriate (page being received, for example).

# PLESSEY SEMICONDUCTORS 12E D 7220513 0009371 3

# **ELECTRICAL CHARACTERISTICS**

**Maximum Ratings** 

Voltage on any pin with respect to Vss

Storage Temperature

-0.3V to +15V -55°C to +150°C T-77-07-05

Exceeding these ratings could cause permanent damage, Functional operation is not guaranteed under these conditions, the operating ranges are specified below.

**Operating Conditions** 

Supply Voltages

VSS = 0V (substrate voltage)

 $VCC = +5V \pm 5\%$   $VDD = +12V \pm 10\%$   $0^{\circ}C \text{ to } +70^{\circ}C$ 

Temperature Range

Characteristic	Min	Тур	Max	Units	Conditions
OUTPUTS Address Outputs (tri-state)					
High level	+2.4		Vcc	٧	loh = -320μA
Low level		+0.2	+0.45	V	lol = 3.2mA
Capacitance			15	рF	V = 0V
Trise, Tfall	· ·	,	200	ns	C load = 100pF
Leakage, high impedance state			5	μΑ	V out = 0V or +5V
Data Outputs (passive pull-up)					
High Level	+2.4		Vcc	٧	loh = -1.5mA
Low Level		+0.2	+0.45	V	lol = 3.2mA
Capacitance	'		15	рF	V out = 0V
R/W and Store Select Outputs					
High Level	+2.4		Vcc	v	Ioh = -320μA
Low Level		+0.2	+0.45	V	Iol = 3.2mA
Capacitance			15	pF	V out = 0V
Current sourced, 'off' state	1.2		2.6	mΑ	V out = 0V
RDAV and DS Outputs			:		
High Level	+2,4		Vcc	V	loh = −25μA
Low Level	į	+0.2	+0.45	V	ioi = 100μA
Capacitance	į		15	pF	V out = 0V
RSYNC Output (Open Drain)					-
Low Level	1	+0.2	+0.45	V	iol = 4mA
Leakage, output off		ł	10	μΑ	V out = +12V
INPUTS (except Clock and		ł			
Teletext Data)			١		
High Level	2.2		Vdd	V	
Low Level	Vss		+0.8	V	
Leakage (except I/O's) Input Capacitance			10	μA	V = +12V V in = 0V
Clock and Teletext Data Inputs			15	pF	V In = 0V
•	1 00	<u> </u>	773-1	,	
High Level Low Level	2.8		Vdd	V	
Capacitance	Vss	1	0.4		V in = 0V
Capacitance Leakage	1		20	pF 	V in = UV V in = +12V
Frequency	1.0		10 7,5	μA MHz	V III - T12V
	'.0			IVITIZ	
POWER					
Vcc Supply Current	1		15	mΑ	Vcc = +5.0V
Vdd Supply Current			72	mA-	Vdd = +12V (at 25°C)