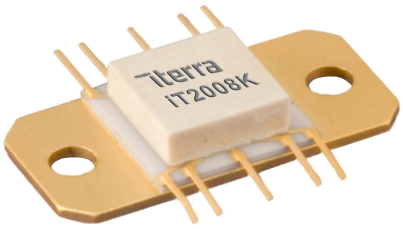
iT2008K
10 MHz – 20 GHz High Power Amplifier

Description

The iT2008K is a broadband traveling wave amplifier designed for high output power applications where low-frequency extension capabilities are also required. The iT2008K provides saturated output power greater than 29 dBm up to 14 GHz and greater than 25 dBm up to 20 GHz. Average gain is 9.5 dB to 20 GHz. DC power consumption as low as 3.15 W is obtained by biasing for best output power and good linearity. Input and output ports are DC coupled.

Features

- Frequency range: 2 GHz – 20 GHz with low-frequency extension to 10 MHz
- P_{3dB} (2 GHz – 14 GHz): 29 dBm
- P_{3dB} (14 GHz – 20 GHz): 27 dBm
- Gain: 9.5 dB
- DC power consumption: 3.15 W
- DC bias conditions: 9 V at 350 mA
- "K" type ceramic flange package



Absolute Maximum Ratings

Symbol	Parameters/conditions	Min.	Max.	Units
V_{DD}	Positive supply voltage		11	V
V_{GG}	Negative supply voltage	-2	0	V
I_{DD}	Positive supply current		900	mA
I_{GG}	Negative supply current		1.8	mA
Pin	RF input power		25	dBm
Pdiss_DC	DC power dissipation (no RF)		5	W
Tch	Operating channel temperature		150	℃
Tm	Mounting temperature (30 s)		320	℃
Tst	Storage temperature	-65	150	℃

Electrical Characteristics

(at 25 ℃)
50 ohm system
V_{DD} = +9 V
Quiescent current (I_{DDQ}) = 350 mA

Symbol	Parameters/conditions	Min.	Typ.	Max.	Units
BW	Frequency range	2		20	GHz
S21	Small signal gain	7.5	9.5		dB
	Gain flatness			+/-2	dB
S11	Input return loss		-12	-8	dB
S22	Output return loss		-12	-8	dB
S12	Isolation	25			dB
P_{3dB}	Output power at 3 dB gain compression				
	2 - 14 GHz	27.5	29		dBm
	14 - 20 GHz	25.5	27		dBm
P_{1dB}	Output power at1 dB gain compression				
	2 - 14 GHz	26.5	28		dBm
	14 - 20 GHz	24.5	26		dBm

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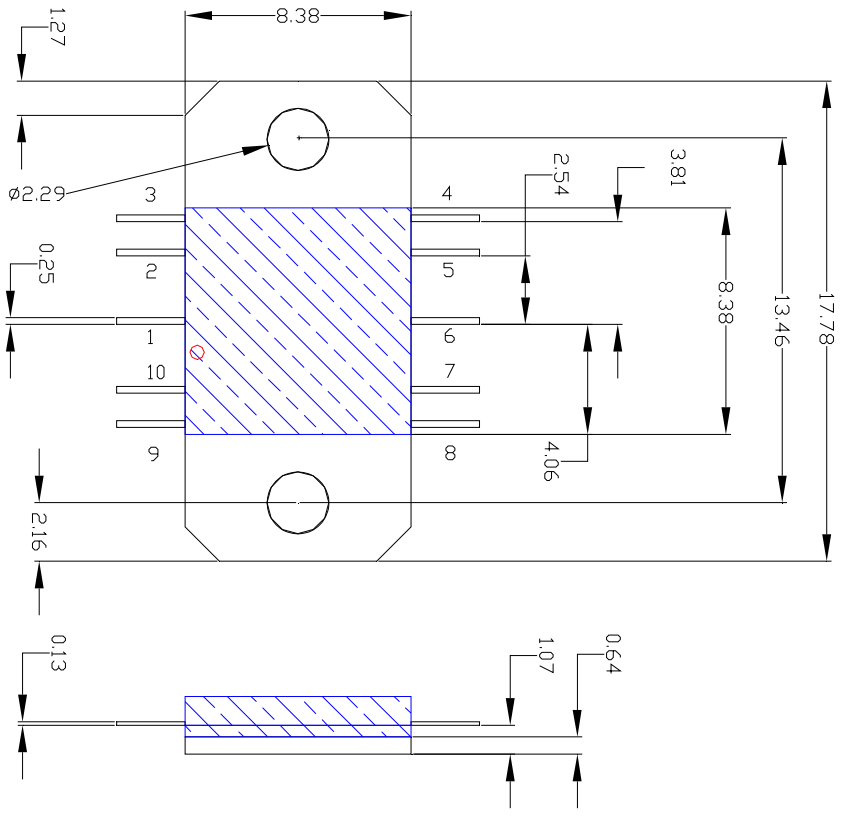
Thermal Characteristics

Symbol	Parameters/conditions	Rth_jb (°C/W)	Tch (°C)	MTFF (Hours)
Rth_jb	Thermal resistance junction-Backside of die No RF: DC bias V_{DD} = 9 V, I_{DQ} = 350 mA , P_{DC} = 3.15 W Tbase = 70 C	10.6	103	>> +1E7
Rth_jb	Thermal resistance junction-Backside of die RF applied: Ouput P3dB = 29 dBm , V_{DD} = 9 V, P_{DISS} = 4.4 W Tbase = 70 C	10.6	117	>> +1E7

Device Diagram

Package Style "K"



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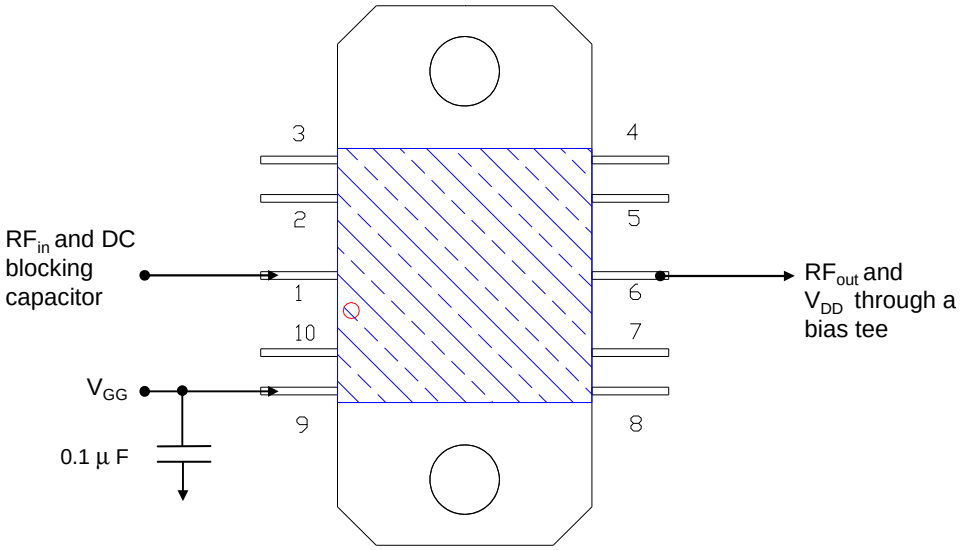
Recommended Assembly Diagram for 2 GHz to 20 GHz Applications

The bypass capacitor on the V_{DD} bias tee must be ≥100 µ F



Pinouts:

1: RF_{input}	6: RF_{output} and V_{dd}
2: NC	7: NC
3: NC	8: NC
4: NC	9: V_{gg}
5: NC	10: NC

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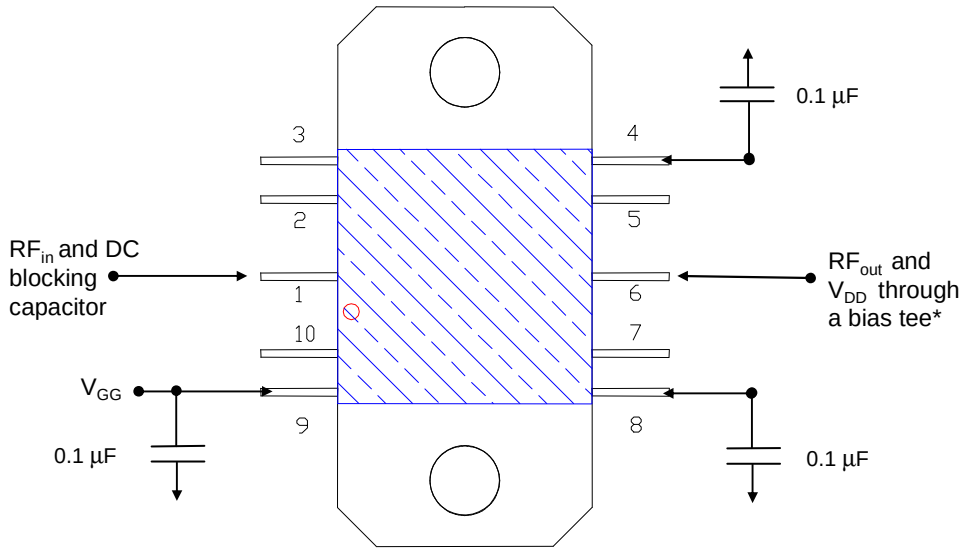
Recommended Assembly Diagram for 10 MHz to 20 GHz Applications

The bypass capacitor on the V_{DD} bias tee must be ≥100 µF



Pinouts:

1: RF$_{input}$	6: RF$_{output}$ and V$_{dd}$
2: NC	7: NC
3: NC	8: Low frequency extension
4: Low frequency extension	9: V$_{gg}$
5: NC	10: NC

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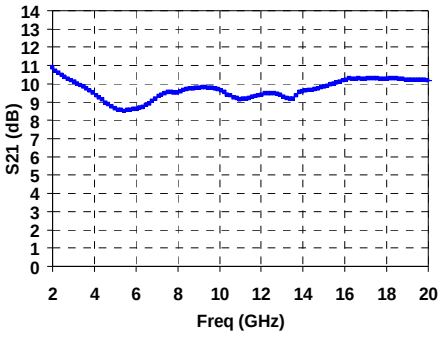
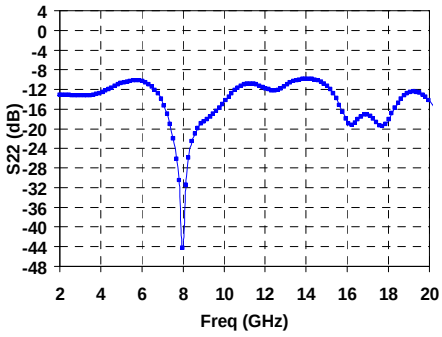
Performance Data
At 25° C

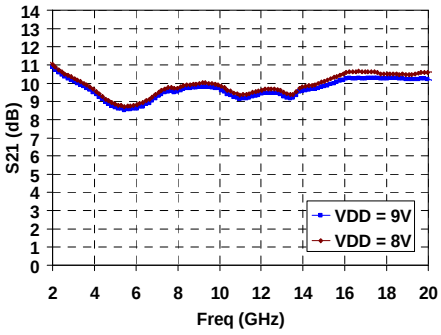
Gain
V_{DD} = 9 V, I_{DDQ} = 350 mA.



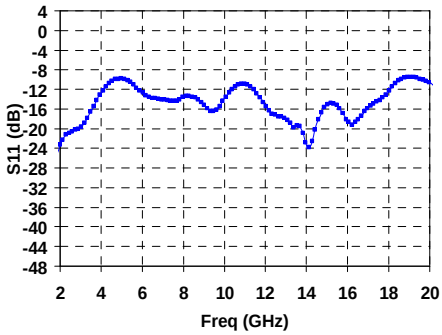
Output Return Loss
V_{DD} = 9 V, I_{DDQ} = 350 mA.



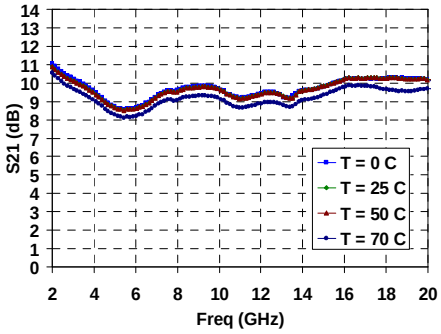
Gain vs. V_{DD}
I_{DDQ} = 350 mA.



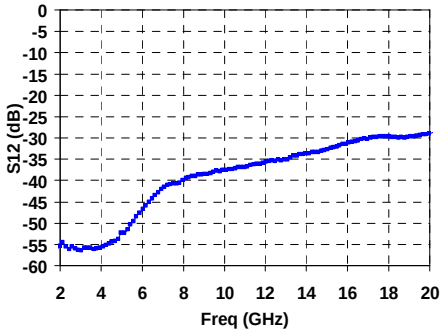
Input Return Loss
V_{DD} = 9 V, I_{DDQ} = 350 mA.



Gain vs. Temperature
V_{DD} = 9 V.



Isolation
V_{DD} = 9 V, I_{DDQ} = 350 mA.



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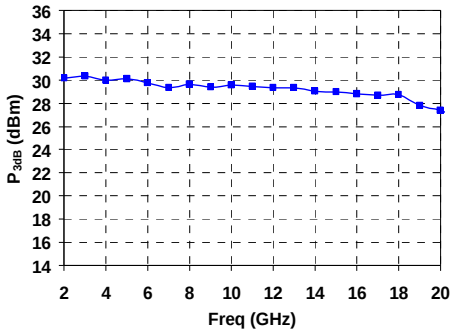
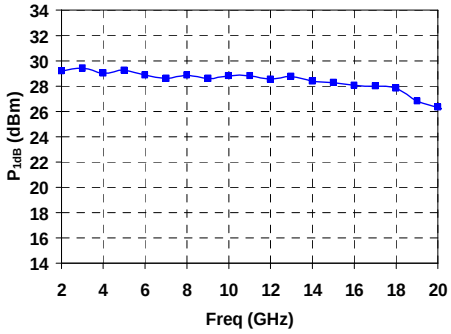
Performance Data

At 25º C

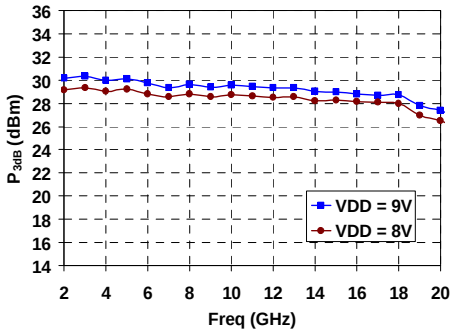
Output P_{3dB}
V_{DD} = 9 V, I_{DDQ} = 350 mA.



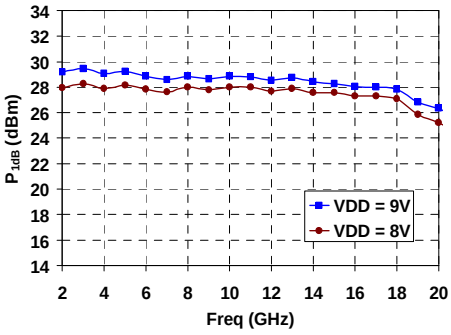
Output P_{1dB}
V_{DD} = 9 V, I_{DDQ} = 350 mA.



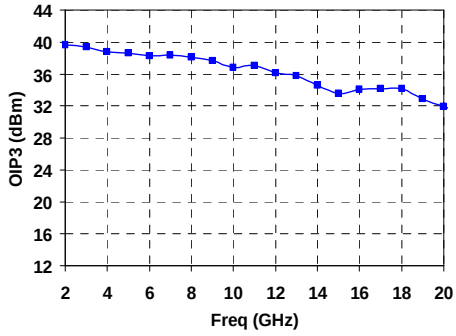
Output P_{3dB} vs. V_{DD}
I_{DDQ} = 350 mA.



Output P_{1dB} vs. V_{DD}
I_{DDQ} = 350 mA.



Output IP3
V_{DD} = 9 V, I_{DDQ} = 350 mA.



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Recommended Procedure for Biasing and Operation

CAUTION: LOSS OF GATE VOLTAGE (V_{GG}) WHILE CORRESPONDING DRAIN VOLTAGE (V_{DD}) IS PRESENT CAN DAMAGE THE AMPLIFIER.

The following procedure must be considered to properly test the amplifier.

The iT2008K amplifier is biased with a positive drain supply (V_{DD}) and one negative gate supply (V_{GG}). The recommended bias conditions for the iT2008 are V_{DD} = 9.0 V, I_{DDQ} = 350 mA. To achieve this drain current level, V_{GG} is typically biased between –0.7 V and –0.9 V. Drain bias V_{DD} MUST be applied through lead 6. An external DC blocking capacitor is needed at the RFin (1) lead. The gate voltage (V_{GG}) MUST be applied prior to the drain voltage (V_{DD}) during power-up and removed after the drain voltage is removed during the power-down.

CAUTION: LOSS OF GATE VOLTAGE (VGG) WHILE CORRESPONDING DRAIN VOLTAGE (VDD) IS PRESENT CAN DAMAGE THE AMPLIFIER.

Biasing sequence:

1. Apply –2 V to V_{GG}.
2. Apply 0 V to V_{DD}.
3. Adjust V_{DD} to 4.5 V.
4. Adjust V_{GG} to –1 V.
5. Adjust V_{DD} to 9 V.
6. Adjust V_{GG} to attain I_{DD} = 350 mA total current.

(V_{GG}, typically biased between –0.7 V and –0.9 V).

Low-Frequency Operation

An external DC blocking capacitor is needed at the RFin (1) lead. 0.1 µF capacitors on leads (4,8) are necessary for low frequency extension. An external low-loss bias tee at the RFout (6) must be used for applications as low as 10 MHz. It is recommended that the drain bias tee be decoupled with a large capacitance (≥100 µF) for low frequency stability.

Application Information

CAUTION: THIS IS AN ESD SENSITIVE DEVICE

These devices should be handled with care and stored in a dry nitrogen environment. These are ESD sensitive devices and should be handled with appropriate caution, including the use of wrist-grounding straps. All die attach and wire/ribbon bond equipment must be grounded to prevent static discharges through the device.

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