NEC

MOS INTEGRATED CIRCUIT

μPD78F0034B, 78F0034BY, 78F0034B(A), 78F0034BY(A)

8-BIT SINGLE-CHIP MICROCONTROLLERS

DESCRIPTION

The μPD78F0034B is a member of the μPD780034A Subseries in the 78K/0 Series, and is equivalent to the μPD780034A (expanded-specification product) but with flash memory in place of internal ROM.

The μPD78F0034BY is a member of the μPD780034AY Subseries, featuring flash memory in place of the internal ROM of the μPD780034AY.

The μPD78F0034B(A) and 78F0034BY(A) are products to which a quality assurance program more stringent than that used for the μPD78F0034B and 78F0034BY (standard models) is applied (NEC Electronics classifies these products as "special" quality grade models).

The μPD78F0034B, 78F0034BY, 78F0034B(A), and 78F0034BY(A) incorporate flash memory, which can be programmed and erased while mounted on the board.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μPD780024A, 780034A, 780024AY, 780034AY Subseries User's Manual: U14046E
78K/0 Series Instruction User's Manual: U12326E

FEATURES

- Pin-compatible with mask ROM versions (except V_{PP} pin)
- Flash memory: 32 KB**Note**
- Internal high-speed RAM: 1,024 bytes**Note**
- Supply voltage: V_{DD} = 1.8 to 5.5 V

Note The flash memory and internal high-speed RAM capacities can be changed with the memory size switching register (IMS).

Remark For the differences between the flash memory and the mask ROM versions, refer to **4. DIFFERENCES BETWEEN μPD78F0034B, 78F0034BY, AND MASK ROM VERSIONS**.

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ORDERING INFORMATION

Part Number	Package	Internal ROM
μPD78F0034BGB-8EU	64-pin plastic LQFP (10 x 10)	Flash memory
μPD78F0034BGC-8BS	64-pin plastic LQFP (14 x 14)	Flash memory
μPD78F0034BGK-9ET	64-pin plastic TQFP (12 x 12)	Flash memory
μPD78F0034BF1-CN3	73-pin plastic FBGA (9 x 9)	Flash memory
μPD78F0034BGB(A)-8EU	64-pin plastic LQFP (10 x 10)	Flash memory
μPD78F0034BGC(A)-8BS	64-pin plastic LQFP (14 x 14)	Flash memory
μPD78F0034BGK(A)-9ET	64-pin plastic TQFP (12 x 12)	Flash memory
μPD78F0034BYGB-8EU	64-pin plastic LQFP (10 x 10)	Flash memory
μPD78F0034BYGC-8BS	64-pin plastic LQFP (14 x 14)	Flash memory
μPD78F0034BYGK-9ET	64-pin plastic TQFP (12 x 12)	Flash memory
μPD78F0034BYF1-CN3	73-pin plastic FBGA (9 x 9)	Flash memory
μPD78F0034BYGB(A)-8EU	64-pin plastic LQFP (10 x 10)	Flash memory
μPD78F0034BYGC(A)-8BS	64-pin plastic LQFP (14 x 14)	Flash memory
μPD78F0034BYGK(A)-9ET	64-pin plastic TQFP (12 x 12)	Flash memory

QUALITY GRADE

Part Number	Package	Quality Grade
μPD78F0034BGB-8EU	64-pin plastic LQFP (10 x 10)	Standard
μPD78F0034BGC-8BS	64-pin plastic LQFP (14 x 14)	Standard
μPD78F0034BGK-9ET	64-pin plastic TQFP (12 x 12)	Standard
μPD78F0034BF1-CN3	73-pin plastic FBGA (9 x 9)	Standard
μPD78F0034BGB(A)-8EU	64-pin plastic LQFP (10 x 10)	Special
μPD78F0034BGC(A)-8BS	64-pin plastic LQFP (14 x 14)	Special
μPD78F0034BGK(A)-9ET	64-pin plastic TQFP (12 x 12)	Special
μPD78F0034BYGB-8EU	64-pin plastic LQFP (10 x 10)	Standard
μPD78F0034BYGC-8BS	64-pin plastic LQFP (14 x 14)	Standard
μPD78F0034BYGK-9ET	64-pin plastic TQFP (12 x 12)	Standard
μPD78F0034BYF1-CN3	73-pin plastic FBGA (9 x 9)	Standard
μPD78F0034BYGB(A)-8EU	64-pin plastic LQFP (10 x 10)	Special
μPD78F0034BYGC(A)-8BS	64-pin plastic LQFP (14 x 14)	Special
μPD78F0034BYGK(A)-9ET	64-pin plastic TQFP (12 x 12)	Special

Please refer to "Quality Grades on NEC Semiconductor Devices" (Document No. C11531E) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

CORRESPONDENCE BETWEEN MASK ROM PRODUCTS AND FLASH MEMORY PRODUCTS

• μPD780024A, 780034A Subseries

Mask ROM Products	Flash Memory Products
Expanded-specification products of μPD780021A, 780022A, 780023A, 780024A Expanded-specification products of μPD780031A, 780032A, 780033A, 780034A	μPD78F0034B
Conventional products of μPD780021A, 780022A, 780023A, 780024A Conventional products of μPD780031A, 780032A, 780033A, 780034A	μPD78F0034A
Expanded-specification products of μPD780021A(A), 780022A(A), 780023A(A), 780024A(A) Expanded-specification products of μPD780031A(A), 780032A(A), 780033A(A), 780034A(A)	μPD78F0034B(A)
Conventional products of μPD780021A(A), 780022A(A), 780023A(A), 780024A(A) Conventional products of μPD780031A(A), 780032A(A), 780033A(A), 780034A(A)	μPD78F0034B(A)

Caution The μPD78F0034B(A) and conventional products of the μPD780021A(A), 780022A(A), 780023A(A), 780024A(A) and μPD780031A(A), 780032A(A), 780033A(A), and 780034A(A) differ in the operating frequency ratings. When using the mask ROM versions in place of the flash memory versions, take note of the power supply voltage and operating frequency used.

Remarks 1. The μPD78F0034B, 78F0034B(A) and 78F0034A differ in the operating frequency ratings and communication mode of the flash memory programming. Refer to **5. DIFFERENCES BETWEEN μPD78F0034B, 78F0034BY AND μPD78F0034A, 78F0034AY**.

2. The expanded-specification products and conventional products of the mask ROM versions differ in the operating frequency ratings. Refer to the data sheets of the products.

3. The special grade version of the μPD78F0034A is not provided (only the standard grade version is provided).

• μPD780024AY, 780034AY Subseries

Mask ROM Products	Flash Memory Products
μPD780021AY, 780022AY, 780023AY, 780024AY μPD780031AY, 780032AY, 780033AY, 780034AY	μPD78F0034AY μPD78F0034BY
μPD780021AY(A), 780022AY(A), 780023AY(A), 780024AY(A) μPD780031AY(A), 780032AY(A), 780033AY(A), 780034AY(A)	μPD78F0034BY(A)

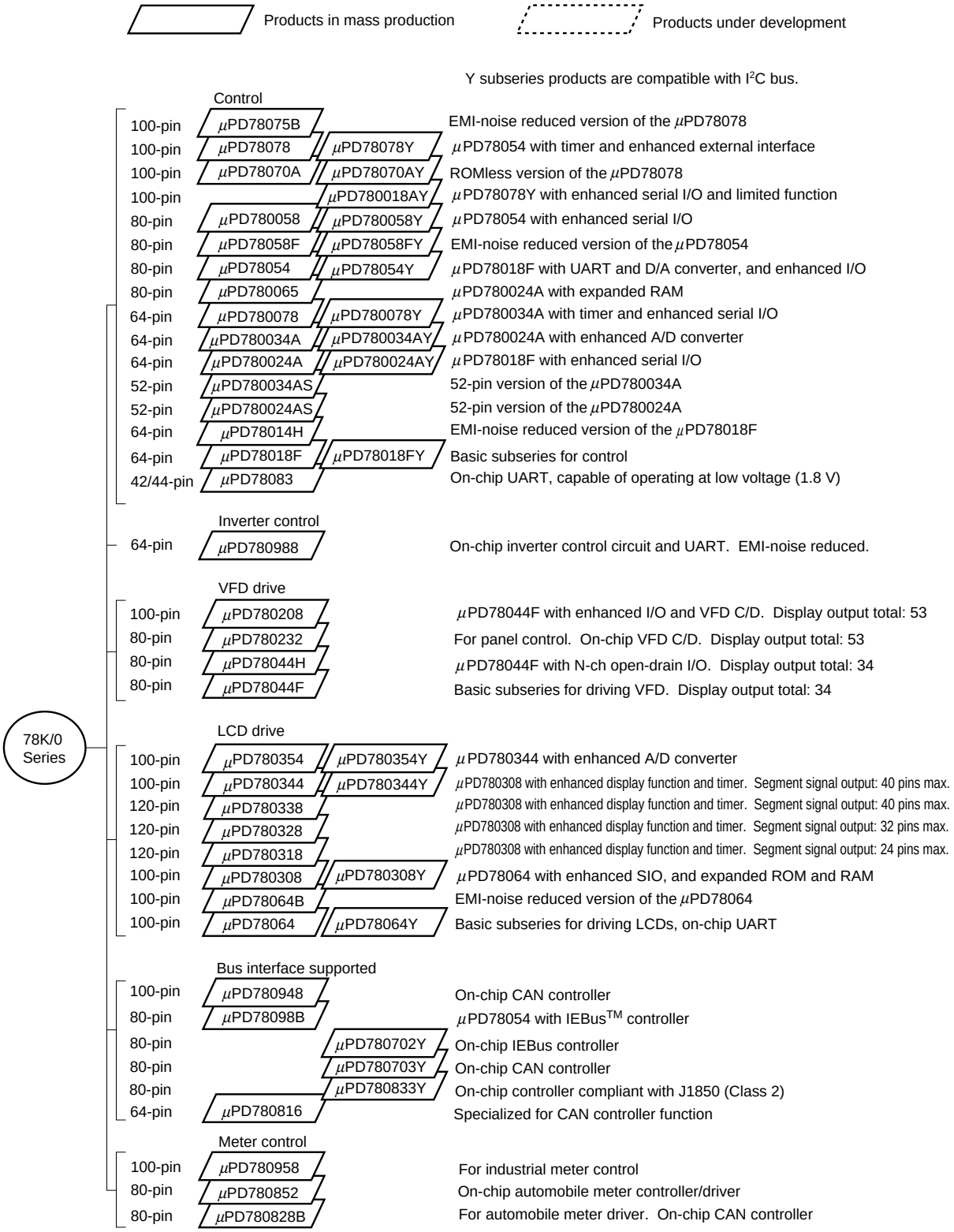
Remarks 1. The μPD78F0034BY, 78F0034BY(A) and 78F0034AY differ in the communication mode of the flash memory programming. Refer to **5. DIFFERENCES BETWEEN μPD78F0034B, 78F0034BY AND μPD78F0034A, 78F0034AY.**

2. The expanded-specification products of the μPD780024AY, 780034AY Subseries are not provided (only the conventional products are provided).

3. The special grade version of the μPD78F0034A is not provided (only the standard grade version is provided).

78K/0 SERIES LINEUP

The products in the 78K/0 Series are listed below. The names enclosed in boxes are subseries names.



Remark VFD (Vacuum Fluorescent Display) is referred to as FIP™ (Fluorescent Indicator Panel) in some documents, but the functions of the two are same.

The major functional differences among the subseries are listed below.

- Non-Y subseries

Subseries Name \ Function		ROM Capacity (Bytes)	Timer				8-Bit A/D	10-Bit A/D	8-Bit D/A	Serial Interface	I/O	V_{DD} MIN. Value	External Expansion
			8-Bit	16-Bit	Watch	WDT							
Control	μPD78075B	32 K to 40 K	4 ch	1 ch	1 ch	1 ch	8 ch	–	2 ch	3 ch (UART: 1 ch)	88	1.8 V	√
	μPD78078	48 K to 60 K											
	μPD78070A	–									61	2.7 V	
	μPD780058	24 K to 60 K	2 ch							3 ch (time-division UART: 1 ch)	68	1.8 V	
	μPD78058F	48 K to 60 K								3 ch (UART: 1 ch)	69	2.7 V	
	μPD78054	16 K to 60 K										2.0 V	
	μPD780065	40 K to 48 K							–	4 ch (UART: 1 ch)	60	2.7 V	
	μPD780078	48 K to 60 K		2 ch			–	8 ch		3 ch (UART: 2 ch)	52	1.8 V	
	μPD780034A	8 K to 32 K		1 ch						3 ch (UART: 1 ch)	51		
	μPD780024A						8 ch	–					
	μPD780034AS						–	4 ch			39		–
	μPD780024AS						4 ch	–					
	μPD78014H						8 ch			2 ch	53		√
	μPD78018F	8 K to 60 K											
	μPD78083	8 K to 16 K		–	–					1 ch (UART: 1 ch)	33		–
Inverter control	μPD780988	16 K to 60 K	3 ch	**Note**	–	1 ch	–	8 ch	–	3 ch (UART: 2 ch)	47	4.0 V	√
VFD drive	μPD780208	32 K to 60 K	2 ch	1 ch	1 ch	1 ch	8 ch	–	–	2 ch	74	2.7 V	–
	μPD780232	16 K to 24 K	3 ch	–	–		4 ch				40	4.5 V	
	μPD78044H	32 K to 48 K	2 ch	1 ch	1 ch		8 ch			1 ch	68	2.7 V	
	μPD78044F	16 K to 40 K								2 ch			
LCD drive	μPD780354	24 K to 32 K	4 ch	1 ch	1 ch	1 ch	–	8 ch	–	3 ch (UART: 1 ch)	66	1.8 V	–
	μPD780344						8 ch	–					
	μPD780338	48 K to 60 K	3 ch	2 ch			–	10 ch	1 ch	2 ch (UART: 1 ch)	54		
	μPD780328										62		
	μPD780318										70		
	μPD780308	48 K to 60 K	2 ch	1 ch			8 ch	–	–	3 ch (time-division UART: 1 ch)	57	2.0 V	
	μPD78064B	32 K								2 ch (UART: 1 ch)			
	μPD78064	16 K to 32 K											
Bus interface supported	μPD780948	60 K	2 ch	2 ch	1 ch	1 ch	8 ch	–	–	3 ch (UART: 1 ch)	79	4.0 V	√
	μPD78098B	40 K to 60 K		1 ch					2 ch		69	2.7 V	–
	μPD780816	32 K to 60 K		2 ch			12 ch		–	2 ch (UART: 1 ch)	46	4.0 V	
Meter control	μPD780958	48 K to 60 K	4 ch	2 ch	–	1 ch	–	–	–	2 ch (UART: 1 ch)	69	2.2 V	–
Dash-board control	μPD780852	32 K to 40 K	3 ch	1 ch	1 ch	1 ch	5 ch	–	–	3 ch (UART: 1 ch)	56	4.0 V	–
	μPD780828B	32 K to 60 K									59		

Note 16-bit timer: 2 channels
10-bit timer: 1 channel

- Y subseries

Subseries Name \ Function		ROM Capacity (Bytes)	Timer				8-Bit A/D	10-Bit A/D	8-Bit D/A	Serial Interface	I/O	V_{DD} MIN. Value	External Expansion
			8-Bit	16-Bit	Watch	WDT							
Control	μPD78078Y	48 K to 60 K	4 ch	1 ch	1 ch	1 ch	8 ch	–	2 ch	3 ch (UART: 1 ch, I^2C: 1 ch)	88	1.8 V	√
	μPD78070AY	–									61	2.7 V	
	μPD780018AY	48 K to 60 K							–	3 ch (I^2C: 1 ch)	88		
	μPD780058Y	24 K to 60 K	2 ch						2 ch	3 ch (time-division UART: 1 ch, I^2C: 1 ch)	68	1.8 V	
	μPD78058FY	48 K to 60 K								3 ch (UART: 1 ch, I^2C: 1 ch)	69	2.7 V	
	μPD78054Y	16 K to 60 K										2.0 V	
	μPD780078Y	48 K to 60 K		2 ch			–	8 ch	–	4 ch (UART: 2 ch, I^2C: 1 ch)	52	1.8 V	
	μPD780034AY	8 K to 32 K		1 ch						3 ch (UART: 1 ch, I^2C: 1 ch)	51		
	μPD780024AY						8 ch	–					
	μPD78018FY	8 K to 60 K								2 ch (I^2C: 1 ch)	53		
LCD drive	μPD780354Y	24 K to 32 K	4 ch	1 ch	1 ch	1 ch	–	8 ch	–	4 ch (UART: 1 ch, I^2C: 1 ch)	66	1.8 V	–
	μPD780344Y						8 ch	–					
	μPD780308Y	48 K to 60 K	2 ch							3 ch (time-division UART: 1 ch, I^2C: 1 ch)	57	2.0 V	
	μPD78064Y	16 K to 32 K								2 ch (UART: 1 ch, I^2C: 1 ch)			
Bus interface supported	μPD780701Y	60 K	3 ch	2 ch	1 ch	1 ch	16 ch	–	–	4 ch (UART: 1 ch, I^2C: 1 ch)	67	3.5 V	–
	μPD780703Y												
	μPD780833Y										65	4.5 V	

Remark Functions other than the serial interface are common to both the Y and non-Y subseries.

OVERVIEW OF FUNCTIONS

Item \ Part Number		μPD78F0034B μPD78F0034B(A)	μPD78F0034BY μPD78F0034BY(A)
Internal memory	Flash memory	32 KB[Note 1]	
	High-speed RAM	1,024 bytes[Note 1]	
Memory space		64 KB	
General-purpose registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)	
Minimum instruction execution time		On-chip minimum instruction execution time cycle variable function	
	When main system	0.166 μs/0.333 μs/0.666 μs/1.33 μs/2.66 μs (@ 12 MHz operation, V_{DD} = 4.5 to 5.5 V)	0.238 μs/0.48 μs/0.95 μs/1.91 μs/3.81 μs (@ 8.38 MHz operation, V_{DD} = 4.0 to 5.5 V)
	When subsystem clock selected	122 μs (@ 32.768 kHz operation)	
Instruction set		• 16-bit operation • Multiply/divide (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, Boolean operation) • BCD adjust, etc.	
I/O ports		Total: 51 • CMOS input: 8 • CMOS I/O: 39 • N-ch open-drain I/O (5 V withstand voltage): 4	
A/D converter		• 10-bit resolution × 8 channels • Operable over a wide power supply voltage range: AV_{DD} = 1.8 to 5.5 V	
Serial interface		• UART mode: 1 channel • 3-wire serial I/O mode: 2 channels	• UART mode: 1 channel • 3-wire serial I/O mode: 1 channel • I^2C bus mode (multimaster supporting): 1 channel
Timers		• 16-bit timer/event counter: 1 channel • 8-bit timer/event counter: 2 channels • Watch timer: 1 channel • Watchdog timer: 1 channel	
Timer outputs		3 (8-bit PWM output capable: 2)	
Clock output		• 93.75 kHz, 187.5 kHz, 375 kHz, 750 kHz, 1.25 MHz, 3 MHz, 6 MHz, 12 MHz (@ 12 MHz operation with main system clock) • 32.768 kHz (@ 32.768 kHz operation with subsystem clock)	• 65.5 kHz, 131 kHz, 262 kHz, 524 kHz, 1.05 MHz, 2.10 MHz, 4.19 MHz, 8.38 MHz (@ 8.38 MHz operation with main system clock) • 32.768 kHz (@ 32.768 kHz operation with subsystem clock)
Buzzer output		1.46 kHz, 2.93 kHz, 5.86 kHz, 11.7 kHz (@ 12 MHz operation with main system clock)	1.02 kHz, 2.05 kHz, 4.10 kHz, 8.19 kHz (@ 8.38 MHz operation with main system clock)
Vectored interrupt sources	Maskable	Internal: 13, external: 5	
	Non-maskable	Internal: 1	
	Software	1	
Test inputs		Internal: 1, external: 1	
Supply voltage		V_{DD} = 1.8 to 5.5 V	
Operating ambient temperature		T_A = –40 to +85°C	
Package		• 64-pin plastic LQFP (10 x 10) • 64-pin plastic LQFP (14 x 14) • 64-pin plastic TQFP (12 x 12) • 73-pin plastic FBGA (9 x 9)[Note 2]	

Notes 1. The capacities of the flash memory and the internal high-speed RAM can be changed with the memory size switching register (IMS).

2. The special grade version of the 73-pin plastic FBGA (9 x 9) is not provided.

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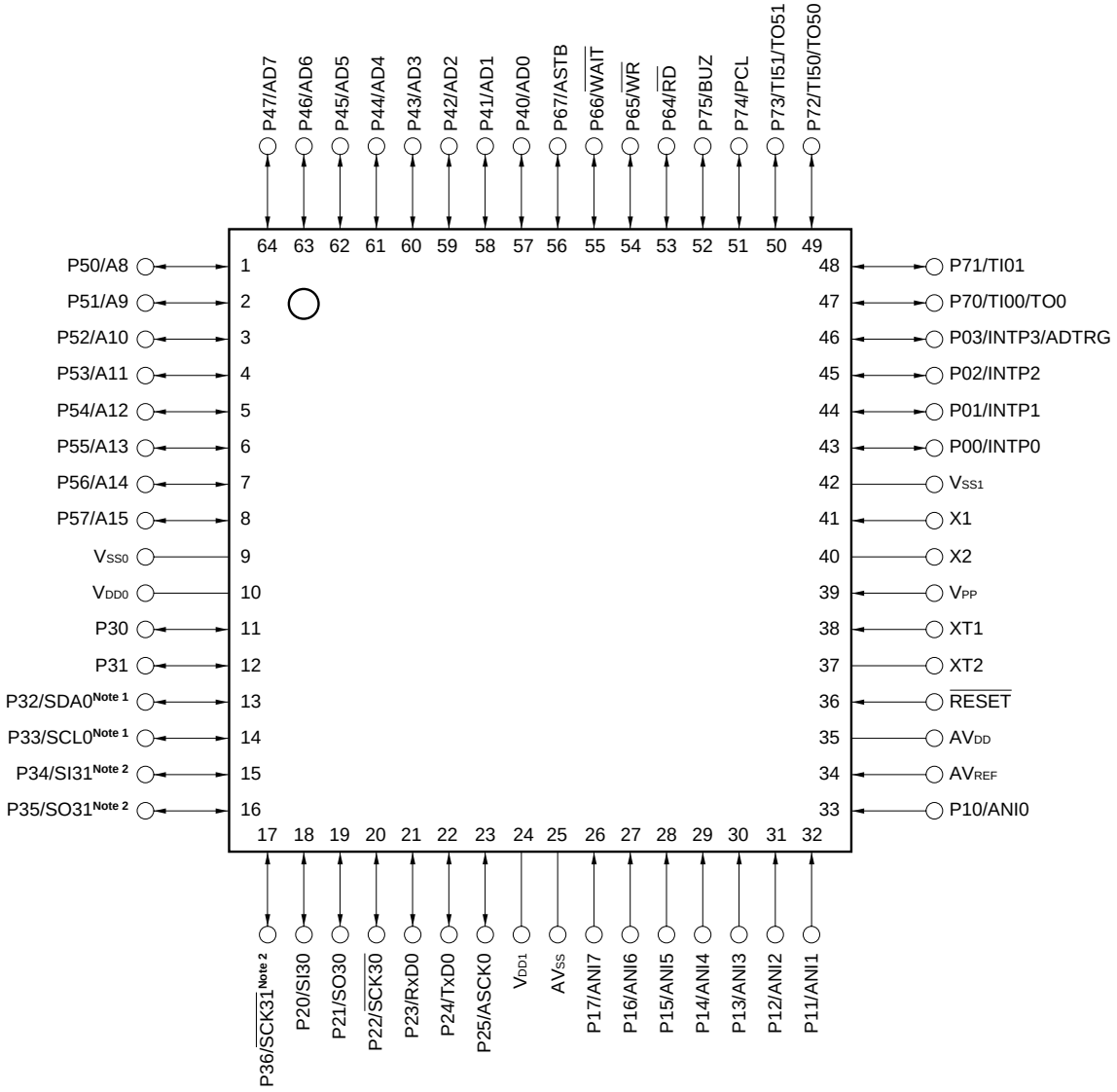
1. PIN CONFIGURATION (TOP VIEW)

- **64-pin plastic LQFP (10 x 10)**
- **64-pin plastic LQFP (14 x 14)**
- **64-pin plastic TQFP (12 x 12)**



Notes 1. SDA0 and SCL0 are incorporated only in the μPD78F0034BY, 78F0034BY(A) Subseries.

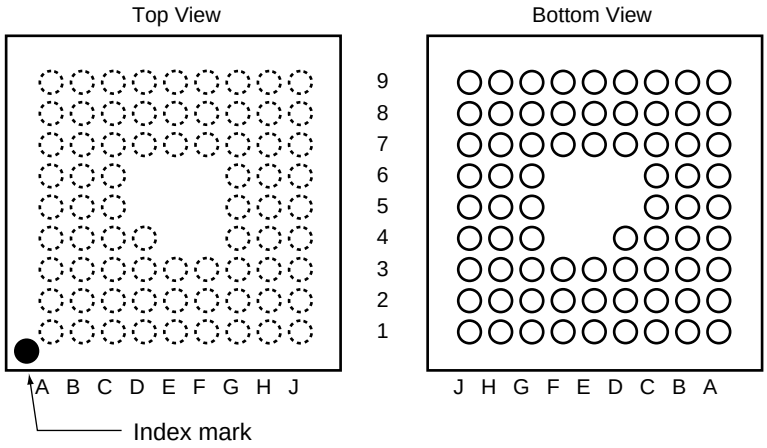
2. SI31, SO31, and $\overline{\text{SCK31}}$ are incorporated only in the μPD78F0034B, 78F0034B(A) Subseries.

Cautions 1. Connect the V_{PP} pin directly to V_{SS0} or V_{SS1} in normal operation mode.

2. Connect the AV_{SS} pin to V_{SS0}.

Remark When the μPD78F0034B, 78F0034BY, 78F0034B(A), and 78F0034BY(A) are used in application fields that require reduction of the noise generated from inside the microcontroller, the implementation of noise reduction measures, such as supplying voltage to V_{DD0} and V_{DD1} individually and connecting V_{SS0} and V_{SS1} to different ground lines, is recommended.

- **73-pin plastic FBGA (9 x 9)**



Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
A1	NC	C1	P52/A10	E1	P57/A15	G1	P33/SCL0Note 1	J1	NC
A2	P46/AD6	C2	P53/A11	E2	V_{DD0}	G2	P32/SDA0Note 1	J2	P36/$\overline{SCK31}$Note 2
A3	P44/AD4	C3	P45/AD5	E3	P54/A12	G3	P20/SI30	J3	NC
A4	P41/AD1	C4	P42/AD2	E4	–	G4	P21/SO30	J4	P25/ASCK0
A5	P67/ASTB	C5	P64/$\overline{RD}$	E5	–	G5	P24/TxD0	J5	NC
A6	P65/$\overline{WR}$	C6	P73/TI51/TO51	E6	–	G6	V_{DD1}	J6	P17/ANI7
A7	P74/PCL	C7	P03/INTP3/ADTRG	E7	P00/INTP0	G7	P16/ANI6	J7	P12/ANI2
A8	NC	C8	P01/INTP1	E8	XT1	G8	AV_{DD}	J8	P13/ANI3
A9	NC	C9	V_{SS1}	E9	X2	G9	NC	J9	NC
B1	P51/A9	D1	P55/A13	F1	P30	H1	P34/SI31Note 2		
B2	P47/AD7	D2	P56/A14	F2	P31	H2	P35/SO31Note 2		
B3	P43/AD3	D3	P50/A8	F3	V_{SS0}	H3	P23/RxD0		
B4	P40/AD0	D4	NC	F4	–	H4	P22/$\overline{SCK30}$		
B5	P66/$\overline{WAIT}$	D5	–	F5	–	H5	AV_{SS}		
B6	P75/BUZ	D6	–	F6	–	H6	P15/ANI5		
B7	P72/TI50/TO51	D7	P02/INTP2	F7	P14/ANI4	H7	P11/ANI1		
B8	P71/TI01	D8	V_{PP}	F8	$\overline{RESET}$	H8	P10/ANI0		
B9	P70/TI00/TO0	D9	X1	F9	XT2	H9	AV_{REF}		

Notes 1. SDA0 and SCL0 are incorporated only in the μPD78F0034BY Subseries.

2. SI31, SO31, and $\overline{SCK31}$ are incorporated only in the μPD78F0034B Subseries.

Cautions 1. Connect the V_{PP} pin directly to V_{SS0} or V_{SS1} in normal operation mode.

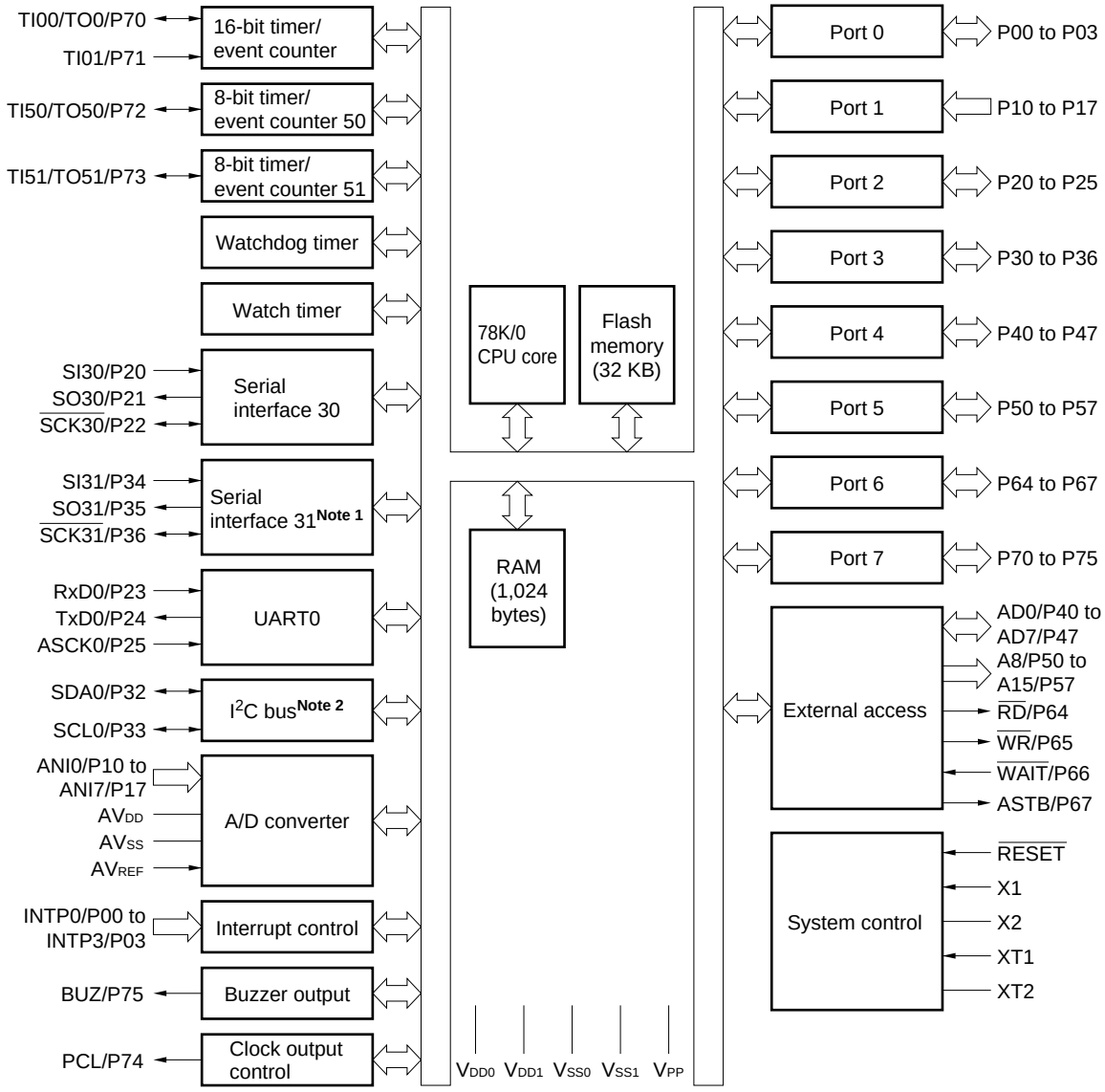
2. Connect the AV_{SS} pin to V_{SS0}.

Remarks 1. When the μPD78F0034B, 78F0034BY, 78F0034B(A), and 78F0034BY(A) are used in application fields that require reduction of the noise generated from inside the microcontroller, the implementation of noise reduction measures, such as supplying voltage to V_{DD0} and V_{DD1} individually and connecting V_{SS0} and V_{SS1} to different ground lines, is recommended.

2. The special grade version of the 73-pin plastic FBGA (9 x 9) is not provided.

A8 to A15:	Address bus	P70 to P75:	Port 7
AD0 to AD7:	Address/data bus	PCL:	Programmable clock
ADTRG:	AD trigger input	$\overline{RD}$:	Read strobe
ANI0 to ANI7:	Analog input	$\overline{RESET}$:	Reset
ASCK0:	Asynchronous serial clock	RxD0:	Receive data
ASTB:	Address strobe	$\overline{SCK30}$, $\overline{SCK31}$, SCL0:	Serial clock
AV_{DD}:	Analog power supply	SDA0:	Serial data
AV_{REF}:	Analog reference voltage	SI30, SI31:	Serial input
AV_{SS}:	Analog ground	SO30, SO31:	Serial output
BUZ:	Buzzer clock	TI00, TI01, TI50, TI51:	Timer input
INTP0 to INTP3:	External interrupt input	TO0, TO50, TO51:	Timer output
NC:	No connection	TxD0:	Transmit data
P00 to P03:	Port 0	V_{DD0}, V_{DD1}:	Power supply
P10 to P17:	Port 1	V_{PP}:	Programming power supply
P20 to P25:	Port 2	V_{SS0}, V_{SS1}:	Ground
P30 to P36:	Port 3	$\overline{WAIT}$:	Wait
P40 to P47:	Port 4	$\overline{WR}$:	Write strobe
P50 to P57:	Port 5	X1, X2:	Crystal (main system clock)
P64 to P67:	Port 6	XT1, XT2:	Crystal (subsystem clock)

2. BLOCK DIAGRAM



Notes 1. Incorporated only in the μPD78F0034B and 78F0034B(A)

2. Incorporated only in the μPD78F0034BY and 78F0034BY(A)

3. PIN FUNCTIONS

3.1 Port Pins (1/2)

Pin Name	I/O	Function		After Reset	Alternate Function
P00	I/O	Port 0 4-bit I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by software.		Input	INTP0
P01					INTP1
P02					INTP2
P03					INTP3/ADTRG
P10 to P17	Input	Port 1 8-bit input-only port.		Input	ANI0 to ANI7
P20	I/O	Port 2 6-bit I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by software.		Input	SI30
P21					SO30
P22					$\overline{\text{SCK30}}$
P23					RxD0
P24					TxD0
P25					ASCK0
P30	I/O	Port 3 7-bit I/O port. Input/output can be specified in 1-bit units.	N-ch open-drain I/O port. LEDs can be driven directly.	Input	–
P31					
P32					SDA0 Note 1
P33					SCL0 Note 1
P34			An on-chip pull-up resistor can be specified by software.		SI31 Note 2
P35					SO31 Note 2
P36					$\overline{\text{SCK31}}$ Note 2
P40 to P47	I/O	Port 4 8-bit I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by software. Interrupt request flag KRIF is set to 1 by falling edge detection.		Input	AD0 to AD7
P50 to P57	I/O	Port 5 8-bit I/O port. LEDs can be driven directly. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by software.		Input	A8 to A15
P64	I/O	Port 6 4-bit I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by software.		Input	$\overline{\text{RD}}$
P65					$\overline{\text{WR}}$
P66					$\overline{\text{WAIT}}$
P67					ASTB

Notes 1. SDA0 and SCL0 are incorporated only in the μPD78F0034BY and 78F0034BY(A).

2. SI31, SO31, and $\overline{\text{SCK31}}$ are incorporated only in the μPD78F0034B and 78F0034B(A).

3.1 Port Pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
P70	I/O	Port 7 6-bit I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by software.	Input	TI00/TO0
P71				TI01
P72				TI50/TO50
P73				TI51/TO51
P74				PCL
P75				BUZ

3.2 Non-Port Pins (1/2)

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	External interrupt request input by which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.	Input	P00
INTP1				P01
INTP2				P02
INTP3				P03/ADTRG
SI30	Input	Serial interface serial data input.	Input	P20
SI31 Note 1				P34
SDA0 Note 2	I/O	Serial interface serial data input/output	Input	P32
SO30	Output	Serial interface serial data output.	Input	P21
SO31 Note 1				P35
$\overline{\text{SCK30}}$	I/O	Serial interface serial clock input/output.	Input	P22
$\overline{\text{SCK31}}$ Note 1				P36
SCL0 Note 2				P33
RxD0	Input	Serial data input for asynchronous serial interface.	Input	P23
TxD0	Output	Serial data output for asynchronous serial interface.	Input	P24
ASCK0	Input	Serial clock input for asynchronous serial interface.	Input	P25
TI00	Input	External count clock input to 16-bit timer/event counter 0. Capture trigger signal input to capture register 01 (CR01) of 16-bit timer/event counter 0.	Input	P70/TO0
TI01		Capture trigger signal input to capture register 00 (CR00) of 16-bit timer/event counter 0.		P71
TI50		External count clock input to 8-bit timer/event counter 50.		P72/TO50
TI51		External count clock input to 8-bit timer/event counter 51.		P73/TO51
TO0	Output	16-bit timer/event counter 0 output.	Input	P70/TI00
TO50		8-bit timer/event counter 50 output (shared with 8-bit PWM output).	Input	P72/TI50
TO51		8-bit timer/event counter 51 output (shared with 8-bit PWM output).		P73/TI51
PCL	Output	Clock output (for trimming of main system clock and subsystem clock).	Input	P74
BUZ	Output	Buzzer output.	Input	P75
AD0 to AD7	I/O	Lower address/data bus for extending memory externally.	Input	P40 to P47

Notes 1. SI31, SO31, and $\overline{\text{SCK31}}$ are incorporated only in the μPD78F0034B and 78F0034B(A).

2. SDA0 and SCL0 are incorporated only in the μPD78F0034BY and 78F0034BY(A).

3.2 Non-Port Pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
A8 to A15	Output	Higher address bus for extending memory externally.	Input	P50 to P57
$\overline{RD}$	Output	Strobe signal output for read operation of external memory.	Input	P64
$\overline{WR}$		Strobe signal output for write operation of external memory.		P65
$\overline{WAIT}$	Input	Inserting wait for accessing external memory.	Input	P66
ASTB	Output	Strobe output which externally latches address information output to ports 4 and 5 to access external memory.	Input	P67
ANI0 to ANI7	Input	A/D converter analog input.	Input	P10 to P17
ADTRG	Input	A/D converter trigger signal input.	Input	P03/INTP3
AV_{REF}	Input	A/D converter reference voltage input.	–	–
AV_{DD}	–	A/D converter analog power supply. Set the voltage equal to V_{DD0} or V_{DD1}.	–	–
AV_{SS}	–	A/D converter ground potential. Set the voltage equal to V_{SS0} or V_{SS1}.	–	–
$\overline{RESET}$	Input	System reset input.	–	–
X1	Input	Connecting crystal resonator for main system clock oscillation.	–	–
X2	–		–	–
XT1	Input	Connecting crystal resonator for subsystem clock oscillation.	–	–
XT2	–		–	–
V_{DD0}	–	Positive power supply voltage for ports.	–	–
V_{SS0}	–	Ground potential of ports.	–	–
V_{DD1}	–	Positive power supply (except ports).	–	–
V_{SS1}	–	Ground potential (except ports).	–	–
V_{PP}	–	Applying high-voltage for program write/verify. Connect to V_{SS0} or V_{SS1} in normal operation mode.	–	–
NC[Note]	–	Not internally connected. Leave open.	–	–

Note NC is incorporated only in the 73-pin plastic FBGA.

3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 3-1. For the input/output configuration of each type, refer to Figure 3-1 .

Table 3-1. Types of Pin I/O Circuits (1/2)

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00/INTP0	8-C	I/O	Input: Independently connect to V_{SS0} or V_{SS1} via a via a resistor. Output: Leave open.
P01/INTP1			
P02/INTP2			
P03/INTP3/ADTRG			
P10/ANI0 to P17/ANI7	25	Input	Directly connect to V_{DD0}, V_{DD1}, V_{SS0}, or V_{SS1}.
P20/SI30	8-C	I/O	Input: Independently connect to V_{DD0}, V_{DD1}, V_{SS0}, or V_{SS1} via a resistor. Output: Leave open.
P21/SO30	5-H		
P22/$\overline{\text{SCK30}}$	8-C		
P23/RxD0			
P24/TxD0	5-H		
P25/ASCK0	8-C		
P30, P31	13-P		Input: Directly connect to V_{SS0} or V_{SS1}. Output: Leave open at low-level output.
P32/SDA0**Note 1**	13-R		
P33/SCL0**Note 1**			
P34/SI31**Note 2**	8-C		Input: Independently connect to V_{DD0}, V_{DD1}, V_{SS0} or V_{SS1} via a resistor. Output: Leave open.
P35/SO31**Note 2**	5-H		
P36/$\overline{\text{SCK31}}$**Note 2**	8-C		
P40/AD0 to P47/AD7	5-H		Input: Independently connect to V_{DD0} or V_{DD1} via a resistor. Output: Leave open.
P50/A8 to P57/A15	5-H		Input: Independently connect to V_{DD0}, V_{DD1}, V_{SS0}, or V_{SS1} via a resistor. Output: Leave open.
P64/$\overline{\text{RD}}$			
P65/$\overline{\text{WR}}$			
P66/$\overline{\text{WAIT}}$			
P67/ASTB			
P70/TI00/TO0	8-C		
P71/TI01			
P72/TI50/TO50			
P73/TI51/TO51			
P74/PCL	5-H		
P75/BUZ			

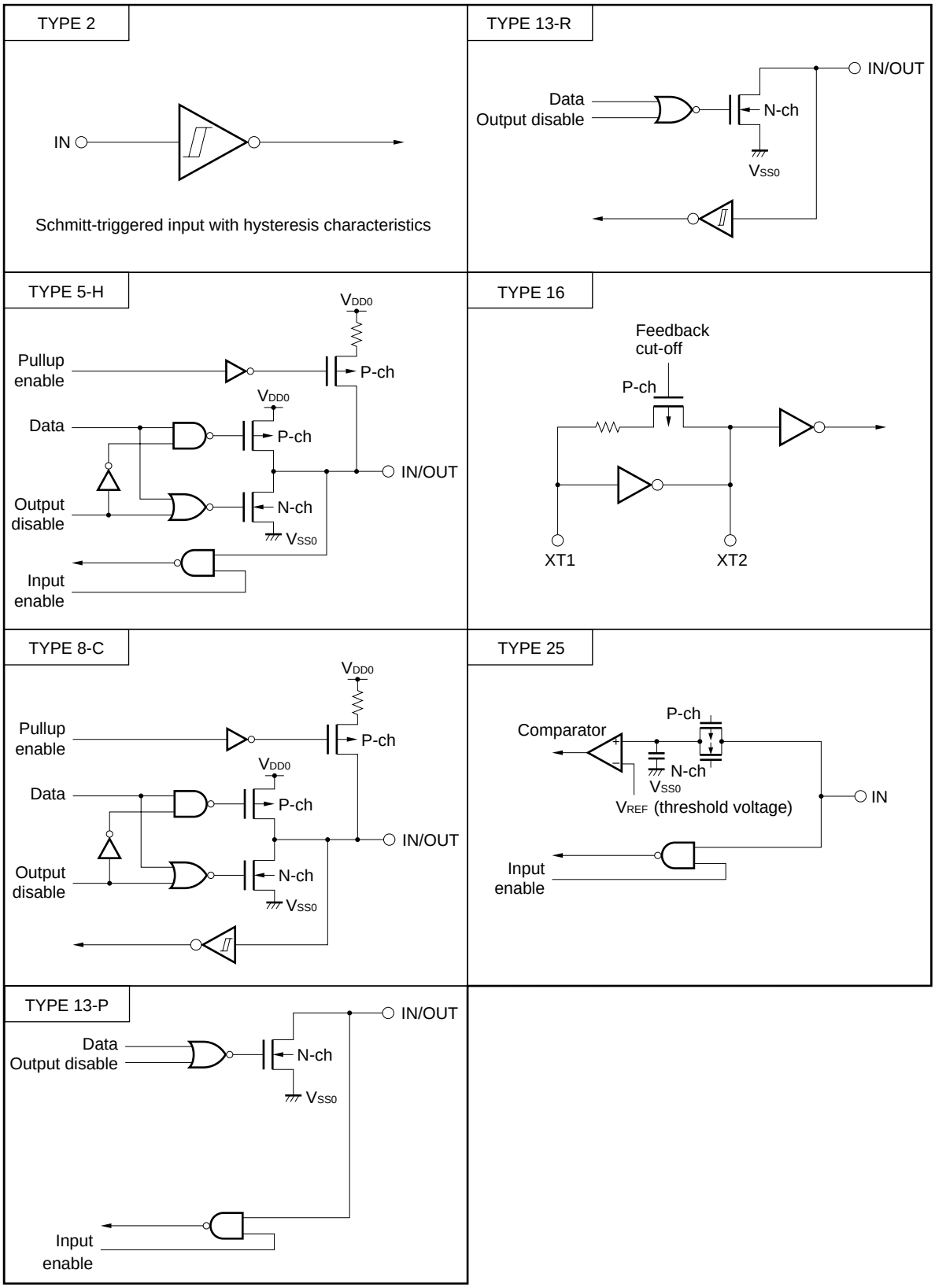
Notes 1. SDA0 and SCL0 are incorporated only in the μPD78F0034BY and 78F0034BY(A).

2. SI31, SO31, and $\overline{\text{SCK31}}$ are incorporated only in the μPD78F0034B and 78F0034B(A).

Table 3-1. Types of Pin I/O Circuits (2/2)

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
$\overline{\text{RESET}}$	2	Input	–
XT1	16		Directly connect to V_{DD0} or V_{DD1}.
XT2		–	Leave open.
AV_{DD}	–		Directly connect to V_{DD0} or V_{DD1}.
AV_{REF}			Directly connect to V_{SS0} or V_{SS1}.
AV_{SS}			
V_{PP}			Connect to V_{SS0} or V_{SS1}.

Figure 3-1. Pin I/O Circuits



4. DIFFERENCES BETWEEN μPD78F0034B, 78F0034BY, AND MASK ROM VERSIONS

The μPD78F0034B and 78F0034BY are products provided with a flash memory which enables writing, erasing, and rewriting of programs with device mounted on the target system.

The functions of the μPD78F0034B and 78F0034BY (except the functions specified for flash memory) can be made the same as those of the mask ROM versions by setting the memory size switching register (IMS).

Tables 4-1 and 4-2 show the differences between the μPD78F0034B, 78F0034BY and the mask ROM versions.

Table 4-1. Differences Between μPD78F0034B and Mask ROM Versions

Item	μPD78F0034B	Mask ROM Versions	
		μPD780034A Subseries	μPD780024A Subseries[Note]
Internal ROM structure	Flash memory	Mask ROM	
Internal ROM capacity	32 KB	μPD780031A: 8 KB μPD780032A: 16 KB μPD780033A: 24 KB μPD780034A: 32 KB	μPD780021A: 8 KB μPD780022A: 16 KB μPD780023A: 24 KB μPD780024A: 32 KB
Internal high-speed RAM capacity	1,024 bytes	μPD780031A: 512 bytes μPD780032A: 512 bytes μPD780033A: 1,024 bytes μPD780034A: 1,024 bytes	μPD780021A: 512 bytes μPD780022A: 512 bytes μPD780023A: 1,024 bytes μPD780024A: 1,024 bytes
Minimum instruction execution time	Minimum instruction execution time variable function incorporated		
When main system clock is selected	<μPD78F0034B and expanded-specification products of the mask ROM versions> 0.166 μs/0.333 μs/0.666 μs/1.33 μs/2.66 μs (@ 12 MHz operation, V_{DD} = 4.5 to 5.5 V) <Conventional products of the mask ROM versions> 0.238 μs/0.48 μs/0.95 μs/1.91 μs/3.81 μs (@ 8.38 MHz operation, V_{DD} = 4.0 to 5.5 V)		
When subsystem clock is selected	122 μs (32.768 kHz)		
Clock output	<μPD78F0034B and expanded-specification products of the mask ROM versions> • 93.75 kHz, 187.5 kHz, 375 kHz, 750 kHz, 1.25 MHz, 3 MHz, 6 MHz, 12 MHz (@ 12 MHz operation with main system clock) • 32.768 kHz (@ 32.768 kHz operation with subsystem clock) <Conventional products of the mask ROM versions> • 65.5 kHz, 131 kHz, 262 kHz, 524 kHz, 1.05 MHz, 2.10 MHz, 4.19 MHz, 8.38 MHz (@ 8.38 MHz operation with main system clock) • 32.768 kHz (@ 32.768 kHz operation with subsystem clock)		
Buzzer output	<μPD78F0034B and expanded-specification products of the mask ROM versions> 1.46 kHz, 2.93 kHz, 5.86 kHz, 11.7 kHz (@ 12 MHz operation with main system clock) <Conventional products of the mask ROM versions> • 1.02 kHz, 2.05 kHz, 4.10 kHz, 8.19 kHz (@ 8.38 MHz operation with main system clock)		
A/D converter resolution	10 bits		8 bits
Mask option specification of on-chip pull-up resistor for pins P30 to P33	Not available	Available	
IC pin	Not provided	Provided	
V_{PP} pin	Provided	Not provided	
Electrical specifications, recommended soldering conditions	Refer to the data sheet of individual products.		

Note The μPD78F0034B can be used as the flash memory version of the μPD780024A Subseries.

Caution There are differences in noise immunity and noise radiation between the flash memory and mask ROM versions. When pre-producing an application set with the flash memory version and then mass producing it with the mask ROM version, be sure to conduct sufficient evaluations on the commercial samples (CS) (not engineering samples (ES)) of the mask ROM versions.

Table 4-2. Differences Between μPD78F0034BY and Mask ROM Versions

Item	μPD78F0034BY	Mask ROM Versions	
		μPD780034AY Subseries	μPD780024AY Subseries[Note]
Internal ROM structure	Flash memory	Mask ROM	
Internal ROM capacity	32 KB	μPD780031AY: 8 KB μPD780032AY: 16 KB μPD780033AY: 24 KB μPD780034AY: 32 KB	μPD780021AY: 8 KB μPD780022AY: 16 KB μPD780023AY: 24 KB μPD780024AY: 32 KB
Internal high-speed RAM capacity	1,024 bytes	μPD780031AY: 512 bytes μPD780032AY: 512 bytes μPD780033AY: 1,024 bytes μPD780034AY: 1,024 bytes	μPD780021AY: 512 bytes μPD780022AY: 512 bytes μPD780023AY: 1,024 bytes μPD780024AY: 1,024 bytes
Minimum instruction execution time	Minimum instruction execution time variable function incorporated		
When main system clock is selected	0.238 μs/0.48 μs/0.95 μs/1.91 μs/3.81 μs (operation at 8.38 MHz, V_{DD} = 4.0 to 5.5 V)		
When subsystem clock is selected	122 μs (32.768 kHz)		
Clock output	• 65.5 kHz, 131 kHz, 262 kHz, 524 kHz, 1.05 MHz, 2.10 MHz, 4.19 MHz, 8.38 MHz (@ 8.38 MHz operation with main system clock) • 32.768 kHz (@ 32.768 kHz operation with subsystem clock)		
Buzzer output	1.02 kHz, 2.05 kHz, 4.10 kHz, 8.19 kHz (@ 8.38 MHz operation with main system clock)		
A/D converter resolution	10 bits		8 bits
Mask option specification of on-chip pull-up resistor for pins P30 and P31	Not available	Available	
IC pin	Not provided	Provided	
V_{PP} pin	Provided	Not provided	
Electrical specifications, recommended soldering conditions	Refer to the data sheet of individual products.		

Note The μPD78F0034BY can be used as the flash memory version of the μPD780024AY Subseries.

Caution There are differences in noise immunity and noise radiation between the flash memory and mask ROM versions. When pre-producing an application set with the flash memory version and then mass producing it with the mask ROM version, be sure to conduct sufficient evaluations on the commercial samples (CS) (not engineering samples (ES)) of the mask ROM versions.

5. DIFFERENCES BETWEEN μPD78F0034B, 78F0034BY AND μPD78F0034A, 78F0034AY

Table 5-1 shows the differences between the μPD78F0034B and μPD78F0034A, and Table 5-2 shows differences between the μPD78F0034BY and 78F0034AY.

Table 5-1. Differences Between μPD78F0034B and μPD78F0034A

Item		μPD78F0034B	μPD78F0034A
Guaranteed operating speed (operating frequency)	4.5 to 5.5 V	12 MHz (0.166 μs)	8.38 MHz (0.238 μs)
	4.0 to 5.5 V	8.38 MHz (0.238 μs)	8.38 MHz (0.238 μs)
	3.0 to 5.5 V	8.38 MHz (0.238 μs)	5 MHz (0.4 μs)
	2.7 to 5.5 V	5 MHz (0.4 μs)	5 MHz (0.4 μs)
	1.8 to 5.5 V	1.25 MHz (1.6 μs)	1.25 MHz (1.6 μs)
Maximum instruction execution time		Minimum instruction execution time variable function incorporated	
When main system clock is selected		0.166 μs/0.333 μs/0.666 μs/1.33 μs/2.66 μs (@ 12 MHz operation, V_{DD} = 4.5 to 5.5 V)	0.238 μs/0.48 μs/0.95 μs/1.91 μs/3.81 μs (@ 8.38 MHz operation, V_{DD} = 4.0 to 5.5 V)
When subsystem clock is selected		122 μs (32.768 kHz)	
Clock output		• 93.75 kHz, 187.5 kHz, 375 kHz, 750 kHz, 1.25 MHz, 3 MHz, 6 MHz, 12 MHz (@ 12 MHz operation with main system clock) • 32.768 kHz (@ 32.768 kHz operation with subsystem clock)	• 65.5 kHz, 131 kHz, 262 kHz, 524 kHz, 1.05 MHz, 2.10 MHz, 4.19 MHz, 8.38 MHz (@ 8.38 MHz operation with main system clock) • 32.768 kHz (@ 32.768 kHz operation with subsystem clock)
Buzzer output		1.46 kHz, 2.93 kHz, 5.86 kHz, 11.7 kHz (@ 12 MHz operation with main system clock)	1.02 kHz, 2.05 kHz, 4.10 kHz, 8.19 kHz (@ 8.38 MHz operation with main system clock)
Communication mode of flash memory programming		• 3-wire serial I/O: 2 channels[Note] • UART: 1 channel • Pseudo 3-wire serial I/O: 1 channel	• 3-wire serial I/O: 2 channels[Note] • UART: 1 channel • Pseudo 3-wire serial I/O: 1 channel
Electrical specifications, recommended soldering conditions		Refer to the data sheet of individual products.	

Note The μPD78F0034B can use one channel (serial interface SIO30) as a handshake mode. The μPD78F0034A cannot use a handshake mode.

Remark The operating frequency ratings of the μPD78F0034B and the expanded-specification products of the mask ROM versions of the μPD780024A, 780034A Subseries are the same. The operating frequency ratings of the μPD78F0034A and the conventional products of the mask ROM versions of the μPD780024A, 780034A Subseries are the same.

Table 5-2. Differences Between μPD78F0034BY and μPD78F0034AY

Item		μPD78F0034BY	μPD78F0034AY
Guaranteed operating speed (operating frequency)	4.5 to 5.5 V	8.38 MHz (0.238 μs)	
	4.0 to 5.5 V	8.38 MHz (0.238 μs)	
	3.0 to 5.5 V	5 MHz (0.4 μs)	
	2.7 to 5.5 V	5 MHz (0.4 μs)	
	1.8 to 5.5 V	1.25 MHz (1.6 μs)	
Maximum instruction execution time		Minimum instruction execution time variable function incorporated	
When main system clock is selected		0.238 μs/0.48 μs/0.95 μs/1.91 μs/3.81 μs (@ 8.38 MHz operation, V_{DD} = 4.0 to 5.5 V)	
When subsystem clock is selected		122 μs (32.768 kHz)	
Clock output		• 65.5 kHz, 131 kHz, 262 kHz, 524 kHz, 1.05 MHz, 2.10 MHz, 4.19 MHz, 8.38 MHz (@ 8.38 MHz operation with main system clock) • 32.768 kHz (@ 32.768 kHz operation with subsystem clock)	
Buzzer output		1.02 kHz, 2.05 kHz, 4.10 kHz, 8.19 kHz (@ 8.38 MHz operation with main system clock)	
Communication mode of flash memory programming		• 3-wire serial I/O: 2 channels[Note] • UART: 1 channel • Pseudo 3-wire serial I/O: 1 channel	• 3-wire serial I/O: 2 channels[Note] • UART: 1 channel • Pseudo 3-wire serial I/O: 1 channel
Electrical specifications, recommended soldering conditions		Refer to the data sheet of individual products.	

Note The μPD78F0034BY can use one channel (serial interface SIO30) as a handshake mode. The μPD78F0034AY cannot use a handshake mode.

Remark The operating frequency ratings of the μPD78F0034BY, 78F0034AY and the mask ROM versions of the μPD780024AY, 780034AY Subseries are the same.

6. DIFFERENCES BETWEEN μPD78F0034B, 78F0034BY AND μPD78F0034B(A), 78F0034BY(A)

The μPD78F0034(A) and 78F0034BY(A) are products to which a quality assurance program more stringent than that used for the μPD780034B and 780034BY (standard models) is applied (NEC Electronics classifies these products as "special" quality grade models).

The μPD78F0034B, 78F0034BY and μPD78F0034B(A), 78F0034BY(A) only differ in the quality grade; there are no differences in functions and electrical specifications.

Table 6-1. Differences Between μPD78F0034B, 78F0034BY and μPD78F0034B(A), 78F0034BY(A)

Item	μPD78F0034B, 78F0034BY	μPD78F0034B(A), 78F0034BY(A)
Quality grade	Standard	Special
Functions and electrical specifications	No differences.	

7. MEMORY SIZE SWITCHING REGISTER (IMS)

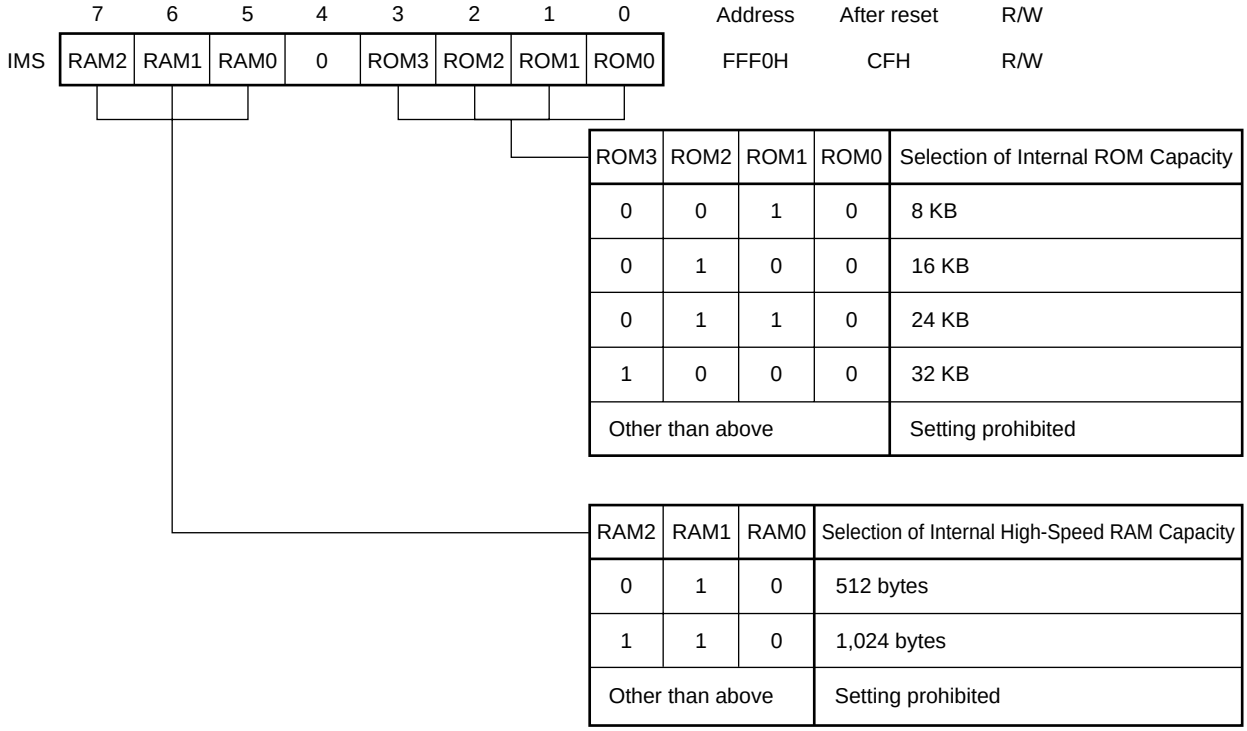
IMS is a register that is set by software and is used to specify a part of the internal memory that is not to be used. By setting memory size switching register (IMS), the internal memory of the μPD78F0034B, 78F0034BY, 78F0034B(A), and 78F0034BY(A) can be mapped identically to that of a mask ROM version.

IMS is set with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets IMS to CFH.

Caution The initial value of IMS is setting disabled (CFH). Be sure to set C8H or the value of the target mask ROM version at the moment of initial setting.

Figure 7-1. Format of Memory Size Switching Register



ROM3	ROM2	ROM1	ROM0	Selection of Internal ROM Capacity
0	0	1	0	8 KB
0	1	0	0	16 KB
0	1	1	0	24 KB
1	0	0	0	32 KB
Other than above				Setting prohibited

RAM2	RAM1	RAM0	Selection of Internal High-Speed RAM Capacity
0	1	0	512 bytes
1	1	0	1,024 bytes
Other than above			Setting prohibited

Table 7-1 shows the IMS set value to make the memory mapping the same as those of mask ROM versions.

Table 7-1. Set Value of Memory Size Switching Register

Target Mask ROM Versions	IMS Set Value
μPD780021A, 780021AY, 780031A, 780031AY	42H
μPD780022A, 780022AY, 780032A, 780032AY	44H
μPD780023A, 780023AY, 780033A, 780033AY	C6H
μPD780024A, 780024AY, 780034A, 780034AY	C8H

8. FLASH MEMORY PROGRAMMING

Writing to flash memory can be performed without removing the memory from the target system (on board programming). Writing is performed with the dedicated flash programmer (Flashpro III (part No.: FL-PR3 and PG-FP3)/(Flashpro IV (part No.: FL-PR4 and PG-FP4)) connected to the host machine and the target system.

Writing to flash memory can also be performed using flash memory writing adapter connected to Flashpro III/ Flashpro IV.

Remark FL-PR3 and FL-PR4 are products of Naito Densei Machida Mfg. Co., Ltd.

8.1 Selection of Communication Mode

Writing to a flash memory is performed using Flashpro III/Flashpro IV in a serial communication. Select one of the communication modes in Tables 8-1 and 8-2. The selection of the communication mode is made by using the format shown in Figure 8-1. Each communication mode is selected by the number of V_{PP} pulses shown in Tables 8-1 and 8-2.

Table 8-1. List of Communication Mode (μPD78F0034B)

Communication Mode	Channels	Pin Used	V_{PP} Pulses
3-wire serial I/O	2	SI30/P20 SO30/P21 $\overline{SCK30}$/P22	0
		SI31/P34 SO31/P35 $\overline{SCK31}$/P36	1
		SI30/P20 SO30/P21 $\overline{SCK30}$/P22 HS/P25	3
UART	1	RxD0/P23 TxD0/P24	8
Pseudo 3-wire serial I/O	1	P72/TI50/TO50 (serial clock input) P71/TI01 (serial data output) P70/TI00/TO0 (serial data input)	12

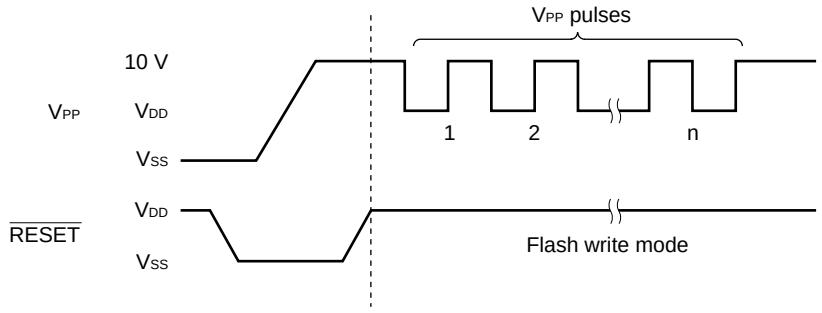
Caution Be sure to select a communication mode using the number of V_{PP} pulses shown in Table 8-1.

Table 8-2. List of Communication Mode (μPD78F0034BY)

Communication Mode	Channels	Pin Used	V_{PP} Pulses
3-wire serial I/O	1	SI30/P20 SO30/P21 $\overline{SCK30}$/P22	0
		SI30/P20 SO30/P21 $\overline{SCK30}$/P22 HS/P25	3
I^2C bus	1	SDA0/P32 SCL0/P33	4
UART	1	RxD0/P23 TxD0/P24	8
Pseudo 3-wire serial I/O	1	P72/TI50/TO50 (serial clock input) P71/TI01 (serial data output) P70/TI00/TO0 (serial data input)	12

Caution Be sure to select a communication mode using the number of V_{PP} pulses shown in Table 8-2.

Figure 8-1. Format of Communication Mode Selection



8.2 Flash Memory Programming Functions

Operations such as writing to flash memory are performed by various command/data transmission and reception operations according to the selected communication mode. Table 8-3 shows major functions of flash memory programming.

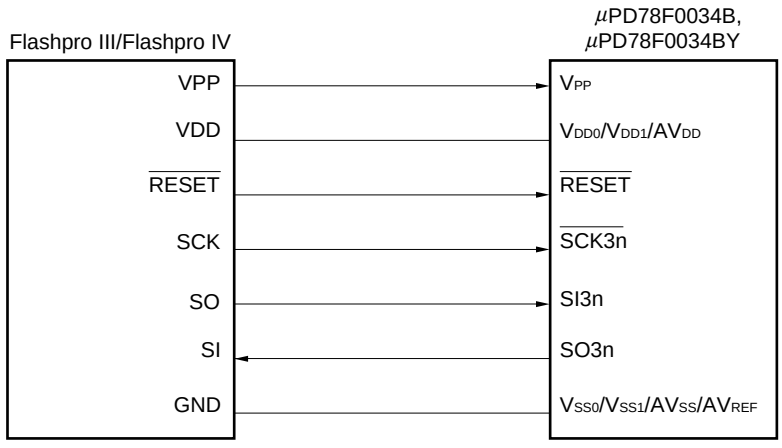
Table 8-3. Major Functions of Flash Memory Programming

Function	Description
Reset	Used to stop write operation and detect transmission cycle.
Batch verify	Compares the entire memory contents with the input data.
Batch erase	Erases the entire memory contents.
Batch blank check	Checks the deletion status of the entire memory.
High-speed write	Performs write to the flash memory based on the write start address and the number of data to be written (number of bytes).
Continuous write	Performs continuous write based on the information input with high-speed write operation.
Status	Used to confirm the current operating mode and operation end.
Oscillation frequency setting	Sets the frequency of the resonator.
Erase time setting	Sets the memory erase time.
Baud rate setting	Sets the communication rate for UART mode
I^2C mode setting	Sets standard/high-speed mode for I^2C bus mode
Silicon signature read	Outputs the device name and memory capacity, and device block information.

8.3 Connection of Flashpro III/Flashpro IV

The connection of Flashpro III/Flashpro IV and the μPD78F0034B or 78F0034BY differs according to the communication mode (3-wire serial I/O, UART, pseudo 3-wire serial I/O, and I^2C bus). The connection for each communication mode is shown in Figures 8-2 to 8-6, respectively.

Figure 6-2. Connection of Flashpro III/Flashpro IV in 3-Wire Serial I/O Mode



Remark μPD78F0034B: n = 0, 1
μPD78F0034BY: n = 0

Figure 8-3. Connection of Flashpro III in 3-Wire Serial I/O Mode (Using Handshake)

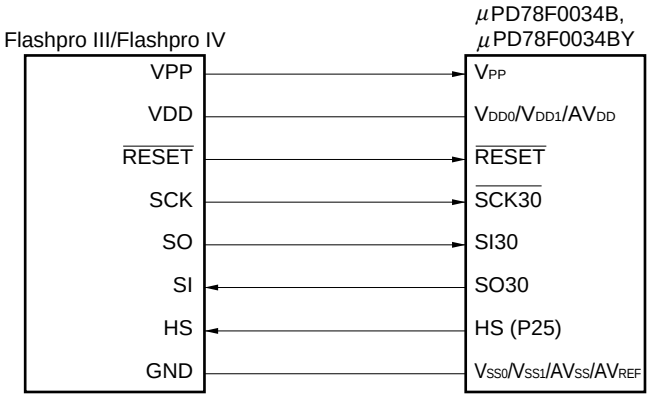


Figure 8-4. Connection of Flashpro III/Flashpro IV for UART Mode

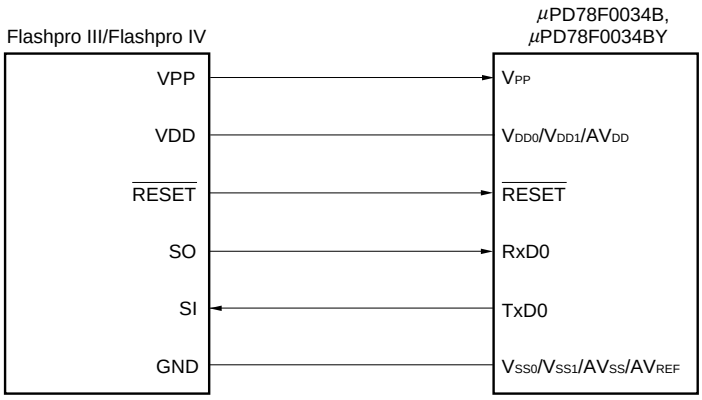


Figure 8-5. Connection of Flashpro III/Flashpro IV for Pseudo 3-Wire Serial I/O Mode

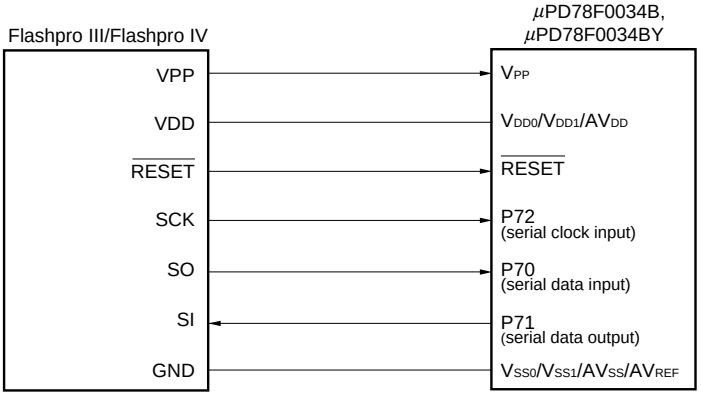
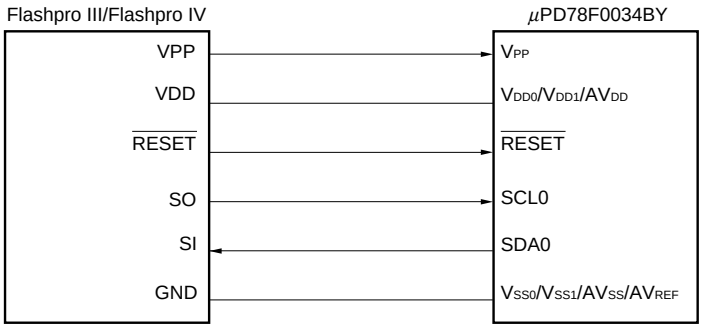


Figure 8-6. Connection of Flashpro III/Flashpro IV for I^2C Bus Mode (μPD78F0034BY only)



9. ELECTRICAL SPECIFICATIONS

9.1 μPD78F0034B, 78F0034B(A)

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V_{DD}			–0.3 to +6.5	V
	V_{PP}	**Note 2**		–0.3 to +10.5	V
	AV_{DD}			–0.3 to V_{DD} + 0.3**Note 1**	V
	AV_{REF}			–0.3 to V_{DD} + 0.3**Note 1**	V
	AV_{SS}			–0.3 to +0.3	V
Input voltage	V_{I1}	P00 to P03, P10 to P17, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75, X1, X2, XT1, XT2, $\overline{\text{RESET}}$		–0.3 to V_{DD} + 0.3**Note 1**	V
	V_{I2}	P30 to P33	N-ch open drain	–0.3 to +6.5	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3**Note 1**	V
Analog input voltage	V_{AN}	P10 to P17	Analog input pin	AV_{SS} –0.3 to AV_{REF} + 0.3**Note 1** and –0.3 to V_{DD} + 0.3**Note 1**	V
Output current, high	I_{OH}	Per pin		–10	mA
		Total for P00 to P03, P40 to P47, P50 to P57, P64 to P67, P70 to P75		–15	mA
		Total for P20 to P25, P30 to P36		–15	mA
Output current, low	I_{OL}	Per pin for P00 to P03, P20 to P25, P34 to P36, P40 to P47, P64 to P67, P70 to P75		20	mA
		Per pin for P30 to P33, P50 to P57		30	mA
		Total for P00 to P03, P40 to P47, P64 to P67, P70 to P75		50	mA
		Total for P20 to P25		20	mA
		Total for P30 to P36		100	mA
		Total for P50 to P57		100	mA
Operating ambient temperature	T_A	During normal operation		–40 to +85	°C
Storage temperature	T_{stg}			–40 to +125	°C

Notes 1. 6.5 V or below

(**Note 2** is explained on the following page.)

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

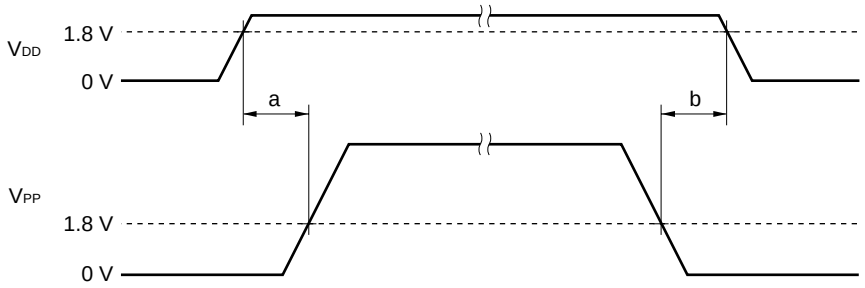
Notes 2. Make sure that the following conditions of the V_{PP} voltage application timing are satisfied when the flash memory is written.

- **When supply voltage rises**

  V_{PP} must exceed V_{DD} 10 μs or more after V_{DD} has reached the lower-limit value (1.8 V) of the operating voltage range (see a in the figure below).

- **When supply voltage drops**

  V_{DD} must be lowered 10 μs or more after V_{PP} falls below the lower-limit value (1.8 V) of the operating voltage range of V_{DD} (see b in the figure below).

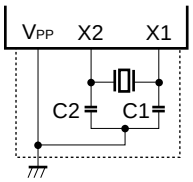
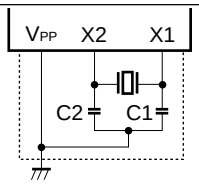
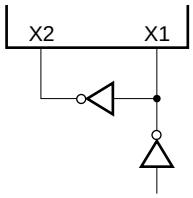


Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V.				15	pF
I/O capacitance	C_{IO}	f = 1 MHz Unmeasured pins returned to 0 V.	P00 to P03, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75,			15	pF
			P30 to P33			20	pF

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

Main System Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)Note 1	4.5 V ≤ V_{DD} ≤ 5.5 V	1.0		12.0	MHz
			3.0 V ≤ V_{DD} < 4.5 V	1.0		8.38	
			1.8 V ≤ V_{DD} < 3.0 V	1.0		5.0	
		Oscillation stabilization timeNote 2	After V_{DD} reaches oscillation voltage range MIN.			4	ms
Crystal resonator		Oscillation frequency (f_X)Note 1	4.5 V ≤ V_{DD} ≤ 5.5 V	1.0		12.0	MHz
			3.0 V ≤ V_{DD} < 4.5 V	1.0		8.38	
			1.8 V ≤ V_{DD} < 3.0 V	1.0		5.0	
		Oscillation stabilization timeNote 2	4.0 V ≤ V_{DD} ≤ 5.5 V			10	ms
			1.8 V ≤ V_{DD} < 4.0 V			30	
External clock		X1 input frequency (f_X)Note 1	4.5 V ≤ V_{DD} ≤ 5.5 V	1.0		12.0	MHz
			3.0 V ≤ V_{DD} < 4.5 V	1.0		8.38	
			1.8 V ≤ V_{DD} < 3.0 V	1.0		5.0	
		X1 input high-/low-level width (t_{XH}, t_{XL})	4.5 V ≤ V_{DD} ≤ 5.5 V	38		500	ns
			3.0 V ≤ V_{DD} < 4.5 V	50		500	
			1.8 V ≤ V_{DD} < 3.0 V	85		500	

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release.

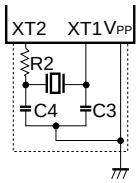
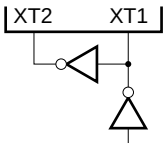
Cautions 1. When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS1}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. When the main system clock is stopped and the system is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

Remark For the resonator selection and oscillator constant, customers are required to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

Subsystem Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT})**Note 1**		32	32.768	35	kHz
		Oscillation stabilization time**Note 2**	4.0 V ≤ V_{DD} ≤ 5.5 V		1.2	2	s
			1.8 V ≤ V_{DD} < 4.0 V			10	
External clock		X1 input frequency (f_{XT})**Note 1**		32		38.5	kHz
		X1 input high-/low-level width (t_{XTH}, t_{XTL})		12		15	μs

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after V_{DD} reaches oscillator voltage MIN.

Cautions 1. When using the subsystem clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor to the same potential as V_{SS1}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The subsystem clock oscillator is designed as a low-amplitude circuit for reducing power consumption, and is more prone to malfunction due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

Remark For the resonator selection and oscillator constant, customers are required to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high	I_{OH}	Per pin				–1	mA
		All pins				–15	mA
Output current, low	I_{OL}	Per pin for P00 to P03, P20 to P25, P34 to P36, P40 to P47, P64 to P67, P70 to P75				10	mA
		Per pin for P30 to P33, P50 to P57				15	mA
		Total for P00 to P03, P40 to P47, P64 to P67, P70 to P75				20	mA
		Total for P20 to P25				10	mA
		Total for P30 to P36				70	mA
		Total for P50 to P57				70	mA
Input voltage, high	V_{IH1}	P10 to P17, P21, P24, P35, P40 to P47, P50 to P57, P64 to P67, P74, P75	2.7 V ≤ V_{DD} ≤ 5.5 V	0.7V_{DD}		V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V	0.8V_{DD}		V_{DD}	V
	V_{IH2}	P00 to P03, P20, P22, P23, P25, P34, P36, P70 to P73, $\overline{\text{RESET}}$	2.7 V ≤ V_{DD} ≤ 5.5 V	0.8V_{DD}		V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V	0.85V_{DD}		V_{DD}	V
	V_{IH3}	P30 to P33 (N-ch open-drain)	2.7 V ≤ V_{DD} ≤ 5.5 V	0.7V_{DD}		5.5	V
			1.8 V ≤ V_{DD} < 2.7 V	0.8V_{DD}		5.5	V
	V_{IH4}	X1, X2	2.7 V ≤ V_{DD} ≤ 5.5 V	V_{DD} – 0.5		V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V	V_{DD} – 0.2		V_{DD}	V
	V_{IH5}	XT1, XT2	4.0 V ≤ V_{DD} ≤ 5.5 V	0.8V_{DD}		V_{DD}	V
			1.8 V ≤ V_{DD} < 4.0 V	0.9V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P10 to P17, P21, P24, P35, P40 to P47, P50 to P57, P64 to P67, P74, P75	2.7 V ≤ V_{DD} ≤ 5.5 V	0		0.3V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V	0		0.2V_{DD}	V
	V_{IL2}	P00 to P03, P20, P22, P23, P25, P34, P36, P70 to P73, $\overline{\text{RESET}}$	2.7 V ≤ V_{DD} ≤ 5.5 V	0		0.2V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V	0		0.15V_{DD}	V
	V_{IL3}	P30 to P33	4.0 V ≤ V_{DD} ≤ 5.5 V	0		0.3V_{DD}	V
			2.7 V ≤ V_{DD} < 4.0 V	0		0.2V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V	0		0.1V_{DD}	V
	V_{IL4}	X1, X2	2.7 V ≤ V_{DD} ≤ 5.5 V	0		0.4	V
			1.8 V ≤ V_{DD} < 2.7 V	0		0.2	V
	V_{IL5}	XT1, XT2	4.0 V ≤ V_{DD} ≤ 5.5 V	0		0.2V_{DD}	V
			1.8 V ≤ V_{DD} < 4.0 V	0		0.1V_{DD}	V
Output voltage, high	V_{OH1}	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = –1 mA		V_{DD} – 1.0		V_{DD}	V
		1.8 V ≤ V_{DD} < 4.0 V, I_{OH} = –100 μA		V_{DD} – 0.5		V_{DD}	V
Output voltage, low	V_{OL1}	P30 to P33	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 15 mA			2.0	V
		P50 to P57			0.4	2.0	V
		P00 to P03, P20 to P25, P34 to P36, P40 to P47, P64 to P67, P70 to P75	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	I_{OL} = 400 μA				0.5	V

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	$V_{IN} = V_{DD}$	P00 to P03, P10 to P17, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75, $\overline{\text{RESET}}$			3	μA
	I_{LIH2}		X1, X2, XT1, XT2			20	μA
	I_{LIH3}	V_{IN} = 5.5 V	P30 to P33			3	μA
Input leakage current, low	I_{LIL1}	V_{IN} = 0 V	P00 to P03, P10 to P17, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75, $\overline{\text{RESET}}$			–3	μA
	I_{LIL2}		X1, X2, XT1, XT2			–20	μA
	I_{LIL3}		P30 to P33			–3	μA
Output leakage current, high	I_{LOH}	$V_{OUT} = V_{DD}$				3	μA
Output leakage current, low	I_{LOL}	V_{OUT} = 0 V				–3	μA
Software pull-up resistor	R	V_{IN} = 0 V, P00 to P03, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75		15	30	90	kΩ

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Power supply current[Note 1]	I_{DD1}[Note 2]	12.0 MHz crystal oscillation operating mode	V_{DD} = 5.0 V ±10%[Note 3]	When A/D converter is stopped		16	32	mA
				When A/D converter is operating[Note 7]		17	34	mA
		8.38 MHz crystal oscillation operating mode	V_{DD} = 5.0 V ±10%[Note 3]	When A/D converter is stopped		10.5	21	mA
				When A/D converter is operating[Note 7]		11.5	23	mA
			V_{DD} = 3.0 V + 10%[Notes 3, 6]	When A/D converter is stopped		7	14	mA
				When A/D converter is operating[Note 7]		8	16	mA
		5.00 MHz crystal oscillation operating mode	V_{DD} = 3.0 V ±10%[Note 3]	When A/D converter is stopped		4.5	9	mA
				When A/D converter is operating[Note 7]		5.5	11	mA
			V_{DD} = 2.0 V ±10%[Note 4]	When A/D converter is stopped		1	2	mA
				When A/D converter is operating[Note 7]		2	6	mA
	I_{DD2}	12.0 MHz crystal oscillation HALT mode	V_{DD} = 5.0 V ±10%[Note 3]	When peripheral functions are stopped		2	4	mA
				When peripheral functions are operating			8	mA
		8.38 MHz crystal oscillation HALT mode	V_{DD} = 5.0 V ±10%[Note 3]	When peripheral functions are stopped		1.2	2.4	mA
				When peripheral functions are operating			5	mA
			V_{DD} = 3.0 V + 10%[Notes 3, 6]	When peripheral functions are stopped		0.6	1.2	mA
				When peripheral functions are operating			2.4	mA
		5.00 MHz crystal oscillation HALT mode	V_{DD} = 3.0 V ±10%[Note 3]	When peripheral functions are stopped		0.4	0.8	mA
				When peripheral functions are operating			1.7	mA
			V_{DD} = 2.0 V ±10%[Note 4]	When peripheral functions are stopped		0.2	0.4	mA
				When peripheral functions are operating			1.1	mA
	I_{DD3}	32.768 kHz crystal oscillation operating mode[Note 5]		V_{DD} = 5.0 V ±10%		115	230	μA
				V_{DD} = 3.0 V ±10%		95	190	μA
				V_{DD} = 2.0 V ±10%		75	150	μA
	I_{DD4}	32.768 kHz crystal oscillation HALT mode[Note 5]		V_{DD} = 5.0 V ±10%		30	60	μA
				V_{DD} = 3.0 V ±10%		6	18	μA
				V_{DD} = 2.0 V ±10%		2	10	μA
	I_{DD5}	XT1 = V_{DD} STOP mode When feedback resistor is not used		V_{DD} = 5.0 V ±10%		0.1	30	μA
				V_{DD} = 3.0 V ±10%		0.05	10	μA
				V_{DD} = 2.0 V ±10%		0.05	10	μA

Notes 1. Total current through the internal power supply (V_{DD0}, V_{DD1}) (except the current through pull-up resistors of ports).

2. I_{DD1} includes the peripheral operation current.

3. When the processor clock control register (PCC) is set to 00H.

4. When PCC is set to 02H.

5. When main system clock operation is stopped.

6. The values show the specifications when V_{DD} = 3.0 to 3.3 V. The value in the TYP. column show the specifications when V_{DD} = 3.0 V.

7. Includes the current through the AV_{DD} pin.

AC Characteristics

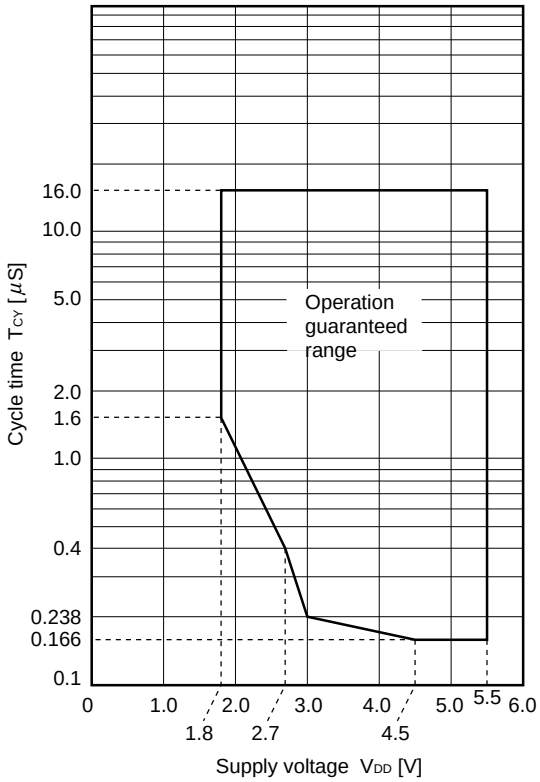
(1) Basic Operation (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (Min. instruction execution time)	T_{CY}	Operating with main system clock	4.5 V ≤ V_{DD} ≤ 5.5 V	0.166		16	μs
			3.0 V ≤ V_{DD} ≤ 4.5 V	0.238		16	μs
			2.7 V ≤ V_{DD} ≤ 3.0 V	0.4		16	μs
			1.8 V ≤ V_{DD} ≤ 2.7 V	1.6		16	μs
		Operating with subsystem clock		103.9 Note 1	122	125	μs
TI00, TI01 input high-/low-level width	t_{TIH0}, t_{TIL0}	3.0 V ≤ V_{DD} ≤ 5.5 V		$2/f_{sam}$+0.1 Note 2			μs
		2.7 V ≤ V_{DD} < 3.0 V		$2/f_{sam}$+0.2 Note 2			μs
		1.8 V ≤ V_{DD} < 2.7 V		$2/f_{sam}$+0.5 Note 2			μs
TI50, TI51 input frequency	f_{TI5}	2.7 V ≤ V_{DD} ≤ 5.5 V		0		4	MHz
		1.8 V ≤ V_{DD} < 2.7 V		0		275	kHz
TI50, TI51 input high-/low-level width	t_{TIH5}, t_{TIL5}	2.7 V ≤ V_{DD} ≤ 5.5 V		100			ns
		1.8 V ≤ V_{DD} < 2.7 V		1.8			ns
Interrupt request input high-/low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP3, P40 to P47	2.7 V ≤ V_{DD} ≤ 5.5 V	1			μs
			1.8 V ≤ V_{DD} < 2.7 V	2			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}	2.7 V ≤ V_{DD} ≤ 5.5 V		10			μs
		1.8 V ≤ V_{DD} < 2.7 V		20			μs

Notes 1. Value when the external clock is used. When a crystal resonator is used, it is 114 μs (MIN.).

2. Selection of fsam = f_X, f_X/4, f_X/64 is possible using bits 0 and 1 (PRM00, PRM01) of prescaler mode register 0 (PRM0). However, if the TI00 valid edge is selected as the count clock, the value becomes fsam = f_X/8.

T_{CY} vs. V_{DD} (main system clock operation)



(2) Read/write operation (T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V) (1/3)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		$0.3t_{CY}$		ns
Address setup time	t_{ADS}		20		ns
Address hold time	t_{ADH}		6		ns
Input time from address to data	t_{ADD1}			$(2 + 2n)t_{CY}$ – 54	ns
	t_{ADD2}			$(3 + 2n)t_{CY}$ – 60	ns
Output time from $\overline{RD}\downarrow$ to address	t_{RDAD}		0	100	ns
Input time from $\overline{RD}\downarrow$ to data	t_{RDD1}			$(2 + 2n)t_{CY}$ – 87	ns
	t_{RDD2}			$(3 + 2n)t_{CY}$ – 93	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		$(1.5 + 2n)t_{CY}$ – 33		ns
	t_{RDL2}		$(2.5 + 2n)t_{CY}$ – 33		ns
Input time from $\overline{RD}\downarrow$ to $\overline{WAIT}\downarrow$	t_{RDWT1}			t_{CY} – 43	ns
	t_{RDWT2}			t_{CY} – 43	ns
Input time from $\overline{WR}\downarrow$ to $\overline{WAIT}\downarrow$	t_{WRWT}			t_{CY} – 25	ns
$\overline{WAIT}$ low-level width	t_{WTL}		$(0.5 + n)t_{CY}$ + 10	$(2 + 2n)t_{CY}$	ns
Write data setup time	t_{WDS}		60		ns
Write data hold time	t_{WDH}		6		ns
$\overline{WR}$ low-level width	t_{WRL1}		$(1.5 + 2n)t_{CY}$ – 15		ns
Delay time from ASTB↓ to $\overline{RD}\downarrow$	t_{ASTRD}		6		ns
Delay time from ASTB↓ to $\overline{WR}\downarrow$	t_{ASTWR}		$2t_{CY}$ – 15		ns
Delay time from $\overline{RD}\uparrow$ to ASTB↑ in external fetch	t_{RDAST}		$0.8t_{CY}$ – 15	$1.2t_{CY}$	ns
Hold time from $\overline{RD}\uparrow$ to address in external fetch	t_{RDADH}		$0.8t_{CY}$ – 15	$1.2t_{CY}$ + 30	ns
Write data output time from $\overline{RD}\uparrow$	t_{RDWD}		40		ns
Write data output time from $\overline{WR}\downarrow$	t_{WRWD}		10	60	ns
Hold time from $\overline{WR}\uparrow$ to address	t_{WRADH}		$0.8t_{CY}$ – 15	$1.2t_{CY}$ + 30	ns
Delay time from $\overline{WAIT}\uparrow$ to $\overline{RD}\uparrow$	t_{WTRD}		$0.8t_{CY}$	$2.5t_{CY}$ + 25	ns
Delay time from $\overline{WAIT}\uparrow$ to $\overline{WR}\uparrow$	t_{WTWR}		$0.8t_{CY}$	$2.5t_{CY}$ + 25	ns

Caution T_{CY} can only be used when the MIN. value is 0.238 μs.

Remarks 1. $t_{CY} = T_{CY}/4$

2. n indicates the number of waits.

3. C_L = 100 pF (C_L is the load capacitance of the AD0 to AD7, A8 to A15, $\overline{RD}$, $\overline{WR}$, $\overline{WAIT}$, and ASTB pins.)

(2) Read/write operation (T_A = –40 to +85°C, V_{DD} = 2.7 to 4.0 V) **(2/3)**

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		$0.3t_{CY}$		ns
Address setup time	t_{ADS}		30		ns
Address hold time	t_{ADH}		10		ns
Input time from address to data	t_{ADD1}			$(2 + 2n)t_{CY}$ – 108	ns
	t_{ADD2}			$(3 + 2n)t_{CY}$ – 120	ns
Output time from $\overline{RD}\downarrow$ to address	t_{RDAD}		0	200	ns
Input time from $\overline{RD}\downarrow$ to data	t_{RDD1}			$(2 + 2n)t_{CY}$ – 148	ns
	t_{RDD2}			$(3 + 2n)t_{CY}$ – 162	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		$(1.5 + 2n)t_{CY}$ – 40		ns
	t_{RDL2}		$(2.5 + 2n)t_{CY}$ – 40		ns
Input time from $\overline{RD}\downarrow$ to $\overline{WAIT}\downarrow$	t_{RDWT1}			t_{CY} – 75	ns
	t_{RDWT2}			t_{CY} – 60	ns
Input time from $\overline{WR}\downarrow$ to $\overline{WAIT}\downarrow$	t_{WRWT}			t_{CY} – 50	ns
$\overline{WAIT}$ low-level width	t_{WTL}		$(0.5 + 2n)t_{CY}$ + 10	$(2 + 2n)t_{CY}$	ns
Write data setup time	t_{WDS}		60		ns
Write data hold time	t_{WDH}		10		ns
$\overline{WR}$ low-level width	t_{WRL1}		$(1.5 + 2n)t_{CY}$ – 30		ns
Delay time from ASTB↓ to $\overline{RD}\downarrow$	t_{ASTRD}		10		ns
Delay time from ASTB↓ to $\overline{WR}\downarrow$	t_{ASTWR}		$2t_{CY}$ – 30		ns
Delay time from $\overline{RD}\uparrow$ to ASTB↑ in external fetch	t_{RDAST}		$0.8t_{CY}$ – 30	$1.2t_{CY}$	ns
Hold time from $\overline{RD}\uparrow$ to address in external fetch	t_{RDADH}		$0.8t_{CY}$ – 30	$1.2t_{CY}$ + 60	ns
Write data output time from $\overline{RD}\uparrow$	t_{RDWD}		40		ns
Write data output time from $\overline{WR}\downarrow$	t_{WRWD}		20	120	ns
Hold time from $\overline{WR}\uparrow$ to address	t_{WRADH}		$0.8t_{CY}$ – 30	$1.2t_{CY}$ + 60	ns
Delay time from $\overline{WAIT}\uparrow$ to $\overline{RD}\uparrow$	t_{WTRD}		$0.5t_{CY}$	$2.5t_{CY}$ + 50	ns
Delay time from $\overline{WAIT}\uparrow$ to $\overline{WR}\uparrow$	t_{WTWR}		$0.5t_{CY}$	$2.5t_{CY}$ + 50	ns

Caution T_{CY} can only be used when the MIN. value is 0.4 μs.

Remarks 1. $t_{CY} = T_{CY}/4$

2. n indicates the number of waits.

3. C_L = 100 pF (C_L is the load capacitance of the AD0 to AD7, A8 to A15, $\overline{RD}$, $\overline{WR}$, $\overline{WAIT}$, and ASTB pins.)

(2) Read/write operation (T_A = –40 to +85°C, V_{DD} = 1.8 to 2.7 V) (3/3)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		$0.3t_{CY}$		ns
Address setup time	t_{ADS}		120		ns
Address hold time	t_{ADH}		20		ns
Input time from address to data	t_{ADD1}			$(2 + 2n)t_{CY}$ – 233	ns
	t_{ADD2}			$(3 + 2n)t_{CY}$ – 240	ns
Output time from $\overline{RD}\downarrow$ to address	t_{RDAD}		0	400	ns
Input time from $\overline{RD}\downarrow$ to data	t_{RDD1}			$(2 + 2n)t_{CY}$ – 325	ns
	t_{RDD2}			$(3 + 2n)t_{CY}$ – 332	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		$(1.5 + 2n)t_{CY}$ – 92		ns
	t_{RDL2}		$(2.5 + 2n)t_{CY}$ – 92		ns
Input time from $\overline{RD}\downarrow$ to $\overline{WAIT}\downarrow$	t_{RDWT1}			t_{CY} – 350	ns
	t_{RDWT2}			t_{CY} – 132	ns
Input time from $\overline{WR}\downarrow$ to $\overline{WAIT}\downarrow$	t_{WRWT}			t_{CY} – 100	ns
$\overline{WAIT}$ low-level width	t_{WTL}		$(0.5 + 2n)t_{CY}$ + 10	$(2 + 2n)t_{CY}$	ns
Write data setup time	t_{WDS}		60		ns
Write data hold time	t_{WDH}		20		ns
$\overline{WR}$ low-level width	t_{WRL1}		$(1.5 + 2n)t_{CY}$ – 60		ns
Delay time from ASTB↓ to $\overline{RD}\downarrow$	t_{ASTRD}		20		ns
Delay time from ASTB↓ to $\overline{WR}\downarrow$	t_{ASTWR}		$2t_{CY}$ – 60		ns
Delay time from $\overline{RD}\uparrow$ to ASTB↑ in external fetch	t_{RDAST}		$0.8t_{CY}$ – 60	$1.2t_{CY}$	ns
Hold time from $\overline{RD}\uparrow$ to address in external fetch	t_{RDADH}		$0.8t_{CY}$ – 60	$1.2t_{CY}$ + 120	ns
Write data output time from $\overline{RD}\uparrow$	t_{RDWD}		40		ns
Write data output time from $\overline{WR}\downarrow$	t_{WRWD}		40	240	ns
Hold time from $\overline{WR}\uparrow$ to address	t_{WRADH}		$0.8t_{CY}$ – 60	$1.2t_{CY}$ + 120	ns
Delay time from $\overline{WAIT}\uparrow$ to $\overline{RD}\uparrow$	t_{WTRD}		$0.5t_{CY}$	$2.5t_{CY}$ + 100	ns
Delay time from $\overline{WAIT}\uparrow$ to $\overline{WR}\uparrow$	t_{WTWR}		$0.5t_{CY}$	$2.5t_{CY}$ + 100	ns

Caution T_{CY} can only be used when the MIN. value is 1.6 μs.

Remarks 1. $t_{CY} = T_{CY}/4$

2. n indicates the number of waits.

3. C_L = 100 pF (C_L is the load capacitance of the AD0 to AD7, A8 to A15, $\overline{RD}$, $\overline{WR}$, $\overline{WAIT}$, and ASTB pins.)

(3) Serial Interface (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

(a) 3-wire serial I/O mode ($\overline{SCK3n}$... Internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK3n}$ cycle time	t_{KCY1}	4.5 V ≤ V_{DD} ≤ 5.5 V		666			ns
		3.0 V ≤ V_{DD} < 4.5 V		954			ns
		2.7 V ≤ V_{DD} < 3.0 V		1600			ns
		1.8 V ≤ V_{DD} < 2.7 V		3200			ns
$\overline{SCK3n}$ high-/low-level width	t_{KH1}, t_{KL1}	3.0 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2 – 50			ns
		1.8 V ≤ V_{DD} < 3.0 V		t_{KCY1}/2 – 100			ns
SI3n setup time (to $\overline{SCK3n}$↑)	t_{SIK1}	3.0 V ≤ V_{DD} ≤ 5.5 V		100			ns
		2.7 V ≤ V_{DD} < 3.0 V		150			ns
		1.8 V ≤ V_{DD} < 2.7 V		300			ns
SI3n hold time (from $\overline{SCK3n}$↑)	t_{KSI1}	4.5 V ≤ V_{DD} ≤ 5.5 V		300			ns
		1.8 V ≤ V_{DD} < 4.5 V		400			ns
Delay time from $\overline{SCK3n}$↓ to SO3n output	t_{KSO1}	C = 100 pF[Note]	4.5 V ≤ V_{DD} ≤ 5.5 V			200	ns
			1.8 V ≤ V_{DD} < 4.5 V			300	ns

Note C is the load capacitance of the $\overline{SCK3n}$ and SO3n output lines.

(b) 3-wire serial I/O mode ($\overline{SCK3n}$... External clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK3n}$ cycle time	t_{KCY2}	4.5 V ≤ V_{DD} ≤ 5.5 V		666			ns
		3.0 V ≤ V_{DD} < 4.5 V		800			ns
		2.7 V ≤ V_{DD} < 3.0 V		1600			ns
		1.8 V ≤ V_{DD} < 2.7 V		3200			ns
$\overline{SCK3n}$ high-/low-level width	t_{KH2}, t_{KL2}	4.5 V ≤ V_{DD} ≤ 5.5 V		333			ns
		3.0 V ≤ V_{DD} < 4.5 V		400			ns
		2.7 V ≤ V_{DD} < 3.0 V		800			ns
		1.8 V ≤ V_{DD} < 2.7 V		1600			ns
SI3n setup time (to $\overline{SCK3n}$↑)	t_{SIK2}			100			ns
SI3n hold time (from $\overline{SCK3n}$↑)	t_{KSI2}	4.5 V ≤ V_{DD} ≤ 5.5 V		300			ns
		1.8 V ≤ V_{DD} < 4.5 V		400			ns
Delay time from $\overline{SCK3n}$↓ to SO3n output	t_{KSO2}	C = 100 pF[Note]	4.5 V ≤ V_{DD} ≤ 5.5 V			200	ns
			1.8 V ≤ V_{DD} < 4.5 V			300	ns

Note C is the load capacitance of the SO3n output line.

Remark n = 0, 1

(c) UART mode (dedicated baud-rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		4.5 V ≤ V_{DD} ≤ 5.5 V			187500	bps
		3.0 V ≤ V_{DD} < 4.5 V			131031	bps
		2.7 V ≤ V_{DD} < 3.0 V			78125	bps
		1.8 V ≤ V_{DD} < 2.7 V			39063	bps

(d) UART mode (external clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK0 cycle time	t_{KCY3}	4.0 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.0 V	1600			ns
		1.8 V ≤ V_{DD} < 2.7 V	3200			ns
ASCK0 high-/low-level width	t_{KH3}, t_{KL3}	4.0 V ≤ V_{DD} ≤ 5.5 V	400			ns
		2.7 V ≤ V_{DD} < 4.0 V	800			ns
		1.8 V ≤ V_{DD} < 2.7 V	1600			ns
Transfer rate		4.0 V ≤ V_{DD} ≤ 5.5 V			39063	bps
		2.7 V ≤ V_{DD} < 4.0 V			19531	bps
		1.8 V ≤ V_{DD} < 2.7 V			9766	bps

(e) UART mode (infrared data transfer mode)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Transfer rate		4.0 V ≤ V_{DD} ≤ 5.5 V		131031	bps
Allowable bit rate error		4.0 V ≤ V_{DD} ≤ 5.5 V		±0.87	%
Output pulse width		4.0 V ≤ V_{DD} ≤ 5.5 V	1.2	0.24/fbr**Note**	μs
Input pulse width		4.0 V ≤ V_{DD} ≤ 5.5 V	4/f_X		μs

Note fbr: Specified baud rate

A/D Converter Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{DD} = 1.8 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	bit
Overall error[Note]		4.0 V ≤ AV_{REF} ≤ 5.5 V		±0.2	±0.4	%FSR
		2.7 V ≤ AV_{REF} < 4.0 V		±0.3	±0.6	%FSR
		1.8 V ≤ AV_{REF} < 2.7 V		±0.6	±1.2	%FSR
Conversion time	t_{CONV}	4.5 V ≤ AV_{DD} ≤ 5.5 V	12		96	μs
		4.0 V ≤ AV_{DD} < 4.5 V	14		96	μs
		2.7 V ≤ AV_{DD} < 4.0 V	17		96	μs
		1.8 V ≤ AV_{DD} < 2.7 V	28		96	μs
Zero-scale error[Notes 1, 2]		4.0 V ≤ AV_{REF} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF} < 4.0 V			±0.6	%FSR
		1.8 V ≤ AV_{REF} < 2.7 V			±1.2	%FSR
Full-scale error[Notes 1, 2]		4.0 V ≤ AV_{REF} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF} < 4.0 V			±0.6	%FSR
		1.8 V ≤ AV_{REF} < 2.7 V			±1.2	%FSR
Integral linearity error[Note 1]		4.0 V ≤ AV_{REF} ≤ 5.5 V			±2.5	LSB
		2.7 V ≤ AV_{REF} < 4.0 V			±4.5	LSB
		1.8 V ≤ AV_{REF} < 2.7 V			±8.5	LSB
Differential linearity error		4.0 V ≤ AV_{REF} ≤ 5.5 V			±1.5	LSB
		2.7 V ≤ AV_{REF} ≤ 4.0 V			±2.0	LSB
		1.8 V ≤ AV_{REF} < 2.7 V			±3.5	LSB
Analog input voltage	V_{IAN}		0		AV_{REF}	V
Reference voltage	AV_{REF}		1.8		AV_{DD}	V
Resistance between AV_{REF} and AV_{SS}	R_{REF}	During A/D conversion operation	20	40		kΩ

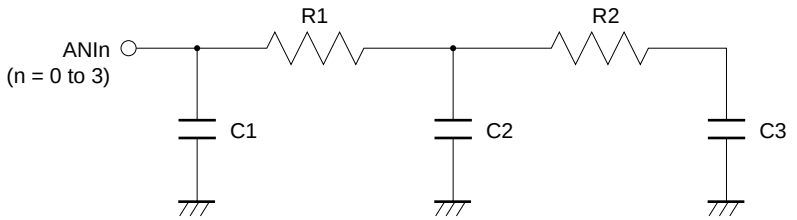
Notes 1. Excluding quantization error (±1/2 LSB).

2. Indicated as a ratio to the full-scale value (%FSR).

Remark When the μPD78F0034B is used as an 8-bit resolution A/D converter, the specifications are the same as for the μPD780024A Subseries A/D converter.

Remark The impedance of the analog input pins is shown below.

[Equivalent circuit]



[Parameter value]

(TYP.)

AV_{DD}	R1	R2	C1	C2	C3
2.7 V	12 kΩ	8.0 kΩ	3.0 pF	3.0 pF	2.0 pF
4.5 V	4 kΩ	2.7 kΩ	3.0 pF	1.4 pF	2.0 pF

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.6		5.5	V
Data retention supply current	I_{DDDR}	Subsystem clock stop (XT1 = V_{DD}) and feed-back resistor disconnected		0.1	30	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{\text{RESET}}$		$2^{17}/f_X$		s
		Release by interrupt request		**Note**		s

Note Selection of $2^{12}/f_X$ and $2^{14}/f_X$ to $2^{17}/f_X$ is possible using bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register (OSTS).

Flash Memory Programming Characteristics (T_A = +10 to +40°C, V_{DD} = 1.8 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

(1) Write erase characteristics

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Operating frequency	f_X	4.5 V ≤ V_{DD} ≤ 5.5 V			1.0		10.0	MHz
		3.0 V ≤ V_{DD} < 4.5 V			1.0		8.38	MHz
		1.8 V ≤ V_{DD} < 3.0 V			1.0		1.25	MHz
V_{PP} supply voltage	V_{PP2}	During flash memory programming			9.7	10.0	10.3	V
V_{DD} supply current	I_{DD}	When V_{PP} = V_{PP2}	10 MHz crystal oscillation operating mode	V_{DD} = 5.0 V±10%			30	mA
			8.38 MHz crystal oscillation operating mode	V_{DD} = 5.0 V±10%			24	mA
				V_{DD} = 3.0 V±10%			17	mA
V_{PP} supply current	I_{PP}	When V_{PP} = V_{PP2}					100	mA
Step erase time[Note 1]	T_{er}				0.199	0.2	0.201	s
Overall erase time[Note 2]	T_{era}	When step erase time = 0.2 s					20	s/chip
Writeback time[Note 3]	T_{wb}				49.4	50	50.6	ms
Number of writebacks per writeback command[Note 4]	C_{wb}	When writeback time = 50 ms					60	Times
Number of erases/writebacks	C_{erwb}						16	Times
Step write time[Note 5]	T_{wr}				48	50	52	μs
Overall write time per word[Note 6]	T_{wrw}	When step write time = 50 μs (1 word = 1 byte)			48		520	μs
Number of rewrites per chip[Note 7]	C_{erwb}	1 erase + 1 write after erase = 1 rewrite					20	Times

Notes 1. The recommended setting value of the step erase time is 0.2 s.

2. The prewrite time before erasure and the erase verify time (writeback time) are not included.

3. The recommended setting value of the writeback time is 50 ms.

4. Writeback is executed once by the issuance of the writeback command. Therefore, the number of retries must be the maximum value minus the number of commands issued.

5. The recommended setting value of the step write time is 50 μs.

6. The actual write time per word is 100 μs longer. The internal verify time during or after a write is not included.

7. When a product is first written after shipment, "erase → write" and "write only" are both taken as one rewrite.

Example: P: Write, E: Erase

Shipped product →P→E→P→E→P: 3 rewrites

Shipped product →E→P→E→P→E→P: 3 rewrites

(2) Serial write operation characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V_{PP} set time	t_{PSRON}	V_{PP} high voltage	1.0			μs
Set time from V_{DD}↑ to V_{PP}↑	t_{DRPSR}	V_{PP} high voltage	10			μs
Set time from V_{PP}↑ to $\overline{RESET}$↑	t_{PSRRF}	V_{PP} high voltage	1.0			μs
V_{PP} count start time from $\overline{RESET}$↑	t_{RFCF}		1.0			μs
Count execution time	t_{COUNT}				2.0	ms
V_{PP} counter high-level width	t_{CH}		8.0			μs
V_{PP} counter low-level width	t_{CL}		8.0			μs
V_{PP} counter noise elimination width	t_{NFW}			40		ns

9.2 μPD78F0034BY, 78F0034BY(A)

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V_{DD}			–0.3 to +6.5	V
	V_{PP}	**Note 2**		–0.3 to +10.5	V
	AV_{DD}			–0.3 to V_{DD} + 0.3**Note 1**	V
	AV_{REF}			–0.3 to V_{DD} + 0.3**Note 1**	V
	AV_{SS}			–0.3 to +0.3	V
Input voltage	V_{I1}	P00 to P03, P10 to P17, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75, X1, X2, XT1, XT2, $\overline{\text{RESET}}$		–0.3 to V_{DD} + 0.3**Note 1**	V
	V_{I2}	P30 to P33	N-ch open drain	–0.3 to +6.5	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3**Note 1**	V
Analog input voltage	V_{AN}	P10 to P17	Analog input pin	AV_{SS} –0.3 to AV_{REF} + 0.3**Note 1** and –0.3 to V_{DD} + 0.3**Note 1**	V
Output current, high	I_{OH}	Per pin		–10	mA
		Total for P00 to P03, P40 to P47, P50 to P57, P64 to P67, P70 to P75		–15	mA
		Total for P20 to P25, P30 to P36		–15	mA
Output current, low	I_{OL}	Per pin for P00 to P03, P20 to P25, P34 to P36, P40 to P47, P64 to P67, P70 to P75		20	mA
		Per pin for P30 to P33, P50 to P57		30	mA
		Total for P00 to P03, P40 to P47, P64 to P67, P70 to P75		50	mA
		Total for P20 to P25		20	mA
		Total for P30 to P36		100	mA
		Total for P50 to P57		100	mA
Operating ambient temperature	T_A	During normal operation		–40 to +85	°C
Storage temperature	T_{stg}			–40 to +125	°C

Notes 1. 6.5 V or below

(**Note 2** is explained on the following page.)

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

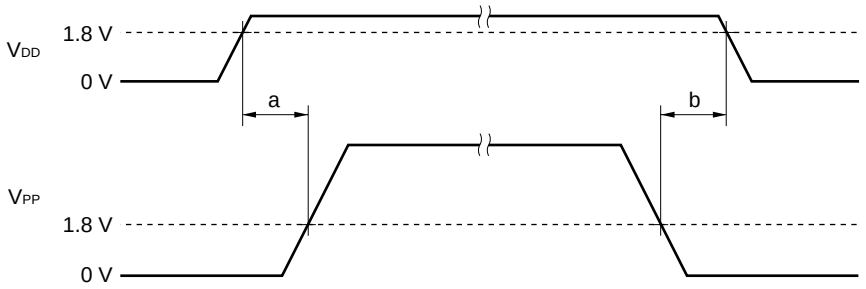
Notes 2. Make sure that the following conditions of the V_{PP} voltage application timing are satisfied when the flash memory is written.

- **When supply voltage rises**

  V_{PP} must exceed V_{DD} 10 μs or more after V_{DD} has reached the lower-limit value (1.8 V) of the operating voltage range (see a in the figure below).

- **When supply voltage drops**

  V_{DD} must be lowered 10 μs or more after V_{PP} falls below the lower-limit value (1.8 V) of the operating voltage range of V_{DD} (see b in the figure below).

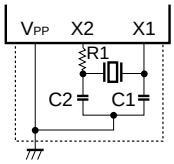
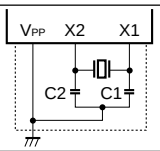
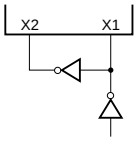


Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V.				15	pF
I/O capacitance	C_{IO}	f = 1 MHz Unmeasured pins returned to 0 V.	P00 to P03, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75,			15	pF
			P30 to P33			20	pF

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

Main System Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)Note 1	4.0 V ≤ V_{DD} ≤ 5.5 V	1.0		8.38	MHz
			1.8 V ≤ V_{DD} < 4.0 V	1.0		5.0	
		Oscillation stabilization timeNote 2	After V_{DD} reaches oscillation voltage range MIN.			4	ms
Crystal resonator		Oscillation frequency (f_X)Note 1	4.0 V ≤ V_{DD} ≤ 5.5 V	1.0		8.38	MHz
			1.8 V ≤ V_{DD} < 4.0 V	1.0		5.0	
		Oscillation stabilization timeNote 2	4.0 V ≤ V_{DD} ≤ 5.5 V			10	ms
			1.8 V ≤ V_{DD} < 4.0 V			30	
External clock		X1 input frequency (f_X)Note 1	4.0 V ≤ V_{DD} ≤ 5.5 V	1.0		8.38	MHz
			1.8 V ≤ V_{DD} < 4.0 V	1.0		5.0	
		X1 input high-/low-level width (t_{XH}, t_{XL})	4.0 V ≤ V_{DD} ≤ 5.5 V	50		500	ns
			1.8 V ≤ V_{DD} < 4.0 V	85		500	

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release.

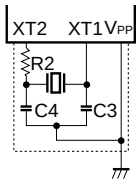
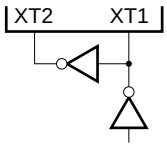
Cautions 1. When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS1}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. When the main system clock is stopped and the system is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

Remark For the resonator selection and oscillator constant, customers are required to either evaluate the oscillation themselves or apply to the resonator manufacture for evaluation.

Subsystem Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT})**Note 1**		32	32.768	35	kHz
		Oscillation stabilization time**Note 2**	4.0 V ≤ V_{DD} ≤ 5.5 V		1.2	2	s
			1.8 V ≤ V_{DD} < 4.0 V			10	
External clock		X1 input frequency (f_{XT})**Note 1**		32		38.5	kHz
		X1 input high-/low-level width (t_{XTH}, t_{XTL})		12		15	μs

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after V_{DD} reaches oscillator voltage MIN.

Cautions 1. When using the subsystem clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor to the same potential as V_{SS1}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The subsystem clock oscillator is designed as a low-amplitude circuit for reducing power consumption, and is more prone to malfunction due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

Remark For the resonator selection and oscillator constant, customers are required to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high	I_{OH}	Per pin				–1	mA
		All pins				–15	mA
Output current, low	I_{OL}	Per pin for P00 to P03, P20 to P25, P34 to P36, P40 to P47, P64 to P67, P70 to P75				10	mA
		Per pin for P30 to P33, P50 to P57				15	mA
		Total for P00 to P03, P40 to P47, P64 to P67, P70 to P75				20	mA
		Total for P20 to P25				10	mA
		Total for P30 to P36				70	mA
		Total for P50 to P57				70	mA
Input voltage, high	V_{IH1}	P10 to P17, P21, P24, P35, P40 to P47, P50 to P57, P64 to P67, P74, P75	2.7 V ≤ V_{DD} ≤ 5.5 V	0.7V_{DD}		V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V	0.8V_{DD}		V_{DD}	V
	V_{IH2}	P00 to P03, P20, P22, P23, P25, P34, P36, P70 to P73, $\overline{\text{RESET}}$	2.7 V ≤ V_{DD} ≤ 5.5 V	0.8V_{DD}		V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V	0.85V_{DD}		V_{DD}	V
	V_{IH3}	P30 to P33 (N-ch open-drain)	2.7 V ≤ V_{DD} ≤ 5.5 V	0.7V_{DD}		5.5	V
			1.8 V ≤ V_{DD} < 2.7 V	0.8V_{DD}		5.5	V
	V_{IH4}	X1, X2	2.7 V ≤ V_{DD} ≤ 5.5 V	V_{DD} – 0.5		V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V	V_{DD} – 0.2		V_{DD}	V
	V_{IH5}	XT1, XT2	4.0 V ≤ V_{DD} ≤ 5.5 V	0.8V_{DD}		V_{DD}	V
			1.8 V ≤ V_{DD} < 4.0 V	0.9V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P10 to P17, P21, P24, P35, P40 to P47, P50 to P57, P64 to P67, P74, P75	2.7 V ≤ V_{DD} ≤ 5.5 V	0		0.3V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V	0		0.2V_{DD}	V
	V_{IL2}	P00 to P03, P20, P22, P23, P25, P34, P36, P70 to P73, $\overline{\text{RESET}}$	2.7 V ≤ V_{DD} ≤ 5.5 V	0		0.2V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V	0		0.15V_{DD}	V
	V_{IL3}	P30 to P33	4.0 V ≤ V_{DD} ≤ 5.5 V	0		0.3V_{DD}	V
			2.7 V ≤ V_{DD} < 4.0 V	0		0.2V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V	0		0.1V_{DD}	V
	V_{IL4}	X1, X2	2.7 V ≤ V_{DD} ≤ 5.5 V	0		0.4	V
			1.8 V ≤ V_{DD} < 2.7 V	0		0.2	V
	V_{IL5}	XT1, XT2	4.0 V ≤ V_{DD} ≤ 5.5 V	0		0.2V_{DD}	V
			1.8 V ≤ V_{DD} < 4.0 V	0		0.1V_{DD}	V
Output voltage, high	V_{OH1}	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = –1 mA		V_{DD} – 1.0		V_{DD}	V
		1.8 V ≤ V_{DD} < 4.0 V, I_{OH} = –100 μA		V_{DD} – 0.5		V_{DD}	V
Output voltage, low	V_{OL1}	P30 to P33	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 15 mA			2.0	V
		P50 to P57			0.4	2.0	V
		P00 to P03, P20 to P25, P34 to P36, P40 to P47, P64 to P67, P70 to P75	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	I_{OL} = 400 μA				0.5	V

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	$V_{IN} = V_{DD}$	P00 to P03, P10 to P17, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75, $\overline{RESET}$			3	μA
	I_{LIH2}		X1, X2, XT1, XT2			20	μA
	I_{LIH3}	V_{IN} = 5.5 V	P30 to P33			3	μA
Input leakage current, low	I_{LIL1}	V_{IN} = 0 V	P00 to P03, P10 to P17, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75, $\overline{RESET}$			–3	μA
	I_{LIL2}		X1, X2, XT1, XT2			–20	μA
	I_{LIL3}		P30 to P33			–3	μA
Output leakage current, high	I_{LOH}	$V_{OUT} = V_{DD}$				3	μA
Output leakage current, low	I_{LOL}	V_{OUT} = 0 V				–3	μA
Software pull-up resistor	R	V_{IN} = 0 V, P00 to P03, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75		15	30	90	kΩ

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Power supply current[Note 1]	I_{DD1}[Note 2]	8.38 MHz crystal oscillation operating mode	V_{DD} = 5.0 V ±10%[Note 3]	When A/D converter is stopped		10.5	21	mA
				When A/D converter is operating[Note 6]		11.5	23	mA
		5.00 MHz crystal oscillation operating mode	V_{DD} = 3.0 V ±10%[Note 3]	When A/D converter is stopped		4.5	9	mA
				When A/D converter is operating[Note 6]		5.5	11	mA
			V_{DD} = 2.0 V ±10%[Note 4]	When A/D converter is stopped		1	2	mA
				When A/D converter is operating[Note 6]		2	6	mA
	I_{DD2}	8.38 MHz crystal oscillation HALT mode	V_{DD} = 5.0 V ±10%[Note 3]	When peripheral functions are stopped		1.2	2.4	mA
				When peripheral functions are operating			5	mA
		5.00 MHz crystal oscillation HALT mode	V_{DD} = 3.0 V ±10%[Note 3]	When peripheral functions are stopped		0.4	0.8	mA
				When peripheral functions are operating			1.7	mA
			V_{DD} = 2.0 V ±10%[Note 4]	When peripheral functions are stopped		0.2	0.4	mA
				When peripheral functions are operating			1.1	mA
	I_{DD3}	32.768 kHz crystal oscillation operating mode[Note 5]		V_{DD} = 5.0 V ±10%[Note 2]		115	230	μA
				V_{DD} = 3.0 V ±10%[Note 2]		95	190	μA
				V_{DD} = 2.0 V ±10%[Note 3]		75	150	μA
	I_{DD4}	32.768 kHz crystal oscillation HALT mode[Note 5]		V_{DD} = 5.0 V ±10%[Note 2]		30	60	μA
				V_{DD} = 3.0 V ±10%[Note 2]		6	18	μA
				V_{DD} = 2.0 V ±10%[Note 3]		2	10	μA
	I_{DD5}	XT1 = V_{DD} STOP mode When feedback resistor is not used		V_{DD} = 5.0 V ±10%[Note 2]		0.1	30	μA
				V_{DD} = 3.0 V ±10%[Note 2]		0.05	10	μA
				V_{DD} = 2.0 V ±10%[Note 3]		0.05	10	μA

Notes 1. Total current through the internal power supply (V_{DD0}, V_{DD1}) (except the current through pull-up resistors of ports).

2. I_{DD1} includes the peripheral operation current.

3. When the processor clock control register (PCC) is set to 00H.

4. When PCC is set to 02H.

5. When main system clock operation is stopped.

6. Includes the current through the AV_{DD} pin.

AC Characteristics

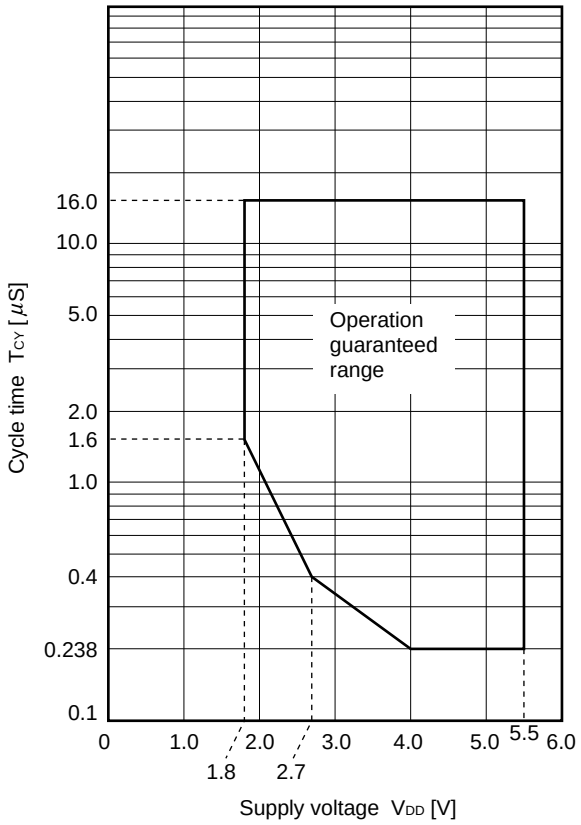
(1) Basic Operation (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (Min. instruction execution time)	T_{CY}	Operating with main system clock	4.0 V ≤ V_{DD} ≤ 5.5 V	0.238		16	μs
			2.7 V ≤ V_{DD} < 4.0 V	0.4		16	μs
			1.8 V ≤ V_{DD} < 2.7 V	1.6		16	μs
		Operating with subsystem clock		103.9Note 1	122	125	μs
TI00, TI01 input high-/low-level width	t_{TIH0}, t_{TIL0}	4.0 V ≤ V_{DD} ≤ 5.5 V		$2/f_{sam}$+0.1Note 2			μs
		2.7 V ≤ V_{DD} < 4.0 V		$2/f_{sam}$+0.2Note 2			μs
		1.8 V ≤ V_{DD} < 2.7 V		$2/f_{sam}$+0.5Note 2			μs
TI50, TI51 input frequency	f_{TI5}	2.7 V ≤ V_{DD} ≤ 5.5 V		0		4	MHz
		1.8 V ≤ V_{DD} < 2.7 V		0		275	kHz
TI50, TI51 input high-/low-level width	t_{TIH5}, t_{TIL5}	2.7 V ≤ V_{DD} ≤ 5.5 V		100			ns
		1.8 V ≤ V_{DD} < 2.7 V		1.8			ns
Interrupt request input high-/low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP3, P40 to P47	2.7 V ≤ V_{DD} ≤ 5.5 V	1			μs
			1.8 V ≤ V_{DD} < 2.7 V	2			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}	2.7 V ≤ V_{DD} ≤ 5.5 V		10			μs
		1.8 V ≤ V_{DD} < 2.7 V		20			μs

Notes 1. Value when the external clock is used. When a crystal resonator is used, it is 114 μs (MIN.).

2. Selection of f_{sam} = f_X, f_X/4, f_X/64 is possible using bits 0 and 1 (PRM00, PRM01) of prescaler mode register 0 (PRM0). However, if the TI00 valid edge is selected as the count clock, the value becomes f_{sam} = f_X/8.

T_{CY} vs. V_{DD} (main system clock operation)



(2) Read/write operation (T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V) **(1/3)**

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		$0.3t_{CY}$		ns
Address setup time	t_{ADS}		20		ns
Address hold time	t_{ADH}		6		ns
Input time from address to data	t_{ADD1}			$(2 + 2n)t_{CY}$ – 54	ns
	t_{ADD2}			$(3 + 2n)t_{CY}$ – 60	ns
Output time from $\overline{RD}\downarrow$ to address	t_{RDAD}		0	100	ns
Input time from $\overline{RD}\downarrow$ to data	t_{RDD1}			$(2 + 2n)t_{CY}$ – 87	ns
	t_{RDD2}			$(3 + 2n)t_{CY}$ – 93	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		$(1.5 + 2n)t_{CY}$ – 33		ns
	t_{RDL2}		$(2.5 + 2n)t_{CY}$ – 33		ns
Input time from $\overline{RD}\downarrow$ to $\overline{WAIT}\downarrow$	t_{RDWT1}			t_{CY} – 43	ns
	t_{RDWT2}			t_{CY} – 43	ns
Input time from $\overline{WR}\downarrow$ to $\overline{WAIT}\downarrow$	t_{WRWT}			t_{CY} – 25	ns
$\overline{WAIT}$ low-level width	t_{WTL}		$(0.5 + n)t_{CY}$ + 10	$(2 + 2n)t_{CY}$	ns
Write data setup time	t_{WDS}		60		ns
Write data hold time	t_{WDH}		6		ns
$\overline{WR}$ low-level width	t_{WRL1}		$(1.5 + 2n)t_{CY}$ – 15		ns
Delay time from ASTB↓ to $\overline{RD}\downarrow$	t_{ASTRD}		6		ns
Delay time from ASTB↓ to $\overline{WR}\downarrow$	t_{ASTWR}		$2t_{CY}$ – 15		ns
Delay time from $\overline{RD}\uparrow$ to ASTB↑ in external fetch	t_{RDAST}		$0.8t_{CY}$ – 15	$1.2t_{CY}$	ns
Hold time from $\overline{RD}\uparrow$ to address in external fetch	t_{RDADH}		$0.8t_{CY}$ – 15	$1.2t_{CY}$ + 30	ns
Write data output time from $\overline{RD}\uparrow$	t_{RDWD}		40		ns
Write data output time from $\overline{WR}\downarrow$	t_{WRWD}		10	60	ns
Hold time from $\overline{WR}\uparrow$ to address	t_{WRADH}		$0.8t_{CY}$ – 15	$1.2t_{CY}$ + 30	ns
Delay time from $\overline{WAIT}\uparrow$ to $\overline{RD}\uparrow$	t_{WTRD}		$0.8t_{CY}$	$2.5t_{CY}$ + 25	ns
Delay time from $\overline{WAIT}\uparrow$ to $\overline{WR}\uparrow$	t_{WTWR}		$0.8t_{CY}$	$2.5t_{CY}$ + 25	ns

Caution T_{CY} can only be used when the MIN. value is 0.238 μs.

Remarks 1. $t_{CY} = T_{CY}/4$

2. n indicates the number of waits.

3. C_L = 100 pF (C_L is the load capacitance of the AD0 to AD7, A8 to A15, $\overline{RD}$, $\overline{WR}$, $\overline{WAIT}$, and ASTB pins.)

(2) Read/write operation (T_A = –40 to +85°C, V_{DD} = 2.7 to 4.0 V) (2/3)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		$0.3t_{CY}$		ns
Address setup time	t_{ADS}		30		ns
Address hold time	t_{ADH}		10		ns
Input time from address to data	t_{ADD1}			$(2 + 2n)t_{CY}$ – 108	ns
	t_{ADD2}			$(3 + 2n)t_{CY}$ – 120	ns
Output time from $\overline{RD}\downarrow$ to address	t_{RDAD}		0	200	ns
Input time from $\overline{RD}\downarrow$ to data	t_{RDD1}			$(2 + 2n)t_{CY}$ – 148	ns
	t_{RDD2}			$(3 + 2n)t_{CY}$ – 162	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		$(1.5 + 2n)t_{CY}$ – 40		ns
	t_{RDL2}		$(2.5 + 2n)t_{CY}$ – 40		ns
Input time from $\overline{RD}\downarrow$ to $\overline{WAIT}\downarrow$	t_{RDWT1}			t_{CY} – 75	ns
	t_{RDWT2}			t_{CY} – 60	ns
Input time from $\overline{WR}\downarrow$ to $\overline{WAIT}\downarrow$	t_{WRWT}			t_{CY} – 50	ns
$\overline{WAIT}$ low-level width	t_{WTL}		$(0.5 + 2n)t_{CY}$ + 10	$(2 + 2n)t_{CY}$	ns
Write data setup time	t_{WDS}		60		ns
Write data hold time	t_{WDH}		10		ns
$\overline{WR}$ low-level width	t_{WRL1}		$(1.5 + 2n)t_{CY}$ – 30		ns
Delay time from ASTB↓ to $\overline{RD}\downarrow$	t_{ASTRD}		10		ns
Delay time from ASTB↓ to $\overline{WR}\downarrow$	t_{ASTWR}		$2t_{CY}$ – 30		ns
Delay time from $\overline{RD}\uparrow$ to ASTB↑ in external fetch	t_{RDAST}		$0.8t_{CY}$ – 30	$1.2t_{CY}$	ns
Hold time from $\overline{RD}\uparrow$ to address in external fetch	t_{RDADH}		$0.8t_{CY}$ – 30	$1.2t_{CY}$ + 60	ns
Write data output time from $\overline{RD}\uparrow$	t_{RDWD}		40		ns
Write data output time from $\overline{WR}\downarrow$	t_{WRWD}		20	120	ns
Hold time from $\overline{WR}\uparrow$ to address	t_{WRADH}		$0.8t_{CY}$ – 30	$1.2t_{CY}$ + 60	ns
Delay time from $\overline{WAIT}\uparrow$ to $\overline{RD}\uparrow$	t_{WTRD}		$0.5t_{CY}$	$2.5t_{CY}$ + 50	ns
Delay time from $\overline{WAIT}\uparrow$ to $\overline{WR}\uparrow$	t_{WTWR}		$0.5t_{CY}$	$2.5t_{CY}$ + 50	ns

Caution T_{CY} can only be used when the MIN. value is 0.4 μs.

Remarks 1. $t_{CY} = T_{CY}/4$

2. n indicates the number of waits.

3. C_L = 100 pF (C_L is the load capacitance of the AD0 to AD7, A8 to A15, $\overline{RD}$, $\overline{WR}$, $\overline{WAIT}$, and ASTB pins.)

(2) Read/write operation (T_A = –40 to +85°C, V_{DD} = 1.8 to 2.7 V) (3/3)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		$0.3t_{CY}$		ns
Address setup time	t_{ADS}		120		ns
Address hold time	t_{ADH}		20		ns
Input time from address to data	t_{ADD1}			$(2 + 2n)t_{CY}$ – 233	ns
	t_{ADD2}			$(3 + 2n)t_{CY}$ – 240	ns
Output time from $\overline{RD}\downarrow$ to address	t_{RDAD}		0	400	ns
Input time from $\overline{RD}\downarrow$ to data	t_{RDD1}			$(2 + 2n)t_{CY}$ – 325	ns
	t_{RDD2}			$(3 + 2n)t_{CY}$ – 332	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		$(1.5 + 2n)t_{CY}$ – 92		ns
	t_{RDL2}		$(2.5 + 2n)t_{CY}$ – 92		ns
Input time from $\overline{RD}\downarrow$ to $\overline{WAIT}\downarrow$	t_{RDWT1}			t_{CY} – 350	ns
	t_{RDWT2}			t_{CY} – 132	ns
Input time from $\overline{WR}\downarrow$ to $\overline{WAIT}\downarrow$	t_{WRWT}			t_{CY} – 100	ns
$\overline{WAIT}$ low-level width	t_{WTL}		$(0.5 + 2n)t_{CY}$ + 10	$(2 + 2n)t_{CY}$	ns
Write data setup time	t_{WDS}		60		ns
Write data hold time	t_{WDH}		20		ns
$\overline{WR}$ low-level width	t_{WRL1}		$(1.5 + 2n)t_{CY}$ – 60		ns
Delay time from ASTB↓ to $\overline{RD}\downarrow$	t_{ASTRD}		20		ns
Delay time from ASTB↓ to $\overline{WR}\downarrow$	t_{ASTWR}		$2t_{CY}$ – 60		ns
Delay time from $\overline{RD}\uparrow$ to ASTB↑ in external fetch	t_{RDAST}		$0.8t_{CY}$ – 60	$1.2t_{CY}$	ns
Hold time from $\overline{RD}\uparrow$ to address in external fetch	t_{RDADH}		$0.8t_{CY}$ – 60	$1.2t_{CY}$ + 120	ns
Write data output time from $\overline{RD}\uparrow$	t_{RDWD}		40		ns
Write data output time from $\overline{WR}\downarrow$	t_{WRWD}		40	240	ns
Hold time from $\overline{WR}\uparrow$ to address	t_{WRADH}		$0.8t_{CY}$ – 60	$1.2t_{CY}$ + 120	ns
Delay time from $\overline{WAIT}\uparrow$ to $\overline{RD}\uparrow$	t_{WTRD}		$0.5t_{CY}$	$2.5t_{CY}$ + 100	ns
Delay time from $\overline{WAIT}\uparrow$ to $\overline{WR}\uparrow$	t_{WTWR}		$0.5t_{CY}$	$2.5t_{CY}$ + 100	ns

Caution T_{CY} can only be used when the MIN. value is 1.6 μs.

Remarks 1. $t_{CY} = T_{CY}/4$

2. n indicates the number of waits.

3. C_L = 100 pF (C_L is the load capacitance of the AD0 to AD7, A8 to A15, $\overline{RD}$, $\overline{WR}$, $\overline{WAIT}$, and ASTB pins.)

(3) Serial Interface (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

(a) 3-wire serial I/O mode ($\overline{SCK30}$... Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK30}$ cycle time	t_{KCY1}	4.0 V ≤ V_{DD} ≤ 5.5 V	954			ns
		2.7 V ≤ V_{DD} < 4.0 V	1600			ns
		1.8 V ≤ V_{DD} < 2.7 V	3200			ns
$\overline{SCK30}$ high-/low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V	t_{KCY1}/2 – 50			ns
		1.8 V ≤ V_{DD} < 4.0 V	t_{KCY1}/2 – 100			ns
SI30 setup time (to $\overline{SCK30}$↑)	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.0 V	150			ns
		1.8 V ≤ V_{DD} < 2.7 V	300			ns
SI3n hold time (from $\overline{SCK30}$↑)	t_{KSI1}		400			ns
Delay time from $\overline{SCK30}$↓ to SO30 output	t_{KSO1}	C = 100 pF**Note**			300	ns

Note C is the load capacitance of the $\overline{SCK30}$ and SO30 output lines.

(b) 3-wire serial I/O mode ($\overline{SCK30}$... External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK30}$ cycle time	t_{KCY2}	4.0 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.0 V	1600			ns
		1.8 V ≤ V_{DD} < 2.7 V	3200			ns
$\overline{SCK30}$ high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ V_{DD} ≤ 5.5 V	400			ns
		2.7 V ≤ V_{DD} < 4.0 V	800			ns
		1.8 V ≤ V_{DD} < 2.7 V	1600			ns
SI30 setup time (to $\overline{SCK30}$↑)	t_{SIK2}		100			ns
SI30 hold time (from $\overline{SCK30}$↑)	t_{KSI2}		400			ns
Delay time from $\overline{SCK30}$↓ to SO30 output	t_{KSO2}	C = 100 pF**Note**			300	ns

Note C is the load capacitance of the SO30 output line.

(c) UART mode (dedicated baud-rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		4.0 V ≤ V_{DD} ≤ 5.5 V			131031	bps
		2.7 V ≤ V_{DD} < 4.0 V			78125	bps
		1.8 V ≤ V_{DD} < 2.7 V			39063	bps

(d) UART mode (external clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK0 cycle time	t_{KCY3}	4.0 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.0 V	1600			ns
		1.8 V ≤ V_{DD} < 2.7 V	3200			ns
ASCK0 high-/low-level width	t_{KH3}, t_{KL3}	4.0 V ≤ V_{DD} ≤ 5.5 V	400			ns
		2.7 V ≤ V_{DD} < 4.0 V	800			ns
		1.8 V ≤ V_{DD} < 2.7 V	1600			ns
Transfer rate		4.0 V ≤ V_{DD} ≤ 5.5 V			39063	bps
		2.7 V ≤ V_{DD} < 4.0 V			19531	bps
		1.8 V ≤ V_{DD} < 2.7 V			9766	bps

(e) UART mode (infrared data transfer mode)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Transfer rate		4.0 V ≤ V_{DD} ≤ 5.5 V		131031	bps
Allowable bit rate error		4.0 V ≤ V_{DD} ≤ 5.5 V		±0.87	%
Output pulse width		4.0 V ≤ V_{DD} ≤ 5.5 V	1.2	0.24/fbr**Note**	μs
Input pulse width		4.0 V ≤ V_{DD} ≤ 5.5 V	4/f_X		μs

Note fbr: Specified baud rate

(f) I^2C bus mode

Parameter		Symbol	Standard Mode		High-Speed Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCL0 clock frequency		f_{CLK}	0	100	0	400	kHz
Bus free time (between stop and start condition)		t_{BUF}	4.7	–	1.3	–	μs
Hold time[Note 1]		$t_{HD:STA}$	4.0	–	0.6	–	μs
SCL0 clock low-level width		t_{LOW}	4.7	–	1.3	–	μs
SCL0 clock high-level width		t_{HIGH}	4.0	–	0.6	–	μs
Start/restart condition setup time		$t_{SU:STA}$	4.7	–	0.6	–	μs
Data hold time	CBUS compatible master	$t_{HD:DAT}$	5.0	–	–	–	μs
	I^2C bus		0[Note 2]	–	0[Note 2]	0.9[Note 3]	μs
Data setup time		$t_{SU:DAT}$	250	–	100[Note 4]	–	ns
SDA0 and SCL0 signal rise time		t_R	–	1,000	20 + 0.1Cb[Note 5]	300	ns
SDA0 and SCL0 signal fall time		t_F	–	300	20 + 0.1Cb[Note 5]	300	ns
Stop condition setup time		$t_{SU:STO}$	4.0	–	0.6	–	μs
Spike pulse width controlled by input filter		t_{SP}	–	–	0	50	ns
Capacitive load per each bus line		Cb	–	400	–	400	pF

Notes 1. In the start condition, the first clock pulse is generated after this hold time.

2. To fill in the undefined area of the SCL0 falling edge, it is necessary for the device to internally provide at least 300 ns of hold time for the SDA0 signal (which is $V_{IHmin.}$ of the SCL0 signal).

3. If the device does not extend the SCL0 signal low hold time (t_{LOW}), only maximum data hold time $t_{HD:DAT}$ needs to be fulfilled.

4. The high-speed mode I^2C bus is available in a standard mode I^2C bus system. At this time, the conditions described below must be satisfied.

- If the device does not extend the SCL0 signal low state hold time

  $t_{SU:DAT} \geq 250$ ns

- If the device extends the SCL0 signal low state hold time

  Be sure to transmit the next data bit to the SDA0 line before the SCL0 line is released ($t_{Rmax.} + t_{SU:DAT}$ = 1,000 + 250 = 1,250 ns by standard mode I^2C bus specification).

5. Cb: Total capacitance per one bus line (unit: pF)

A/D Converter Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{DD} = 1.8 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	bit
Overall error[Note]		4.0 V ≤ AV_{REF} ≤ 5.5 V		±0.2	±0.4	%FSR
		2.7 V ≤ AV_{REF} < 4.0 V		±0.3	±0.6	%FSR
		1.8 V ≤ AV_{REF} < 2.7 V		±0.6	±1.2	%FSR
Conversion time	t_{CONV}	4.5 V ≤ AV_{DD} ≤ 5.5 V	12		96	μs
		4.0 V ≤ AV_{DD} < 4.5 V	14		96	μs
		2.7 V ≤ AV_{DD} < 4.0 V	17		96	μs
		1.8 V ≤ AV_{DD} < 2.7 V	28		96	μs
Zero-scale error[Notes 1, 2]		4.0 V ≤ AV_{REF} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF} < 4.0 V			±0.6	%FSR
		1.8 V ≤ AV_{REF} < 2.7 V			±1.2	%FSR
Full-scale error[Notes 1, 2]		4.0 V ≤ AV_{REF} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF} < 4.0 V			±0.6	%FSR
		1.8 V ≤ AV_{REF} < 2.7 V			±1.2	%FSR
Integral linearity error[Note 1]		4.0 V ≤ AV_{REF} ≤ 5.5 V			±2.5	LSB
		2.7 V ≤ AV_{REF} < 4.0 V			±4.5	LSB
		1.8 V ≤ AV_{REF} < 2.7 V			±8.5	LSB
Differential linearity error		4.0 V ≤ AV_{REF} ≤ 5.5 V			±1.5	LSB
		2.7 V ≤ AV_{REF} ≤ 4.0 V			±2.0	LSB
		1.8 V ≤ AV_{REF} < 2.7 V			±3.5	LSB
Analog input voltage	V_{IAN}		0		AV_{REF}	V
Reference voltage	AV_{REF}		1.8		AV_{DD}	V
Resistance between AV_{REF} and AV_{SS}	R_{REF}	During A/D conversion operation	20	40		kΩ

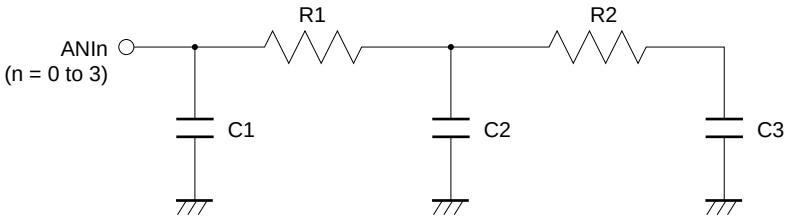
Notes 1. Excluding quantization error (±1/2 LSB).

2. Indicated as a ratio to the full-scale value (%FSR).

Remark When the μPD78F0034BY is used as an 8-bit resolution A/D converter, the specifications are the same as for the μPD780024AY Subseries A/D converter.

Remark The impedance of the analog input pins is shown below.

[Equivalent circuit]



[Parameter value]

(TYP.)

AV_{DD}	R1	R2	C1	C2	C3
2.7 V	12 kΩ	8.0 kΩ	3.0 pF	3.0 pF	2.0 pF
4.5 V	4 kΩ	2.7 kΩ	3.0 pF	1.4 pF	2.0 pF

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.6		5.5	V
Data retention supply current	I_{DDDR}	Subsystem clock stop (XT1 = V_{DD}) and feed-back resistor disconnected		0.1	30	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{\text{RESET}}$		$2^{17}/f_X$		s
		Release by interrupt request		**Note**		s

Note Selection of $2^{12}/f_X$ and $2^{14}/f_X$ to $2^{17}/f_X$ is possible using bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register (OSTS).

Flash Memory Programming Characteristics (T_A = +10 to +40°C, V_{DD} = 1.8 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

(1) Write erase characteristics

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Operating frequency	f_X	4.5 V ≤ V_{DD} ≤ 5.5 V			1.0		10.0	MHz
		3.0 V ≤ V_{DD} < 4.5 V			1.0		8.38	MHz
		1.8 V ≤ V_{DD} < 3.0 V			1.0		1.25	MHz
V_{PP} supply voltage	V_{PP2}	During flash memory programming			9.7	10.0	10.3	V
V_{DD} supply current	I_{DD}	When V_{PP} = V_{PP2}	10 MHz crystal oscillation operating mode	V_{DD} = 5.0 V±10%			30	mA
			8.38 MHz crystal oscillation operating mode	V_{DD} = 5.0 V±10%			24	mA
				V_{DD} = 3.0 V±10%			17	mA
V_{PP} supply current	I_{PP}	When V_{PP} = V_{PP2}					100	mA
Step erase time[Note 1]	T_{er}				0.199	0.2	0.201	s
Overall erase time[Note 2]	T_{era}	When step erase time = 0.2 s					20	s/chip
Writeback time[Note 3]	T_{wb}				49.4	50	50.6	ms
Number of writebacks per writeback command[Note 4]	C_{wb}	When writeback time = 50 ms					60	Times
Number of erases/writebacks	C_{erwb}						16	Times
Step write time[Note 5]	T_{wr}				48	50	52	μs
Overall write time per word[Note 6]	T_{wrw}	When step write time = 50 μs (1 word = 1 byte)			48		520	μs
Number of rewrites per chip[Note 7]	C_{erwb}	1 erase + 1 write after erase = 1 rewrite					20	Times

Notes 1. The recommended setting value of the step erase time is 0.2 s.

2. The prewrite time before erasure and the erase verify time (writeback time) are not included.

3. The recommended setting value of the writeback time is 50 ms.

4. Writeback is executed once by the issuance of the writeback command. Therefore, the number of retries must be the maximum value minus the number of commands issued.

5. The recommended setting value of the step write time is 50 μs.

6. The actual write time per word is 100 μs longer. The internal verify time during or after a write is not included.

7. When a product is first written after shipment, "erase → write" and "write only" are both taken as one rewrite.

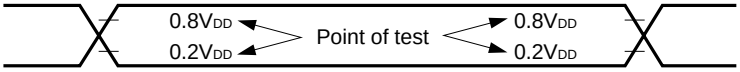
Example: P: Write, E: Erase
Shipped product →P→E→P→E→P: 3 rewrites
Shipped product →E→P→E→P→E→P: 3 rewrites

(2) Serial write operation characteristics

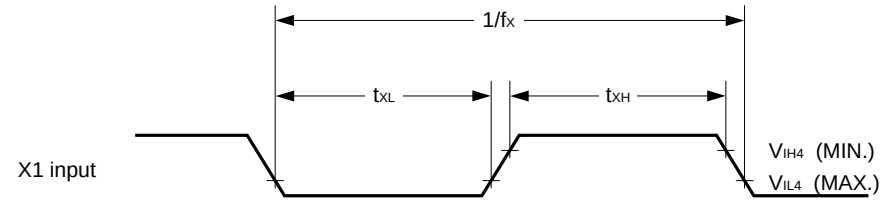
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V_{PP} set time	t_{PSRON}	V_{PP} high voltage	1.0			μs
Set time from V_{DD}↑ to V_{PP}↑	t_{DRPSR}	V_{PP} high voltage	10			μs
Set time from V_{PP}↑ to $\overline{RESET}$↑	t_{PSRRF}	V_{PP} high voltage	1.0			μs
V_{PP} count start time from $\overline{RESET}$↑	t_{RFCF}		1.0			μs
Count execution time	t_{COUNT}				2.0	ms
V_{PP} counter high-level width	t_{CH}		8.0			μs
V_{PP} counter low-level width	t_{CL}		8.0			μs
V_{PP} counter noise elimination width	t_{NFW}			40		ns

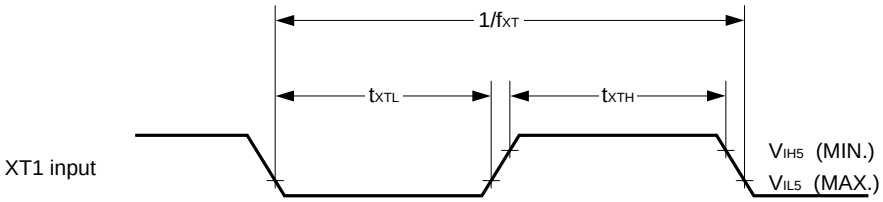
9.3 Timing Chart

AC Timing Test Point (Excluding X1, XT1 Input)

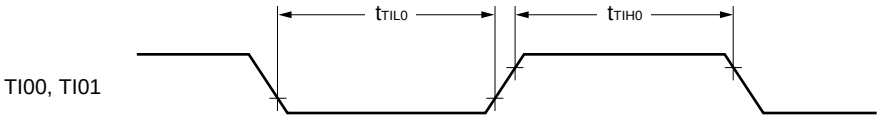


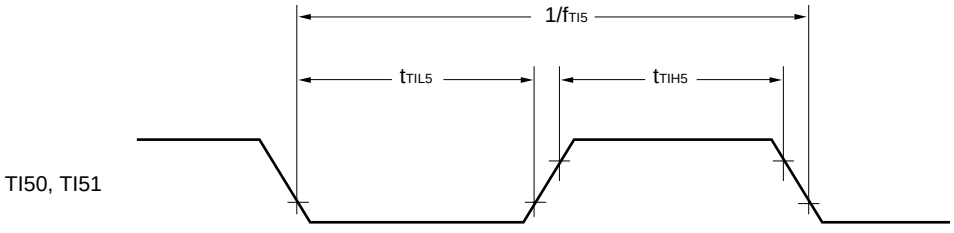
Clock Timing



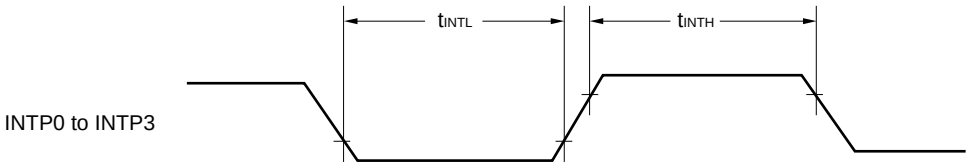


TI Timing

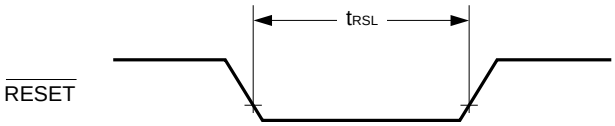




Interrupt Request Input Timing

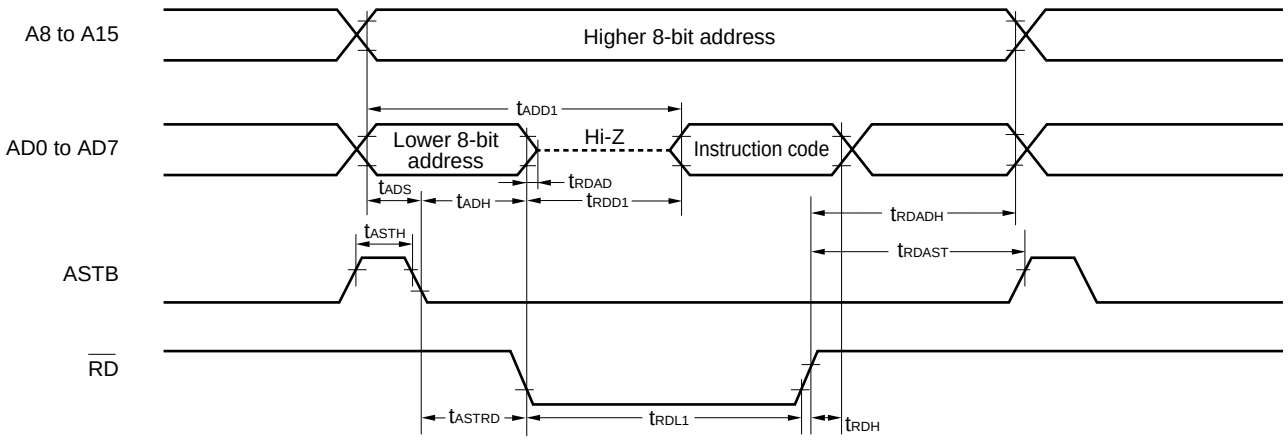


$\overline{\text{RESET}}$ Input Timing

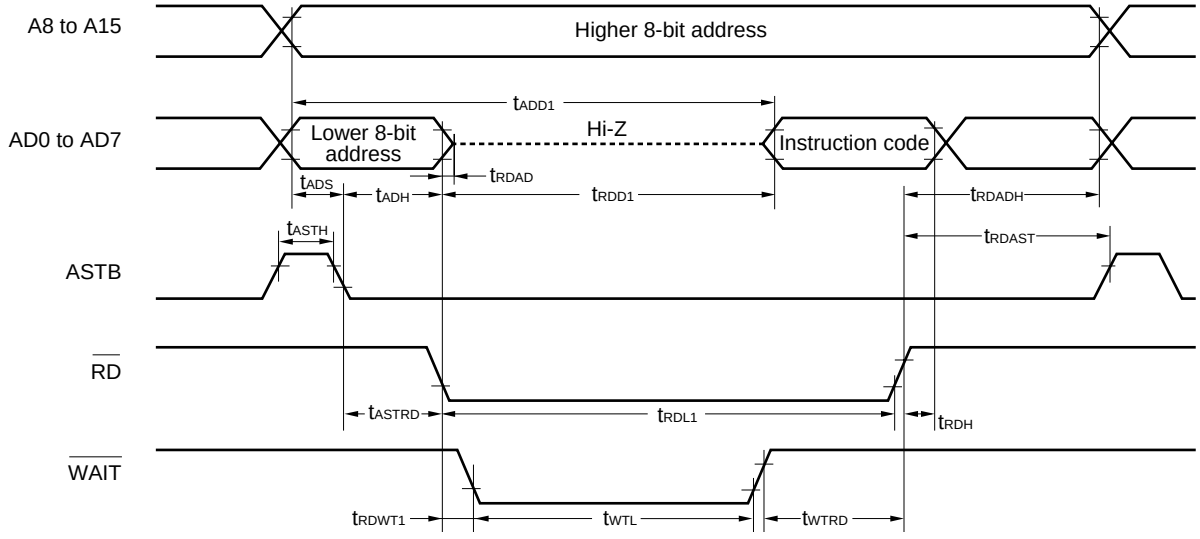


Read/Write Operation

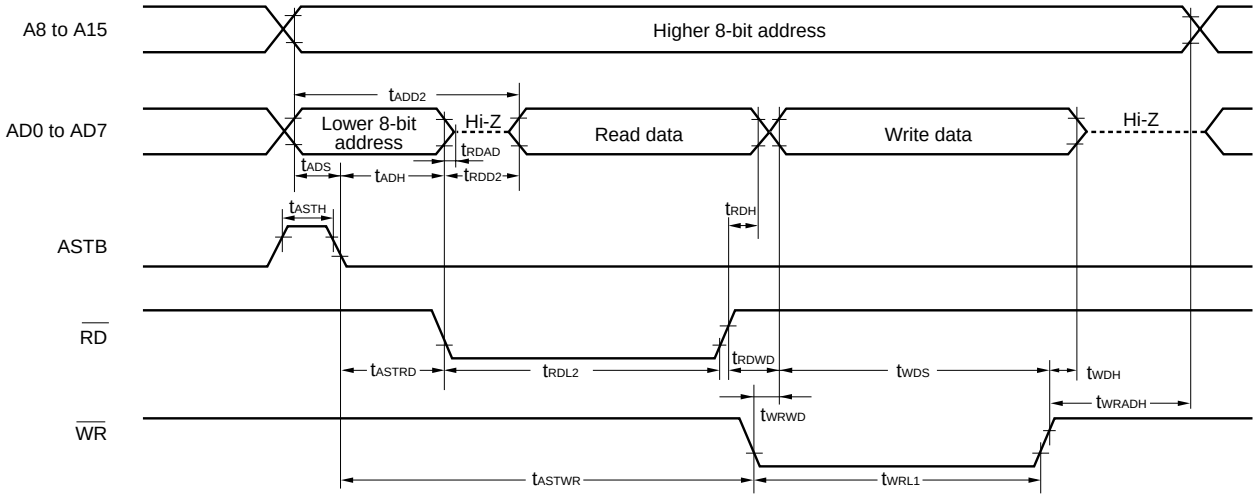
External fetch (no wait):



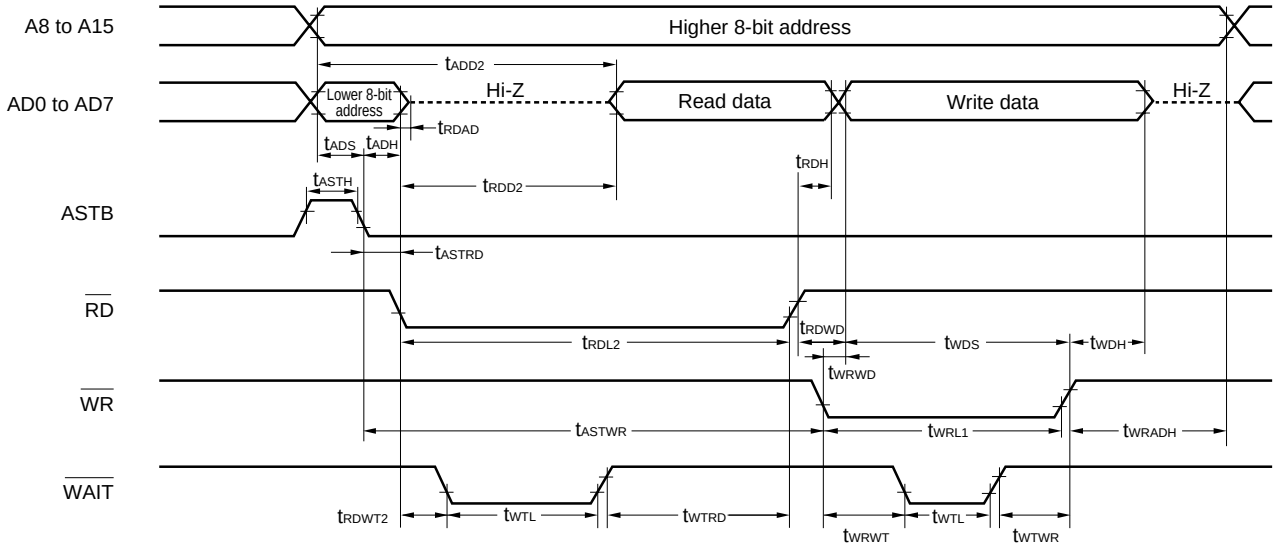
External fetch (wait insertion):



External data access (no wait):

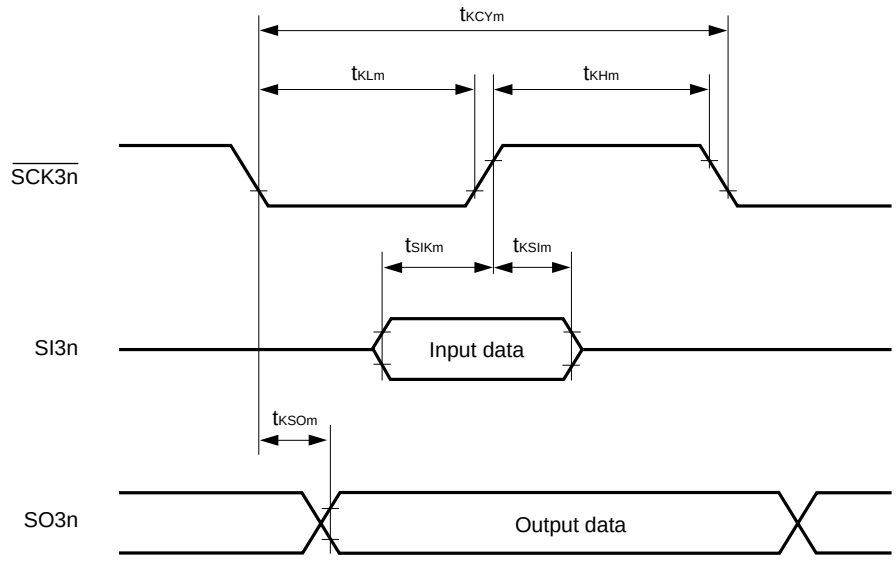


External data access (wait insertion):



Serial Transfer Timing

3-wire serial I/O mode:

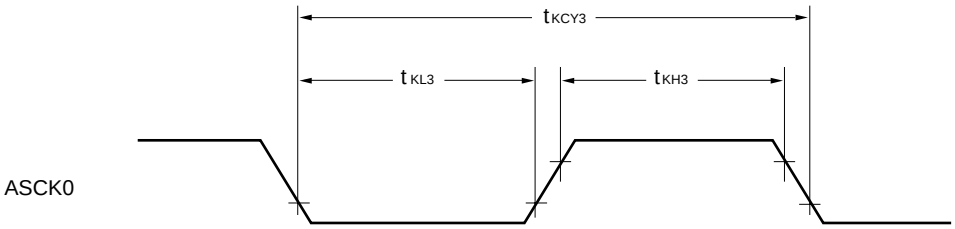


Remarks 1. m = 1, 2

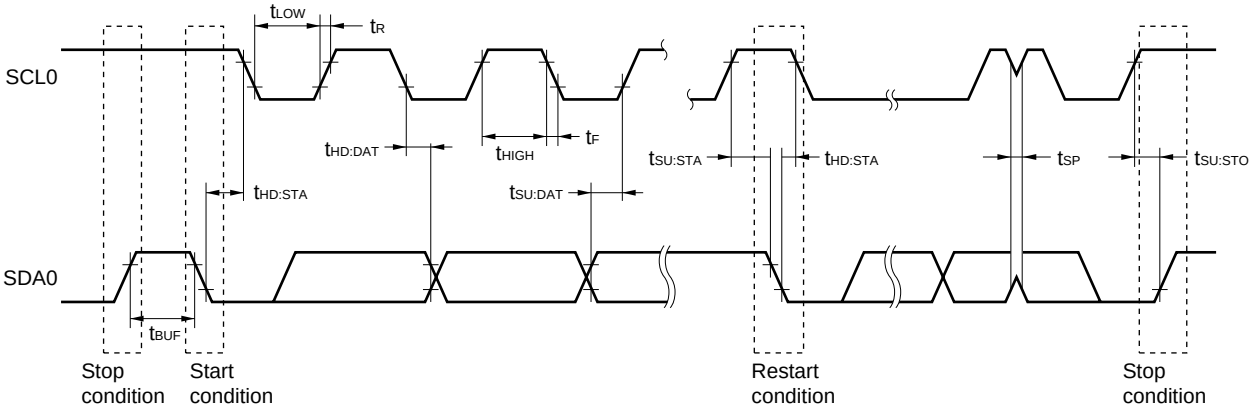
2. μPD78F0034B and 78F0034B(A): n = 0, 1

3. μPD78F0034BY and 78F0034BY(A): n = 0

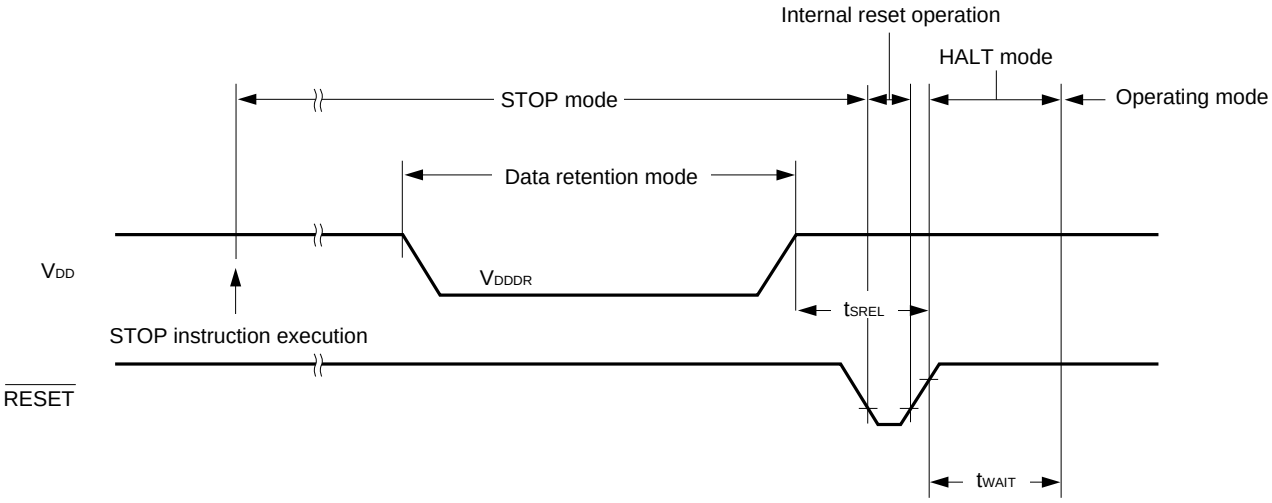
UART mode (external clock input):



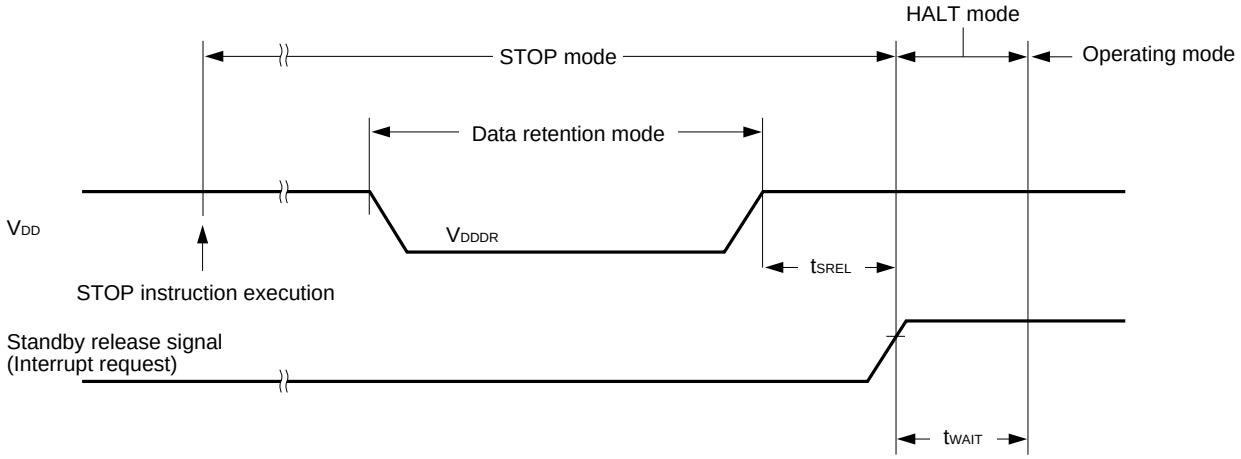
I²C bus mode (μPD78F0034BY only):



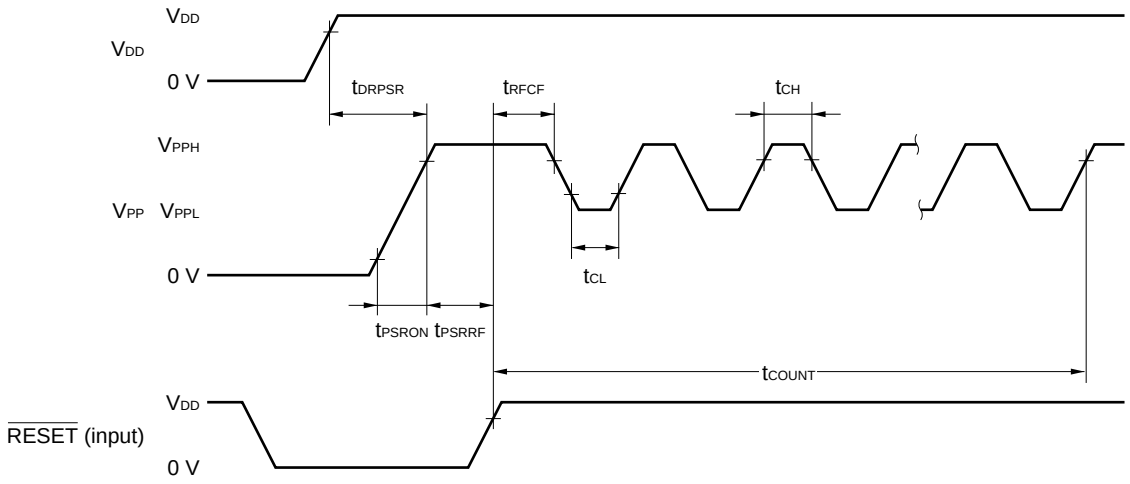
Data Retention Timing (STOP Mode Release by $\overline{\text{RESET}}$)



Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Request Signal)

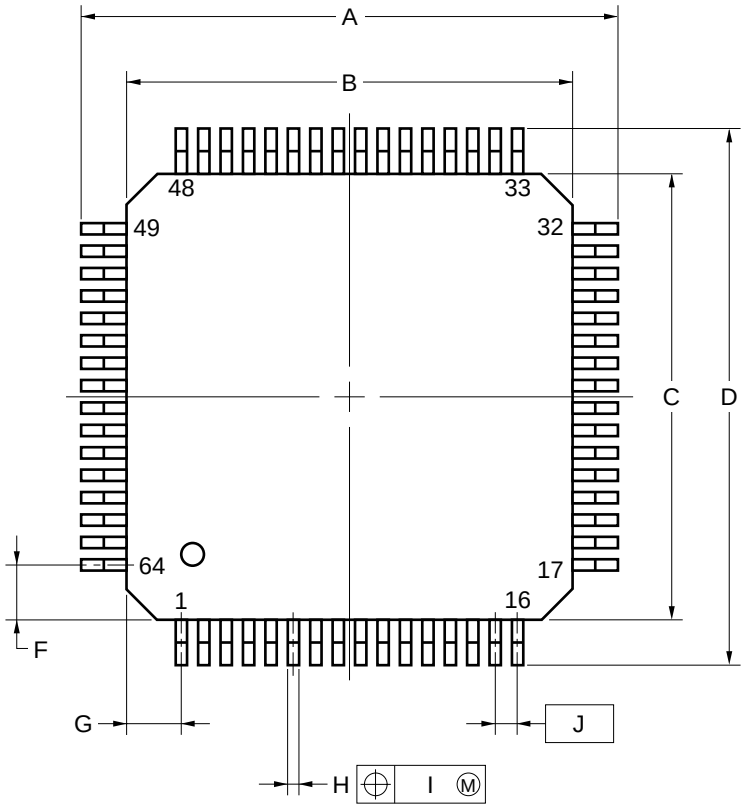


Flash Memory Write Mode Set Timing

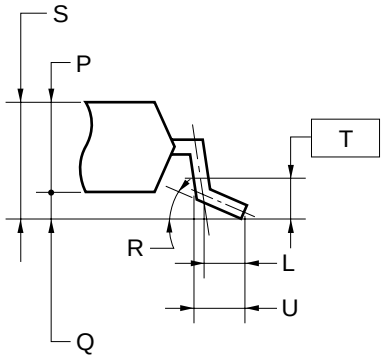


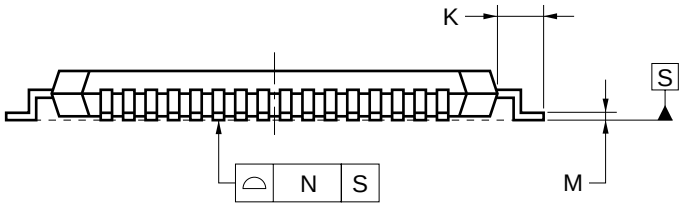
10. PACKAGE DRAWINGS

64-PIN PLASTIC LQFP (10x10)



detail of lead end





NOTE

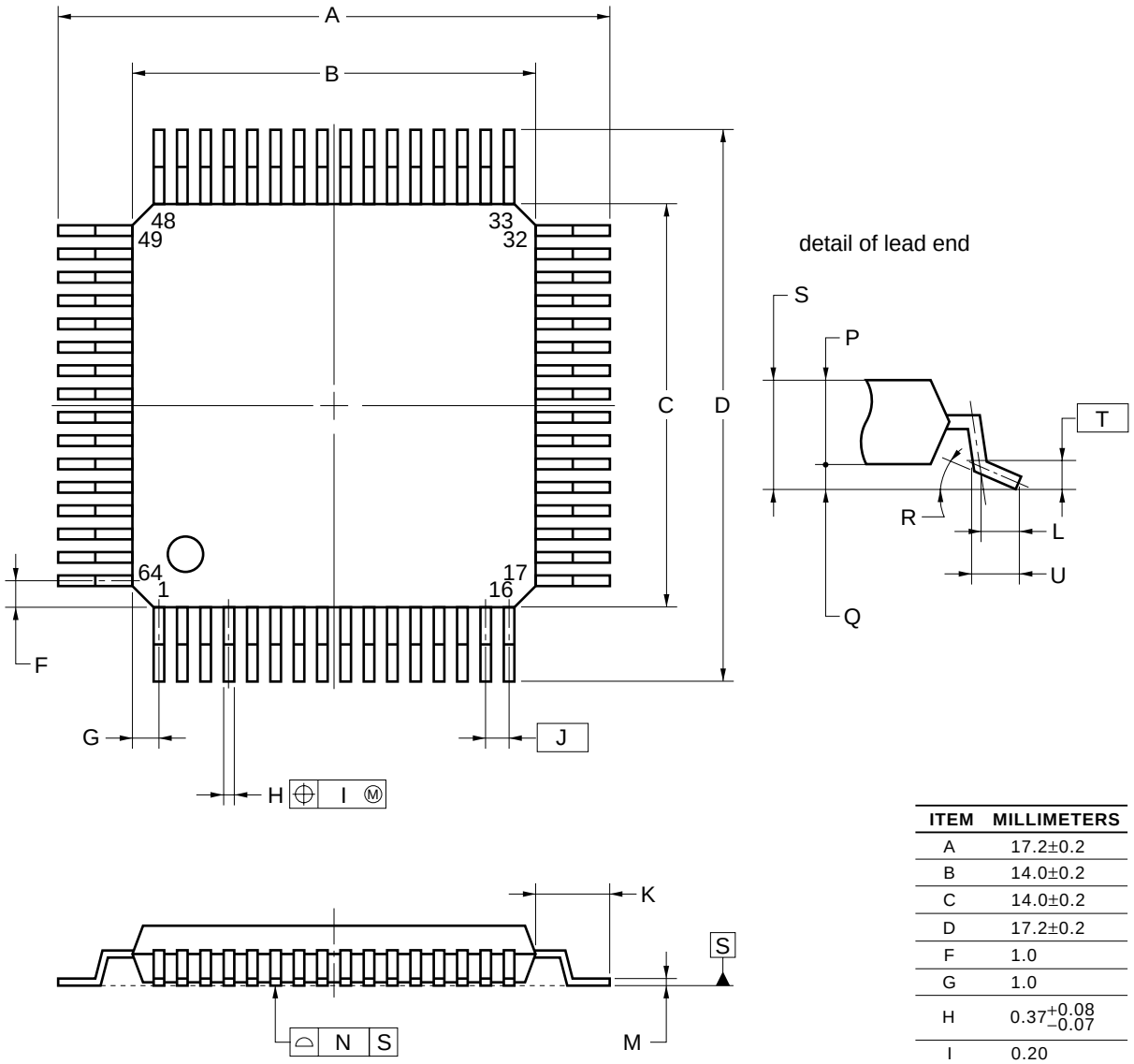
Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	12.0±0.2
B	10.0±0.2
C	10.0±0.2
D	12.0±0.2
F	1.25
G	1.25
H	0.22±0.05
I	0.08
J	0.5 (T.P.)
K	1.0±0.2
L	0.5
M	$0.17^{+0.03}_{-0.07}$
N	0.08
P	1.4
Q	0.1±0.05
R	$3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$
S	1.5±0.10
T	0.25
U	0.6±0.15

S64GB-50-8EU-2

Remark The package and material of ES products are the same as mass produced products.

64-PIN PLASTIC LQFP (14x14)



ITEM	MILLIMETERS
A	17.2±0.2
B	14.0±0.2
C	14.0±0.2
D	17.2±0.2
F	1.0
G	1.0
H	$0.37^{+0.08}_{-0.07}$
I	0.20
J	0.8 (T.P.)
K	1.6±0.2
L	0.8
M	$0.17^{+0.03}_{-0.06}$
N	0.10
P	1.4±0.1
Q	0.127±0.075
R	$3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$
S	1.7 MAX.
T	0.25
U	0.886±0.15

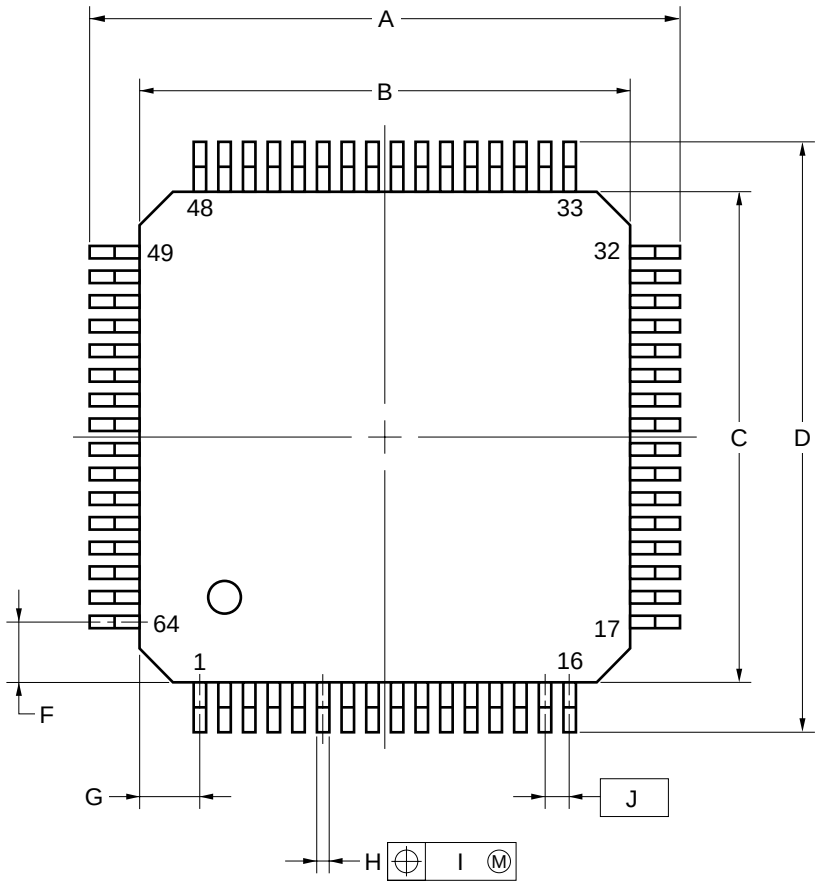
P64GC-80-8BS

NOTE

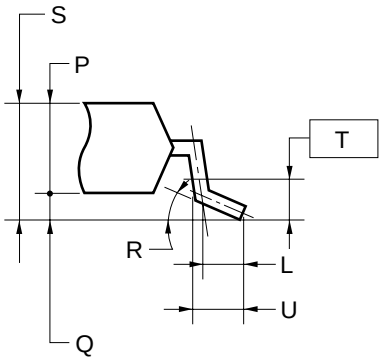
Each lead centerline is located within 0.20 mm of its true position (T.P.) at maximum material condition.

Remark The package and material of ES products are the same as mass produced products.

64-PIN PLASTIC TQFP (12x12)



detail of lead end



NOTE

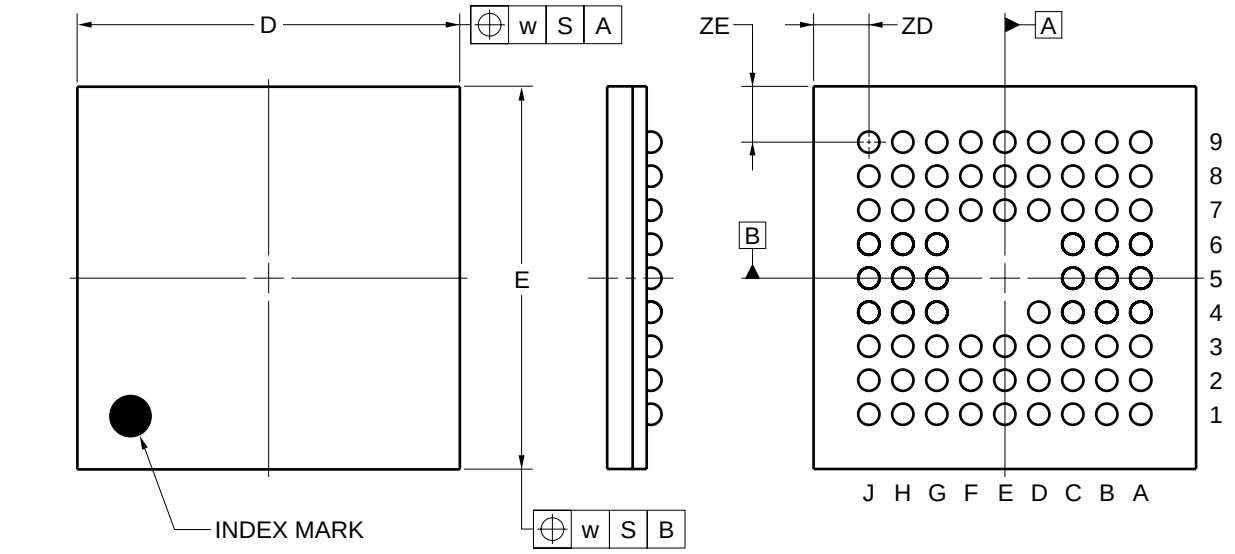
Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

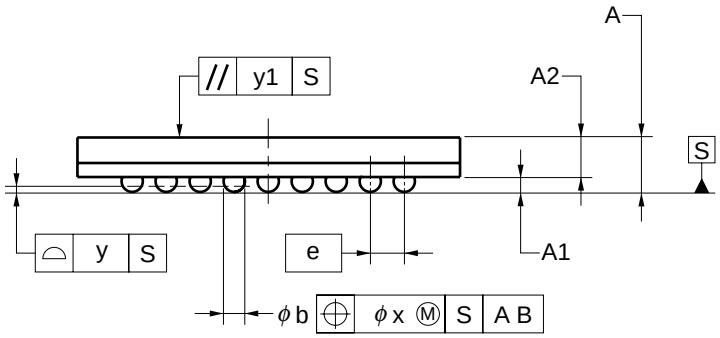
ITEM	MILLIMETERS
A	14.0±0.2
B	12.0±0.2
C	12.0±0.2
D	14.0±0.2
F	1.125
G	1.125
H	$0.32^{+0.06}_{-0.10}$
I	0.13
J	0.65 (T.P.)
K	1.0±0.2
L	0.5
M	$0.17^{+0.03}_{-0.07}$
N	0.10
P	1.0
Q	0.1±0.05
R	$3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$
S	1.1±0.1
T	0.25
U	0.6±0.15

P64GK-65-9ET-3

Remark The package and material of ES products are the same as mass produced products.

73-PIN PLASTIC FBGA (9x9)





(UNIT:mm)

ITEM	DIMENSIONS
D	9.00±0.10
E	9.00±0.10
w	0.20
A	1.28±0.10
A1	0.35±0.06
A2	0.93
e	0.80
b	$0.50^{+0.05}_{-0.10}$
x	0.08
y	0.10
y1	0.20
ZD	1.30
ZE	1.30

P73F1-80-CN3

Remark The external dimensions and materials of the ES version are the same as those of the mass-produced version.

11. RECOMMENDED SOLDERING CONDITIONS

The μPD78F0034B, 78F0034BY, 78F0034B(A), and 78F0034BY(A) should be soldered and mounted under the following recommended conditions.

For details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact an NEC Electronics sales representative.

Table 11-1. Surface Mounting Type Soldering Conditions (1/2)

(1) μPD78F0034BGB-8EU: 64-pin plastic LQFP (10 x 10)
μPD78F0034BGB(A)-8EU: 64-pin plastic LQFP (10 x 10)
μPD78F0034BYGB-8EU: 64-pin plastic LQFP (10 x 10)
μPD78F0034BYGB(A)-8EU: 64-pin plastic LQFP (10 x 10)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Two times or less, Exposure limit: 7 days[Note] (after 7 days, prebake at 125°C for 10 hours)	IR35-107-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Two times or less, Exposure limit: 7 days[Note] (after 7 days, prebake at 125°C for 10 hours)	VP15-107-2
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

(2) μPD78F0034BGC-8BS: 64-pin plastic LQFP (14 x 14)
μPD78F0034BGC(A)-8BS: 64-pin plastic LQFP (14 x 14)
μPD78F0034BYGC-8BS: 64-pin plastic LQFP (14 x 14)
μPD78F0034BYGC(A)-8BS: 64-pin plastic LQFP (14 x 14)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Two times or less	IR35-00-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Two times or less	VP15-00-2
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: Once, Preheating temperature: 120°C max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	–

Caution Do not use different soldering methods together (except for partial heating).

Table 11-1. Surface Mounting Type Soldering Conditions (2/2)

(3) μPD78F0034BGK-9ET: 64-pin plastic TQFP (12 x 12)
μPD78F0034BGK(A)-9ET: 64-pin plastic TQFP (12 x 12)
μPD78F0034BYGK-9ET: 64-pin plastic TQFP (12 x 12)
μPD78F0034BYGK(A)-9ET: 64-pin plastic TQFP (12 x 12)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Two times or less, Exposure limit: 7 days[Note] (after 7 days, prebake at 125°C for 10 hours)	IR35-107-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Two times or less, Exposure limit: 7 days[Note] (after 7 days, prebake at 125°C for 10 hours)	VP15-107-2
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: Once, Preheating temperature: 120°C max. (package surface temperature), Exposure limit: 7 days[Note] (after 7 days, prebake at 125°C for 10 hours)	WS60-107-1
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

(4) μPD78F0034BF1-CN3: 73-pin plastic FBGA (9 x 9)
μPD78F0034BYF1-CN3: 73-pin plastic FBGA (9 x 9)

Soldering Method	Soldering Conditions	Recommended ConditionSymbol
Infrared reflow	Package peak temperature: 260°C, Time: 60 seconds max. (at 220°C or higher), Count: Three times or less, Exposure limit: 3 days[Note] (after that, prebake at 125°C for 20 hours)	IR60-203-3
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Three times or less, Exposure limit: 3 days[Note] (after that, prebake at 125°C for 20 hours)	VP15-203-3

Note After opening the dry pack, store it at 25°C or less and 65%RH or less for the allowable storage period.

Caution Do not use different soldering methods together.

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD780034B, 780034BY. Also refer to **(6) Cautions on Using Development Tools.**

(1) Software Package

SP78K0	CD-ROM in which various software tools for 78K/0 development are integrated in one package

(2) Language Processing Software

RA78K0	Assembler package common to 78K/0 Series
CC78K0	C compiler package common to 78K/0 Series
DF780034	Device file for μPD780034A, 780034AY Subseries
CC78K0-L	C compiler library source file common to 78K/0 Series

(3) Flash Memory Writing Tools

Flashpro III (FL-PR3, PG-FP3) Flashpro IV (FL-PR4, PG-FP4)	Flash programmer dedicated to microcontrollers with on-chip flash memory
FA-64GB-8EU FA-64GC-8BS-A FA-64GK-9ET FA-73F1-CN3-A	Adapter for flash memory writing used connected to the Flashpro III/Flashpro IV. • FA-64GB-8EU: 64-pin plastic LQFP (GB-8EU type) • FA-64GC-8BS-A: 64-pin plastic LQFP (GC-8BS type) • FA-64GK-9ET: 64-pin plastic TQFP (GK-9ET type) • FA-73F1-CN3-A: 73-pin plastic FBGA (F1-CN3 type)

(4) Debugging Tools

- **When using in-circuit emulator IE-78K0-NS**

IE-78K0-NS	In-circuit emulator common to 78K/0 Series
IE-70000-MC-PS-B	Power supply unit for IE-78K0-NS
IE-78K0-NS-PA	Performance board to enhance and expand the functions of IE-78K0-NS
IE-70000-98-IF-C	Adapter required when using PC-9800 series as host machine (excluding notebook PCs) (C bus supported)
IE-70000-CD-IF-A	PC card and interface cable when using notebook PC as host machine (PCMCIA socket supported)
IE-70000-PC-IF-C	Adapter required when using IBM PC/AT™ or compatible as host machine (ISA bus supported)
IE-70000-PCI-IF-A	Adapter required when using PC in which PCI bus is incorporated as host machine
IE-780034-NS-EM1	Emulation board to emulate μPD780034A, 780034AY Subseries
NP-64GC NP-64GC-TQ NP-H64GC-TQ	Emulation probe for 64-pin plastic LQFP (GC-8BS type)
NP-64GK NP-H64GK-TQ	Emulation probe for 64-pin plastic TQFP (GK-9ET type)
NP-H64GB-TQ	Emulation probe for 64-pin plastic LQFP (GB-8EU type)
NP-73F1-CN3**Note**	Emulation probe for 73-pin plastic FBGA (F1-CN3 type)
EV-9200GC-64	Conversion socket to connect the NP64GC and a target system board on which a 64-pin plastic LQFP (GC-8BS type) can be mounted.
TGC-064SAP	Conversion adapter to connect the NP-64GC-TQ or NP-H64GC-TQ and a target system board on which a 64-pin plastic LQFP (GC-8BS type) can be mounted
TGK-064SBW	Conversion adapter to connect the NP-64GK or NP-H64GK-TQ and a target system on which a 64-pin plastic TQFP (GK-9ET type) can be mounted
TGB-064SDP	Conversion socket to connect the NP-H64GB-TQ and a target system board on which a 64-pin plastic LQFP (GB-8EU type) can be mounted
CSICE73A0909N01, LSPACK73A0909N01, CSSOCKET73A0909N01	Conversion socket to connect the NP-73F1-CN3 and a target system board on which a 73-pin plastic FBGA (F1-CN3 type) can be mounted
ID78K0-NS	Integrated debugger for IE-78K0-NS
SM78K0	System simulator common to 78K/0 Series
DF780034	Device file for μPD780034A, 780034AY Subseries

Note The conversion socket (CSICE73A0909N01, LSPACK73A0909N01, or CSSOCKET73A0909N01) is supplied with the emulation probe (NP-73F1-CN3).

• When using in-circuit emulator IE-78001-R-A

IE-78001-R-A	In-circuit emulator common to 78K/0 Series
IE-70000-98-IF-C	Adapter required when using PC-9800 series as host machine (excluding notebook PCs) (C bus supported)
IE-70000-PC-IF-C	Interface adapter when using IBM PC/AT or compatible as host machine (ISA bus supported)
IE-70000-PCI-IF-A	Adapter required when using PC in which PCI bus is incorporated as host machine
IE-780034-NS-EM1	Emulation board to emulate μPD780034A, 780034AY Subseries
IE-78K0-R-EX1	Emulation probe conversion board necessary when using IE-780034-NS-EM1 on IE-78001-R-A
EP-78240GC-R	Emulation probe for 64-pin plastic LQFP (GC-8BS type)
EP-78012GK-R	Emulation probe for 64-pin plastic TQFP (GK-9ET type)
EV-9200GC-64	Conversion socket to connect the EP-78240GC-R and a target system board on which a 64-pin plastic LQFP (GC-8BS type) can be mounted
TGK-064SBW	Conversion adapter to connect the EP-78012GK-R and a target system board on which a 64-pin plastic TQFP (GK-9ET type) can be mounted
ID78K0	Integrated debugger for IE-78001-R-A
SM78K0	System simulator common to 78K/0 Series
DF780034	Device file for μPD780034A, 780034AY Subseries

(5) Real-Time OS

RX78K0	Real-time OS for 78K/0 Series

Caution The 64-pin plastic LQFP (GB-8EU type) and 73-pin plastic FBGA (F1-CN3 type) do not support the IE-78001-R-A.

(6) Cautions on Using Development Tools

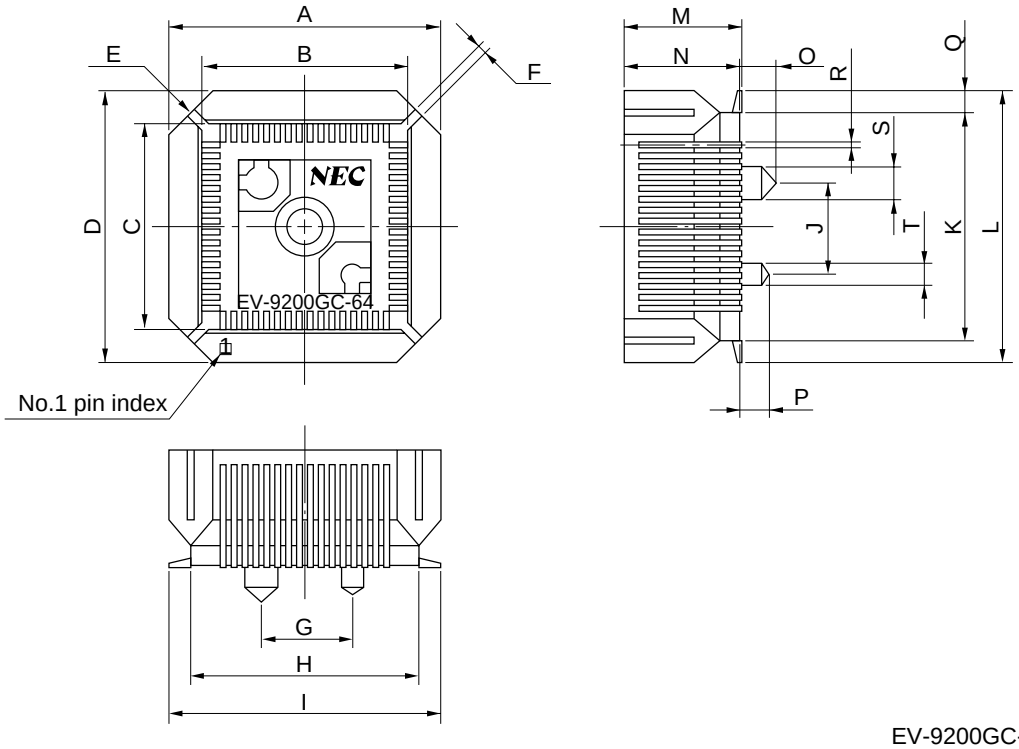
- The ID78K0-NS, ID78K0, and SM78K0 are used in combination with the DF780034.
- The CC78K0 and RX78K0 are used in combination with the RA78K0 and the DF780034.
- FL-PR3, FL-PR4, FA-64GC-8BS-A, FA-64GB-8EU, FA-64GK-9ET, FA-73F1-CN3-A, NP-64GC, NP-64GC-TQ, NP-H64GC-TQ, NP-64GK, NP-H64GK-TQ, NP-H64GB-TQ, and NP-73F1-CN3 are products made by Naito Densei Machida Mfg. Co., Ltd. (+81-45-475-4191).
- TGC-064SAP, TGK-064SBW, TGB-064SDP, CSICE73A0909N01, LSPACK73A0909N01, and CSSOCKET73A0909N01 are products made by TOKYO ELETECH CORPORATION.
  Contact: Daimaru Kogyo, Ltd.
  Tokyo Electronic Division (+81-3-3820-7112)
  Osaka Electronic Division (+81-6-6244-6672)
- For third-party development tools, see the **Single-chip Microcontroller Development Tool Selection Guide (U11069E)**.
- The host machines and OSs supporting each software are as follows.

Host Machine / [OS] / Software	PC PC-9800 series [Japanese Windows™] IBM PC/AT and compatibles [Japanese/English Windows]	EWS HP9000 series 700™ [HP-UX™] SPARCstation™ [SunOS™, Solaris™]
RA78K0	√ **Note**	√
CC78K0	√ **Note**	√
ID78K0-NS	√	–
ID78K0	√	–
SM78K0	√	–
RX78K0	√ **Note**	√

Note DOS-based software

Conversion Socket Drawing (EV-9200GC-64) and Footprints

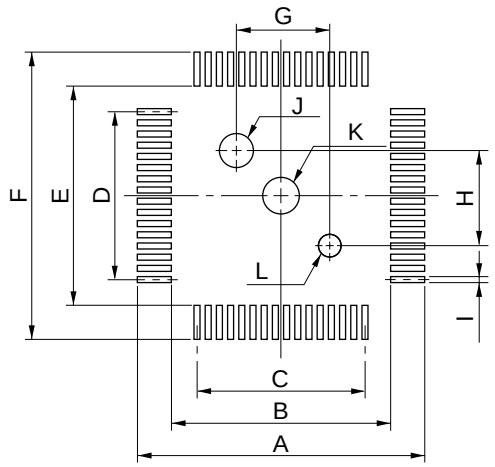
Figure A-1. EV-9200GC-64 Drawing (For Reference Only)



EV-9200GC-64-G0

ITEM	MILLIMETERS	INCHES
A	18.8	0.74
B	14.1	0.555
C	14.1	0.555
D	18.8	0.74
E	4-C 3.0	4-C 0.118
F	0.8	0.031
G	6.0	0.236
H	15.8	0.622
I	18.5	0.728
J	6.0	0.236
K	15.8	0.622
L	18.5	0.728
M	8.0	0.315
N	7.8	0.307
O	2.5	0.098
P	2.0	0.079
Q	1.35	0.053
R	0.35 ± 0.1	$0.014^{+0.004}_{-0.005}$
S	ϕ2.3	ϕ0.091
T	ϕ1.5	ϕ0.059

Figure A-2. EV-9200GC-64 Footprints (For Reference Only)



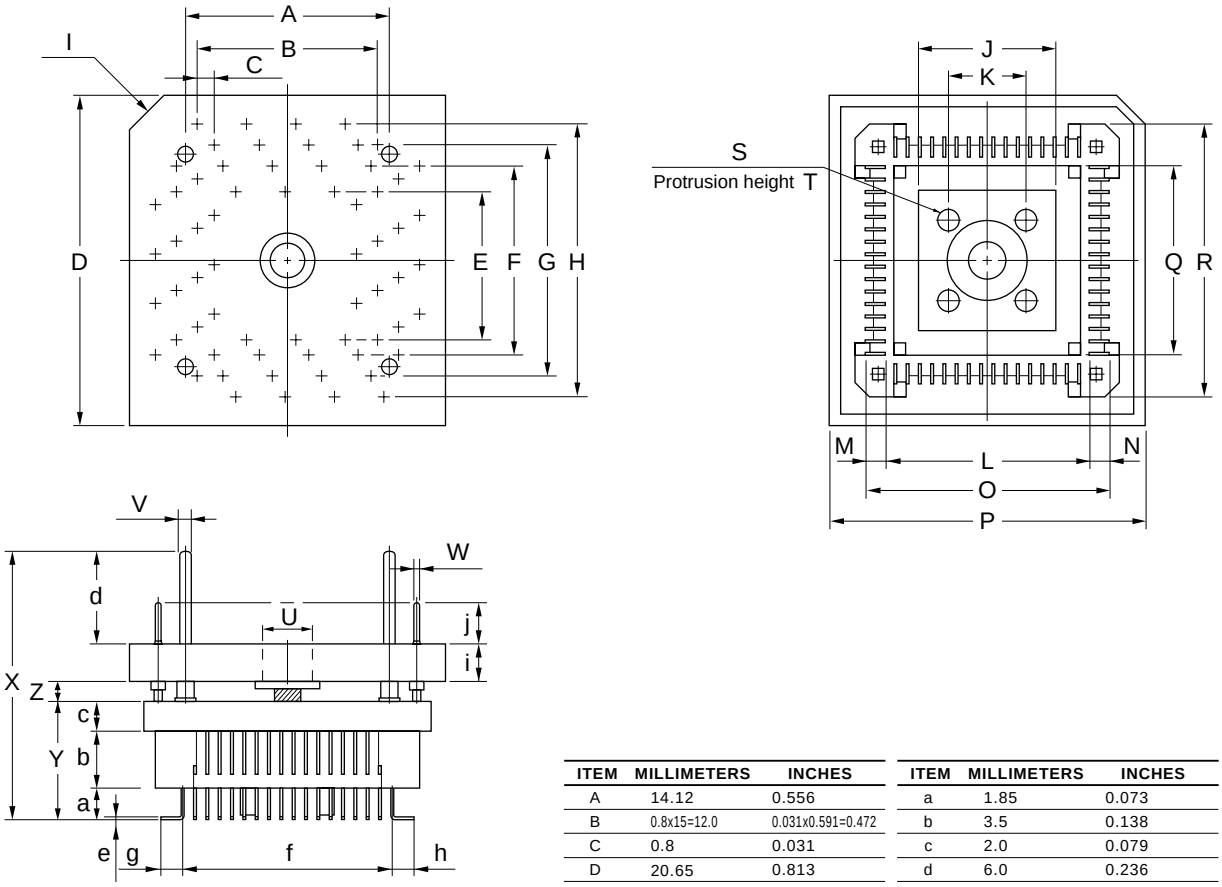
EV-9200GC-64-P1E

ITEM	MILLIMETERS	INCHES
A	19.5	0.768
B	14.8	0.583
C	$0.8\pm0.02\times15=12.0\pm0.05$	$0.031^{+0.002}_{-0.001}\times0.591=0.472^{+0.003}_{-0.002}$
D	$0.8\pm0.02\times15=12.0\pm0.05$	$0.031^{+0.002}_{-0.001}\times0.591=0.472^{+0.003}_{-0.002}$
E	14.8	0.583
F	19.5	0.768
G	6.00 ± 0.08	$0.236^{+0.004}_{-0.003}$
H	6.00 ± 0.08	$0.236^{+0.004}_{-0.003}$
I	0.5 ± 0.02	$0.197^{+0.001}_{-0.002}$
J	$\phi2.36\pm0.03$	$\phi0.093^{+0.001}_{-0.002}$
K	$\phi2.2\pm0.1$	$\phi0.087^{+0.004}_{-0.005}$
L	$\phi1.57\pm0.03$	$\phi0.062^{+0.001}_{-0.002}$

Caution Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E).

Conversion Adapter Drawing (TGC-064SAP)

Figure A-3. TGC-064SAP Drawing (For Reference Only)



ITEM	MILLIMETERS	INCHES
A	14.12	0.556
B	0.8x15=12.0	0.031x0.591=0.472
C	0.8	0.031
D	20.65	0.813
E	10.0	0.394
F	12.4	0.488
G	14.8	0.583
H	17.2	0.677
I	C 2.0	C 0.079
J	9.05	0.356
K	5.0	0.197
L	13.35	0.526
M	1.325	0.052
N	1.325	0.052
O	16.0	0.630
P	20.65	0.813
Q	12.5	0.492
R	17.5	0.689
S	4-ϕ1.3	4-ϕ0.051
T	1.8	0.071
U	ϕ3.55	ϕ0.140
V	ϕ0.9	ϕ0.035
W	ϕ0.3	ϕ0.012
X	(19.65)	(0.667)
Y	7.35	0.289
Z	1.2	0.047

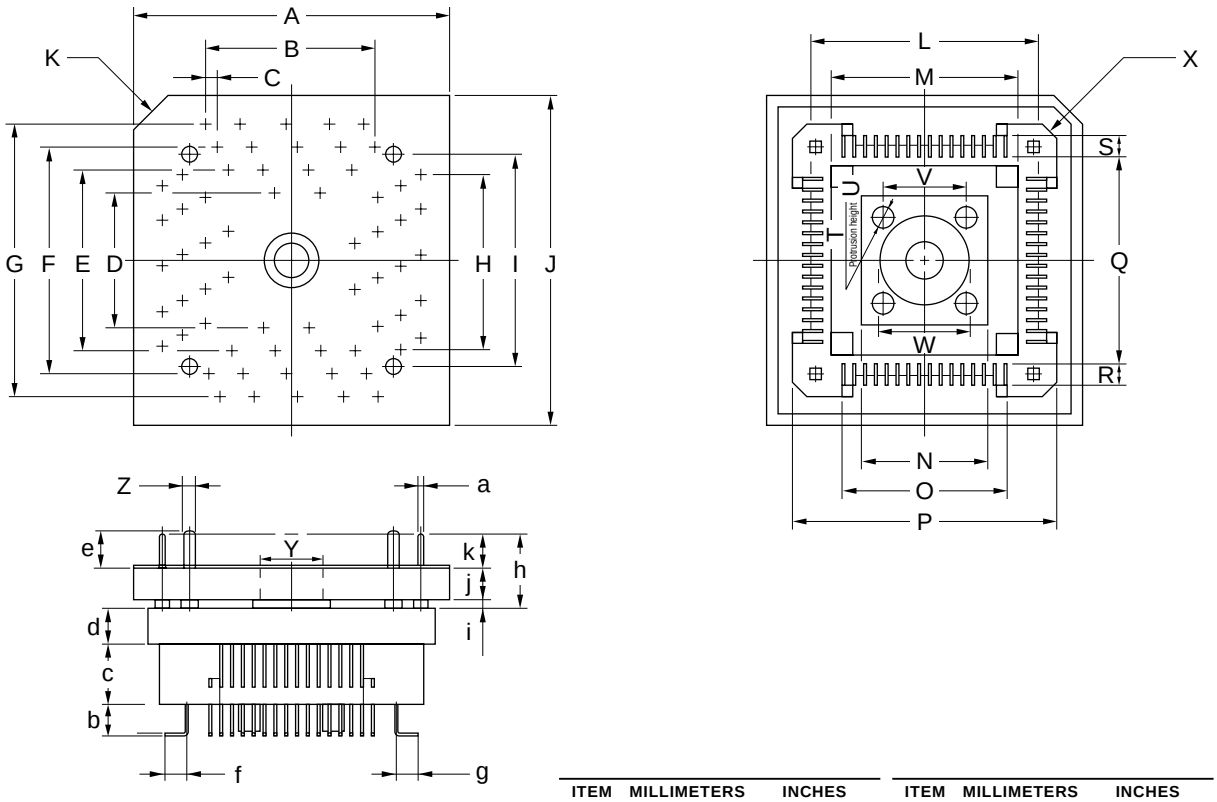
ITEM	MILLIMETERS	INCHES
a	1.85	0.073
b	3.5	0.138
c	2.0	0.079
d	6.0	0.236
e	0.25	0.010
f	13.6	0.535
g	1.2	0.047
h	1.2	0.047
i	2.4	0.094
j	2.7	0.106

TGC-064SAP-G0E

note: Product by TOKYO ELETECH CORPORATION.

Conversion Adapter Drawing (TGK-064SBW)

Figure A-4. TGK-064SBW Drawing (For Reference Only) (Unit: mm)



ITEM	MILLIMETERS	INCHES
A	18.4	0.724
B	0.65x15=9.75	0.026x0.591=0.384
C	0.65	0.026
D	7.75	0.305
E	10.15	0.400
F	12.55	0.494
G	14.95	0.589
H	0.65x15=9.75	0.026x0.591=0.384
I	11.85	0.467
J	18.4	0.724
K	C 2.0	C 0.079
L	12.45	0.490
M	10.25	0.404
N	7.7	0.303
O	10.02	0.394
P	14.92	0.587
Q	11.1	0.437
R	1.45	0.057
S	1.45	0.057
T	4-ϕ1.3	4-ϕ0.051
U	1.8	0.071
V	5.0	0.197
W	ϕ5.3	ϕ0.209
X	4-C 1.0	4-C 0.039
Y	ϕ3.55	ϕ0.140
Z	ϕ0.9	ϕ0.035

ITEM	MILLIMETERS	INCHES
a	ϕ0.3	ϕ0.012
b	1.85	0.073
c	3.5	0.138
d	2.0	0.079
e	3.9	0.154
f	1.325	0.052
g	1.325	0.052
h	5.9	0.232
i	0.8	0.031
j	2.4	0.094
k	2.7	0.106

TGK-064SBW-G1E

note: Product by TOKYO ELETECH CORPORATION.

APPENDIX B. RELATED DOCUMENTS

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents Related to Devices

Document Name	Document No.
μPD780024A, 780034A, 780024AY, 780034AY Subseries User's Manual	U14046E
μPD780021A, 780022A, 780023A, 780024A, 780021AY, 780022AY, 780023AY, 780024AY Data Sheet	U14042E
μPD780021A(A), 780022A(A), 780023A(A), 780024A(A), 780021AY(A), 780022AY(A), 780023AY(A), 780024AY(A) Data Sheet	U15131E
μPD780031A, 780032A, 780033A, 780034A, 780031AY, 780032AY, 780033AY, 780034AY Data Sheet	U14044E
μPD780031A(A), 780032A(A), 780033A(A), 780034A(A), 780031AY(A), 780032AY(A), 780033AY(A), 780034AY(A) Data Sheet	U15132E
μPD78F0034A, 78F0034AY Data Sheet	U14040E
μPD78F0034B, 78F0034BY, 78F0034B(A), 78F0034BY(A) Data Sheet	This document
78K/0 Series User's Manual Instruction	U12326E

Documents Related to Development Software Tools (User's Manuals)

Document Name		Document No.
RA78K0 Assembler Package	Operation	U14445E
	Language	U14446E
	Structured Assembly Language	U11789E
CC78K0 C Compiler	Operation	U14297E
	Language	U14298E
SM78K Series System Simulator Ver. 2.30 or Later	Operation (Windows Based)	U15373E
	External Part User Open Interface Specifications	U15802E
ID78K Series Integrated Debugger Ver. 2.30 or Later	Operation (Windows Based)	U15185E
RX78K0 Real-time OS	Fundamentals	U11537E
	Installation	U11536E
Project Manager Ver. 3.12 or Later (Windows Based)		U14610E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

Documents Related to Development Hardware Tools (User's Manuals)

Document Name	Document No.
IE-78K0-NS In-Circuit Emulator	U13731E
IE-78K0-NS-A In-Circuit Emulator	U14889E
IE-780034-NS-EM1 Emulation Board	U14642E
IE-78001-R-A In-Circuit Emulator	U14142E
IE-78K0-R-EX1 In-Circuit Emulator	To be prepared

Documents Related to Flash Memory Writing

Document Name	Document No.
PG-FP3 Flash Memory Programmer User's Manual	U13502E
PG-FP4 Flash Memory Programmer User's Manual	U15260E

Other Related Documents

Document Name	Document No.
SEMICONDUCTORS SELECTION GUIDE - Products & Packages -	X13769E
Semiconductor Device Mounting Technology Manual	C10535E
Quality Grades on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Device availability
- Ordering information
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- Availability of related technical literature
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- Network requirements

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NEC Electronics America, Inc. (U.S.)
Santa Clara, California
Tel: 408-588-6000
800-366-9782
Fax: 408-588-6130
800-729-9288

NEC Electronics (Europe) GmbH
Duesseldorf, Germany
Tel: 0211-65 03 01
Fax: 0211-65 03 327

- **Sucursal en España**
  Madrid, Spain
  Tel: 091-504 27 87
  Fax: 091-504 28 60

- **Succursale Française**
  Vélizy-Villacoublay, France
  Tel: 01-30-67 58 00
  Fax: 01-30-67 58 99

- **Filiale Italiana**
  Milano, Italy
  Tel: 02-66 75 41
  Fax: 02-66 75 42 99

- **Branch The Netherlands**
  Eindhoven, The Netherlands
  Tel: 040-244 58 45
  Fax: 040-244 45 80

- **Tyskland Filial**
  Taeby, Sweden
  Tel: 08-63 80 820
  Fax: 08-63 80 388

- **United Kingdom Branch**
  Milton Keynes, UK
  Tel: 01908-691-133
  Fax: 01908-670-290

NEC Electronics Hong Kong Ltd.
Hong Kong
Tel: 2886-9318
Fax: 2886-9022/9044

NEC Electronics Hong Kong Ltd.
Seoul Branch
Seoul, Korea
Tel: 02-528-0303
Fax: 02-528-4411

NEC Electronics Shanghai, Ltd.
Shanghai, P.R. China
Tel: 021-6841-1138
Fax: 021-6841-1137

NEC Electronics Taiwan Ltd.
Taipei, Taiwan
Tel: 02-2719-2377
Fax: 02-2719-5951

NEC Electronics Singapore Pte. Ltd.
Novena Square, Singapore
Tel: 6253-8311
Fax: 6250-3583

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