TCC110

Caller-ID on Call Waiting (CIDCW) Receiver

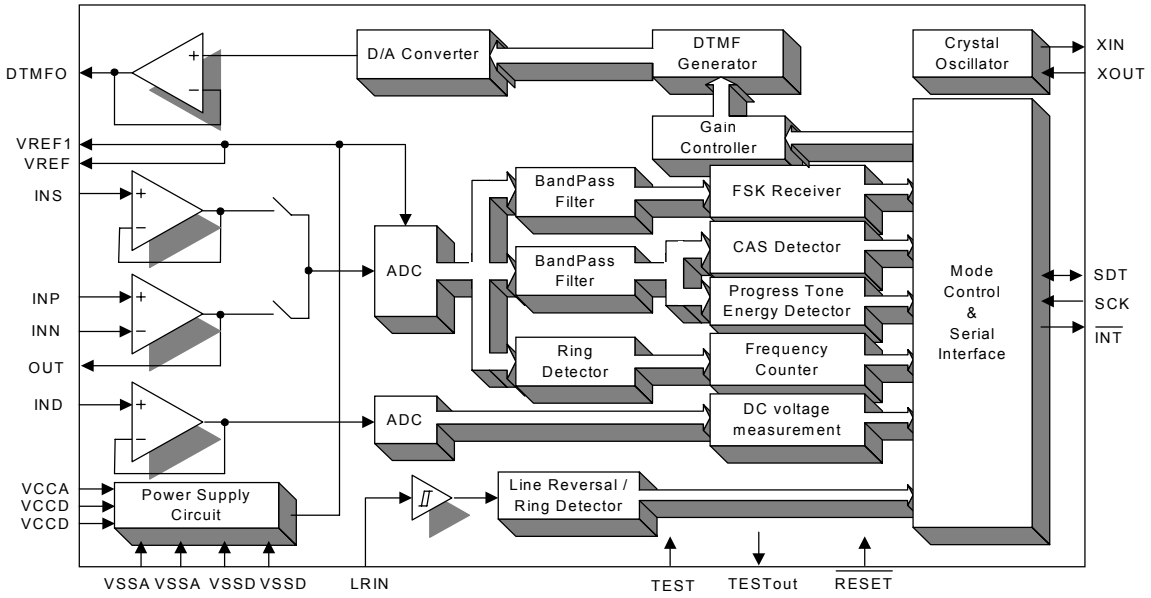
June 2001 Specifications

FEATURES

- 1200 baud FSK (Frequency Shift Keying) demodulator with sensitivity –38dBm (in 600Ω) conforms to Bell 202 and CCITT V.23 standards
- Receive sensitivity of –32dBm (in 600Ω) for CAS (CPE Alerting Signal)
- Progress Tone Energy (PTE) detector with sensitivity of –27dBm
- Ring or Line Reversal detector
- Ring Frequency measurement
- Line voltage measurement
- DTMF generator with gain controller for all 16 characters
- On-hook and off-hook applications according to Bellcore TR-NWT-000030 and SR-TSV-002476 specifications
- Compatible with ETSI standards ETS 300 659-1 and ETS 300 659-2
- 3V ~ 5V operation
- On-chip 3.579545MHz crystal oscillator
- Power-down mode
- 24-pin SOP package
- 0.5um CMOS triple metal process

APPLICATIONS

- Bellcore CID and CIDCW systems
- CID and CIDCW feature phones and adjunct boxes
- Computer Telephony Integrated systems
- Voice-Mail Equipment



GENERAL DESCRIPTION

The TCC110 is a low power CMOS device used for receiving physical layer signals like Bellcore's CPE Alerting Signal (CAS) and similar evolving systems. This device also meets the requirements of emerging Calller ID on Call Waiting (CIDCW) services. In addition, two different signal inputs are available to support Tip/Ring and Hybrid connectivity. The device also includes a 1200 baud Bell 202/V.23 compatible FSK data demodulator, a ring or line reversal detector, a Progress Tone Energy detector, a DTMF generator and a DC line voltage level measurement unit. The status of the TCC110, the received FSK data, the ring frequency and other received information can be read and control options can be written via the serial interface. An on-chip 3.579545MHz oscillator is available. In power-down mode only the ring or line reversal detector can be active. The operating voltage is 3V ~ 5V and the device is available in a 24-pin SOP package.

1. PIN DESCRIPTIONS

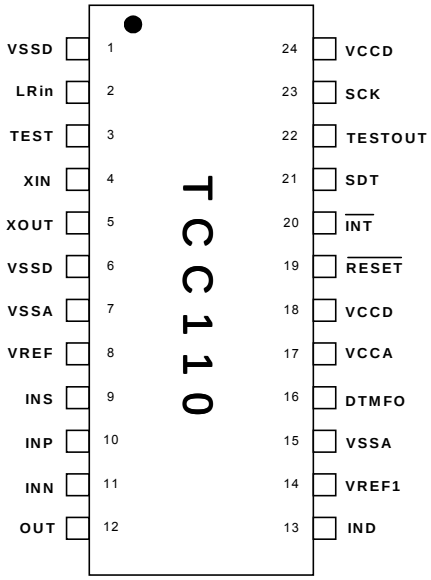


Table 1: Pin descriptions

Number	Pin name	Function	Pin description
1	VSSD	Supply	Negative supply voltage (ground)
2	Lrin	Schmitt Input	Input for line reversal or ring detection
3	TEST	Input	Test pin, must be connected to ground
4	XIN	Input	3.579545 MHz crystal input
5	XOUT	Output	3.579545 MHz crystal output
6	VSSD	Supply	Negative supply voltage (ground)
7	VSSA	Supply	Negative supply voltage for analog operations (ground)
8	VREF	Analog output	Reference voltage for input signals
9	INS	Analog input	Input op-amp single ended input signal for CAS, FSK and PTE
10	INP	Analog input	Input op-amp positive input signal for CAS, FSK and PTE
11	INN	Analog input	Input op-amp negative input signal for CAS, FSK and PTE
12	OUT	Analog output	Input op-amp output signal for CAS, FSK and PTE
13	IND	Analog input	Input op-amp single ended input signal for DC Voltage level measurement
14	VREF1	Analog output	Reference voltage for input signals
15	VSSA	Supply	Negative supply voltage for analog operations (ground)
16	DTMFO	Analog output	DTMF signal output
17	VCCA	Supply	Positive supply voltage for analog operations
18	VCCD	Supply	Positive supply voltage
19	$\overline{\text{RESET}}$	Input	Resets the TCC110 to known state
20	$\overline{\text{INT}}$	Open drain output	Interrupt output (active low)
21	SDT	Open drain input/output	Bi-directional open drain pin for serial interface data input and output
22	TESTOUT	Output	Test pin, must be floating
23	SCK	Input	Serial interface clock
24	VCCD	Supply	Positive supply voltage

2. BLOCK DIAGRAM

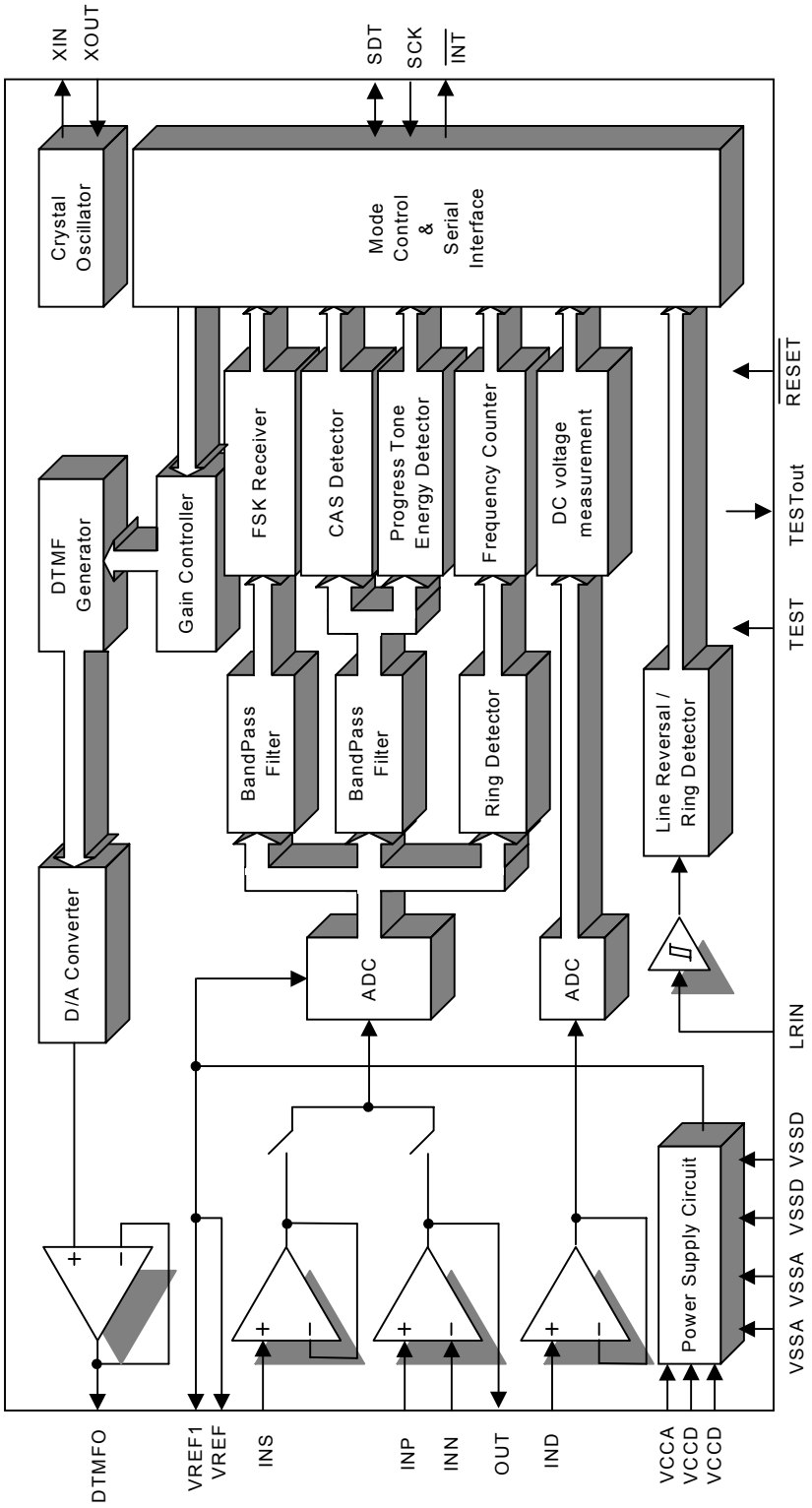


Figure 1. Block diagram

3. APPLICATION DIAGRAM

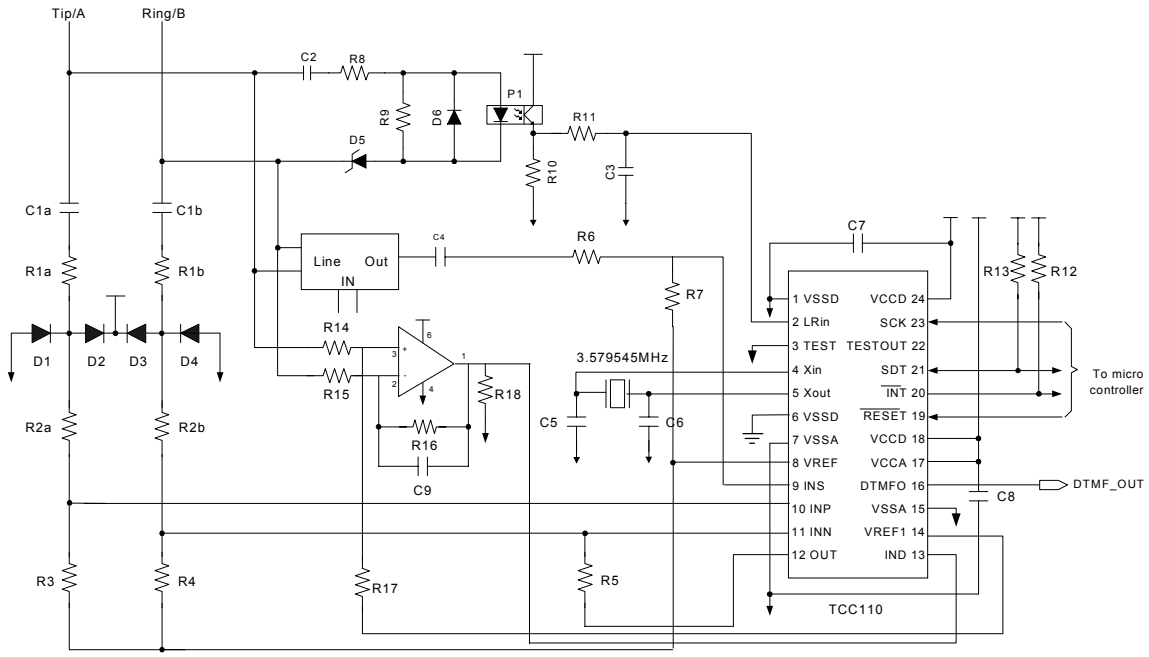


Figure 2. Recommended external components for typical application

Table 2. Recommended external component values for typical application

Differential input stage		**Single ended input stage**	
C1a, C1b	2.2nF (1KV)	C4	100nF
R1a, R1b	390KΩ(0.5W)	R6	100KΩ
R2a, R2b	47KΩ	R7	100KΩ
R3	68KΩ	**DC input stage**	
R4	220KΩ	R14,R15	10MΩ
R5	100KΩ	R16	270KΩ
D1, D2, D3, D4	IN4007	R17	330KΩ
Ring or Line Reversal Detector		R18	1KΩ
C2	0.22uF (250V)	C9	1nF
C3	10nF	O1	LM358
R8	36KΩ	**Other components**	
R9	3.9KΩ	C5,C6	20pF
R10,R11	20KΩ	R12,R13	10KΩ
D5	24V	C7,C8	10nF
D6	1N4148	X1	3.579545MHz ± 0.1%
P1	PC817/LTV817		

Notes on recommended external components :

- Values for R6 and R7 are based on a hybrid that has a loss free path from LINE to OUT
- The components are specified for a typical application. For conformance to standards in certain applications, other component values and/or ratings may be necessary.

4. FUNCTION DESCRIPTION

4.1 Analog input and preprocessor

The preprocessor for the FSK receiver and the CAS, the PTE detectors, comprises two input signal buffers, an Analog-to-Digital Converter (=ADC1) and digital bandpass filters. Bandpass filters are used to attenuate out band noise and interfering signals, which might otherwise reach the FSK receiver and CAS, PTE detectors. The CAS and PTE detectors share a single digital filter while the FSK receiver has its own separate filter.

To measure the DC voltage of the telephone line, a DC input buffer and another Analog-to-Digital Converter (=ADC2) are used. The TCC110 can be forced into a power-down state by switching off the 3.579545 MHz system clock and all ADC's and op-amps.

4.1.1 Differential input buffer

The differential input buffer is used to convert the balanced telephone line signal to the input signal of ADC1 in the TCC110.

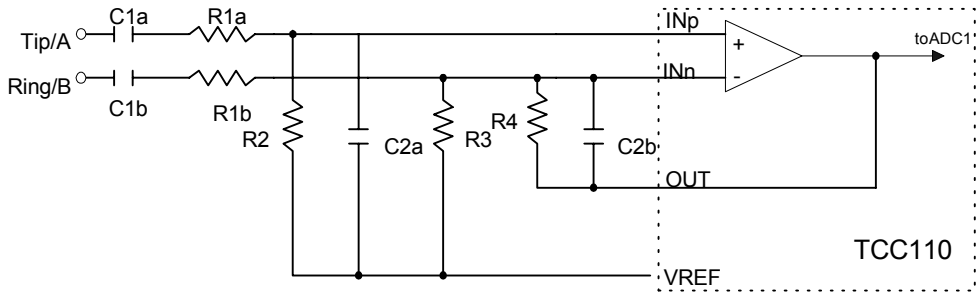


Figure 3. Differential input buffer of the TCC110

Design equations for this buffer are;

The differential voltage gain = R4/R1b.

R1a = R1b

C1a = C1b

R2 = R3 * R4 / (R3 + R4)

The target differential voltage gain should be adjusted to obtain the expected signal level at the 'OUT' pin.

4.1.2 Single ended input buffer

The single ended input buffer may also be used with the telephone line signal connected to the hybrid as shown in Figure 4.

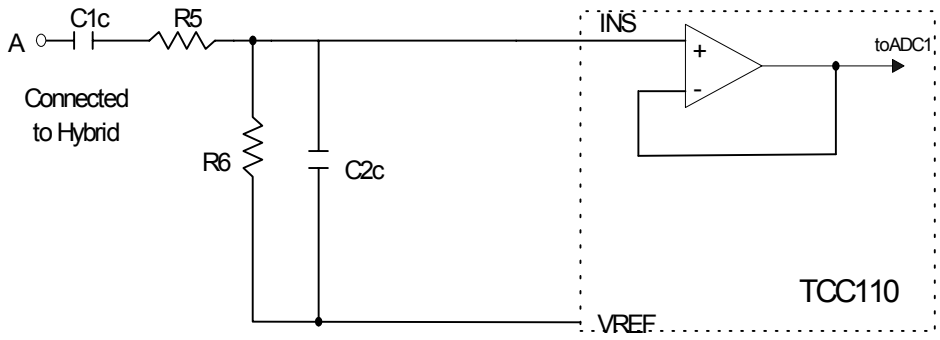


Figure 4. Single ended buffer of the TCC110

The voltage gain is R6 / (R5 + R6)
The target voltage gain should be adjusted to obtain the expected signal level at the INS input.

The BFS (Buffer selection) bit in the Function register chooses between the output of the single-ended input buffer and the output of the differential input buffer, sending the selected output to the ADC1. The differential input buffer is selected when BFS is '0' and the single ended input buffer is selected when BFS is '1'. The default value of BFS is '0'

4.1.3 DC input buffer

The DC input buffer can be used to convert the telephone line voltage level to the ADC2 input voltage level.

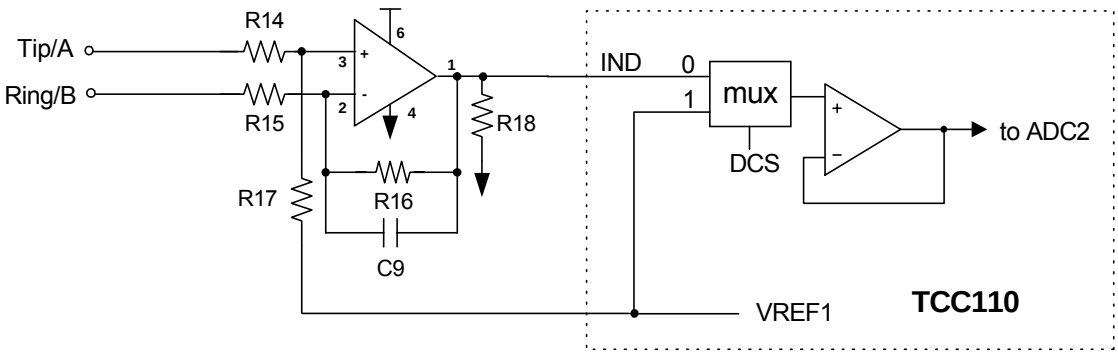


Figure 5. DC input buffer of the TCC110

The range of telephone line voltages is determined by the register values at the input. The input range at IND can be from 0V to 5V.

4.2 CAS tone detection

The TCC110 CAS detection algorithm is capable of detecting the CAS signals during speech with high talk-down and talk-off performance without the use of a hybrid, and 100% Bellcore compliant performance with use of a hybrid.

If the CAS detection is enabled the TCC110 will generate an interrupt (Interrupt register, bit 1 is set) when a correct dual tone (2130 and 2750 Hz) is detected.

CAS detection is enabled when the CASenable bit in the Function register is set and the FSK and PTE enable bits in the Function register are cleared.

The parameters of the CAS Detector are shown in table 1.

Table 3: CAS detector parameters

Parameter	Value
Low tone frequency	2130Hz ± 0.5%
High tone frequency	2750Hz ± 0.5%
Accepted signal level	-5.2dBm to –32dBm
Twist	-6dB to +6dB

When a valid CAS signal is detected, the CASdetect status bit of the Status register and the CASint bit of the interrupt register are set and an interrupt is generated. When the signal level is below the accepted signal level the status bit of the status register is cleared and the CASint interrupt bit is set , generating another interrupt.

The CASint interrupt bit is reset when the interrupt register is read (see Figure 6).

In order to accurately detect the end of a CAS tone, it is recommended to mute the near end speech immediately after the CAS tone has been detected.

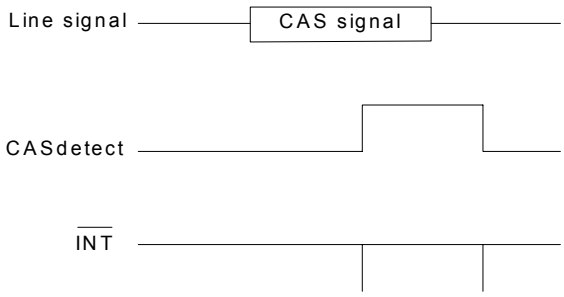


Figure 6: CASdetect, CASint and INT related to the CAS tone

4.3 FSK reception

4.3.1 FSK data reception sequence

The on-chip FSK Receiver satisfies all target specifications of Bellcore. The FSK receiver function can be enabled by setting the FSKenable bit (Function register, bit2) and clearing the CASenable (Function register, bit1) and the PTEenable (Function register, bit5) bits.

When the FSK Receiver is enabled, the TCC110 continuously checks for a signal in the FSK band (~1200 - ~2200 Hz) above the minimum signal level threshold. The TCC110 waits for mark bits, which are transmitted after

the channel seizure. When mark bits are detected, the FSK receiver starts receiving FSK data bytes. An FSK data word consists of one start bit (space) followed by eight data bits and one stop bit (mark). After the FSK receiver has detected a start bit it starts receiving the data bits (LSB first). After the 8th data bit the FSKint interrupt bit (Interrupt register, bit2) is set and an interrupt is generated.
The FSKint interrupt bit is cleared when the Interrupt register is read. The interrupt register and the FSKDT register should be read every time an interrupt occurs.

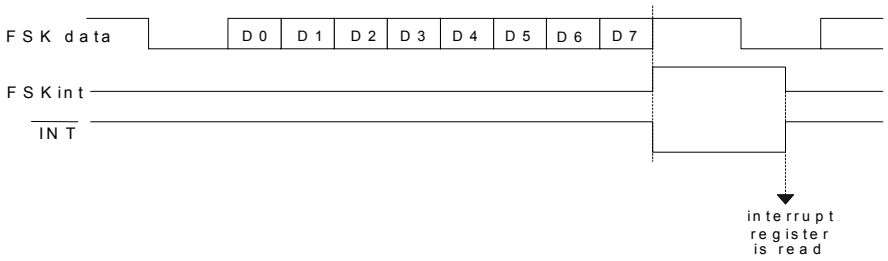


Figure 7. Sequence to receive an FSK data byte

The parameters of the FSK receiver are shown in Table 4.

Table 4: FSK Receiver parameters

Parameter	Bellcore	CCITT / V23
Mark frequency (logic 1)	1200Hz 1%	1300Hz 1.5%
Space frequency (logic 0)	2200Hz 1%	2100Hz 1.5%
Maximum allowed signal level	0dBm	-8dBV
Minimum signal level threshold	<-38dBm	<-40dBV
Twist	-10dB to +10dB	-6dB to +6dB
Accepted S/N (0Hz – 200Hz)	<-20dB	<-20dB
Accepted S/N (200Hz – 3200Hz)	<6dB	<6dB
Accepted S/N (3200Hz – 15000Hz)	<-20dB	<-20dB
Transmission rate	1200 bits per second 1%	1200 bits per second 1%

4.3.2 Begin Of Mark (BOM) detection

Due to noise etc. and the channel seizure signal the FSK receiver can mis-interpret the channel seizure or noise as normal data. This will cause the FSK receiver to generate unwanted interrupts before a BOM has been detected (see figure 9). The block of marks is a string of logic 1 and will not generate interrupts because there are no start bits.
To prevent occurrence of unwanted interrupts, the BOMDC bit (Mode register, bit6) must be set to '0'. When this is done the BOMdetect bit (Interrupt register, bit6) will be set and the FSK interrupts will be generated after a mark period of at least 16 sequential 1's has been detected. Interrupt will therefore not be generated during the channel seizure and during the block of marks. The status of BOMdetect is available in the Interrupt register. BOMdetect itself does not generate an interrupt. This behavior is shown in Figure 8. This bit will be cleared when the FSK receiver is disabled or a signal drop out occurs for more than 18.3ms. In the latter case the FSK receiver will behave as if it has just been disabled.

The reset value of the BOMDC bit is ‘0’ and this value is recommended to prevent unnecessary interrupt overloading of the micro-controller.

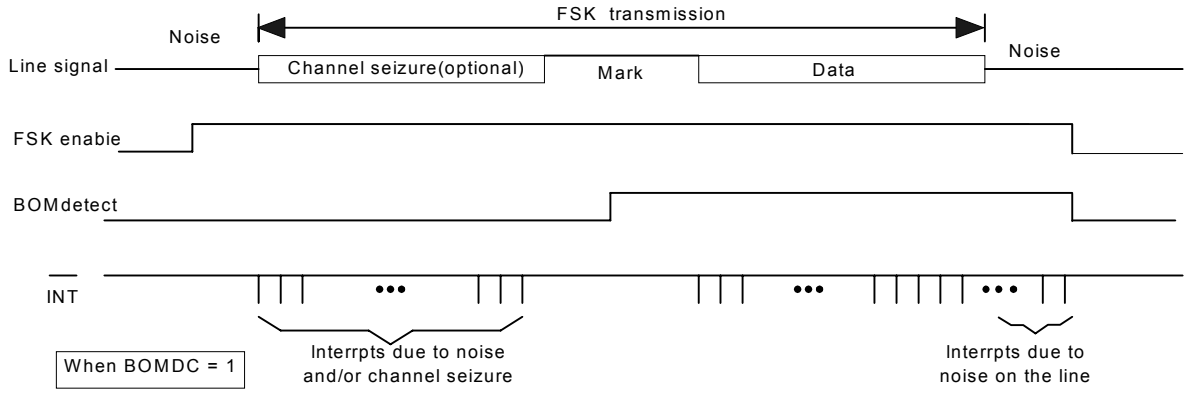


Figure 8: Interrupt behavior of the FSK receiver with BOMDC = 1

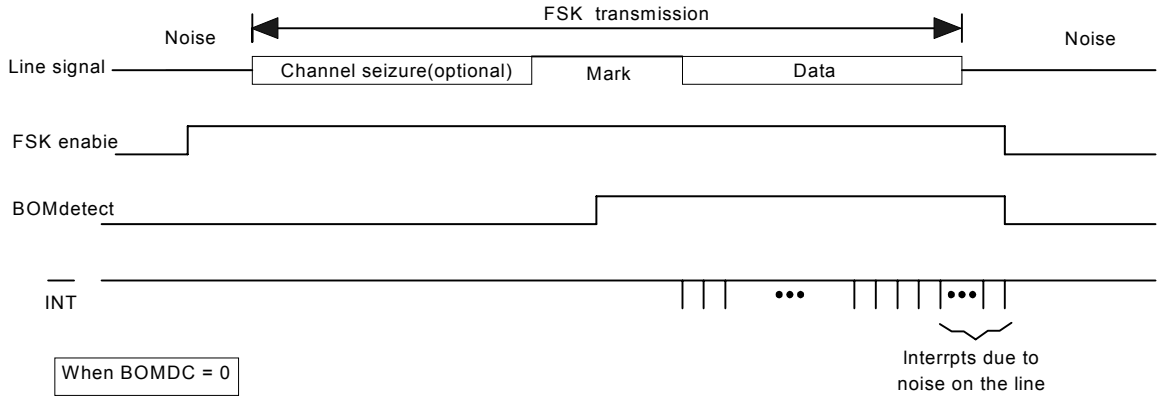


Figure 9: Interrupt behavior of the FSK receiver with BOMDC = 0

During FSK data reception, no new interrupts will occur after a signal dropout when BOMDC = '0'. If it is necessary to receive as much data as possible (even with a part missing) then the BOMDC can be set to '1' when reception of data starts.

4.4 Progress Tone Energy (PTE) detector

This block is enabled when the TCC110 is set to PTE enable mode (Function register, bit5) and all the other functions in the Function register are disabled.

The detector measures the total signal level for every 8.6ms. When the total signal level is above -27dBm in the Progress Tone band (305Hz to 640Hz) the PTEdetect bit in the Status register is set. When the total signal level is below –27dBm the PTEdetect bit is cleared. Each time PTEdetect changes the PTEint bit is set and an interrupt is generated. The PTEint bit is cleared when the Interrupt register is read. This behavior is shown in Figure 10.

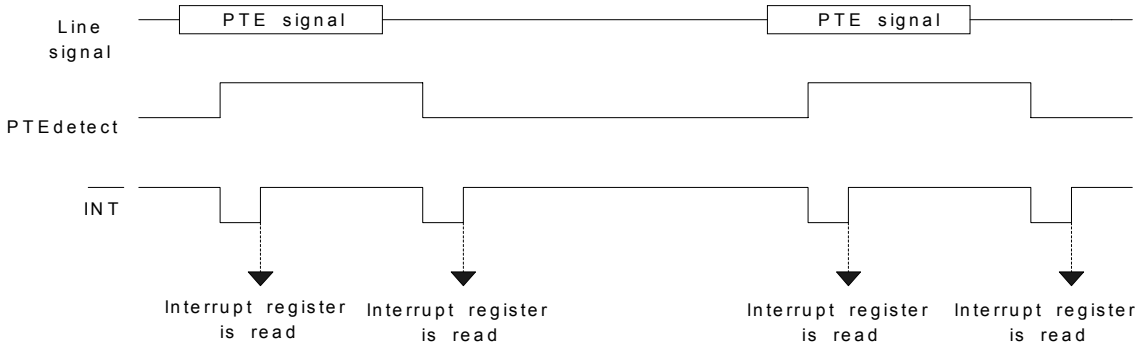


Figure 10: PTE detector operation

4.4 DTMF generator

The DTMF generator is able to generate 16 standard dual tones (see Table 5). These tones can be programmed by writing the DTMF register via the serial interface.

The DTMF generator is enabled when the DTMFenable bit (Function register, bit3) is set to '1'. When the ON-OFF bit in the DTMF register is programmed to '0', no tone will be generated; when it is programmed to '1', the tone specified in bits T3 to T0 will be generated. The code for each dual tone is shown in Table 5.

The DTMFG register can control the output gain of DTMF signal. The default power of the DTMF signal is –7.5dBm for high tone and –9.5dBm for low tone. The DTMFG register contains the gain factor that is multiplied to the default signal power to obtain the DTMF signal power. The gain factor is an unsigned number. The most significant bit (M) of the DTMFG register is the mantissa and the remaining bits (E6 to E0) denote the exponent. The output power of the DTMF signal can be obtained by the following equation.

DTMF signal power = Default signal power * DTMFG

Symbol	7	6	5	4	3	2	1	0
DTMFG	M	E6	E5	E4	E3	E2	E1	E0

The DTMFG register can be programmed within the range from 0.0000001B (0.0078 in decimal) to 1.1000111B (1.5546 in decimal). For example, if DTMFG is set to 80H (1.0000000 in binary or 1.0 in decimal) the DTMF signal power will be the same as the default power. If the DTMFG register is 0.1100110H (0.7969 in decimal) the DTMF signal power will be 1.97dB lower than the default power as follows.

20log(default power*0.7969 – default power) = 20log0.7969 = -1.97dB

The high tone power = -9.47dB
The low Tone power = -11.47dB

Table 5: DTMF frequencies code table

D3	D2	D1	D0	Character	Low frequency	High frequency
0	0	0	1	1	697.0Hz	1209Hz
0	0	1	0	2	697.0Hz	1336Hz
0	0	1	1	3	697.0Hz	1477Hz
0	1	0	0	4	770.0Hz	1209Hz
0	1	0	1	5	770.0Hz	1336Hz
0	1	1	0	6	770.0Hz	1477Hz
0	1	1	1	7	852.0Hz	1209Hz
1	0	0	0	8	852.0Hz	1336Hz
1	0	0	1	9	852.0Hz	1477Hz
1	0	1	0	0	941.0Hz	1336Hz
1	0	1	1	*	941.0Hz	1209Hz
1	1	0	0	#	941.0Hz	1477Hz
1	1	0	1	A	697.0Hz	1633Hz
1	1	1	0	B	770.0Hz	1633Hz
1	1	1	1	C	852.0Hz	1633Hz
0	0	0	0	D	941.0Hz	1633Hz

4.5 Ring or line reversal detector

For ring or line reversal detection, some external components are needed to generate a pulse each time a ring or line reversal occurs, as shown in Figure 11. Interrupt generation of the ring or line reversal detector is controlled by the LRenable bit in the Function register. When LRenable is set to ‘1’, the LRint bit of the interrupt register will be set and interrupts will be generated at every transition of the LRstatus bit. When LRenable is ‘0’, interrupts will not generated.

The LRstatus bit (reset value is high) in the Status register is cleared to ‘0’ at any positive edge of the LRin. If no positive edges of LRin are detected in Tguard time the LRstatus bit is set to ‘1’. The LRint bit is cleared when the Interrupt register is read.

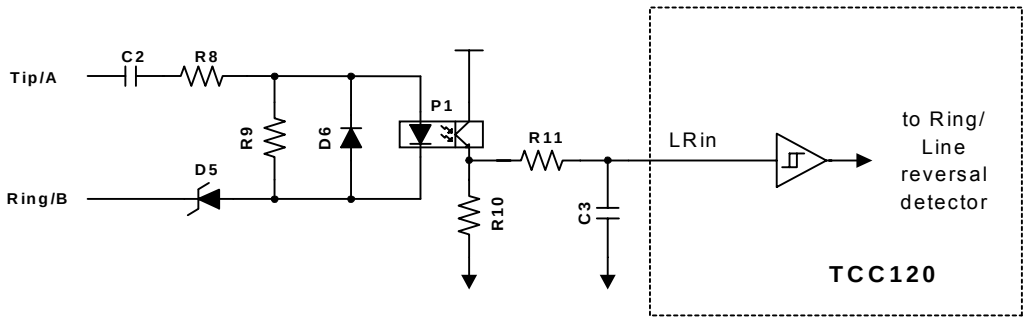


Figure 11. External component to generate LRin

If an LRint interrupt has been generated in power-down mode, it is recommended to disable power-down mode to

be able to count the guard time counter using the main clock (XIN). The guard time counter is reset at the positive edge of LRin. The guard time (Tguard) can be programmed by writing the GTIME register as follows.

Tguard = 143us * (GTIME[6:0] * 4 + 3)

(Ex. Tguard = 34.749ms = 0.143ms * (0111100B * 4 + 3))

Figure 11 and Figure 12 show line reversal and ring detection respectively.

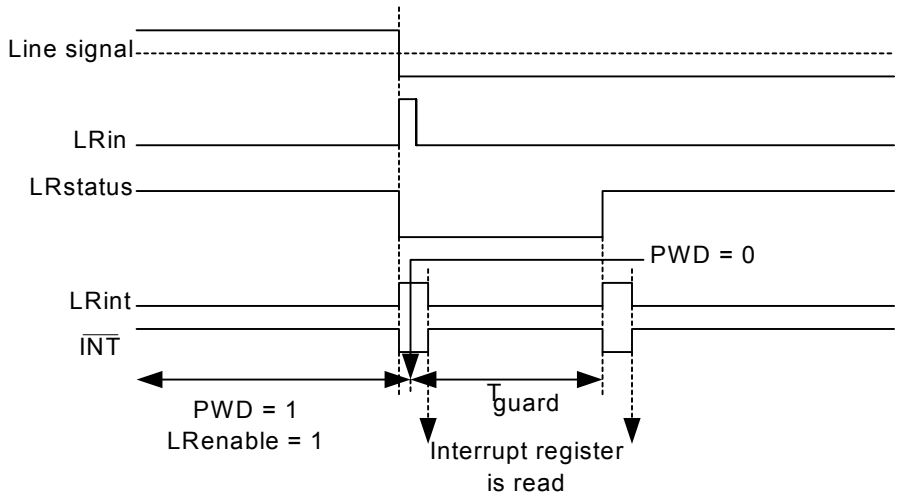


Figure 12 : Behavior of signals on a line reversal

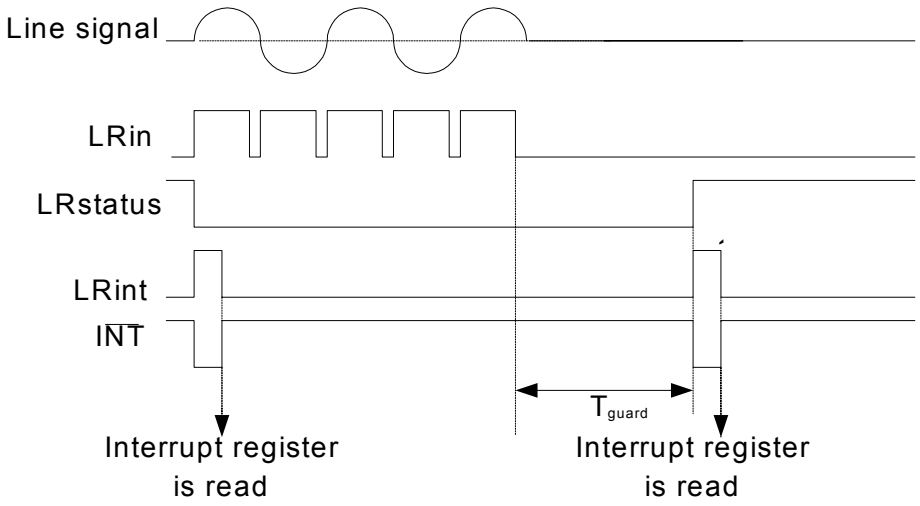


Figure 13: Behavior of signals during ring

4.6 DC voltage measurement block

The DC voltage measurement block can measure the DC voltage on the telephone line to check multiple extension interoperability. DC voltage measurement block is shown in Figure 14.

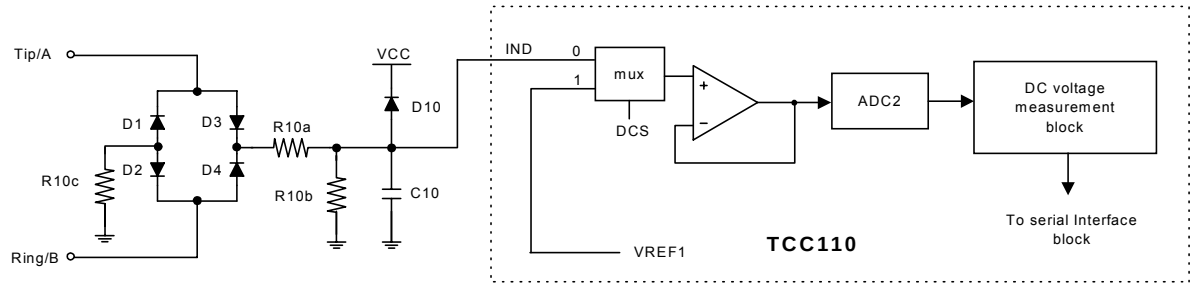


Figure 14: DC voltage measurement block

The voltage at IND is determined by:

IND = (VTip - VRing) * ((R10b+R10c) / (R10a+R10b+R10c))

The reference voltage (VREF1) level can be measured by setting the reference voltage measurement mode. When the reference voltage measurement mode is set (DCM[1:0] = 01), the measured reference voltage level (VREF1) is stored in the VREF1 data register (see Figure 19). But do not use this mode in application. The measured DC voltage on the telephone line is obtained as follows:

DCdata =K * IND

where K is 51 and DCdata is a signed 9 bit value. DCD0 and the LSB of DCD1 contain the data of DCdata and the sign bit, respectively.
Each time a new value is stored in DCdata, its absolute value is compared with two programmable positive 8-bit thresholds (DCTH and DCTL). The comparison result is presented in the DC-HIGH and DC-LOW bits (comparison status bits) of the Status register. The meanings of these bits are shown in Table 6 and Figure 15.

Table 6: Meanings of values in DC-HIGH and DC-LOW

Bit	Value	Meaning
DC-HIGH	1	| DCdata | >= DCTH
	0	| DCdata | < DCTH
DC-LOW	1	| DCdata | >= DCTL
	0	| DCdata | < DCTL

With these bits it is possible to detect easily whether the line voltage goes up or down by programming the thresholds such that DCTH is above the current DCdata value and DCTL is below the current DCdata value

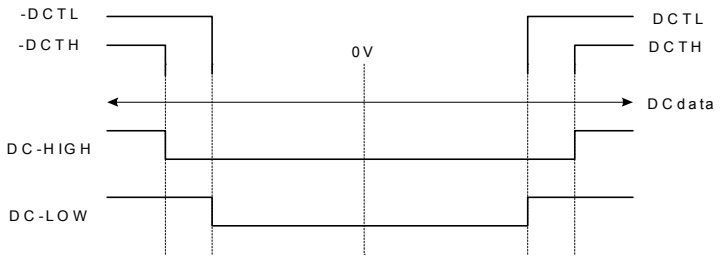


Figure 15: Behavior of DC-HIGH and DC-LOW related to DCdata, DCTH and DCTL

4.6.1 DC measurement time

The time period for calculating the average value of the DC line voltage is programmed with the DC measurement time register (DCMT):

Tmeasure = DCMT * 143us

DCMT should be a power of 2. (2, 4, 8, 16, 32, 64, 128)

4.6.2 Interrupt generation by the DC voltage measurement block

The way interrupts are generated is determined by the DC-INT mode bit in the Mode register. When DC-INT mode = 0, interrupts are generated when a change in the comparison status bits occurs (see Figure 16) When DC-INT mode = 1, interrupts are generated each time a new measurement has been completed (see Figure 17). Each time an interrupt is generated the DCint interrupt bit is set. The DCint interrupt bit is cleared when the Interrupt register is read. To prevent unpredictable behavior when programming new thresholds, be sure that the new threshold values are programmed before a new measurement time has expired.

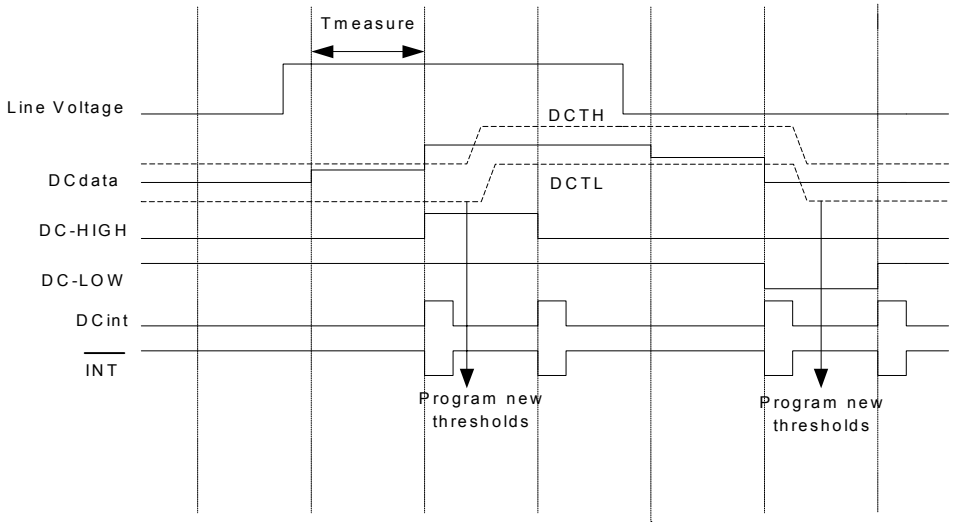


Figure 16: Interrupt generation of the DC voltage measurement block when DC-INT mode = 0

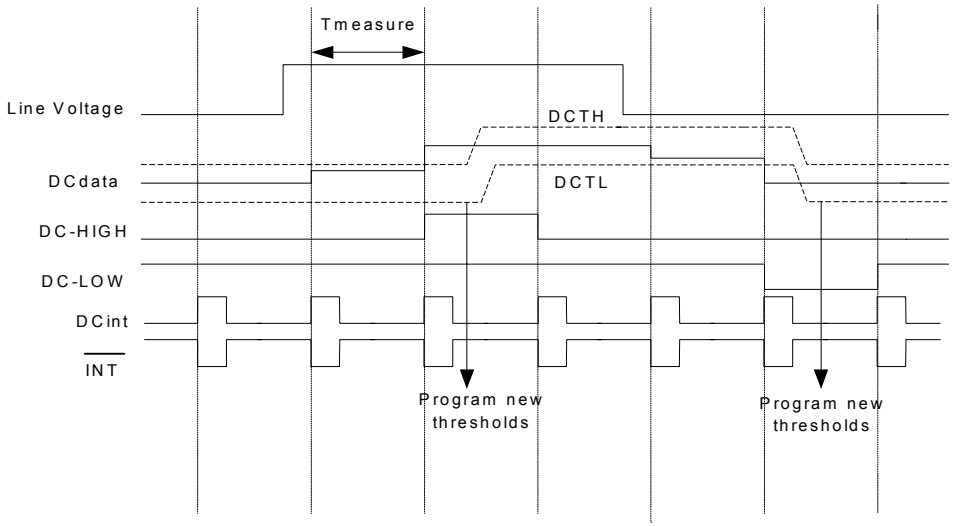


Figure 17: Interrupt generation of the DC voltage measurement block when DC-INT mode = 1

4.6.3 DC voltage measurement mode

The DC voltage measurement block has four modes in which it can operate. These modes are selected with the DMC1 and DCM0 bits in the Mode register. The mode selection is shown in Table 6.

Table 6: Description of the DC voltage measurement modes

DCM1	DCM0	Mode	Description
0	0	DC line voltage measurement mode	DCdata = IND – VREF1 (DCS = 0)
0	1	Reference voltage measurement mode	Reference voltage (VREF1) level is measured in this mode (DCS = 1) – Do not use
1	1	Reserved	
1	0	reserved	

4.6.3.1 DC line voltage measurement mode

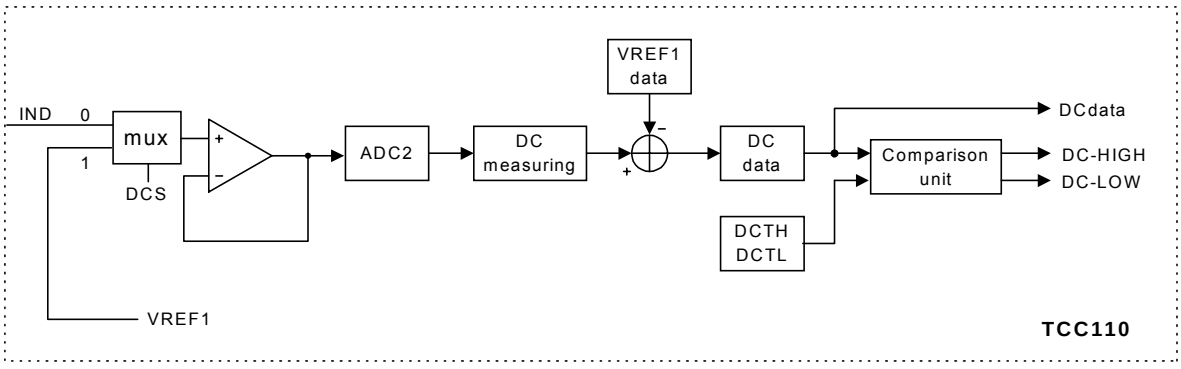


Figure 18: DC measurement block configuration for DC line voltage measurement mode

In DC voltage measurement mode the data coming from the DC measuring unit is subtracted by the VREF1 data register. The result is passed to DCdata and the comparison unit (see Figure 18). In the comparison unit the absolute value of DCdata is compared with DCTH and DCTL. The result is presented in the DC-HIGH and DC-LOW bits of the Status register.

4.6.3.2 Reference voltage measurement mode. (Do not use this mode in application)

To obtain the reference voltage (VREF1) data the reference voltage measurement mode is used. In this mode the voltage at IND is ignored and the reference voltage (VREF1) is selected to determine the reference voltage level. The reference voltage measurement is done within the time specified in the DCMT register. The result of the measurement is written into the VREF1 data register (see Figure 19)
When in this mode the status bits (coming from the Comparison unit) are not updated.
The result of the reference voltage measurement can be used by the TCC110 in the DC voltage measurement mode.

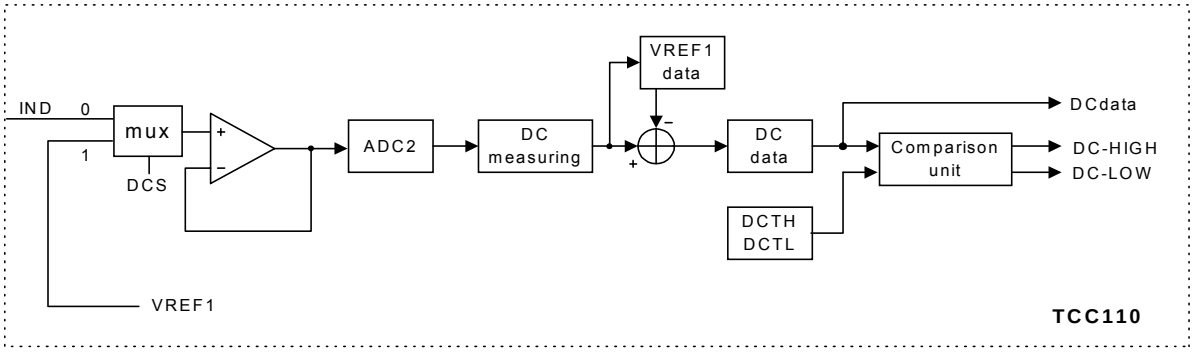


Figure 19: DC Level Detector configuration for reference voltage measurement mode

The VREF1 data register is an internal register that cannot be accessed via the serial interface.
NOTE: Since reference voltage may change in time (due to change of temperature, supply voltage, etc.) it is recommended to measure the reference voltage regularly.

4.7 Ring detection

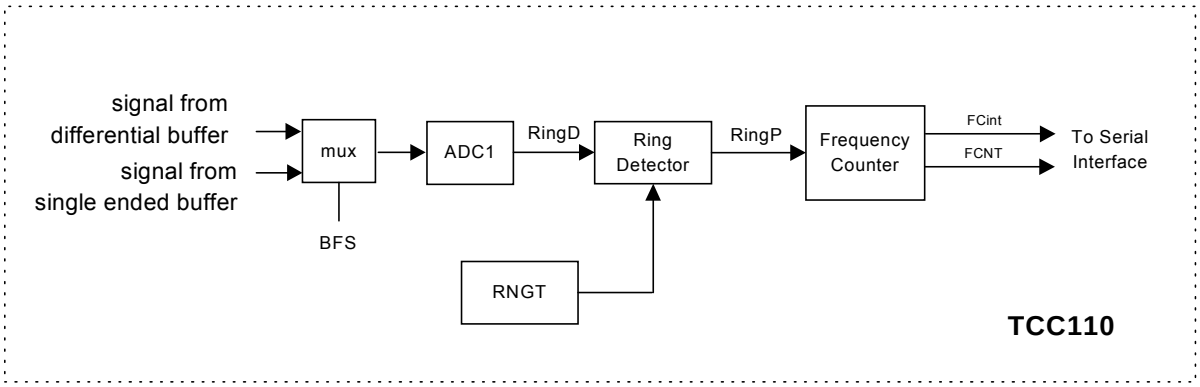


Figure 20: Ring detection and frequency counting block

The TCC110 can extract the ring signal and its frequency (see Figure 20).. The ADC1 is used for converting the ring signal to the digital signal (RingD) and the ring detector removes the DC level of the RingD signal. The result is compared with the RNGT register. When the amplitude of RingD is higher than RNGT, pulses (RingP) are sent to the frequency counter. The frequency counter then generates interrupts (when enabled) and provides information about the ring frequency

The minimum amplitude threshold of the ring signal that must be detected can be programmed via the RNGT register. The threshold is an 8-bit positive value. The higher the threshold is, the higher the ring amplitude must be in order to be detected. The behavior of RingP is shown in Figure 21.

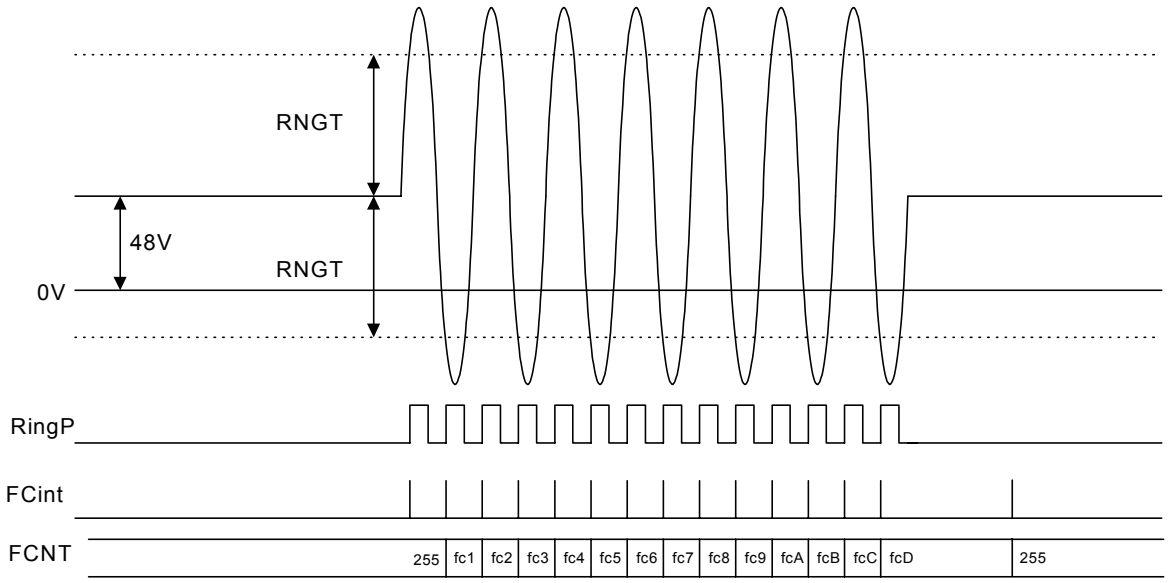


Figure 21: Behavior of RING when a ring occurs on the line
(FCint only behaves as shown when FCenable = 1)

4.8 Frequency counter

The frequency counter is enabled when the FCenable bit in the Function register is set. When the frequency counter is enabled, it counts the time between two positive edges of the RingP signal from the Ring Detection block. On every positive edge of RingP the current result is written into the FCNT register, the FCint bit is set and an interrupt is generated (see Figure 21, where fc1, fc2, … , fcD and 255 are frequency counting results at each positive edge of the RingP signal)

When the frequency counter has reached its maximum value (255), it stops counting, writes 255 into the FCNT register, sets the FCint bit and generates an interrupt. When 255 is read from the FCNT register this means that the end of the ring has been reached.

The FCint interrupt bit is cleared when the Interrupt register is read.

FCNT represents the counted time as follows:

T = FCNT * 0.572ms

4.9 Serial Interface

The serial interface is accessed through the SDT and SCK pins. The SDT pin is an open drain bi-directional pin (its output can be HiZ or logic0).

4.9.1 Serial bus configuration

The serial bus consists of the SDT with a pull-up resistor (Rpu) and the SCK for each TCC110. The SCK is a transmission clock and the SDT transmits bi-directional data.
The micro-controller always initiates a transmission and generates the transmission clock on the SCK line. When multiple TCC110s are used, all TCC110s are connected in parallel to the SDT line and each TCC110 has its own serial clock (SCK) from the micro-controller. Only the TCC110 of which the SCK is active is accessible and only one SCK may be active at any time.

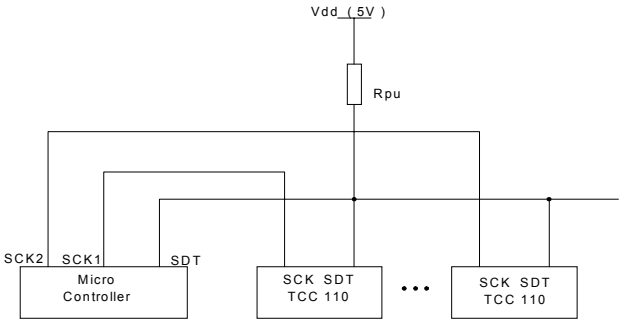


Figure 22: Serial bus configuration

4.9.2 Start and stop conditions

The SDT and SCK lines remain high when the bus is not busy. A high-to-low transition of the SDT line while the SCK is high is defined as the start condition. A low-to-high transition of the SDT while the SCK is high is defined as a stop condition
When a start condition occurs between a normal start condition and a stop condition, this is called a repeated start condition.

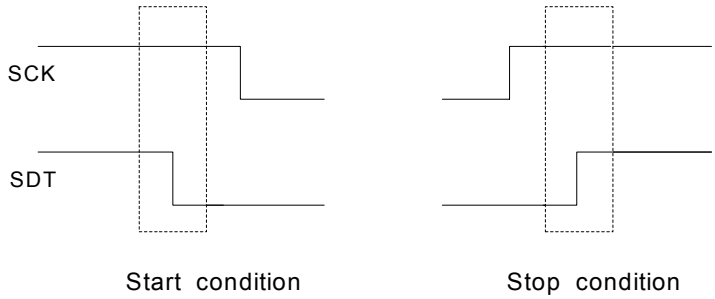


Figure 23: Start and stop conditions

4.9.3 Bit transfer

After a start condition one data bit is transferred during each SCK pulse. The data on the SDT line must remain stable during the high period of the SCK pulse as changes in the data line at this time will be interpreted as a control signal

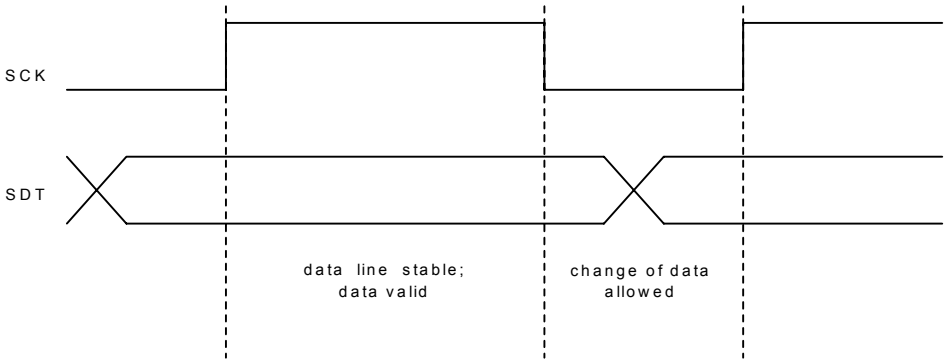


Figure 24. Bit transfer timing

4.9.4 Byte transmission and acknowledge

The number of data bytes transferred between the start and the stop conditions from the transmitter to the receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a high level signal put on the bus by the transmitter during which time the micro-controller generates an extra acknowledge-related clock pulse.

The TCC110 must generate an acknowledge after the reception of address field data or a register start address. Also the micro-controller must generate an acknowledge after the reception of each byte that has been clocked out of the TCC110.

The device that acknowledges must pull down the SDT line during the acknowledge clock period immediately after the 8th SCK pulse, so that the SDT line is stable low during the high period of the acknowledge-related SCK pulse.

The micro-controller must signal an end-of-data to the TCC110 by not generating an acknowledge on the last byte that has been clocked out of the TCC110. In this event the TCC110 must leave the SDT line high to enable the micro-controller to generate a stop condition.

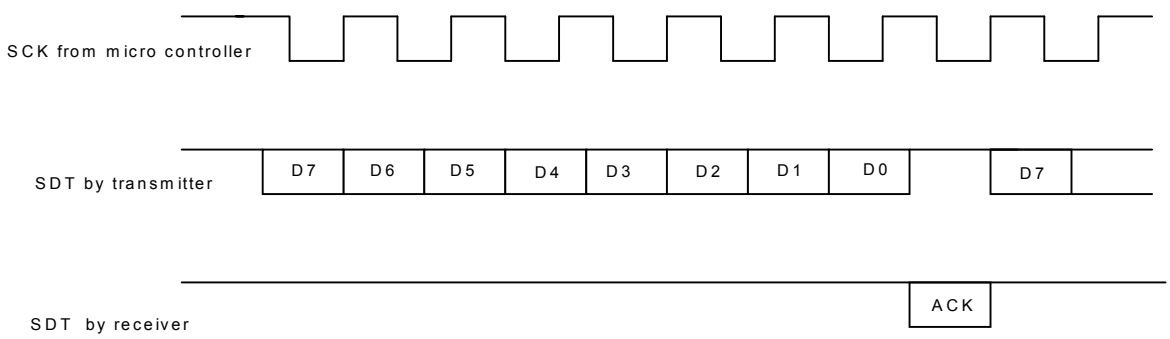


Figure 25. Byte transmission and acknowledge

4.9.5 Address field

Before any data is transmitted on the SDT line, the TCC110, which should respond, is addressed first. The addressing is always carried out with the first byte (Address field) transmitted after the start procedure. The interface address is reserved for the TCC110, 30H for write and 31H for read.

When the address matches the address of the TCC110, the acknowledge is given; when it does not match, no acknowledge is given.

The address field is built of two parts as follows

- Interface Address (A6 to A0)
- Read/Write control (R/$\overline{W}$)

A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$
0	0	1	1	0	0	0	1/0

Figure 26: Specification of the bits of the address field

4.9.6 Register address

The register address is the second byte transmitted by the micro-controller. This address is stored in the TCC110 and used for the following read and write actions. When multiple bytes are accessed, the first byte is written to the specified register address and the register address of the TCC110 is auto-incremented on each acknowledge.

4.9.7 Serial communication protocol

The serial communication protocol is shown in Figure 27 and Figure 28. The micro-controller can initiate two kinds of sequence, the write sequence and the read sequence. Both sequences are initiated with a start condition that is followed by the TCC110 address with the read/write control bit cleared. The first byte after the TCC110 address is interpreted as the address of a TCC110 register. During the write sequence the register address of the TCC110 is increased automatically on each acknowledge. The write sequence is ended with the stop condition from the micro-controller.

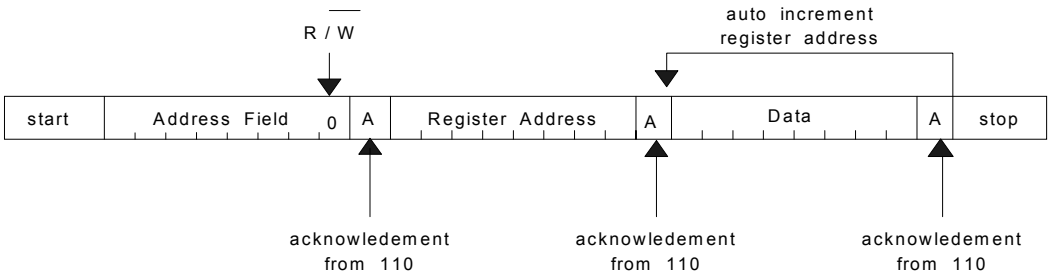
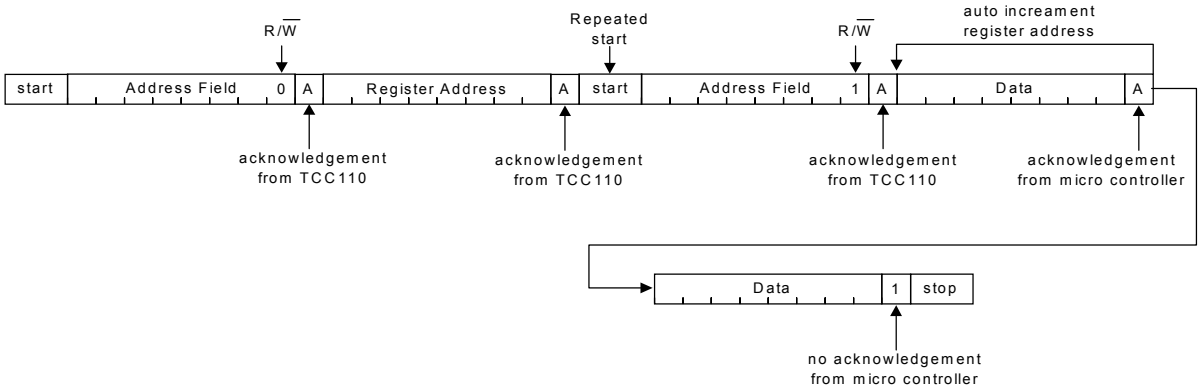


Figure 27: Write sequence of the serial interface

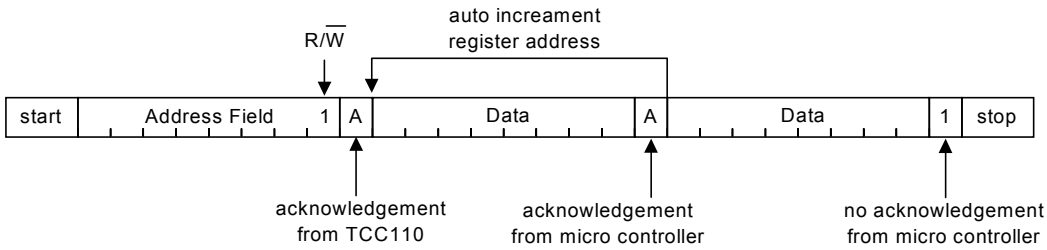
For the read sequence, after a register address of the TCC110, a repeated start condition is generated by the micro-controller which is followed by the TCC110 address with the read/write control bit set. The data is read from the previously-set register address. When the micro-controller responds with an acknowledge the address of the register is auto incremented and the TCC110 will put the data from the next register on the SDT line. When the

micro-controller stops giving an acknowledge the TCC110 will stop transmitting data and the micro-controller will generate a stop condition.

When the read sequence is initiated with a start condition that is followed by the TCC110 address with the read/write control bit set, the data is read from the last set register address. (See Figure 28)



(a)



(b)

Figure 28: Read sequence of the serial interface
(a) New register start address is programmed (b) No register start address is programmed.

4.10 Power-down mode

The TCC110 can be put in power-down mode by programming the PDW bit in the Mode register to '1'. In this mode the input signal buffers, ADC's, the reference bias generator, the DTMF output buffer and the oscillator are switched off. However the Ring/Line Reversal detection can be active by programming the LRenable bit in the function register to be set. The serial interface can always be accessed, even in power-down mode. In power-down mode, if ring or line reversal occur when LRenable bit is '1', the LRint bit is set and an interrupt is generated. When the TCC110 is put in power-down mode, all interrupt bits in the interrupt register cannot be set except for the LRint bit.

4.11 Interrupt

The interrupt output ($\overline{INT}$) is active low. The $\overline{INT}$ pin is in Hi-Z state when not active, so an external pull-up resister is required. The flag in the interrupt register indicates the interrupt cause. Interrupt flags are set by hardware but must be reset by software. All flags of the interrupt register are reset when the register is read via the serial interface.

The Table 7 shows interrupt sources of the TCC110.

Table 7: Interrupt sources of the TCC110

Source Block	generation
Ring / line reversal detector	. When LRstatus changes
Frequency counter	. When a new measurement is started . When frequency counter reaches 255
FSK receiver	. reception of a new FSK data byte
DC voltage measurement block	. DC-INT mode = 0 : When DC-HIGH or DC-LOW changes . DC-INT mode = 1 : Every time a new measurement has been completed
CAS detector	. When CASdetect changes
PTE detector	. When PTEdetect changes

4.12 3.579545MHz oscillator circuitry

The on-chip oscillator is a single-stage-inverting amplifier biased by an internal feedback resistor. The oscillator circuit is shown in Figure 29.

To drive the device with an external clock source, apply the external clock signal to XIN, and leave XOUT to float. If the amplitude of the input signal is less than VCC to VSS or a sign wave is applied, capacitive decoupling is needed. In the power-down mode (Mode register, bit7 = 1), the oscillator is stopped and XIN is internally pulled HIGH and the feedback path through the Rfd is opened to switch off the oscillator current.

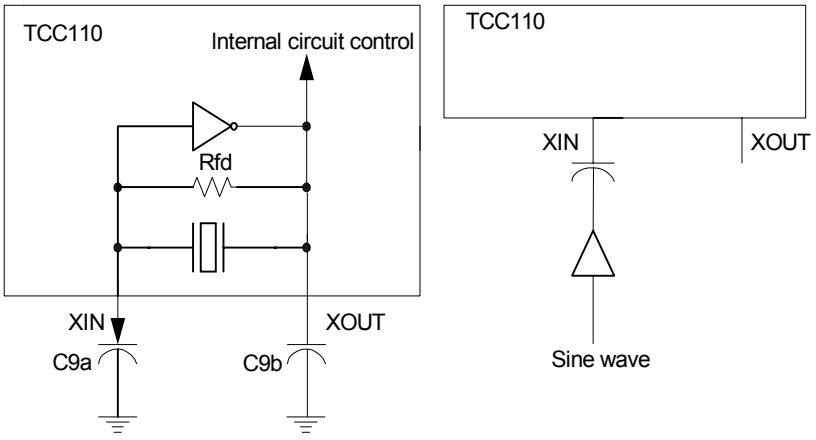


Figure 29: (a) oscillator with external capacitor (b) External clock: sine wave

5. REGISTER MAPS

The registers that are available in the TCC110 are shown in the following tables.

Register overview

Register name	Address	Function	Default value	Read / Write
MODE	00H	Mode register	0000 0000	read / write
FUNC	01H	Function register	0000 0000	read / write
DTMFT	02H	DTMF tone select register	0000 0000	read / write
DCMT	03H	DC measurement time register	0000 0000	read / write
DCTH	04H	High DC threshold register	0000 0000	read / write
DCTL	06H	Low DC threshold register	0000 0000	read / write
RNGT	08H	Ring signal threshold register	0000 0000	read / write
GTIME	0aH	Guard time register	0000 0000	read / write
INTR	80H	Interrupt register	0000 0000	read only
STAT	81H	Status register	0000 0100	read only
FSKDT	82H	FSK data register	0000 0000	read only
FCNT	83H	Frequency counter register	0000 0000	read only
DCD0	84H	Measured DC data register	0000 0000	read only
DCD1	85H	Measured sign bit register of DC data	0000 0000	read only
DTMFG	f0H	DTMF output gain control register	0000 0000	read / write
CONT1	F1H	FSK control register 1	0000 0000	read / write
CONT2	F5H	FSK control register2	0000 0000	read / write

Mode register (MODE)

Address 00H; read / write.

7	6	5	4	3	2	1	0
PDW	BOMDC	-	-	DCenable	DC-INT mode	DCM1	DCM0

Description of MODE bits

Bit	Symbol	Description
MODE.7	PWD	1: Puts the TCC110 in power-down mode 0: Puts the TCC110 in active mode
MODE.6	BOMDC	0: Forbids FSK interrupts until BOMDC is ‘1’ 1: Allows FSK interrupts before BOMDC is ‘0’
MODE.3	DCenable	1: Enables the DC Level measurement unit 0: Disables the DC Level measurement unit
MODE.2	DC-INT mode	1: The DC level measurement block generates an interrupt for every DC measurement time period. 0: The DC level measurement block generates an interrupt when DC-HIGH or DC-LOW status bit changes
MODE.1 & MODE.0	DCM1 DCM0	00 : DC line voltage measurement mode 01 : Reference voltage measurement mode 10,11 : reserved

Function register (FUNC)

Address 01H; read / write.

7	6	5	4	3	2	1	0
BFS	-	PTEenable	FCenable	DTMFenable	FSKenable	CASenable	LRenable

Description of FUNC bits

Bit	Symbol	Description
FUNC.7	BFS	1: Selects the single-ended input buffer 0: Selects the differential input buffer
FUNC.5	PTEenable	1: Enables the PTE detector 0: Disables the PTE detector
FUNC.4	FCenable	1: Enables the frequency counter 0: Disables the frequency counter
FUNC.3	DTMFenable	1: Enables the DTMF generator 0: Disables the DTMF generator
FUNC.2	FSKenable	1: Enables FSK receiver 0: Disables FSK receiver
FUNC.1	CASenable	1: Enables CAS detector 0: Disables CAS detector
FUNC.0	LRenable	1: Enables LR interrupts 0: Disables LR interrupts

DTMF tone select register (DTMFT)

Address 02H; read / write.

7	6	5	4	3	2	1	0
ON-OFF	-	-	-	T3	T2	T1	T0

Description of DTFMT bits

Bit	Symbol	Description
DTMFT.7	ON-OFF	1: Enables DTMF tone output 0: Disables DTMF tone output
DTMFT.3 to DTMFT.0	T3 to T0	DTMF code to be generated (See table 999)

DC measurement time register (DCMT)

Address 03H; read / write.

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Description of DCMT bits

Bit	Symbol	Description
DCMT.7 to DCMT.0	D7 to D0	Determines the DC measurement period

High DC threshold register (DCTH)

Address 04H; read / write.

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Description of DCTH bits

Bit	Symbol	Description
DCTH.7 to DCTH.0	D7 to D0	High threshold value to be compared with the measured DC voltage.

Low DC threshold register (DCTL)

Address 06H; read / write.

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Description of DCTL bits

Bit	Symbol	Description
DCTL.7 to DCTL.0	D7 to D0	Low threshold value to be compared with the measured DC voltage.

Ring signal threshold register (RNGT)

Address 08H; read / write.

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Description of RNGT bits

Bit	Symbol	Description
RNGT.7 to RNGT.0	D7 to D0	Threshold value to be compared with the absolute value of measured ring signal

Guard time register (GTIME)

Address 0aH; read / write.

7	6	5	4	3	2	1	0
-	G6	G5	G4	G3	G2	G1	G0

Description of GTIME bits

Bit	Symbol	Description
GTIME.6 to GTIME.0	D6 to D0	Guard time to indicate the end of a line reversal or ring

Interrupt register (INTR)

Address 80H; read only.

7	6	5	4	3	2	1	0
-	BOMdetect	PTEint	FCint	DCint	FSKint	CASint	LRint

Description of INTR bits

Bit	Symbol	Description
INTR.6	BOMdetect	1: Indicates that the Begin Of the Mark period during FSK reception has been detected
INTR.5	PTEint	1: Indicates that PTEdetect has been changed
INTR.4	FCint	1: Indicates that a frequency counter result is stored and starts new counting.
INTR.3	DCint	1: Indicates that a DC interrupt has occurred (depends on DC-INT mode)
INTR.2	FSKint	1: Indicates that a new FSK frame has been received
INTR.1	CASint	1: Indicates that CASdetect has been detected
INTR.0	LRint	1: Indicates that LRstatus has been changed

Status register (STAT)

Address 81H; read only.

7	6	5	4	3	2	1	0
-	-	PTEdetect	-	DC-HIGH	DC-LOW	CASdetect	LRstatus

Description of STAT bits

Bit	Symbol	Description
STAT.5	PTEdetect	1: Indicates that the PTE detector detects the signal that satisfies the specified frequency and energy level; 0: No more Progress Tone is detected
STAT.3	DC-HIGH	1: | measured DC voltage | >= DCTH (When DCenable is '1') 0: | measured DC voltage | < DCTH (reset value)
STAT.2	DC-LOW	1: | measured DC voltage | >= DCTL (reset value) 0: | measured DC voltage | < DCTL (When DCenable is '1')
STAT.1	CASdetect	1: Indicates that a CAS tone has been detected 0: No more CAS Tone is detected
STAT.0	LRstatus	1: LRint has not occurred until expiring GTIME (reset value) 0: LRint has occurred before expiring GTIME

FSK data register (FSKDT)

Address 82H; read only.

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Description of FSKDT bits

Bit	Symbol	Description
FSKDT.7 to FSKDT.0	D7 to D0	Last received FSK data byte

Frequency counter register (FCNT)

Address 83H; read only.

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Description of FCNT bits

Bit	Symbol	Description
FCNT.7 to FCNT.0	D7 to D0	Last measured frequency data

Measured DC data register (DCD0)

Address 84H; read only.

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Description of DCD0 bits

Bit	Symbol	Description
DCD0.7 to DCD0.0	D7 to D0	Last measured DC voltage of the telephone line

Measured DC data sign bit register (DCD1)

Address 85H; read only.

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	SIGN

Description of DCD1 bits

Bit	Symbol	Description
DCD0.0	SIGN	Last measured sign bit of the DC voltage of the telephone line

DTMF output gain control register (DTMFG)

Address f0H; read / write

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Description of DTMFG bits

Bit	Symbol	Description
DTMFG.7 to DTMFG.0	D7 to D0	This byte multiplied to control the output gain of DTMF generator

Special control register (CONT1)

Address f1H; read / write

7	6	5	4	3	2	1	0
-	-	-	-	0	1	1	1

This register should be written with ‘07h’.

Special control register (CONT2)

Address f5H; read / write

7	6	5	4	3	2	1	0
-	-	0	0	0	0	0	0

This register should be written with ‘00h’.

Notes:

1. To allow for future extensions, reserved bits (indicated with ‘-‘) must be written with '0'.
2. When reading from a register, the reserved bits (indicated with ‘-‘) return an undefined value (either '0' or '1').
3. The value of DCMT register should be power of 2 (0, 2, 4, 8, 16, 32, 64, 128)

6. ELECTRICAL SPECIFICATIONS

6.1 Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
VCC	DC supply voltage (VCCA, VCCD)	-0.3	7	V
V_{IN}	DC input voltage	-0.3	VCC+0.3	V
I_{IN}	DC input current	-10	10	mA
Tstg	Storage temperature	-40	125	°C

6.2 DC electrical characteristics

VDD = 5V ± 5%, TA = 0 to 70°C, XIN = 3.579545MHz ± 0.1%

Symbol	Parameter	Min	Typ	Max	Unit
VCC	DC supply voltage (VCCA, VCCD)	4,75	5.0	5.25	V
Logical inputs and outputs (pins SCK, SDT, $\overline{INT}$, $\overline{RESET}$, LRin, TEST, TESTOUT)					
V_{IH}	High level input voltage	0.7VCC			V
V_{IL}	Low level input voltage			0.3VCC	V
V_{T+}	Schmitt trigger, positive-going threshold			0.8VCC	V
V_{T-}	Schmitt trigger, negative-going threshold	0.2VCC			V
I_{IH}	High level input current (V_{IN} = VCC)	-10		10	uA
I_{IL}	Low level input current (V_{IN} = VSS) Low level input current with pull-up	-10 -100	 -50	10 -10	uA uA
V_{OH}	High level output voltage (I_{OH}=4mA)	2.4			V
V_{OL}	Low level output voltage (I_{OL}=4mA)			0.4	V

6.3 Electrical characteristics

VDD = 5V ± 5%, TA = 0 to 70°C, XIN = 3.579545MHz ± 0.1%

Symbol	Parameter	Min	Typ	Max	Unit
Crystal Oscillator					
Fx	Normal frequency		3.579545		MHz
Tol	Frequency tolerance	-0.1		0.1	%
Cxi,Cxo	Input capacitance on XIN and XOUT		7		pF
Voltage reference					
VREF	Reference voltage output		2.25		V
CAS detector					
THac	Input accept threshold (in 600 Ω load)	-32			dBm
Pic	Input signal power (in 600 Ω load)	-32		0	dBm

VDD = 5V ± 5%, TA = 0 to 70℃, XIN = 3.579545MHz ± 0.1%

Symbol	Parameter	Min	Typ	Max	Unit
flc	Low tone frequency		2130		Hz
fhc	High tone frequency		2750		Hz
∆fmaxc	maximum frequency deviation	-0.6		+0.6	%
Twc	Twist	-6		6	dB
FSK receiver					
Pif	Input signal power (in 600 Ω load)	-38		0	dBm
fD	data transmission rate frequency	1188	1200	1212	Baud
fmb	mark frequency (Bell202)	1188	1200	1212	Hz
fsb	space frequency (Bell202)	2178	2200	2222	Hz
fmv	mark frequency (CCITT/V23)		1300		Hz
fsv	space frequency (CCITT/V23)		2100		Hz
Twf	twist	-10		10	dB
S/N0	signal to noise ratio (0Hz – 200Hz)	-25			dB
S/N1	signal to noise ratio (200Hz – 3.2kHz)	6			dB
S/N3	signal to noise ratio (3.2kHz – 15kHz)	-25			dB
Progress tone energy detector					
BW	detection bandwidth	305		640	Hz
THap	Input accept threshold (in 600 Ω load)	-27		0	dBm
Analog Input of A/D converter					
Vadc1	voltage range of ADC1(OUT pin)		2.828		Vp-p
Vadc2	voltage range of ADC2 (INSE pin)		2.1739		Vp-p
Aimp	Analog input impedance	10			kΩ

6.4 AC Timing values

CAS timing characteristics

Parameter	Min	Typ	Max	Unit
TDETC		51.6		ms
TOFFC		25.8		ms
TWIDTHC	25.8			ms

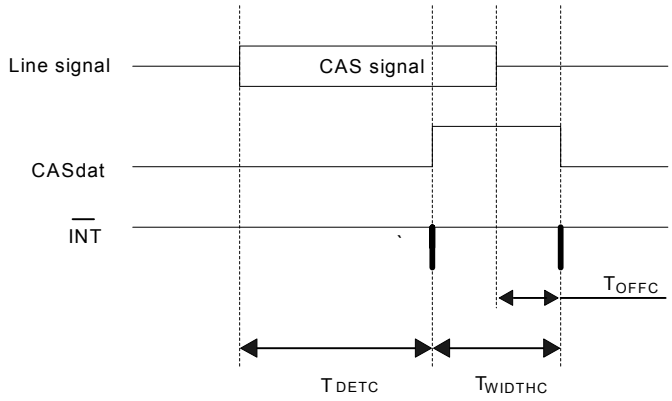


Figure 30: Timing of the CAS detection signals related to the CAS tone

PTE timing characteristics

Parameter	Min	Typ	Max	Unit
TDETP		18.3		ms
TOFFP		18.3		ms

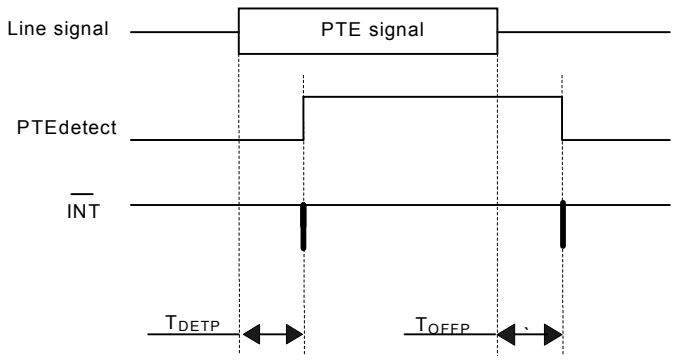


Figure 31: Timing of the PTE detection signals related to the progress tone

Serial Interface timing characteristics

Parameter	Min	Typ	Max	Unit
Tstart	50			ns
Tstop	50			ns
TSCKL	500			ns
TSCKH	500			ns
Tsu (setup)	50			ns
Thd (hold)	50			ns

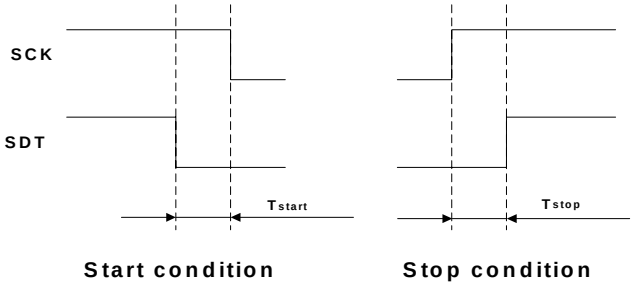


Figure 32: Timing constraints of start and stop conditions

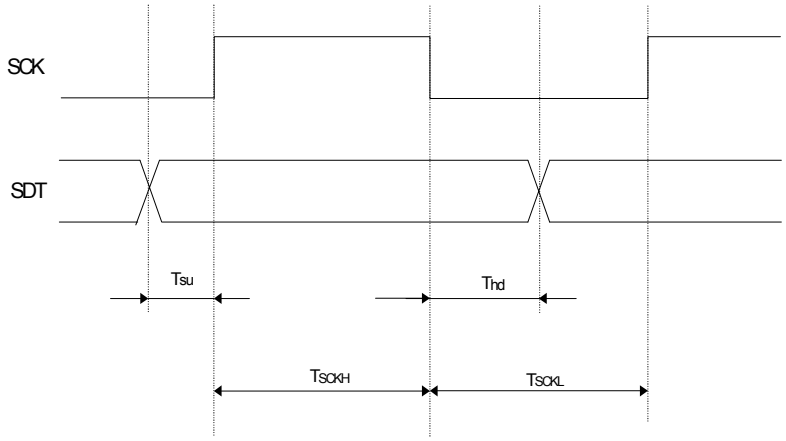


Figure 33: Timing of SCK and SDT during byte transmission

7. PACKAGE

Package dimensions

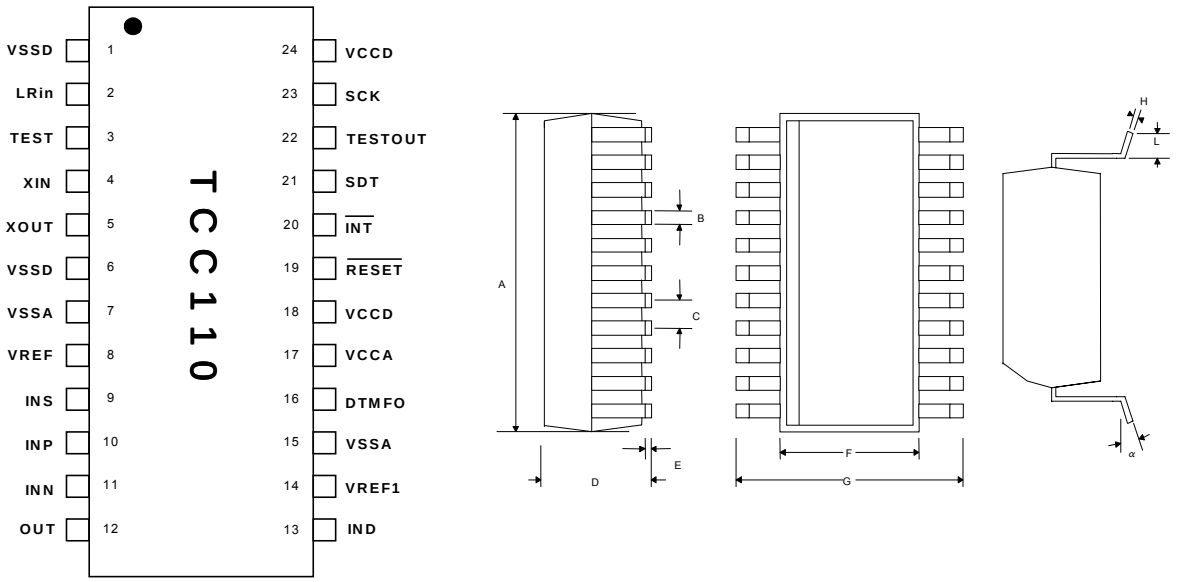


Figure 34: 24-pin SOP package dimensions

	mm	
	min	max.
A	15.2	15.6
B	0.33	0.51
C	1.27	1.27
D	2.35	2.65
E	0.1	0.3
F	7.4	7.6
G	10.00	10.65
H	0.23	0.32
L	0.4	1.27
α	0	8

Revision history

May 25, 2001 LRin application circuit modified (page 11 - figure 11)
DC measurement mode (DCS) modified (page 15 - table 6)
DC_INT mode figure modified (page 14 - figure 16. & page 15 - figure 17)

Jun 8, 2001 TESTOUT(#22) pin should be not connected (floating).
DC input buffer circuit is modified. (page 6 - figure 5)