

# 1Mb Ultra-Low Power Asynchronous CMOS SRAM

64K × 16 bit

## Overview

The N01L163WC2A is an integrated memory device containing a 1 Mbit Static Random Access Memory organized as 65,536 words by 16 bits. The device is designed and fabricated using NanoAmp's advanced CMOS technology to provide both high-speed performance and ultra-low power. The device operates with two chip enable ( $\overline{CE1}$  and  $\overline{CE2}$ ) controls and output enable ( $\overline{OE}$ ) to allow for easy memory expansion. Byte controls ( $\overline{UB}$  and  $\overline{LB}$ ) allow the upper and lower bytes to be accessed independently and can also be used to deselect the device. The N01L163WC2A is optimal for various applications where low-power is critical such as battery backup and hand-held devices. The device can operate over a very wide temperature range of -40°C to +85°C and is available in JEDEC standard packages compatible with other standard 64Kb x 16 SRAMs

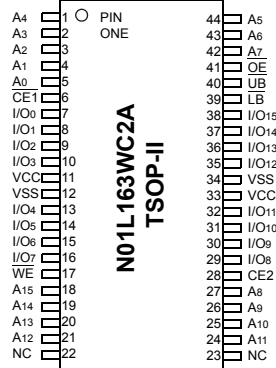
## Features

- **Single Wide Power Supply Range**  
2.3 to 3.6 Volts
- **Very low standby current**  
2.0µA at 3.0V (Typical)
- **Very low operating current**  
2.0mA at 3.0V and 1µs (Typical)
- **Very low Page Mode operating current**  
0.8mA at 3.0V and 1µs (Typical)
- **Simple memory control**  
Dual Chip Enables ( $\overline{CE1}$  and  $\overline{CE2}$ )  
Byte control for independent byte operation  
Output Enable ( $\overline{OE}$ ) for memory expansion
- **Low voltage data retention**  
 $V_{CC} = 1.8V$
- **Very fast output enable access time**  
30ns  $\overline{OE}$  access time
- **Automatic power down to standby mode**
- **TTL compatible three-state output driver**
- **Compact space saving BGA package available**

## Product Family

Part Number	Package Type	Operating Temperature	Power Supply (Vcc)	Speed	Standby Current ( $I_{SB}$ ), Typical	Operating Current ( $I_{CC}$ ), Typical
N01L163WC2AB	48 - BGA	-40°C to +85°C	2.3V - 3.6V	55ns @ 2.7V 70ns @ 2.3V	2 µA	2 mA @ 1MHz
N01L163WC2AT	44 - TSOP II					
N01L163WC2AB1	48 - BGA Pb-Free					
N01L163WC2AT2	44 - TSOP II Green					

### Pin Configuration



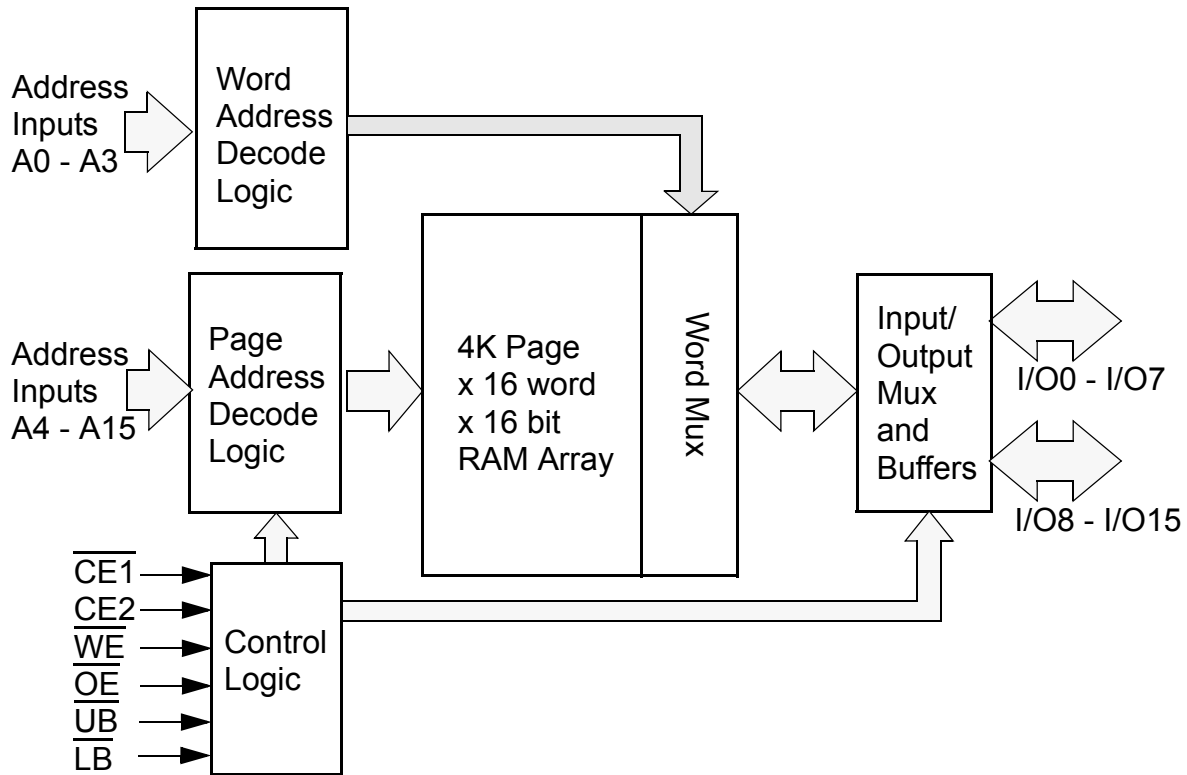
	1	2	3	4	5	6
A	$\overline{\text{LB}}$	$\overline{\text{OE}}$	A <sub>0</sub>	A <sub>1</sub>	A <sub>2</sub>	CE2
B	I/O <sub>8</sub>	$\overline{\text{UB}}$	A <sub>3</sub>	A <sub>4</sub>	$\overline{\text{CE1}}$	I/O <sub>0</sub>
C	I/O <sub>9</sub>	I/O <sub>10</sub>	A <sub>5</sub>	A <sub>6</sub>	I/O <sub>1</sub>	I/O <sub>2</sub>
D	V <sub>SS</sub>	I/O <sub>11</sub>	NC	A <sub>7</sub>	I/O <sub>3</sub>	V <sub>CC</sub>
E	V <sub>CC</sub>	I/O <sub>12</sub>	NC	NC	I/O <sub>4</sub>	V <sub>SS</sub>
F	I/O <sub>14</sub>	I/O <sub>13</sub>	A <sub>14</sub>	A <sub>15</sub>	I/O <sub>5</sub>	I/O <sub>6</sub>
G	I/O <sub>15</sub>	NC	A <sub>12</sub>	A <sub>13</sub>	$\overline{\text{WE}}$	I/O <sub>7</sub>
H	NC	A <sub>8</sub>	A <sub>9</sub>	A <sub>10</sub>	A <sub>11</sub>	NC

48 Pin BGA (top)  
6 x 8 mm

### Pin Descriptions

Pin Name	Pin Function
A <sub>0</sub> -A <sub>15</sub>	Address Inputs
$\overline{\text{WE}}$	Write Enable Input
$\overline{\text{CE1}}$ , CE2	Chip Enable Input
$\overline{\text{OE}}$	Output Enable Input
$\overline{\text{LB}}$	Lower Byte Enable Input
$\overline{\text{UB}}$	Upper Byte Enable Input
I/O <sub>0</sub> -I/O <sub>15</sub>	Data Inputs/Outputs
V <sub>CC</sub>	Power
V <sub>SS</sub>	Ground
NC	Not Connected

**Functional Block Diagram**



**Functional Description**

$\overline{CE1}$	$\overline{CE2}$	$\overline{WE}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	I/O <sub>0</sub> - I/O <sub>15</sub> <sup>1</sup>	MODE	POWER
H	X	X	X	X	X	High Z	Standby <sup>2</sup>	Standby
X	L	X	X	X	X	High Z	Standby <sup>2</sup>	Standby
L	H	X	X	H	H	High Z	Standby	Standby
L	H	L	X <sup>3</sup>	L <sup>1</sup>	L <sup>1</sup>	Data In	Write <sup>3</sup>	Active
L	H	H	L	L <sup>1</sup>	L <sup>1</sup>	Data Out	Read	Active
L	H	H	H	L <sup>1</sup>	L <sup>1</sup>	High Z	Active	Active

1. When  $\overline{UB}$  and  $\overline{LB}$  are in select mode (low), I/O<sub>0</sub> - I/O<sub>15</sub> are affected as shown. When  $\overline{LB}$  only is in the select mode only I/O<sub>0</sub> - I/O<sub>7</sub> are affected as shown. When  $\overline{UB}$  is in the select mode only I/O<sub>8</sub> - I/O<sub>15</sub> are affected as shown.

2. When the device is in standby mode, control inputs ( $\overline{WE}$ ,  $\overline{OE}$ ,  $\overline{UB}$ , and  $\overline{LB}$ ), address inputs and data input/outputs are internally isolated from any external influence and disabled from exerting any influence externally.

3. When  $\overline{WE}$  is invoked, the  $\overline{OE}$  input is internally disabled and has no effect on the circuit.

**Capacitance<sup>1</sup>**

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0V, f = 1 MHz, T <sub>A</sub> = 25°C		8	pF
I/O Capacitance	C <sub>I/O</sub>	V <sub>IN</sub> = 0V, f = 1 MHz, T <sub>A</sub> = 25°C		8	pF

1. These parameters are verified in device characterization and are not 100% tested

**Absolute Maximum Ratings<sup>1</sup>**

Item	Symbol	Rating	Unit
Voltage on any pin relative to $V_{SS}$	$V_{IN,OUT}$	-0.3 to $V_{CC}+0.3$	V
Voltage on $V_{CC}$ Supply Relative to $V_{SS}$	$V_{CC}$	-0.3 to 4.5	V
Power Dissipation	$P_D$	500	mW
Storage Temperature	$T_{STG}$	-40 to 125	°C
Operating Temperature	$T_A$	-40 to +85	°C
Soldering Temperature and Time	$T_{SOLDER}$	260°C, 10sec	°C

1. Stresses greater than those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Operating Characteristics (Over Specified Temperature Range)**

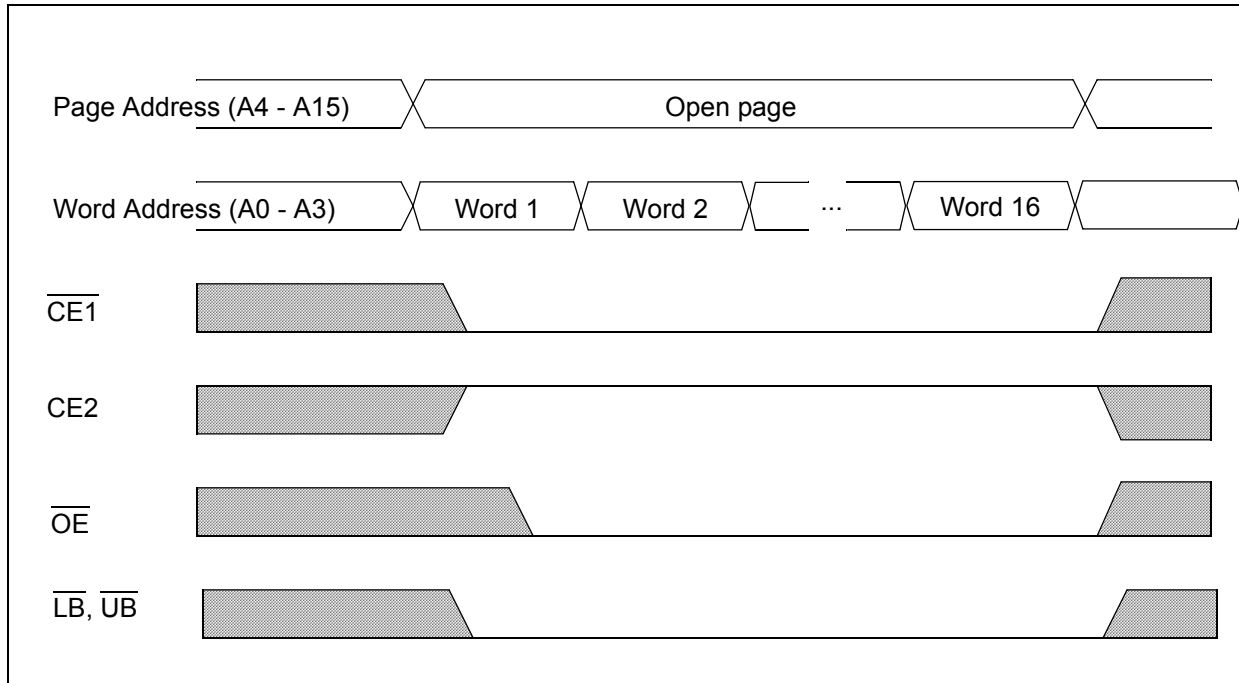
Item	Symbol	Test Conditions	Min.	Typ <sup>1</sup>	Max	Unit
Supply Voltage	$V_{CC}$		2.3	3.0	3.6	V
Data Retention Voltage	$V_{DR}$	Chip Disabled <sup>3</sup>	1.8			V
Input High Voltage	$V_{IH}$		1.8		$V_{CC}+0.3$	V
Input Low Voltage	$V_{IL}$		-0.3		0.6	V
Output High Voltage	$V_{OH}$	$I_{OH} = 0.2mA$	$V_{CC}-0.2$			V
Output Low Voltage	$V_{OL}$	$I_{OL} = -0.2mA$			0.2	V
Input Leakage Current	$I_{LI}$	$V_{IN} = 0$ to $V_{CC}$			0.5	μA
Output Leakage Current	$I_{LO}$	$\overline{OE} = V_{IH}$ or Chip Disabled			0.5	μA
Read/Write Operating Supply Current @ 1 μs Cycle Time <sup>2</sup>	$I_{CC1}$	$V_{CC}=3.6V$ , $V_{IN}=V_{IH}$ or $V_{IL}$ Chip Enabled, $I_{OUT} = 0$		2.0	3.0	mA
Read/Write Operating Supply Current @ 70 ns Cycle Time <sup>2</sup>	$I_{CC2}$	$V_{CC}=3.6V$ , $V_{IN}=V_{IH}$ or $V_{IL}$ Chip Enabled, $I_{OUT} = 0$		9.5	14.0	mA
Page Mode Operating Supply Current @ 70ns Cycle Time <sup>2</sup> (Refer to Power Savings with Page Mode Operation diagram)	$I_{CC3}$	$V_{CC}=3.6V$ , $V_{IN}=V_{IH}$ or $V_{IL}$ Chip Enabled, $I_{OUT} = 0$		4		mA
Read/Write Quiescent Operating Supply Current <sup>3</sup>	$I_{CC4}$	$V_{CC}=3.6V$ , $V_{IN}=V_{IH}$ or $V_{IL}$ Chip Enabled, $I_{OUT} = 0$ , $f = 0$			3.0	mA
Maximum Standby Current <sup>3</sup>	$I_{SB1}$	$V_{IN} = V_{CC}$ or 0V Chip Disabled $t_A = 85^\circ C$ , $V_{CC} = 3.6V$		2.0	20	μA
Maximum Data Retention Current <sup>3</sup>	$I_{DR}$	$V_{CC} = 1.8V$ , $V_{IN} = V_{CC}$ or 0 Chip Disabled, $t_A = 85^\circ C$			10	μA

1. Typical values are measured at  $V_{CC}=V_{CC}$  Typ.,  $T_A=25^\circ C$  and not 100% tested.

2. This parameter is specified with the outputs disabled to avoid external loading effects. The user must add current required to drive output capacitance expected in the actual system.

3. This device assumes a standby mode if the chip is disabled ( $\overline{CE1}$  high or  $CE2$  low). In order to achieve low standby current all inputs must be within 0.2 volts of either  $V_{CC}$  or  $V_{SS}$

**Power Savings with Page Mode Operation ( $\overline{WE} = V_{IH}$ )**



Note: Page mode operation is a method of addressing the SRAM to save operating current. The internal organization of the SRAM is optimized to allow this unique operating mode to be used as a valuable power saving feature.

The only thing that needs to be done is to address the SRAM in a manner that the internal page is left open and 16-bit words of data are read from the open page. By treating addresses A0-A3 as the least significant bits and addressing the 16 words within the open page, power is reduced to the page mode value which is considerably lower than standard operating currents for low power SRAMs.

**Timing Test Conditions**

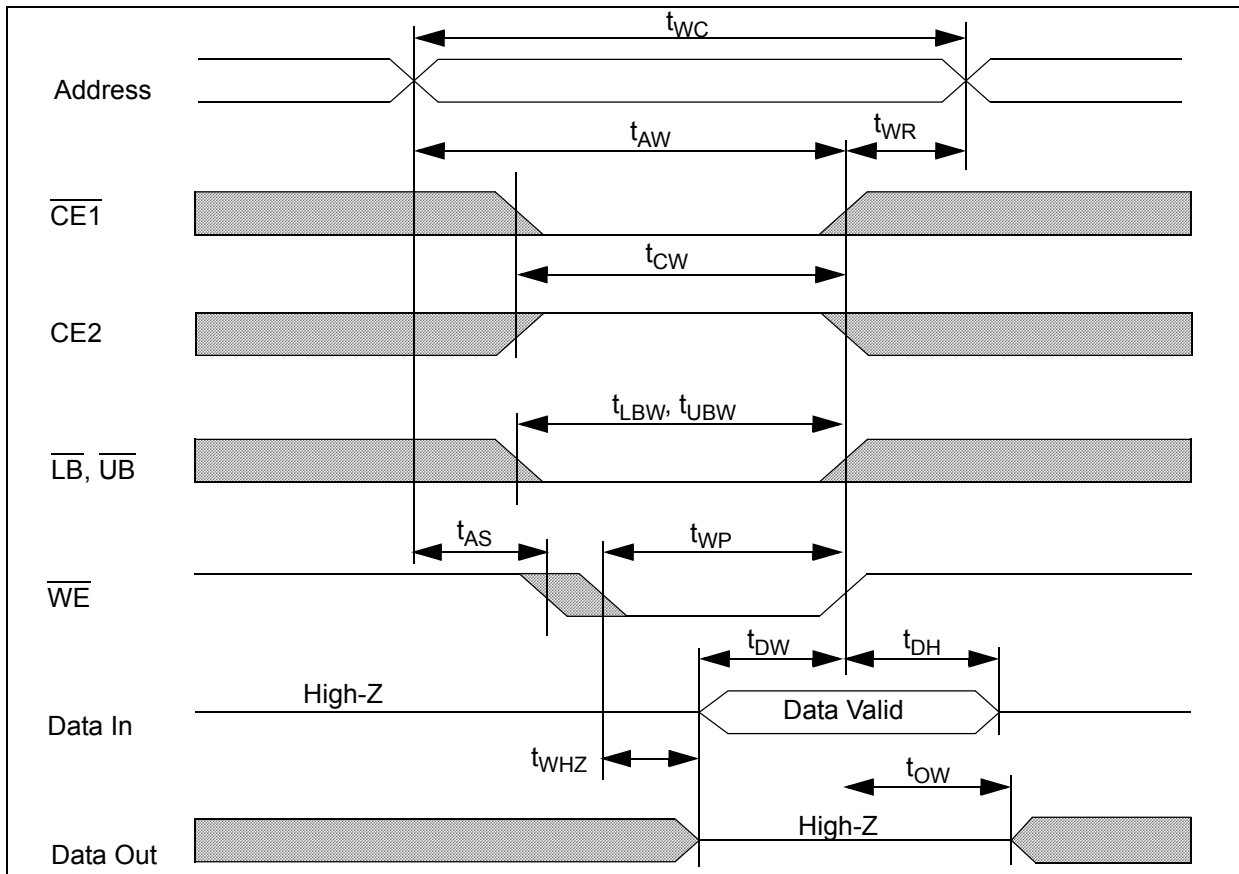
Item	
Input Pulse Level	0.1V <sub>CC</sub> to 0.9 V <sub>CC</sub>
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	0.5 V <sub>CC</sub>
Output Load	CL = 30pF
Operating Temperature	-40 to +85 °C

**Timing**

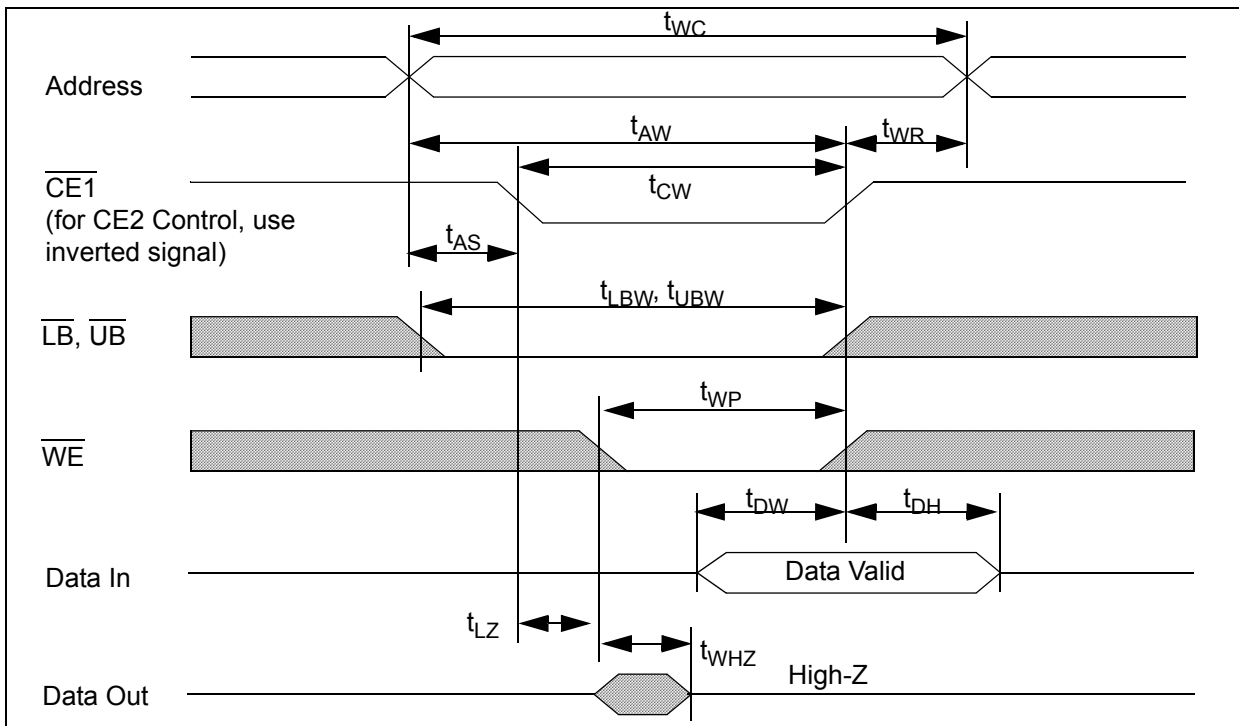
Item	Symbol	2.3 - 3.6 V		2.7 - 3.6 V		Units
		Min.	Max.	Min.	Max.	
Read Cycle Time	t <sub>RC</sub>	70		55		ns
Address Access Time	t <sub>AA</sub>		70		55	ns
Chip Enable to Valid Output	t <sub>CO</sub>		70		55	ns
Output Enable to Valid Output	t <sub>OE</sub>		35		30	ns
Byte Select to Valid Output	t <sub>LB</sub> , t <sub>UB</sub>		70		55	ns
Chip Enable to Low-Z output	t <sub>LZ</sub>	10		10		ns
Output Enable to Low-Z Output	t <sub>OLZ</sub>	5		5		ns
Byte Select to Low-Z Output	t <sub>LBZ</sub> , t <sub>UBZ</sub>	10		10		ns
Chip Disable to High-Z Output	t <sub>HZ</sub>	0	20	0	20	ns
Output Disable to High-Z Output	t <sub>OHZ</sub>	0	20	0	20	ns
Byte Select Disable to High-Z Output	t <sub>LBHZ</sub> , t <sub>UBHZ</sub>	0	20	0	20	ns
Output Hold from Address Change	t <sub>OH</sub>	10		10		ns
Write Cycle Time	t <sub>WC</sub>	70		55		ns
Chip Enable to End of Write	t <sub>CW</sub>	50		40		ns
Address Valid to End of Write	t <sub>AW</sub>	50		40		ns
Byte Select to End of Write	t <sub>LBW</sub> , t <sub>UBW</sub>	50		40		ns
Write Pulse Width	t <sub>WP</sub>	40		40		ns
Address Setup Time	t <sub>AS</sub>	0		0		ns
Write Recovery Time	t <sub>WR</sub>	0		0		ns
Write to High-Z Output	t <sub>WHZ</sub>		20		20	ns
Data to Write Time Overlap	t <sub>DW</sub>	40		35		ns
Data Hold from Write Time	t <sub>DH</sub>	0		0		ns
End Write to Low-Z Output	t <sub>OW</sub>	5		10		ns



**Timing Waveform of Write Cycle ( $\overline{WE}$  control)**

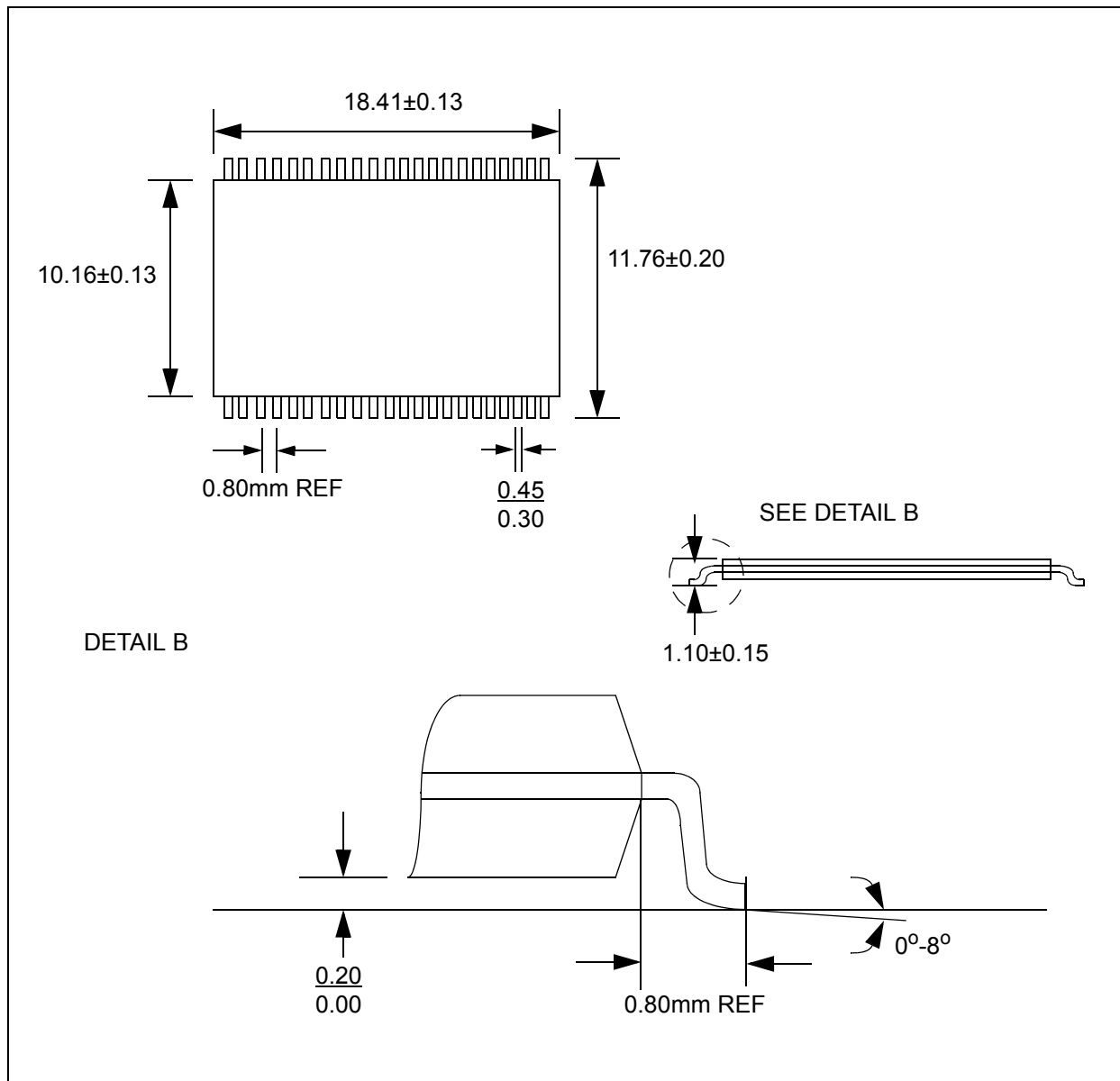


**Timing Waveform of Write Cycle ( $\overline{CE1}$  Control)**





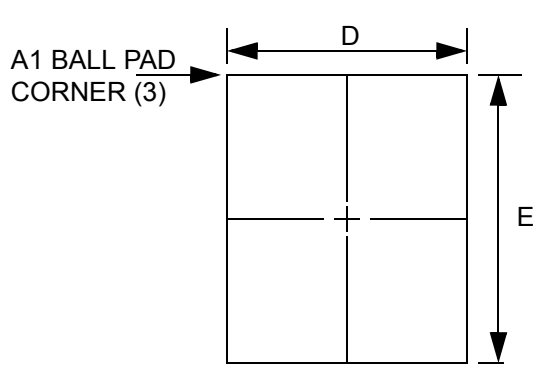
**44-Lead TSOP II Package (T44)**



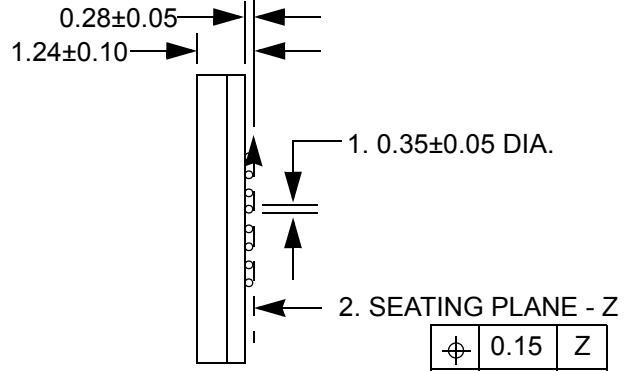
Note:

1. All dimensions in inches (Millimeters)
2. Package dimensions exclude molding flash

**Ball Grid Array Package**

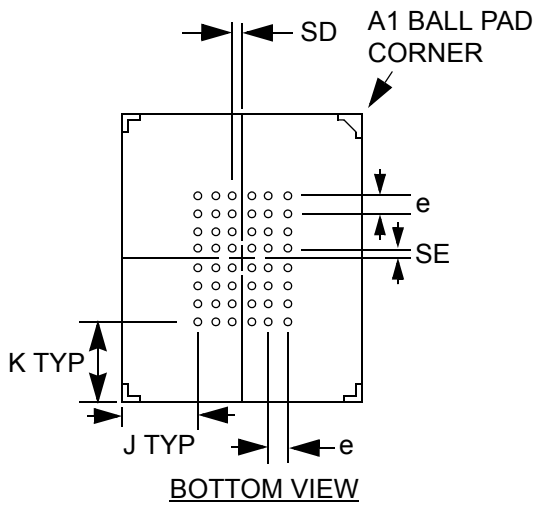


TOP VIEW



SIDE VIEW

⌀	0.15	Z
⌀	0.05	Z



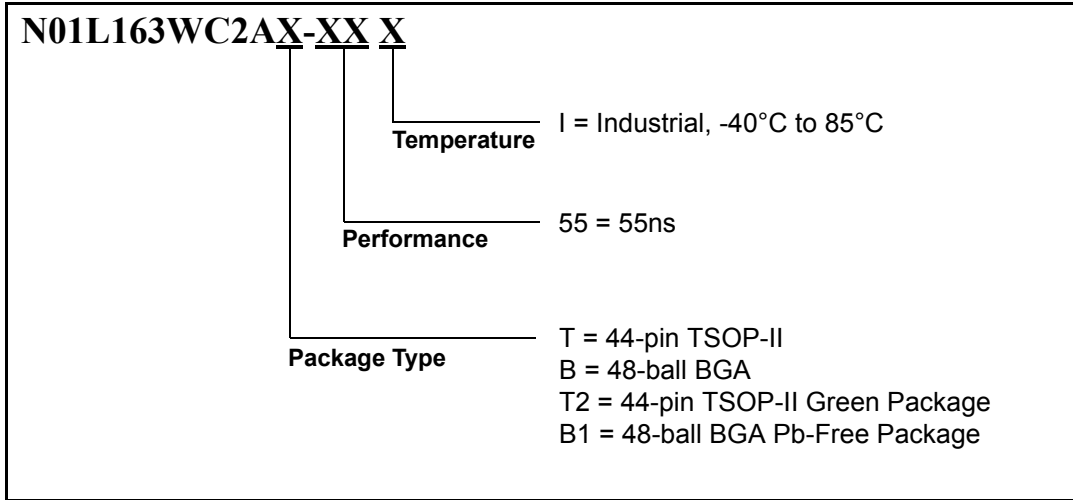
BOTTOM VIEW

1. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER. PARALLEL TO PRIMARY Z.
2. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. A1 BALL PAD CORNER I.D. TO BE MARKED BY INK.

**Dimensions (mm)**

D	E	e = 0.75				BALL MATRIX TYPE
		SD	SE	J	K	
6±0.10	8±0.10	0.375	0.375	1.125	1.375	FULL

**Ordering Information**



**Revision History**

Revision	Date	Change Description
A	Jan 2001	Initial preliminary release
B	Mar 2001	Corrected Figure 1: TSOP Pin Configuration, pins 18-22. Modified I <sub>CC3</sub> , figure 8, other minor edits
C	April 2001	Modified timing table, changed access time to 55 ns
D	Dec. 2001	Part number change from EM064J16, modified Overview and Features, Added Page Mode Operation diagram, revised Operating Characteristics table, Functional Description table and Ordering Information diagram
E	Nov. 2002	Replaced Isb and Icc on Product Family table with typical values
F	Oct. 2004	Added Pb-Free and Green Package Option

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