MC145403
MC145404
MC145405
MC145408

Drivers/Receivers
EIA–232–E and CCITT V.28

These devices are silicon gate CMOS ICs that combine both the transmitter and receiver to fulfill the electrical specifications of EIA Standard 232–E and CCITT V.28. The drivers feature true TTL input compatibility, slew rate limiting outputs, 300 Ω power–off source impedance, and output typically switching to within 25% of the supply rails. The receivers can handle up to ± 25 V while presenting 3 to 7 kΩ impedance. Hysteresis in the receivers aid in the reception of noisy signals. By combining both drivers and receivers in a single CMOS chip, these devices provide efficient, low–power solutions for both EIA–232–E and V.28 applications.

These devices offer the following performance features:

Drivers

- ± 5 to ± 12 V Supply Range
- 300 Ω Power–Off Source Impedance
- Output Current Limiting
- TTL and CMOS Compatible Inputs
- Driver Slew Rate Range Limited to 30 V/μs Maximum

Receivers

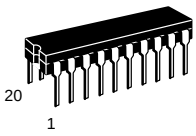
- ± 25 V Input Range
- 3 to 7 kΩ Input Impedance
- 0.8 V of Hysteresis for Enhanced Noise Immunity
- TTL and CMOS Compatible Outputs

Available Driver/Receiver Combinations

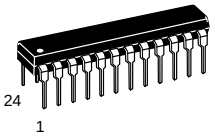
Device	Drivers	Receivers	Figure	No. of Pins
MC145403	3	5	1	20
MC145404	4	4	2	20
MC145405	5	3	3	20
MC145408	5	5	4	24

Alternative EIA–232 devices to consider are:

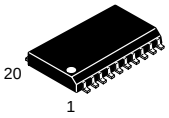
Three Supply	Single Supply
MC145406 (3 x 3)	MC145407 (3 x 3)
	MC145705 (2 x 3) with Power Down
	MC145706 (3 x 2) with Power Down
	MC145707 (3 x 3) with Power Down



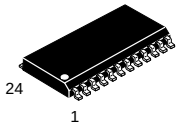
P SUFFIX
PLASTIC DIP
CASE 738



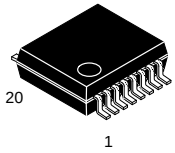
P SUFFIX
PLASTIC DIP
CASE 724



DW SUFFIX
SOG PACKAGE
CASE 751D



DW SUFFIX
SOG PACKAGE
CASE 751E



SD SUFFIX
SSOP
CASE 940B

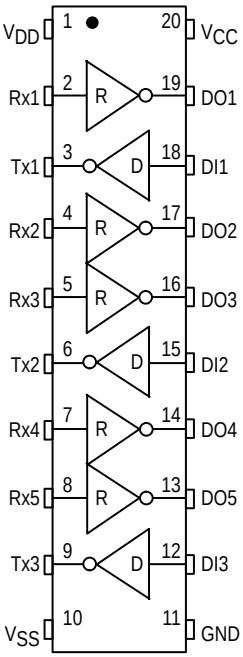
ORDERING INFORMATION

MC145403P	Plastic DIP
MC145404P	Plastic DIP
MC145405P	Plastic DIP
MC145408P	Plastic DIP
MC145403DW	SOG Package
MC145404DW	SOG Package
MC145405DW	SOG Package
MC145408DW	SOG Package
MC145405SD	SSOP

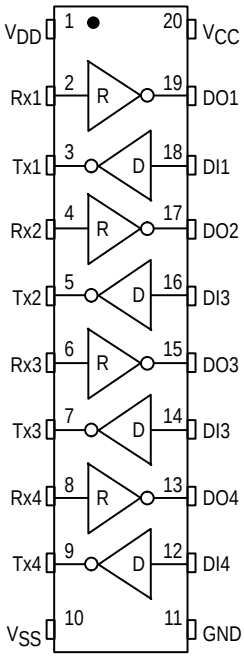
REV 2
1/97 TN97010600

PIN ASSIGNMENTS
(DIP, SOG, AND SSOP)

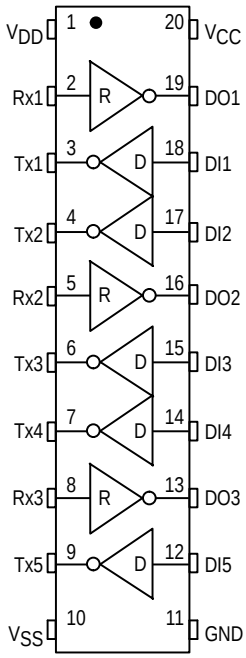
MC145403
3 DRIVERS/5 RECEIVERS



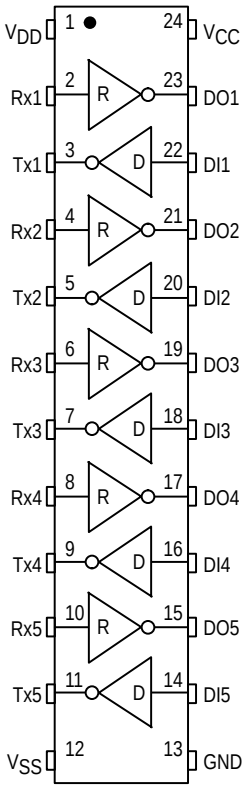
MC145404
4 DRIVERS/4 RECEIVERS



MC145405
5 DRIVERS/3 RECEIVERS

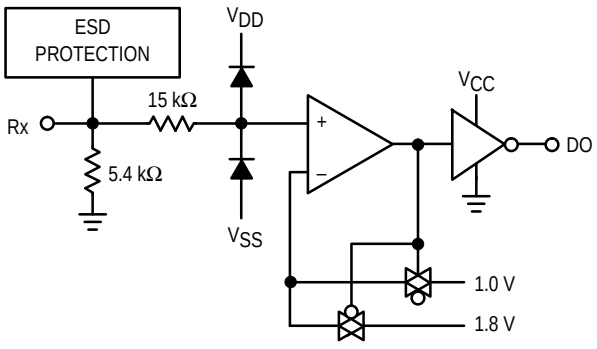


MC145408
5 DRIVERS/5 RECEIVERS

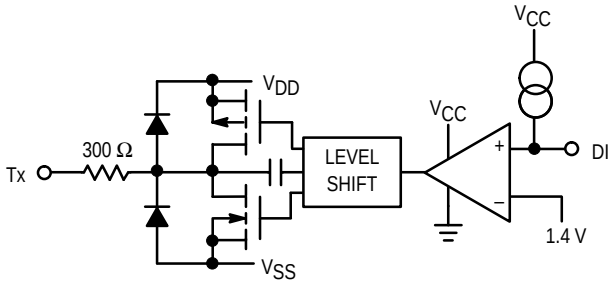


FUNCTIONAL DIAGRAM

RECEIVER



DRIVER



ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND, except where noted)

Rating	Symbol	Value	Unit
DC Supply Voltage ($V_{DD} \geq V_{CC}$)	V_{DD} V_{SS} V_{CC}	– 0.5 to + 13.5 + 0.5 to – 13.5 – 0.5 to + 6.0	V
Input Voltage Range Rx1 – Rx*n* DI1 – DI*n*	V_{IR}	 V_{SS} – 15 to V_{DD} + 15 0.5 to V_{CC} + 15	V
DC Current Drain per Pin	I	± 00	mA
Power Dissipation	P_D	1	W
Operating Temperature Range	T_A	– 40 to + 85	°C
Storage Temperature Range	T_{stg}	– 85 to + 150	°C

This device contains circuitry to protect the inputs and outputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit.

For proper operation it is recommended that V_{out} and V_{in} be constrained to the ranges described as follows:

Digital I/O: Driver Inputs (DI):
($GND \leq V_{DI} \leq V_{CC}$).

Receiver Outputs (DO):
($GND \leq V_{DO} \leq V_{CC}$).

EIA–232 I/O: Driver Outputs (Tx):
($V_{SS} \leq V_{Tx1 - Tx\mathit{n}} \leq V_{DD}$).

Receiver Inputs (Rx):
V_{SS} – 15 V ≤ $V_{Rx1 - Rx\mathit{n}} \leq V_{DD}$ + 15 V).

Reliability of operation is enhanced if unused outputs are tied off to an appropriate logic voltage level (e.g., either GND or V_{CC} for DI, and GND for Rx).

DC ELECTRICAL CHARACTERISTICS (All polarities referenced to GND = 0 V, T_A = – 40 to + 85°C)

Parameter		Symbol	Min	Typ	Max	Unit
DC Supply Voltage		V_{DD} V_{SS} V_{CC}	4.5 – 4.5 4.5	5 to 12 – 5 to – 12 5	13.2 – 13.2 5.5	V
Quiescent Supply Current (Outputs Unloaded, Inputs Low)	V_{DD} = + 12 V V_{SS} = – 12 V V_{CC} = + 5 V	I_{DD} I_{SS} I_{CC}	— — —	425 – 400 110	635 – 600 200	µA

RECEIVER ELECTRICAL SPECIFICATIONS

(Voltage polarities referenced to GND = 0 V, V_{DD} = + 12 V, V_{SS} = – 12 V, T_A = – 40 to + 85°C, V_{CC} = + 5 V, ± 10%)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Turn–On Threshold $V_{DO} = V_{OL}$	Rx1 – Rx*n*	V_{on}	1.35	1.8	2.35	V
Input Turn–Off Threshold $V_{DO} = V_{OH}$	Rx1 – Rx*n*	V_{off}	0.75	1	1.25	V
Input Threshold Hysteresis $\Delta = V_{on} - V_{off}$		V_{hys}	0.6	0.8	—	V
Input Resistance (V_{SS} – 15 V) ≤ V Rx1 – Rx*n* ≤ (V_{DD} + 15 V)		R_{in}	3	5.4	7	kΩ
High Level Output Voltage V_{Rx} = – 3 to – 25 V* (DO1 – DO*n*)	I_{out} = – 20 µA I_{out} = – 1.0 mA	V_{OH}	4.9 3.8	4.9 4.3	— —	V
Low Level Output Voltage V_{Rx} = + 3 to + 25 V* (DO1 – DO*n*)	I_{out} = + 2 mA I_{out} = + 4 mA	V_{OL}	— —	0.02 0.5	0.5 0.7	V

* This is the range of input voltages as specified by EIA–232–E to cause a receiver to be in the high or low.

DRIVER ELECTRICAL SPECIFICATIONS

(Voltage Polarities Referenced to GND = 0 V, V_{DD} = + 12 V, V_{SS} = – 12 V, T_A = – 40 to + 85°C, V_{CC} = + 5 V, ± 10%)

Characteristic		Symbol	Min	Typ	Max	Unit
Digital Input Voltage	DI1 – DI*n*					V
Logic 0		V_{IL}	—	—	0.8	
Logic 1		V_{IH}	2	—	—	
Input Current	DI1 – DI*n*					μA
V_{DI} = GND		I_{IL}	—	7	—	
V_{DI} = V_{CC}		I_{IH}	—	—	± 1.0	
Output High Voltage	Tx1 – Tx*n*	V_{OH}				V
V_{DI} = Logic 0, R_L = 3 kΩ						
V_{DD} = + 5.0 V, V_{SS} = – 5.0 V			3.5	3.9	—	
V_{DD} = + 6.0 V, V_{SS} = – 6.0 V			4.3	4.7	—	
V_{DD} = + 12.0 V, V_{SS} = – 12.0 V			9.2	9.5	—	
Output Low Voltage*	Tx1 – Tx*n*	V_{OL}				V
V_{DI} = Logic 1, R_L = 3 kΩ						
V_{DD} = + 5.0 V, V_{SS} = – 5.0 V			– 4	– 4.3	—	
V_{DD} = + 6.0 V, V_{SS} = – 6.0 V			– 4.5	– 5.2	—	
V_{DD} = + 12.0 V, V_{SS} = – 12.0 V			– 10	– 10.3	—	
Input Current (Figure 5)	Tx1 – Tx*n*	Z_{off}	300	—	—	Ω
Output Short Circuit Current	Tx1 – Tx*n*	I_{SC}				mA
V_{DD} = + 12 V, V_{SS} = – 12 V						
Tx Shorted to GND**			—	± 22	± 60	
Tx Shorted to ± 15 V***			—	± 60	± 100	

* Voltage specifications are in terms of absolute values.

** Specification is for one Tx output pin to be shorted at a time. Should all three driver outputs be shorted simultaneously, device power dissipation limits will be exceeded.

*** This condition could exceed package limitations.

SWITCHING CHARACTERISTICS (V_{CC} = + 5 V, ± 10%, V_{DD} = + 12 V, V_{SS} = – 12 V, T_A = – 40 to + 85°C; See Figures 2 and 3)

Characteristic	Symbol	Min	Typ	Max	Unit
Drivers					
Propagation Delay Time Tx	t_{PLH}				ns
Low–to–High					
R_L = 3 kΩ, C_L = 50 pF		—	500	1000	
High–to–Low	t_{PHL}				
R_L = 3 kΩ, C_L = 50 pF		—	700	1000	
Output Slew Rate	SR				V/μs
Minimum Load					
R_L = 7 kΩ, C_L = 0 pF (V_{DD} = 6 to 12 V, V_{SS} = – 6 to – 12 V)		—	± 6	± 30	
Maximum Load					
R_L = 3 kΩ, C_L = 2500 pF (V_{DD} = 12 V, V_{SS} = – 12 V, V_{CC} = 5 V)		4	—	—	
Receivers (C_L = 50 pF)					
Propagation Delay Time	t_{PLH}				ns
Low–to–High		—	360	610	
High–to–Low	t_{PHL}	—	130	610	
Output Rise Time	t_r	—	250	400	ns
Output Fall Time	t_f	—	40	100	ns

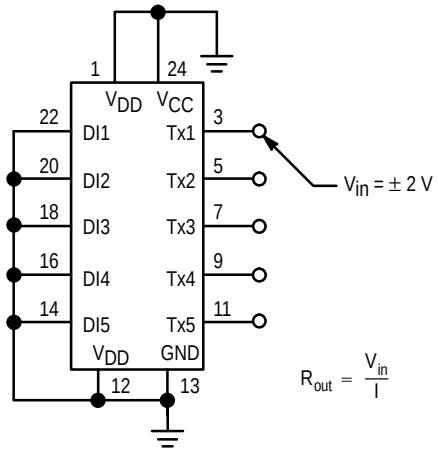


Figure 1. Power–Off Source Resistance Illustrated for MC145408

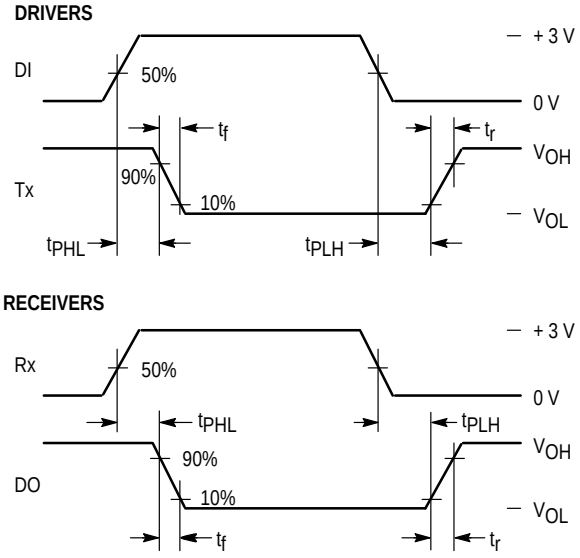


Figure 2. Switching Characteristics

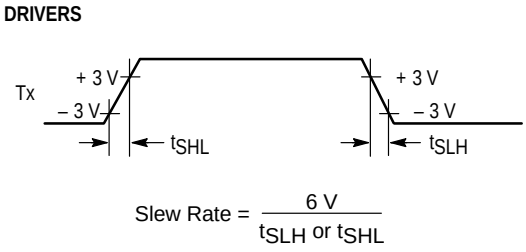


Figure 3. Slew Rate Characteristics

PIN DESCRIPTIONS

V_{CC}
Digital Power Supply

The digital supply pin, which is connected to the logic power supply (+ 5.5 V maximum).

GND
Ground

Ground return pin is typically connected to the signal ground pin of the EIA–232–E connector (Pin 7) as well as to the logic power supply ground.

V_{DD}
Most Positive Device Pin

The most positive power supply pin, which is typically + 5 to + 12 V.

V_{SS}
Most Negative Device Pin

The most negative power supply pin, which is typically – 5 to – 12 V.

Rx1 – Rx*n*
Receive Data Input Pins

These are the EIA–232–E receive signal inputs. A voltage between + 3 and + 25 V is decoded as a space, and causes the corresponding DO pin to swing to ground (0 V). A voltage between – 3 and – 25 V is decoded as a mark, and causes the corresponding DO pin to swing to V_{CC}.

DO1 – DO*n*
Data Output Pins

These are the receiver digital output pins which swing from V_{CC} to GND. Each output pin is capable of driving one LSTTL input load.

DI1 – DI*n*
Data Input Pins

These are the high impedance digital input pins to the drivers. Input voltage levels on these pins are LSTTL compatible and must be between V_{CC} and GND. A weak pull–up on each input sets all unused DI pins to V_{CC}, causing the corresponding unused driver outputs to be at V_{SS}.

Tx1 – TX*n*
Transmit Data Output Pins

These are the EIA–232–E transmit signal output pins, which swing from V_{DD} to V_{SS}. A logic 1 at the DI input causes the corresponding Tx output to swing to V_{SS}. A logic 0 at the DI input causes the corresponding Tx out to swing to V_{DD}. The actual levels and slew rate achieved will depend on the output loading ($R_L \parallel C_L$).

APPLICATION INFORMATION

POWER SUPPLY CONSIDERATIONS

Figure 4 shows a technique to guard against excessive device current.

The diode D1 prevents excessive current from flowing through an internal diode from the V_{CC} pin to the V_{DD} pin when $V_{DD} < V_{CC}$ by approximately 0.6 V or greater. This high current condition can exist for a short period of time during power up/down. Additionally, if the + 12 V supply is switched off while the + 5 V is on and the off supply is a low impedance to ground, the diode D1 will prevent current flow through the internal diode.

The diode D2 is used as a voltage clamp, to prevent V_{SS} from drifting positive to V_{CC}, in the event that power is removed from V_{SS} (Pin 12). If V_{SS} power is removed, and the impedance from the V_{SS} pin to ground is greater than approximately 3 kΩ, this pin will be pulled to V_{CC} by internal circuitry causing excessive current in the V_{CC} pin.

If by design, neither of the above conditions are allowed to exist, then the diodes D1 and D2 are not required.

ESD PROTECTION

ESD protection on IC devices that have their pins accessible to the outside world is essential. High static voltages applied to the pins when someone touches them either directly or indirectly can cause damage to gate oxides and transistor junctions by coupling a portion of the energy from the I/O pin to the power supply buses of the IC. This coupling will usually occur through the internal ESD protection diodes. The key to protecting the IC is to shunt as much of the energy to ground as possible before it enters the IC. Figure 4 shows a technique which will clamp the ESD voltage at approximately ± 15 V using the MMBZ15VDLT1. Any residual voltage which appears on the supply pins is shunted to ground through the capacitors C1 – C3. This scheme has provided protection to the interface part up to ± 10 kV, using the human body model test.

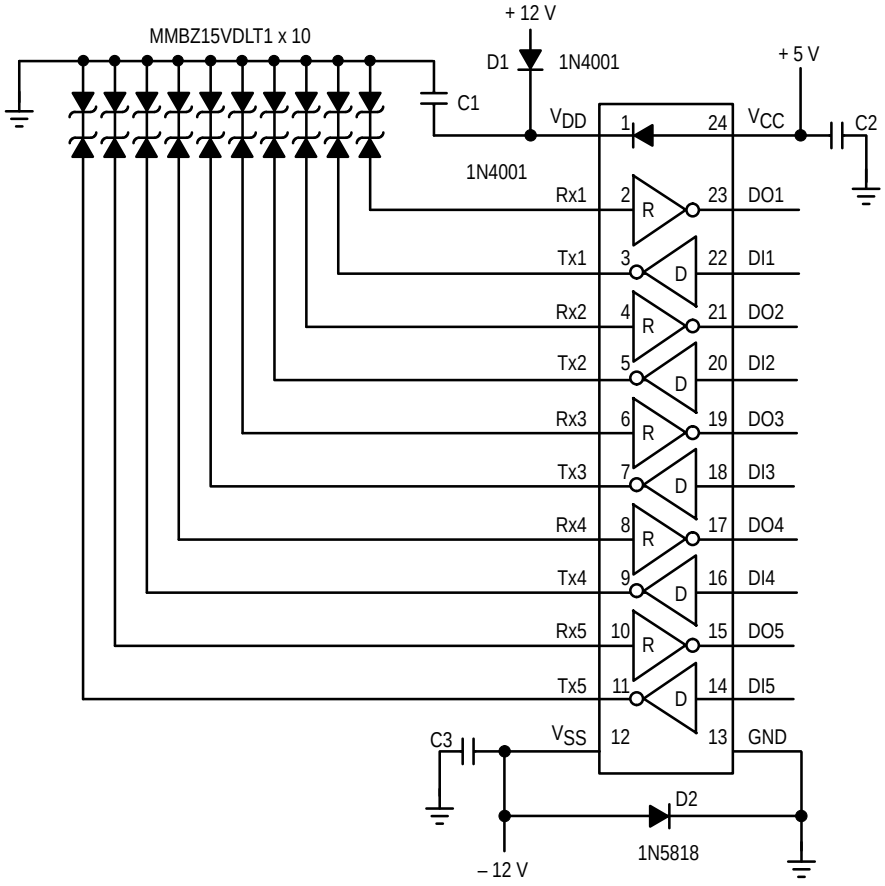
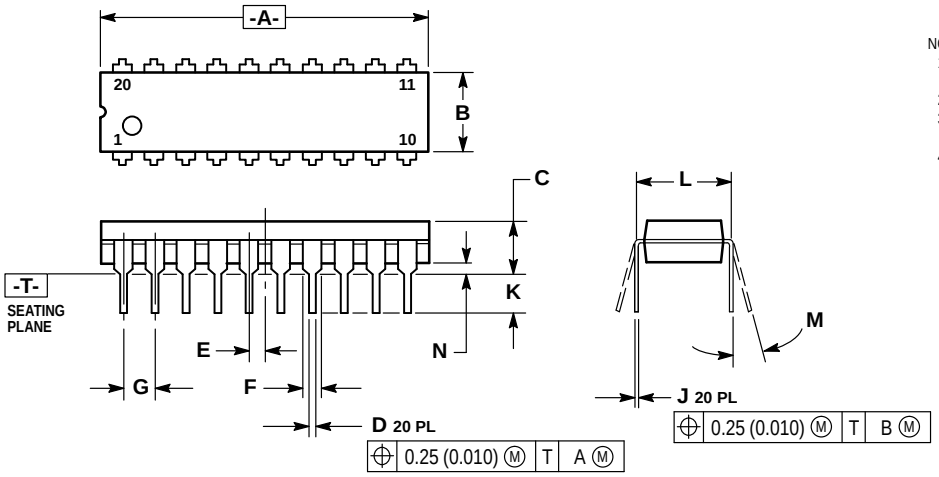


Figure 4.

PACKAGE DIMENSIONS

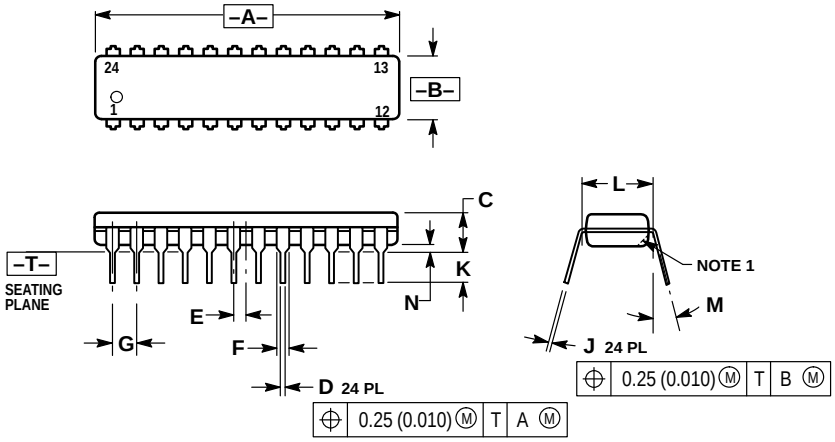
P SUFFIX
PLASTIC DIP
CASE 738–03



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

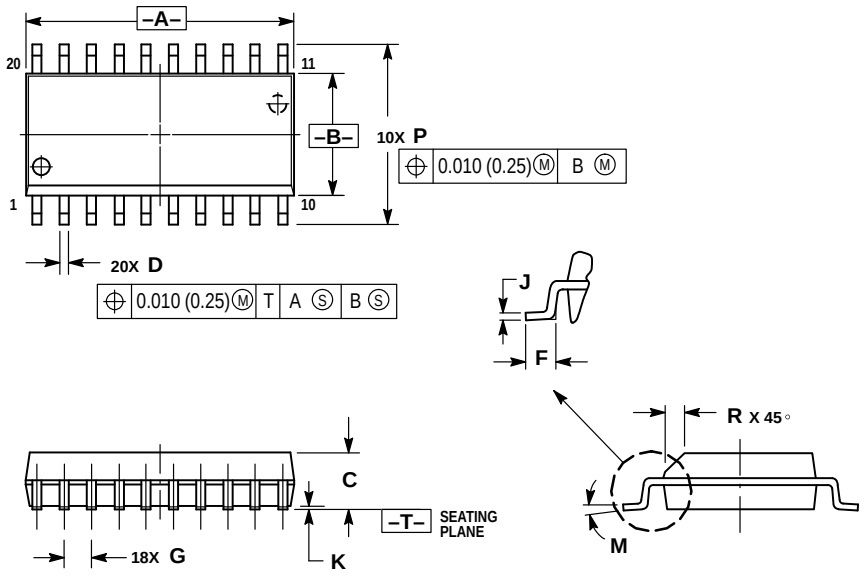
P SUFFIX
PLASTIC DIP
CASE 724–03



NOTES:
1. CHAMFERED CONTOUR OPTIONAL.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.230	1.265	31.25	32.13
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.020	0.38	0.51
E	0.050 BSC		1.27 BSC	
F	0.040	0.060	1.02	1.52
G	0.100 BSC		2.54 BSC	
J	0.007	0.012	0.18	0.30
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

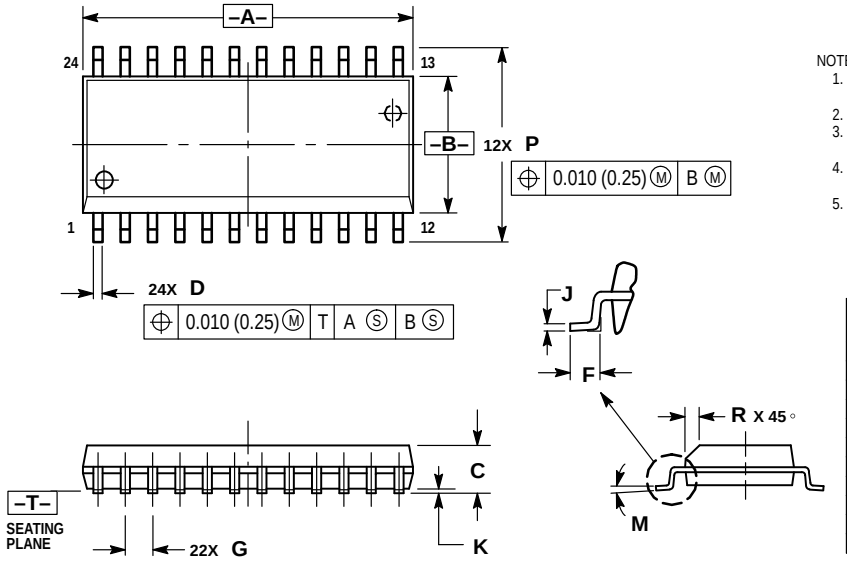
DW SUFFIX
SOG PACKAGE
CASE 751D–04



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

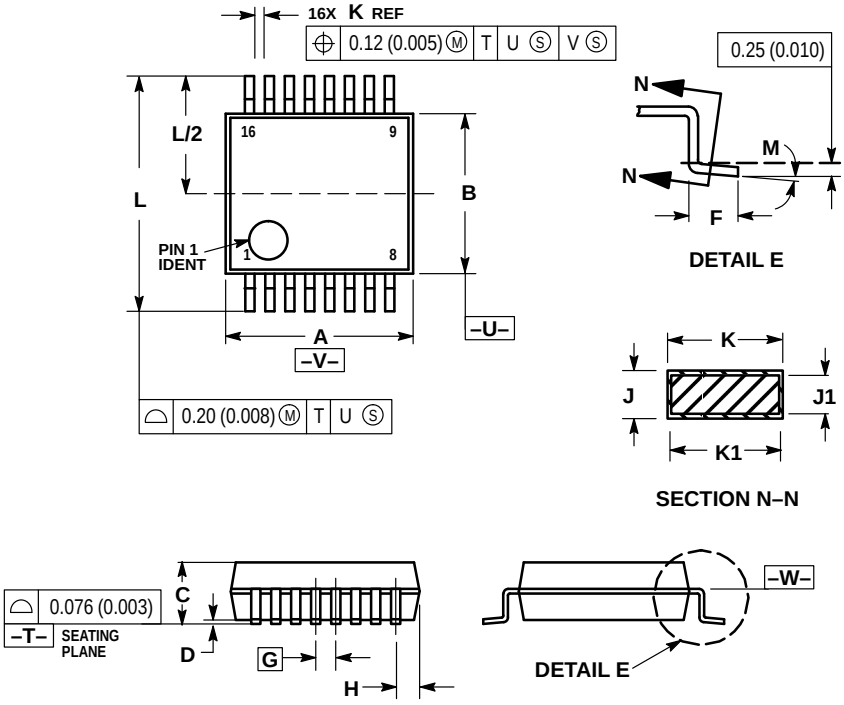
DW SUFFIX
SOG PACKAGE
CASE 751E–04



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

SD SUFFIX
SSOP
CASE 940B–03



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF K DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION K BY MORE THAN 0.07 (0.002) AT LEAST MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.07	6.33	0.238	0.249
B	5.20	5.38	0.205	0.212
C	1.73	1.99	0.068	0.078
D	0.05	0.21	0.002	0.008
F	0.63	0.95	0.024	0.037
G	0.65 BSC		0.026 BSC	
H	0.73	0.90	0.028	0.035
J	0.09	0.20	0.003	0.008
J1	0.09	0.16	0.003	0.006
K	0.25	0.38	0.010	0.015
K1	0.25	0.33	0.010	0.013
L	7.65	7.90	0.301	0.311
M	0 °	8 °	0°	8°

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