

## Features

- ESD Protect for 2 high-speed I/O channels
- Provide ESD protection for each channel to IEC 61000-4-2 (ESD)  $\pm 18\text{kV}$  (air),  $\pm 14\text{kV}$  (contact) IEC 61000-4-4 (EFT) (5/50ns) Level-3, 20A for I/O, 80A for Power IEC 61000-4-5 (Lightning) 6.5A (8/20 $\mu\text{s}$ )
- 5V operating voltage
- Low capacitance : 1.3pF typical
- Fast turn-on and Low clamping voltage
- Array of surge rated diodes with internal equivalent TVS diode
- Small package saves board space
- Solid-state silicon-avalanche and active circuit triggering technology

## Applications

- USB2.0 Power and Data lines protection
- Notebook and PC Computers
- Monitors and Flat Panel Displays
- IEEE 1394 Firewire Ports
- Video Graphics Cards
- SIM ports

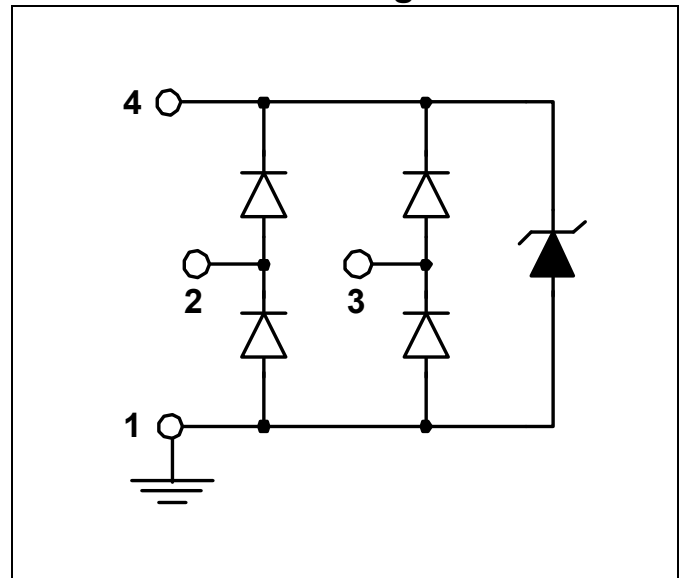
## Description

AZC015-02N is a high performance and low cost design which includes surge rated diode arrays to protect high speed data interfaces. The AZC015-02N family has been specifically designed to protect sensitive components, which are connected to data and transmission lines, from over-voltage caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), and Lightning.

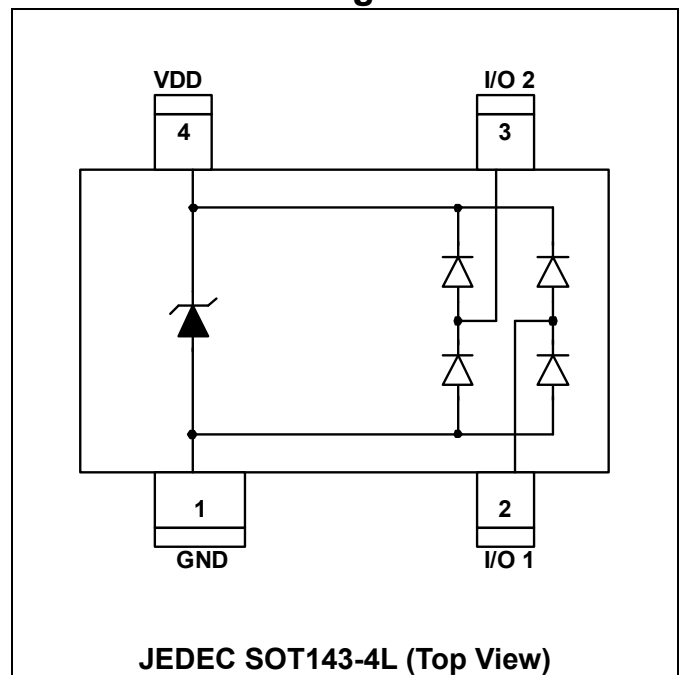
AZC015-02N is a unique design which includes surge rated, low capacitance steering diodes and a unique design of clamping cell which is an equivalent TVS diode in a single package. During transient conditions, the steering diodes direct the transient to either the power supply line or to the ground line. The internal unique design of clamping cell prevents over-voltage on the power line, protecting any downstream components.

AZC015-02N may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 ( $\pm 15\text{kV}$  air,  $\pm 8\text{kV}$  contact discharge).

## Circuit Diagram



## Pin Configuration



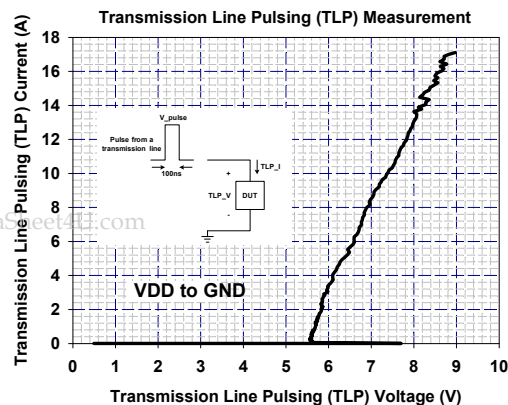
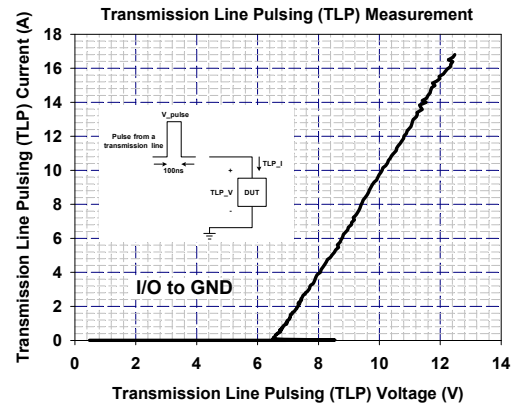
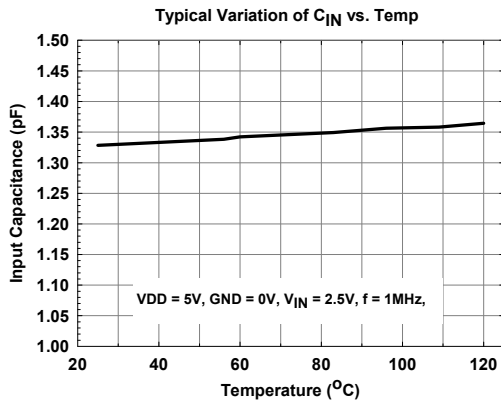
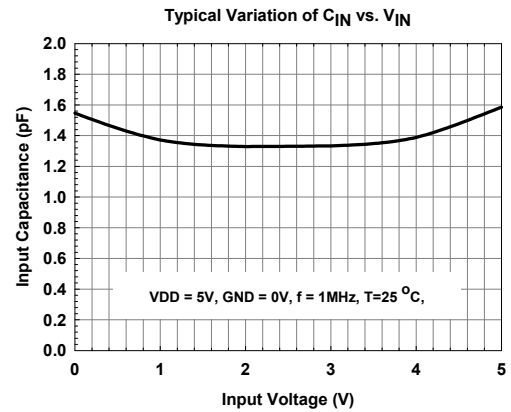
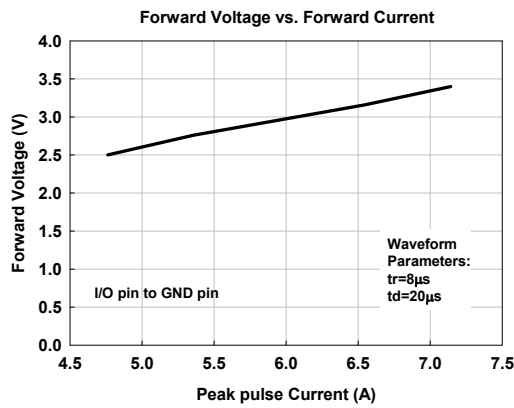
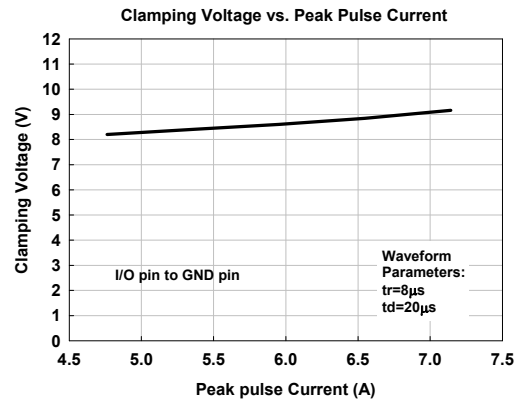
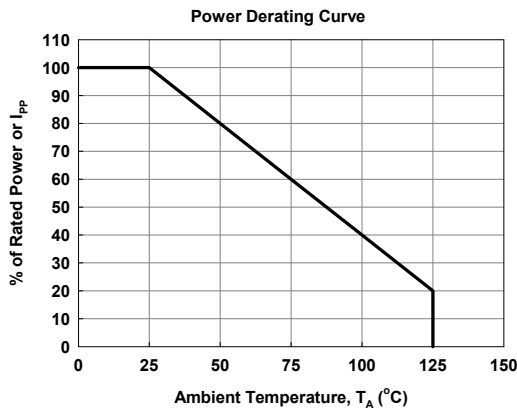
JEDEC SOT143-4L (Top View)

## SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS			
PARAMETER	PARAMETER	RATING	UNITS
Peak Pulse Current (tp =8/20μs)	I <sub>PP</sub>	6.5	A
Operating Supply Voltage (VDD-GND)	V <sub>DC</sub>	6	V
ESD per IEC 61000-4-2 (Air)(I/O to GND)	V <sub>ESD_I/O</sub>	18	kV
ESD per IEC 61000-4-2 (Contact) (I/O to GND)		14	
ESD per IEC 61000-4-2(Air)(VDD-GND)	V <sub>ESD_VDD</sub>	30	kV
ESD per IEC 61000-4-2(Contact) (VDD-GND)		30	
Lead Soldering Temperature	T <sub>SOL</sub>	260 (10 sec.)	°C
Operating Temperature	T <sub>OP</sub>	-55 to +85	°C
Storage Temperature	T <sub>STO</sub>	-55 to +150	°C
DC Voltage at any I/O pin	V <sub>IO</sub>	(GND – 0.5) to (VDD + 0.5)	V

ELECTRICAL CHARACTERISTICS						
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Reverse Stand-Off Voltage	V <sub>RWM</sub>	Pin 4 to pin 1, T=25 °C			5	V
Reverse Leakage Current	I <sub>Leak</sub>	V <sub>RWM</sub> = 5V, T=25 °C, Pin 4 to pin 1			5	μA
Channel Leakage Current	I <sub>CH_Leak</sub>	V <sub>Pin 4</sub> = 5V, V <sub>Pin 1</sub> = 0V, T=25 °C, V <sub>CH</sub> = 0 ~ 5V			1	μA
Reverse Breakdown Voltage	V <sub>BV</sub>	I <sub>BV</sub> = 1mA, T=25 °C Pin 4 to Pin 1	6		9	V
Forward Voltage	V <sub>F</sub>	I <sub>F</sub> = 15mA, T=25 °C Pin 1 to Pin 4		0.8	1	V
Clamping Voltage	V <sub>CL</sub>	I <sub>PP</sub> =5A, tp=8/20μs, T=25 °C Any Channel pin to Ground		8.1	9	V
ESD Clamping Voltage –I/O	V <sub>clamp_io</sub>	IEC 61000-4-2 +6kV, T=25 °C, Contact mode, Any Channel pin to Ground		12.5		V
ESD Clamping Voltage –VDD	V <sub>clamp_VDD</sub>	IEC 61000-4-2 +6kV, T=25 °C, Contact mode, VDD pin to Ground		9		V
ESD Dynamic Turn-on Resistance –I/O	R <sub>dynamic_io</sub>	IEC 61000-4-2 0~+6kV, T=25 °C, Contact mode, Any Channel pin to Ground		0.35		Ω
ESD Dynamic Turn-on Resistance –VDD	R <sub>dynamic_VDD</sub>	IEC 61000-4-2 0~+6kV, T=25 °C, Contact mode, VDD pin to Ground		0.2		Ω
Channel Input Capacitance	C <sub>IN</sub>	V <sub>pin4</sub> = 5V, V <sub>pin1</sub> = 0V, V <sub>IN</sub> = 2.5V, f = 1MHz, T=25 °C, Any Channel pin to Ground		1.3	1.6	pF
Channel to Channel Input Capacitance	C <sub>CROSS</sub>	V <sub>pin4</sub> = 5V, V <sub>pin1</sub> = 0V, V <sub>IN</sub> = 2.5V, f = 1MHz, T=25 °C, Between Channel pins		0.12	0.14	pF
Variation of Channel Input Capacitance	ΔC <sub>IN</sub>	V <sub>pin4</sub> = 5V, V <sub>pin1</sub> = 0V, V <sub>IN</sub> = 2.5V, f = 1MHz, T=25 °C, Channel_x pin to Ground - Channel_y pin to Ground		0.05	0.07	pF

## Typical Characteristics



## Applications Information

### A. Design Considerations

The ESD protection scheme for system I/O connector is shown in the Fig. 1. In Fig. 1, the diodes D1 and D2 are general used to protect data line from ESD stress pulse. If the power-rail ESD clamping circuit is not placed between VDD and GND rails, the positive pulse ESD current ( $I_{ESD1}$ ) will pass through the ESD current path1. Thus, the ESD clamping voltage  $V_{CL}$  of data line can be described as follow:

$$V_{CL} = \text{Fwd voltage drop of D1} + \text{supply voltage of VDD rail} + L_1 \times d(I_{ESD1})/dt + L_2 \times d(I_{ESD1})/dt$$

Where  $L_1$  is the parasitic inductance of data line, and  $L_2$  is the parasitic inductance of VDD rail.

An ESD current pulse can rise from zero to its peak value in a very short time. As an example, a level 4 contact discharge per the IEC61000-4-2 standard results in a current pulse that rises from zero to 30A in 1ns. Here  $d(I_{ESD1})/dt$  can be approximated by  $\Delta I_{ESD1}/\Delta t$ , or  $30/(1 \times 10^{-9})$ . So

just 10nH of total parasitic inductance ( $L_1$  and  $L_2$  combined) will lead to over 300V increment in  $V_{CL}$ ! Besides, the ESD pulse current which is directed into the VDD rail may potentially damage any components that are attached to that rail. Moreover, it is common for the forward voltage drop of discrete diodes to exceed the damage threshold of the protected IC. This is due to the relatively small junction area of typical discrete components. Of course, the discrete diode is also possible to be destroyed due to its power dissipation capability is exceeded.

The AZC015-02N has an integrated power-rail ESD clamped circuit between VDD and GND rails. It can successfully overcome previous disadvantages. During an ESD event, the positive ESD pulse current ( $I_{ESD2}$ ) will be directed through the integrated power-rail ESD clamped circuit to GND rail (ESD current path2). The clamping voltage  $V_{CL}$  on the data line is small and protected IC will not be damaged because power-rail ESD clamped circuit offer a low impedance path to discharge ESD pulse current.

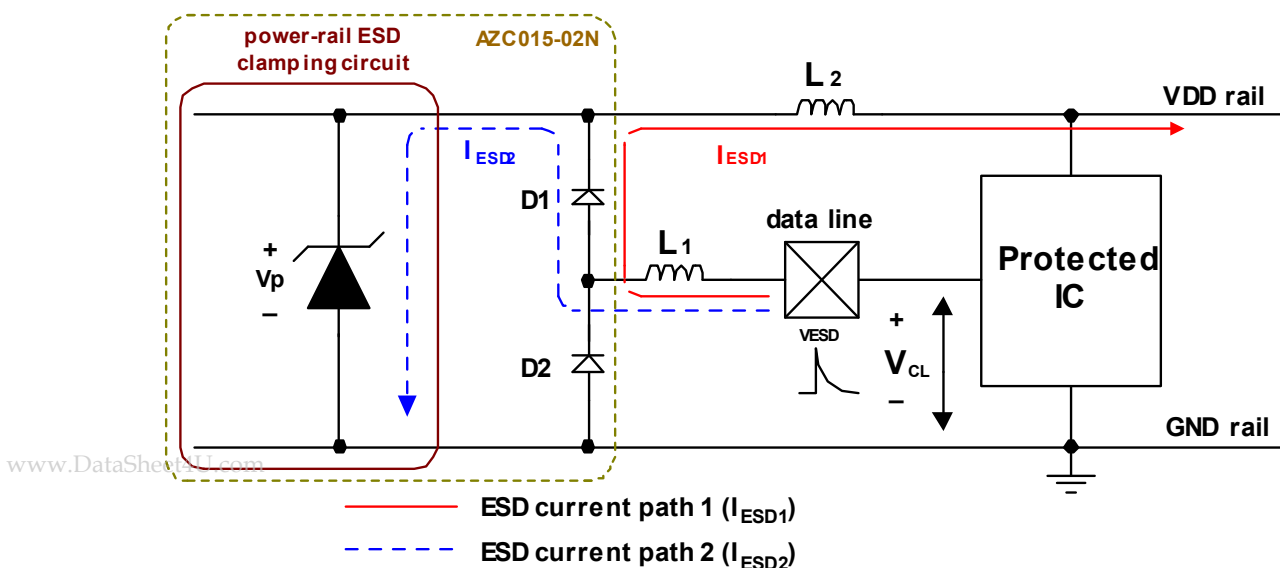


Fig. 1 Application of positive ESD pulse between data line and GND rail.

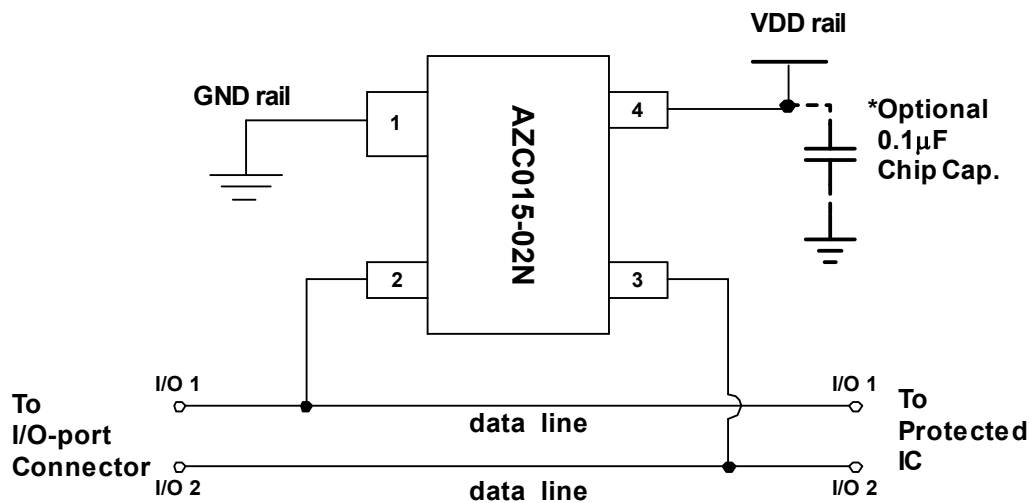
## B. Device Connection

The AZC015-02N is designed to protect two data lines and power rails from transient over-voltage (such as ESD stress pulse). The device connection of AZC015-02N is shown in the Fig. 2. In Fig. 2, the two protected data lines are connected to the ESD protection pins (pin2 and pin3) of AZC015-02N. The ground pin (pin1) of AZC015-02N is a negative reference pin. This pin should be directly connected to the GND rail of PCB (Printed Circuit Board). To get minimum parasitic inductance, the path length should keep as short as possible. In addition, the power pin (pin 4) of AZC015-02N is a positive reference pin. This pin should directly connect to the VDD rail of PCB. When pin 4 of AZC015-02N is connected to the VDD rail, the leakage current of ESD

protection pin of AZC015-02N becomes very small. Because the pin 4 of AZC015-02N is directly connected to VDD rail, the VDD rail also can be protected by the power-rail ESD clamped circuit (not shown) of AZC015-02N.

AZC015-02N can provide protection for 2 I/O signal lines simultaneously. If the number of I/O signal lines is less than 2, the unused I/O pins can be simply left as NC pins.

**In some cases, systems are not allowed to be reset or restart after the ESD stress directly applying at the I/O-port connector. Under this situation, in order to enhance the sustainable ESD Level, a 0.1μF chip capacitor can be added between the VDD and GND rails. The place of this chip capacitor should be as close as possible to the AZC015-02N.**



**Fig. 2 Data lines and power rails connection of AZC015-02N.**

## C. Applications

### 1. Universal Serial Bus (USB) ESD Protection

The AZC015-02N can be used to protect the USB port on the monitors, computers, peripherals or portable systems. The ESD protection scheme for single USB ports is shown in Fig. 3. In the Fig.3, the voltage bus ( $V_{BUS}$ ) of USB port is connected to the power pin (pin 4) of AZC015-02N. Each data line (D+/D-) of USB port is connected to the ESD protection pin (pin2/pin3)

of AZC015-02N.

When ESD voltage pulse appears on the data line, the ESD pulse current will be conducted by AZC015-02N away from the USB controller chip. In addition, the ESD pulse current also can be conducted by AZC015-02N away from the USB controller chip when the ESD voltage pulse appears on the voltage bus ( $V_{BUS}$ ) of USB port. Therefore, the data lines (D+/D-) and voltage bus ( $V_{BUS}$ ) of two USB ports are complementally protected with an AZC015-02N.

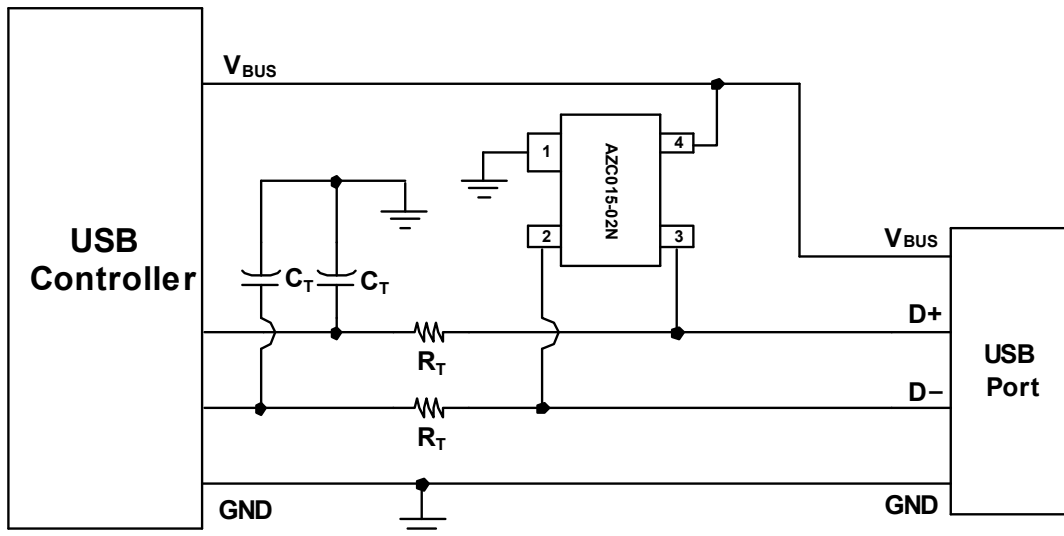


Fig. 3 ESD Protection scheme for single USB ports by using AZC015-02N.

## 2. Audio Interface ESD Protection

For the audio interface, the Right/Left channels should be protected from the ESD stress. The AZC015-02N can be used for the audio interface ESD protection. The ESD protection scheme for audio interface is shown in the Fig. 4. In the Fig. 4, the Right and Left channels of audio connector are connected to ESD protection pins (such as pin 2 and pin 3) of AZC015-02N. For the power pin (pin 4) of

AZC015-02N, it should directly connect to the VDD power supply. As well, for the ground pin (pin 1) of AZC015-02N, it should directly connect to the Ground plate.

When ESD voltage pulse appears on the Right/Left channel of audio connector, the ESD pulse current will be discharged by AZC015-02N. Therefore, the Right/Left channels of audio chip are complementally protected with an AZC015-02N.

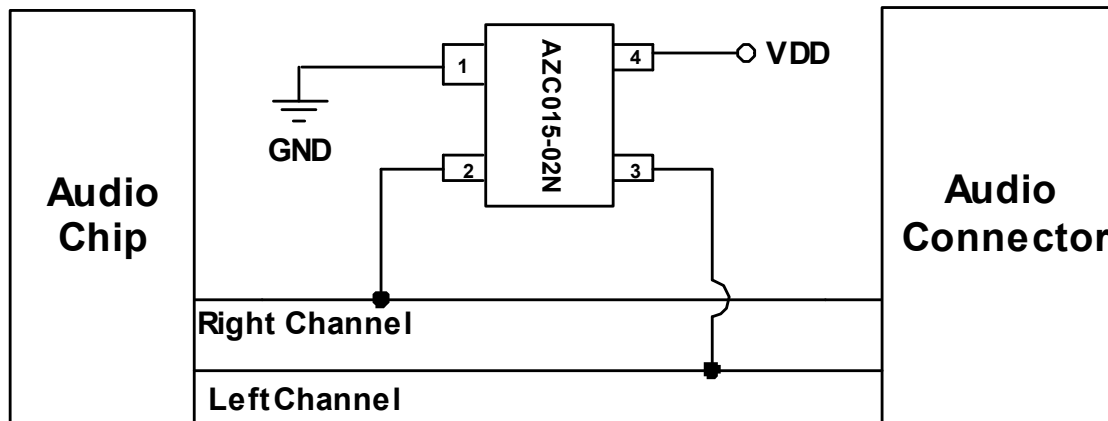
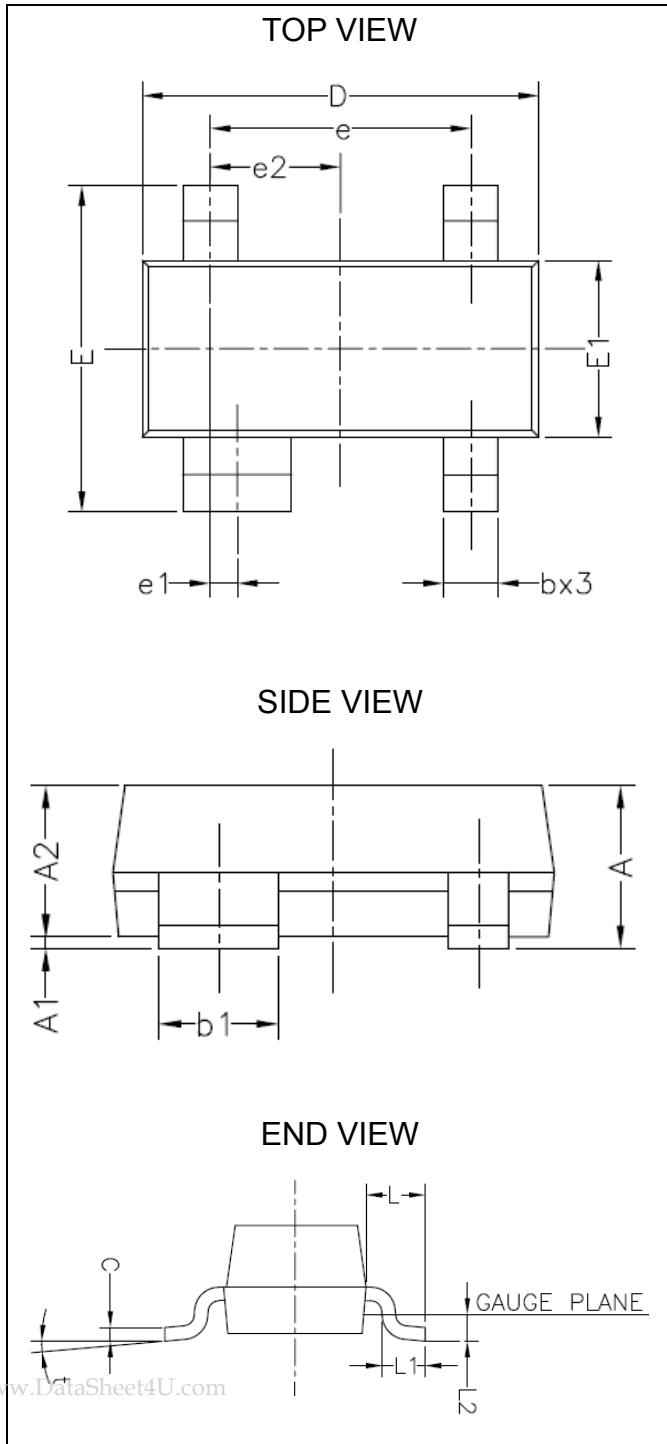


Fig. 4 ESD Protection scheme for audio interface by using AZC015-02N.

## Mechanical Details

### SOT1143-4L

#### PACKAGE DIAGRAMS

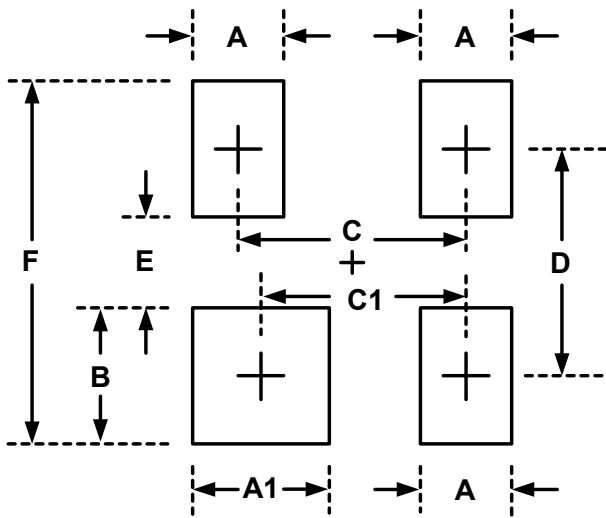


#### PACKAGE DIMENSIONS

Symbol	Millimeters		Inches	
	MIN.	MAX.	MIN.	MAX.
A	0.95	1.17	.037	.046
A1	0.05	0.10	.002	.004
A2	0.90	1.07	.035	.042
b	0.37	0.50	.015	.020
b1	0.76	0.89	.030	.035
C	0.10	0.18	.004	.007
D	2.80	3.04	.110	.120
E1	1.20	1.40	.047	.055
E	2.30	2.50	.091	.098
e1	0.20 BSC.		.008 BSC.	
e2	0.96 BSC.		.038 BSC.	
e	1.92 BSC.		.0755 BSC.	
L	0.55 REF.		.021 REF.	
L1	0.40	0.60	.015	.023
L2	0.25 REF.		.010 REF.	
t	0°~8°		0°~8°	



## LAND LAYOUT

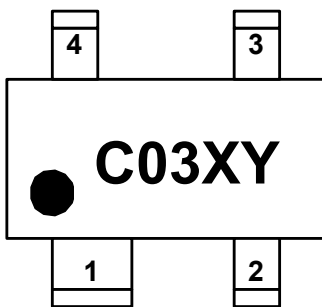


Dimensions		
Index	Millimeter	Inches
A	1.00	0.039
A1	1.40	0.055
B	1.40	0.055
C	1.92	0.076
C1	1.72	0.068
D	2.20	0.087
E	0.80	0.031
F	3.60	0.141

### Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

## MARKING CODE



C03 = Device Code  
X = Date Code  
Y = Control Code

Part Number	Marking Code
AZC015-02N (Rohs part)	C03XY
AZC015-02N (Green part)	C09XY

## Revision History

Revision	Modification Description
Revision 2007/02/02	Original Release.
Revision 2007/05/15	Update the Marking Code from C03X to C03XY.
Revision 2007/12/17	1. Add the Absolute Maximum Ratings of VDD-GND ESD Level, $V_{ESD\_VDD}$ . 2. Update the maximum Reverse Leakage Current, $I_{Leak}$ , value from 2uA to 5uA. 3. Add the parameters of $V_{clamp\_VDD}$ , $R_{dynamic\_io}$ , $R_{dynamic\_VDD}$ . 4. Add the TLP curve of VDD to GND. 5. Add the maximum value of $V_{BV}$ .
Revision 2008/10/14	Add marking code for the Green part.