

Single Event Radiation Hardened Quad Voltage Comparator



The single event effects and total dose radiation hardened IS-139ASRH consists of four independent single or dual supply

voltage comparators on a single monolithic substrate. The common mode input voltage range includes ground, even when operated from a single supply, and the low supply current makes these comparators suitable for low power applications. These types were designed to directly interface with TTL and CMOS inputs.

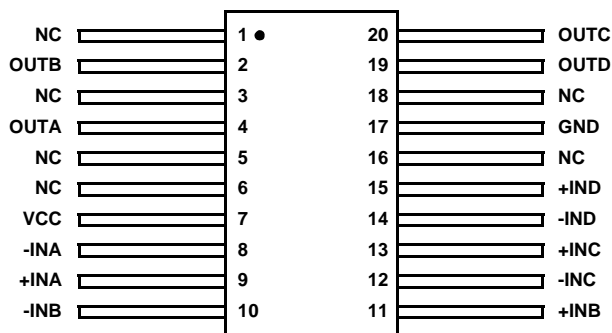
The IS-139ASRH is fabricated on our dielectrically isolated Rad Hard Silicon Gate (RSG) process, which provides immunity to single event latch-up and the capability of highly reliable performance in any radiation environment.

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed below must be used when ordering.

Detailed Electrical Specifications for the IS-139ASRH are contained in SMD 5962-01510. A "hot-link" is provided on the Intersil website for downloading.

Pinout

IS9-139ASRH (FLATPACK CDFP4-F20)
TOP VIEW



Features

- Electrically Screened to SMD # 5962-01510
- QML Qualified per MIL-PRF-38535 Requirements
- Radiation Hardness
 - Total Dose 300krad(Si) (Max)
 - Single Event Latch-up >84MeV/mg/cm²
 - Single Event Upset >84MeV/mg/cm²
- Operating Supply Voltage Range. 9V to 30V
- Input Offset Voltage (V_{IO}) 5mV (Max)
- Quiescent Supply Current 3mA (Max)
- Differential Input Voltage Range Equal to the Supply Voltage
- 100V Output Voltage Withstand Capability

Applications

- DC-DC Power Conversion
- Pulse Generators
- Timing Circuitry
- Level Shifting
- Analog to Digital Conversion

Ordering Information

ORDERING NUMBER	INTERNAL MKT. NUMBER	TEMP. RANGE (°C)
5962F0151001VXC	IS9-139ASRH-Q	-55 to 125
5962F0151001QXC	IS9-139ASRH-8	-55 to 125
IS9-139ASRH/Proto	IS9-139ASRH/Proto	-55 to 125

Die Characteristics

DIE DIMENSIONS

3750 μ m x 4510 μ m (148 mils x 178 mils)
483 μ m \pm 25.4 μ m (19 mils \pm 1 mil)

INTERFACE MATERIALS

Glassivation

Type: Silox (SiO₂)
Thickness: 8.0k Å \pm 1.0k Å

Top Metallization

Type: AlSiCu
Thickness: 16.0k Å \pm 2k Å

Substrate

Radiation Hardened Silicon Gate, Dielectric Isolation

Backside Finish

Silicon

ASSEMBLY RELATED INFORMATION

Substrate Potential

Unbiased (DI)

ADDITIONAL INFORMATION

Worst Case Current Density

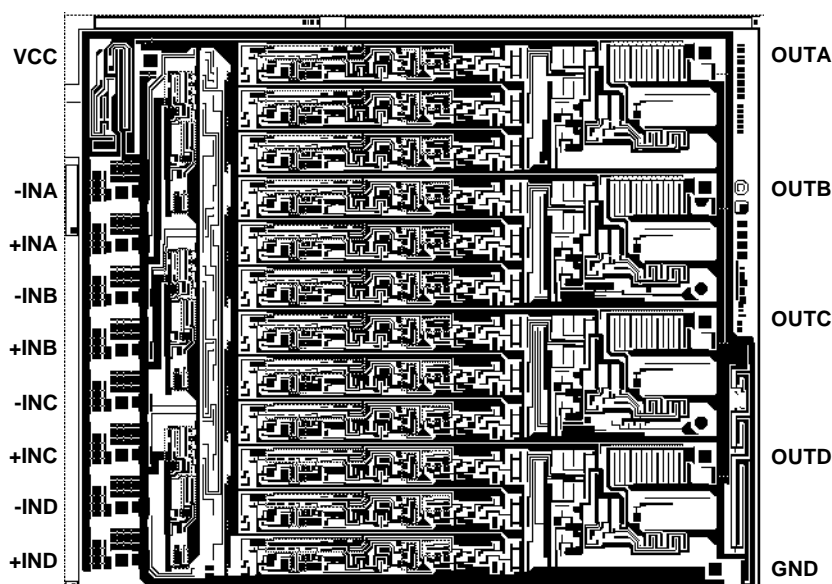
$<2.0 \times 10^5$ A/cm²

Transistor Count

644

Metallization Mask Layout

IS-139ASRH



All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.
Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com