# ASM3P2474A

# Peak EMI Reducing Solution

## Features

- Generates an EMI optimized clock signal at the output.
- Integrated loop filter components.
- Operates with a 3.3V Supply.
- Operating current less than 6mA.
- CMOS design.
- Input frequency range : 13MHz to 30MHz
- Generates a 1X and 2X low EMI spread spectrum clock of the input frequency.
- Output Frequency Selection through FSEL pin
- Frequency deviation : -1.5% (Typ) @25MHz
  -1.5% (Typ) @50MHz
- Available in 6L-TSOP (6L-TSOT-23) package.

## Product Description

The ASM3P2474A is a versatile spread spectrum frequency modulator designed specifically for a wide range of clock frequencies. The ASM3P2474A reduces electromagnetic interference (EMI) at the clock source, allowing system wide reduction of EMI of all clock dependent signals. The ASM3P2474A allows significant system cost savings by reducing the number of circuit board layers, ferrite beads and shielding that are traditionally required to pass EMI regulations.

The ASM3P2474A uses the most efficient and optimized modulation profile approved by the FCC and is implemented by using a proprietary all digital method.

The ASM3P2474A modulates the output of a single PLL in order to “spread” the bandwidth of a synthesized clock, and more importantly, decreases the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most frequency generators. Lowering EMI by increasing a signal’s bandwidth is called ‘spread spectrum clock generation.’

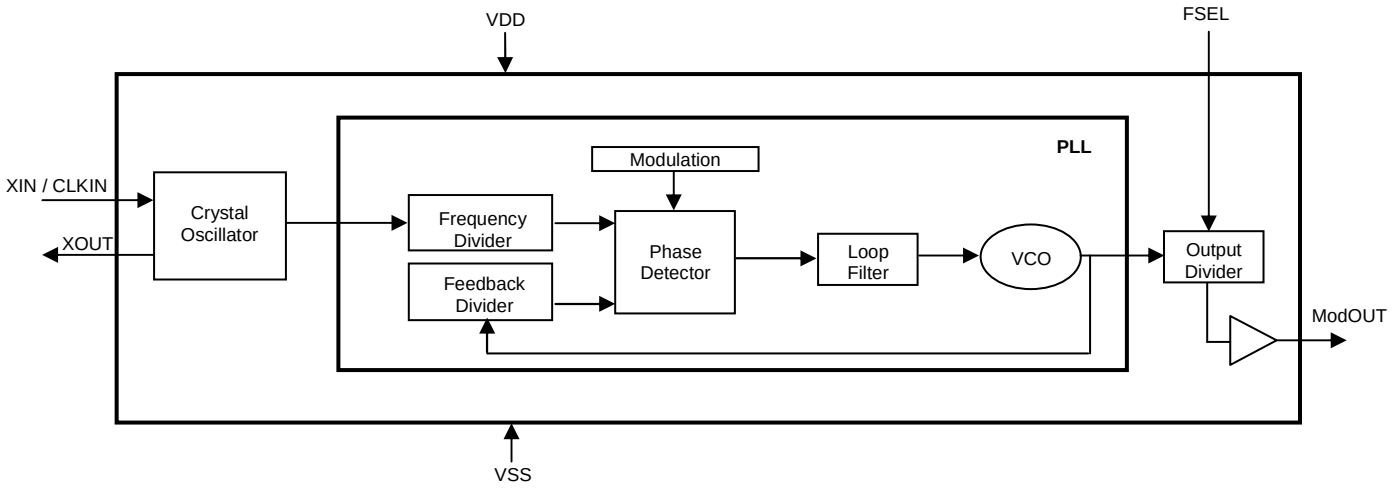
## Applications

The ASM3P2474A is targeted towards all portable devices like MP3 players and digital still cameras.

## Key Specifications

| Description | | Specification |
|---|---|---|
| Supply voltages | | VDD = 3.3V ± 0.3V |
| Cycle-to-Cycle Jitter | | ±200pS (Typ) |
| Output Duty Cycle | | 45/55% (worst case) |
| Modulation Rate Equation | | $F_{IN}/640$ |
| Frequency Deviation | FSEL=0 | -1.5% (Typ) @ 50MHz |
| | FSEL=1 | -1.5% (Typ) @ 25MHz |

## Block Diagram





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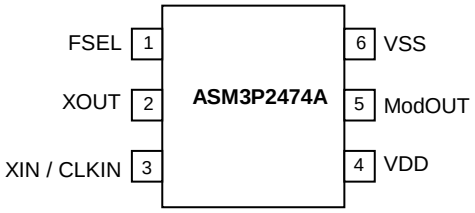
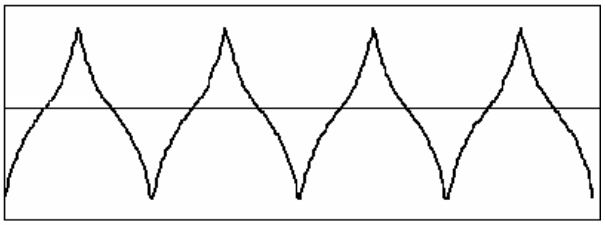
## Pin Configuration (6L-TSOP Package)




## Pin Description

| Pin# | Pin Name | Type | Description |
|---|---|---|---|
| 1 | FSEL | I | Selection Pin for 1X and 2X Output Frequency Options. Please refer to the table *Frequency Selection Options* for further details. |
| 2 | XOUT | O | Crystal connection. If using an external reference, this pin must be left unconnected. |
| 3 | XIN / CLKIN | I | Crystal connection or external reference frequency input. This pin has dual functions. It can be connected either to an external crystal or an external reference clock. |
| 4 | VDD | P | Power supply for the entire chip. |
| 5 | ModOUT | O | Spread spectrum clock output. |
| 6 | VSS | P | Ground connection. |

## Modulation Profile



## Specifications

| Description | Specification | |
|---|---|---|
| Frequency Range | 13MHz < CLKIN < 30MHz | |
| Modulation Equation | $F_{IN}/640$ | |
| Frequency Deviation | FSEL=0 | -1.5% (Typ) @ 50MHz |
| | FSEL=1 | -1.5% (Typ) @ 25MHz |

## Frequency Selection Options

| FSEL Pin | Input Frequency (MHz) | Output Frequency (MHz) |
|---|---|---|
| 0 | 13-30 | 26-60 |
| 1 | 13-30 | 13-30 |

### Absolute Maximum Ratings

| Symbol | Parameter | Rating | Unit |
|---|---|---|---|
| VDD, $V_{IN}$ | Voltage on any pin with respect to Ground | -0.5 to +4.6 | V |
| $T_{STG}$ | Storage temperature | -65 to +125 | ℃ |
| $T_s$ | Max. Soldering Temperature (10 sec) | 260 | ℃ |
| $T_J$ | Junction Temperature | 150 | ℃ |
| $T_{DV}$ | Static Discharge Voltage<br>(As per JEDEC STD22- A114-B) | 2 | KV |

Note: These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

### Operating Conditions

| Parameter | Description | Min | Max | Unit |
|---|---|---|---|---|
| VDD | Supply Voltage | 3 | 3.6 | V |
| $T_A$ | Operating Temperature (Ambient Temperature) | 0 | 70 | ℃ |
| $C_L$ | Load Capacitance | | 15 | pF |
| $C_{IN}$ | Input Capacitance | | 7 | pF |

### DC Electrical Characteristics

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{IL}$ | Input low voltage | VSS-0.3 | | 0.8 | V |
| $V_{IH}$ | Input high voltage | 2.0 | | VDD+0.3 | V |
| $I_{IL}$ | Input low current | | | -35 | µA |
| $I_{IH}$ | Input high current | | | 35 | µA |
| $I_{XOL}$ | XOUT output low current (@ 0.4V, VDD = 3.3V) | | 3 | | mA |
| $I_{XOH}$ | XOUT output high current (@ 2.5V, VDD = 3.3V) | | 3 | | mA |
| $V_{OL}$ | Output low voltage (VDD = 3.3V, $I_{OL}$ = 8mA) | | | 0.4 | V |
| $V_{OH}$ | Output high voltage (VDD = 3.3V, $I_{OH}$ = 8mA) | 2.5 | | | V |
| $I_{DD}$ | Static supply current[1] | | 1.6 | | mA |
| $I_{CC}$ | Dynamic supply current<br>(3.3V, 25MHz and no load and FSEL=1) | | 4.0 | | mA |
| VDD | Operating voltage | 3.0 | 3.3 | 3.6 | V |
| $t_{ON}$ | Power-up time (first locked cycle after power-up) | | | 5 | mS |
| $Z_{OUT}$ | Output impedance | | 45 | | Ω |

Note: 1. XIN /CLKIN pin is pulled low.

## AC Electrical Characteristics

| Symbol | Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| CLKIN | Input frequency | | 13 | | 30 | MHz |
| ModOUT | Output frequency | FSEL = 0 | 26 | | 60 | MHz |
| | | FSEL = 1 | 13 | | 30 | |
| $f_d$ | Frequency Deviation | Output Frequency = 13MHz | | -1.8 | | % |
| | | Output Frequency = 30MHz | | -0.9 | | |
| $f_d$ | Frequency Deviation | Output Frequency = 26MHz | | -1.8 | | % |
| | | Output Frequency = 60MHz | | -0.9 | | |
| $t_{LH}$[1] | Output rise time (measured from 0.8 to 2.0V) | | 0.4 | 0.85 | 1.1 | nS |
| $t_{HL}$[1] | Output fall time (measured at 2.0V to 0.8V) | | 0.3 | 0.7 | 0.9 | nS |
| $t_{JC}$ | Jitter (cycle-to-cycle) | | | ±200 | | pS |
| $t_D$ | Output duty cycle | | 45 | 50 | 55 | % |

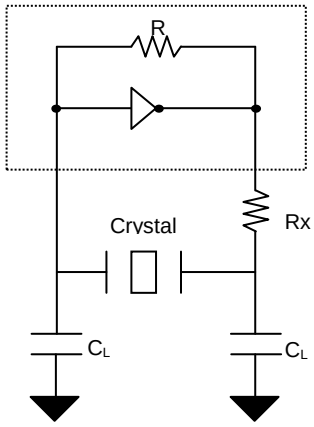
Note: 1. $t_{LH}$ and $t_{HL}$ are measured into a capacitive load of 15pF.

## Typical Crystal Specifications

| Fundamental AT cut parallel resonant crystal | |
|---|---|
| Nominal frequency | 25MHz |
| Frequency tolerance | ± 30 ppm or better at 25℃ |
| Operating temperature range | -25℃ to +85℃ |
| Storage temperature | -40℃ to +85℃ |
| Load capacitance($C_P$) | 18pF |
| Shunt capacitance | 7pF maximum |
| ESR | 25 Ω |

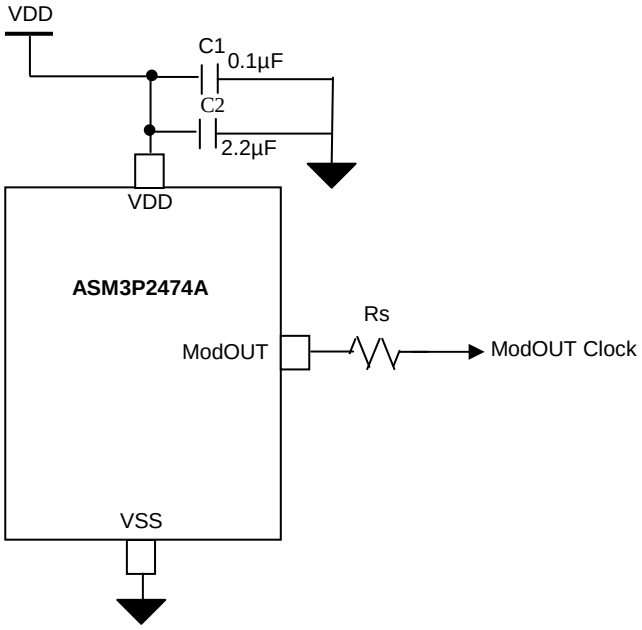
Note: Note: $C_L$ is Load Capacitance and Rx is used to prevent oscillations at overtone frequency of the Fundamental frequency.

## Typical Crystal Interface Circuit



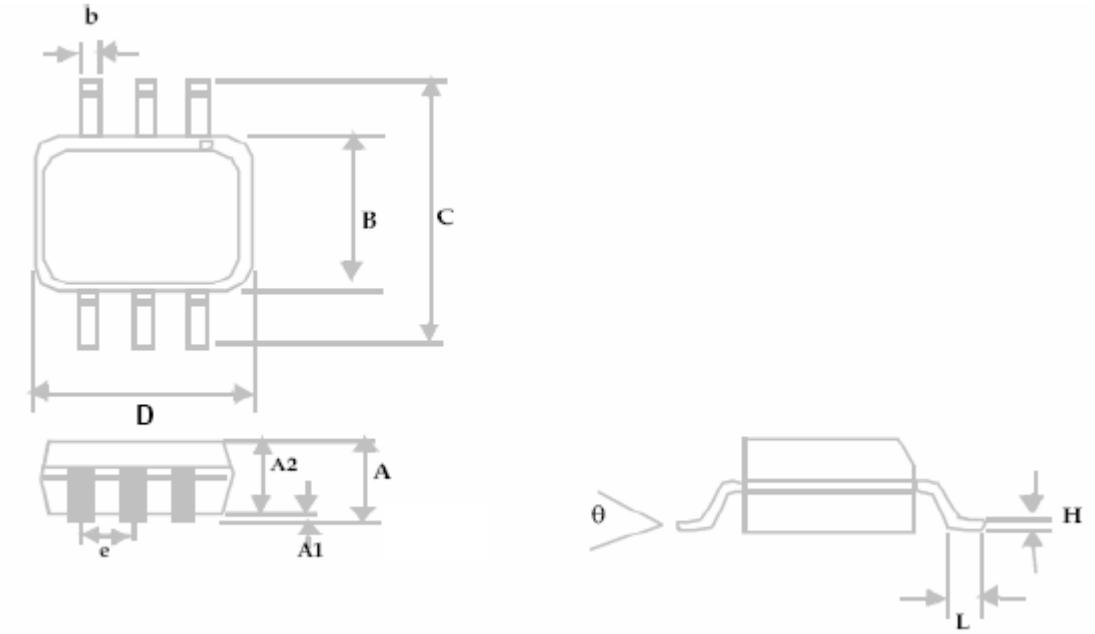

$C_L = 2*(C_P – C_S)$,
Where $C_P$ = Load capacitance of crystal
$C_S$ = Stray capacitance due to $C_{IN,}$ PCB, Trace etc.

## Typical Application Schematic



## Package Information

### 6L-TSOP Package




| Symbol | Dimensions | | | |
|---|---|---|---|---|
| | Inches | | Millimeters | |
| | Min | Max | Min | Max |
| A | | 0.04 | | 1.00 |
| A1 | 0.00 | 0.004 | 0.00 | 0.10 |
| A2 | 0.033 | 0.036 | 0.84 | 0.90 |
| b | 0.012 | 0.02 | 0.30 | 0.50 |
| H | 0.005 BSC | | 0.127 BSC | |
| D | 0.114 BSC | | 2.90 BSC | |
| B | 0.06 BSC | | 1.60 BSC | |
| e | 0.0374 BSC | | 0.950 BSC | |
| C | 0.11 BSC | | 2.80 BSC | |
| L | 0.0118 | 0.02 | 0.30 | 0.50 |
| θ | 0° | 4° | 0° | 4° |

## Ordering Information

| Part Number | Marking | Package Type | Temperature |
|---|---|---|---|
| ASM3P2474AF-06OR | W4L | 6L-TSOP (6L-TSOT-23), TAPE & REEL, Pb Free | 0℃ to +70℃ |

A “microdot” placed at the end of last row of marking or just below the last row toward the center of package indicates Pb-free.

Licensed under US Patent #5,488,627 and #5,631,921.

Note: This product utilizes US Patent #6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003.



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