OKI semiconductor

MSM6262-01

DOT MATRIX LCD CONTROLLER WITH 48 DOT COMMON DRIVER

GENERAL DESCRIPTION

The OKI MSM6262GS is a dot matrix LCD controller which is fabricated by OKI's low power consumption CMOS silicon gate technology. In combination with 8-bit microcontroller, the MSM6262GS can control the dot matrix character type LCD module. The MSM6262GS consists of 48 dots COMMON driver, DISPLAY RAM, character generator RAM, character generator ROM and control circuit.

The MSM6262GS is provided with an serial data transfer output. So, Max. 160 characters can be controlled by MSM6262GS by using together with the MSM5259GS or the MSM5839CGS.

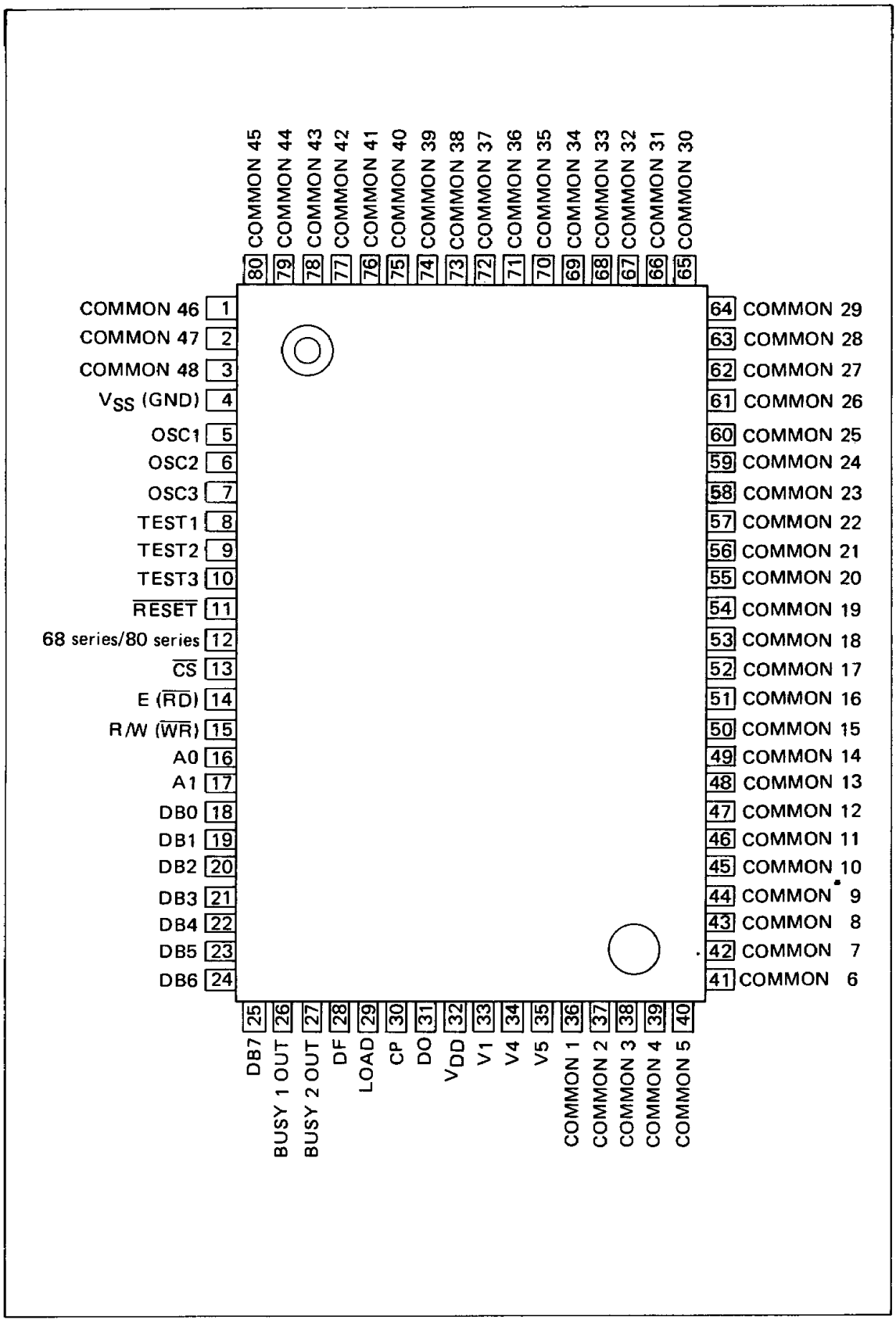
FEATURES

- Easy interface with 8-bit microprocessor or 8-bit microcontroller
- Dot matrix LCD controller/48 dot driver for three different fout configuration (5 x 7 dots, 5 x 11 dots and 5 x 12 dots)
- Max. 160 characters can be controlled
- Display RAM ... 160 x 9-bit
- On-chip character generator ROM (CGROM) for 256 different characters
  - 5 x 7 dots ... 128 characters
  - 5 x 11 dots ... 96 characters
  - 5 x 12 dots ... 32 characters
- On-chip character generator RAM (CGRAM) of 32 x 8-bit for 2 different character fonts
  - 5 x 8 dots ... 4
  - 5 x 12 dots ... 2
- Under-line function
- Shift function for g, j, p, q and y
- 80 pin -VI plastic QFP (QFP80-P-1420-VIK)

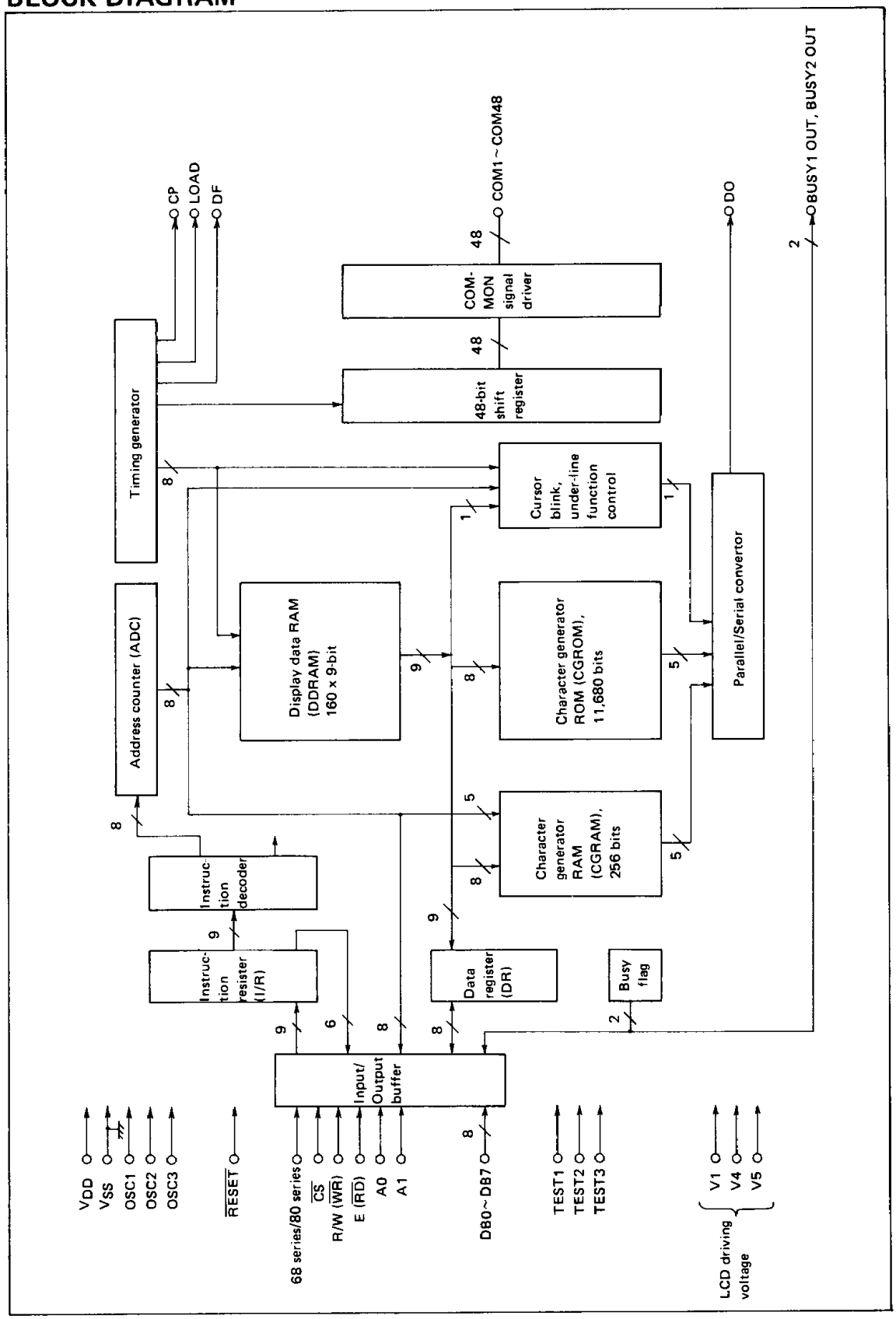
SELECTABLE DRIVING DUTY

Duty	Font Configuration (dot)	Cursor	Display (Characters x line)
1/16	5 x 7 (5 x 8)	O	80 x 2
1/24	5 x 11 (5 x 12)	O	80 x 2
1/32	5 x 7 (5 x 8)	O	40 x 4
1/48	5 x 11 (5 x 12)	O	40 x 4

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Limits	Unit	Applicable terminal
Supply voltage	V_{DD}	ta = 25°C	−0.3 ~ 7.0	V	$V_{DD}-V_{SS}$
Supply voltage for LCD driving	V_1, V_4, V_5	ta = 25°C	$V_{DD}-12$ ~ $V_{DD}+0.3$	V	V_1, V_4, V_5
Input voltage	VIN	ta = 25°C	−0.3 ~ $V_{DD}+0.3$	V	OSC1 $\overline{\text{RESET}}$ 68 series/80 series $\overline{\text{CS}}$, A0, A1 $\overline{\text{WR}}$ (R/W) $\overline{\text{RD}}$ (E) DB_0 ~ DB_7
Power dissipation	P_D	ta = 25°C	500	mW	
Storage temperature	T_{stg}	—	−55 ~ +125	°C	
Operating temperature	T_{opr}	—	−20 ~ +75	°C	

DC CHARACTERISTICS

(V_{DD} = 4.5 ~ 5.5V, ta = –20 ~ +75°C)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit	Applicable terminal
"H" input voltage	V_{IH1}	–	2.2	–	V_{DD}	V	$\overline{CS}$, $\overline{WR}$ (R/W) $\overline{RD}$ (E), A0, A1 DB0 ~ DB7
"L" input voltage	V_{IL1}	–	–0.3	–	0.7	V	
"H" output voltage	V_{OH1}	I_O = –250 μA	2.4	–	–	V	DB0 ~ DB7
"L" output voltage	V_{OL1}	I_O = 1.8 mA	–	–	0.4	V	
"H" input voltage	V_{IH2}	–	V_{DD}–0.8	–	V_{DD}	V	OSC1 $\overline{RESET}$ 68series/80 series
"L" input voltage	V_{IL2}	–	–0.3	–	0.8	V	
"H" output voltage	V_{OH2}	I_O = –500 μA	0.85V_{DD}	–	–	V	DO, LOAD, DF
"L" output voltage	V_{OL2}	I_O = 500 μA	–	–	0.15V_{DD}	V	
"H" output voltage	V_{OH3}	I_O = –1mA	0.85V_{DD}	–	–	V	CP
"L" output voltage	V_{OL3}	I_O = 1mA	–	–	0.15V_{DD}		
"H" output voltage	V_{OH4}	I_O = –100 μA	2.4	–	–	V	BUSY1 BUSY2
"L" output voltage	V_{OL4}	I_O = 1.6 mA	–	–	0.4	V	
COM voltage drop	V_{COM}	Note 1 I_O = ± 50 μA	–	–	2.9	V	COM1 ~ COM48
"H" input current	I_{ILH1}	V_{IN} = V_{DD}	–	–	1	μA	$\overline{CS}$, $\overline{WR}$ (R/W) $\overline{RD}$ (E), A0, A1 OSC1, 68 series/ 80 series
"L" input current	$I_{IL\ L1}$	V_{IN} = V_{SS}	–	–	–1	μA	
Current consumption	I_{DD1}	Note 2 V_{DD} = 5V, f_{OSC} = 500kHz	–	–	1.5	mA	V_{DD}
	I_{DD2}	Note 2 V_{DD} = 5V, f_{IN} = 500kHz	–	–	1.5	mA	
LCD driving voltage	V_{LCD1}	Note 3 V_{DD} – V_5 1/5 bias	3.0	–	11	V	V_1, V_4, V_5
	V_{LCD2}	1/6 ~ 1/7 bias	4.0	–	11	V	
		1/8 bias	4.5	–	11	V	
"H" input current	$I_{IL\ L2}$	V_{IN} = V_{DD}	–	–	2	μA	$\overline{RESET}$
"L" input current	$I_{IL\ L2}$	V_{IN} = V_{SS}, V_{DD} = 5V	–8	–20	–60	μA	
Input frequency	f_{IN}	Note 4, Note 5	300	–	700	kHz	OSC1
Input clock duty	f_{Duty}	Note 5	45	50	55	%	
Input clock falling time	tr	Note 5	–	–	100	nS	
Input clock falling time	tf	Note 5	–	–	100	nS	
CR oscillation frequency	f_{CR}	Note 6	300	–	700	kHz	OSC1, 2, 3
"H" input current	I_{ILH3}	V_{IN} = V_{DD}			1	μA	DB0 ~ DB7
"L" input current	I_{ILL3}	V_{IN} = V_{SS} V_{DD} = 5V	–45	–120	–250	μA	

Note 1. This is applicable to the voltage drop which is caused between V_{DD}, V_1, V_4, V_5 and COM1 ~ COM48 when a current of 50μA is flew in/out to/from all of COM1 ~ COM48. (When the output level is either V_{DD} or V_1, it should be applied only when the current flows in. When the output level is either V_4 or V_5, it should be applied only when the current flows in.
In this case, +5V is applied to V_{DD}, V_1 and V_2, while −6V is applied to V_4 and V_5.)

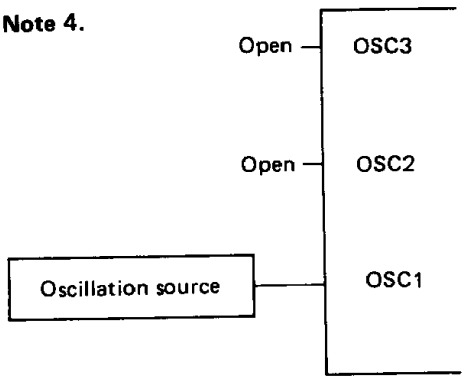
Note 2. This is applicable to the current which flows in to V_{DD} under following conditions.
V_{DD} = 5V, V_{SS} = 0V, V_1 = 2.8V, V_4 = −3.8V, V_5 = −6V, No load, No interface with CPU

Note 3. V_1 ~ V_5 should be set at as follows.

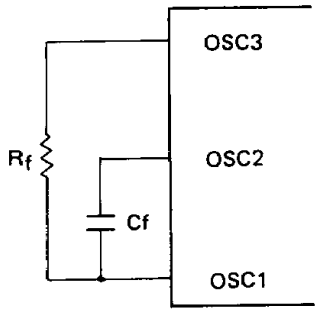
No. of lines (N) / Font configuration / Terminal	2 lines		4 lines	
	5 x 8	5 x 12	5 x 8	5 x 12
V_1	$V_{DD}-\frac{1}{5}V_{LCD}$	$V_{DD}-\frac{1}{6}V_{LCD}$	$V_{DD}-\frac{1}{7}V_{LCD}$	$V_{DD}-\frac{1}{8}V_{LCD}$
V_4	$V_{DD}-\frac{4}{5}V_{LCD}$	$V_{DD}-\frac{5}{6}V_{LCD}$	$V_{DD}-\frac{6}{7}V_{LCD}$	$V_{DD}-\frac{7}{8}V_{LCD}$
V_5	$V_{DD}-V_{LCD}$	$V_{DD}-V_{LCD}$	$V_{DD}-V_{LCD}$	$V_{DD}-V_{LCD}$

V_{LCD} = LCD driving voltage

Note 4.

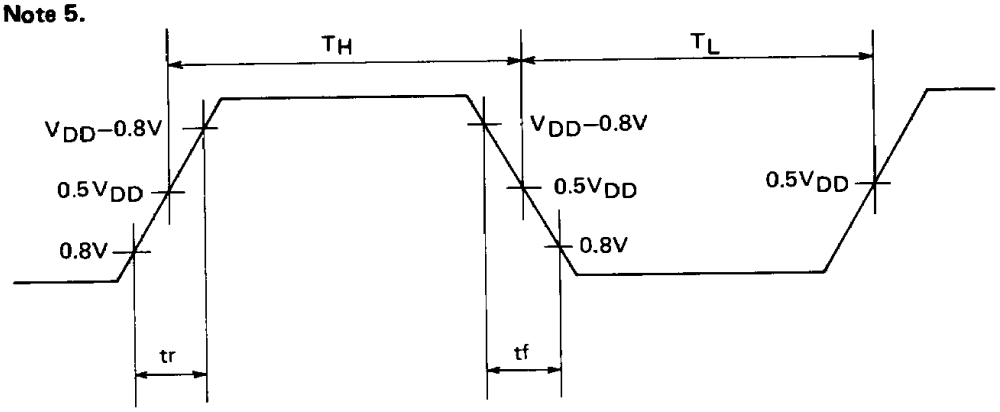


Note 6.



R_f = 39kΩ ± 5%
C_f = 22pF ± 10%

Note 5.

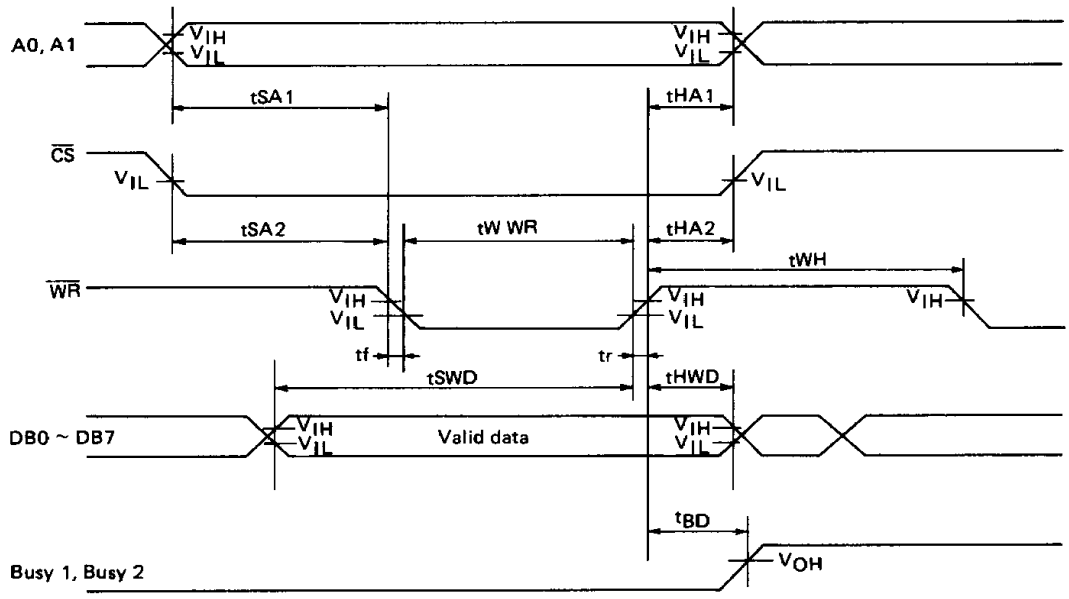


$$f_{Duty} = \frac{T_H}{T_H + T_L} \times 100\%$$

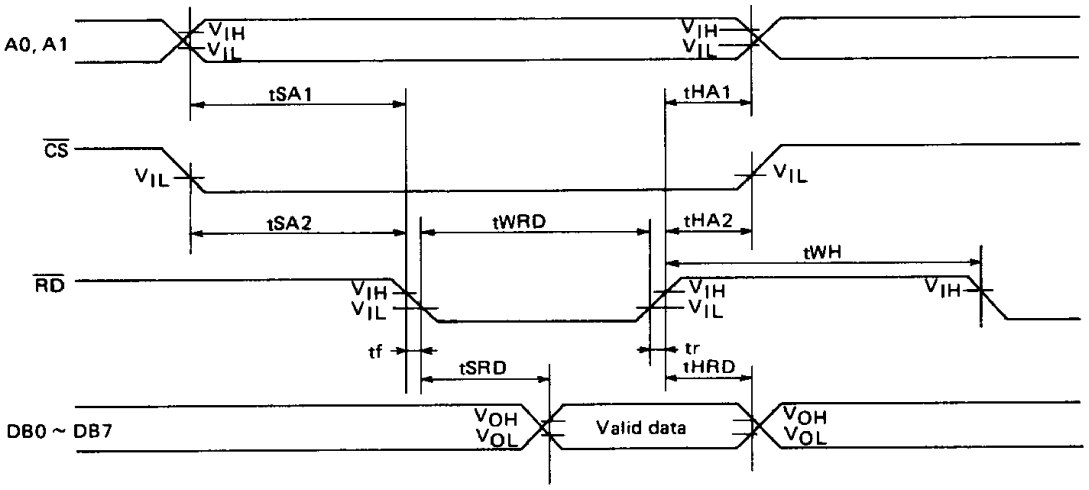
SWITCHING CHARACTERISTICS

Interface 80 series CPU

Write operation



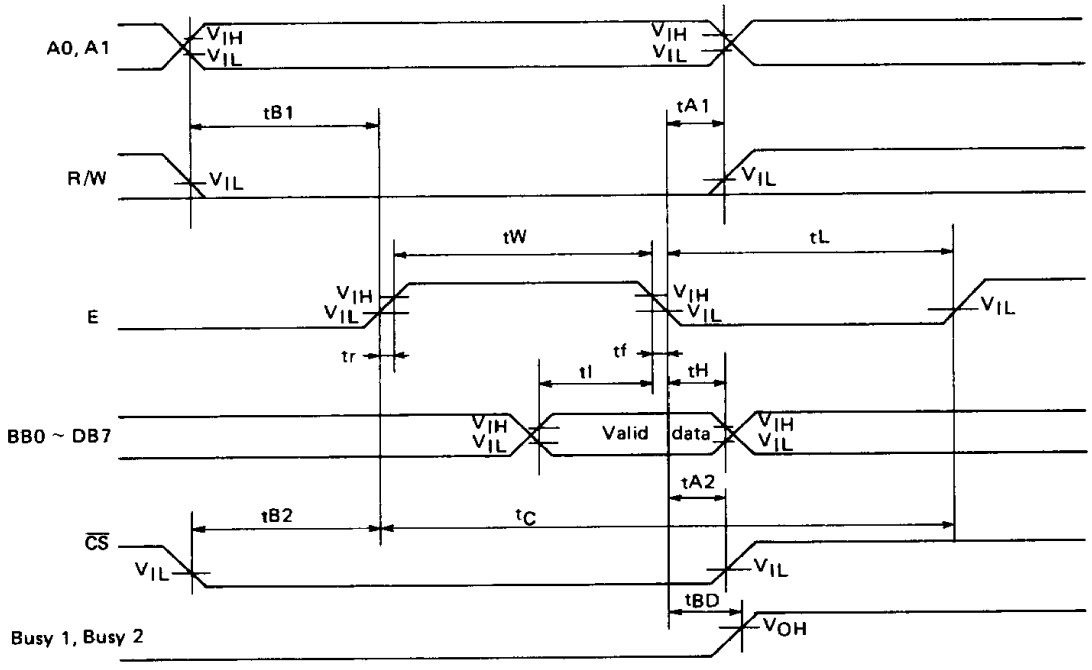
Read operation



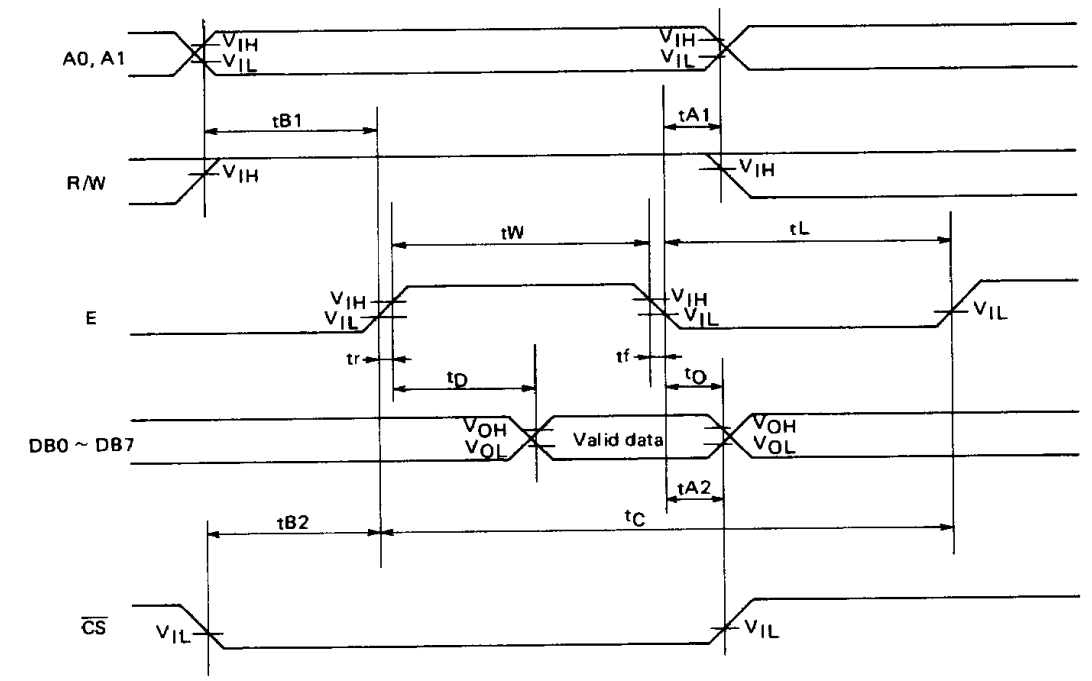
Refer to the chapter of DC characteristics for the definition of V_{IH}, V_{IL}, V_{OH} and V_{OL}.

Interface with 68 series CPU

Write operation

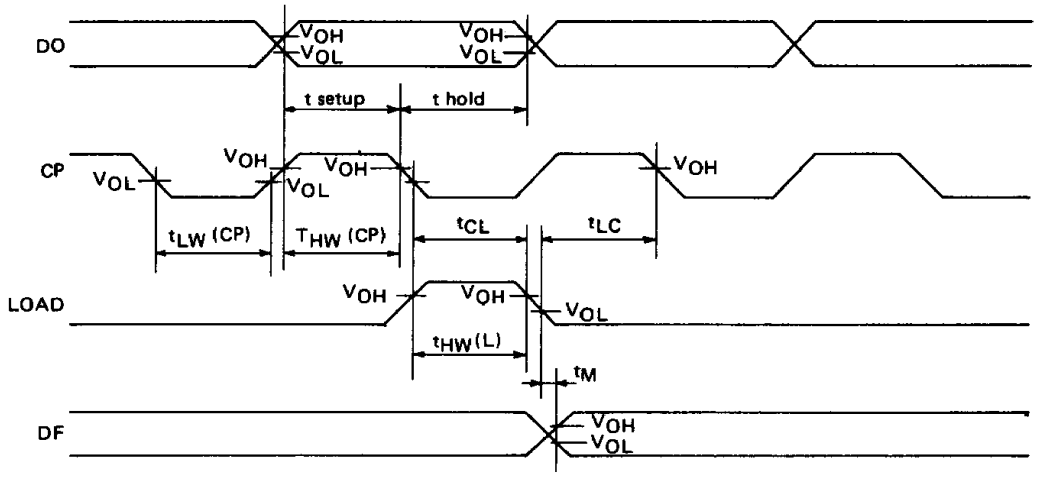


Read operation

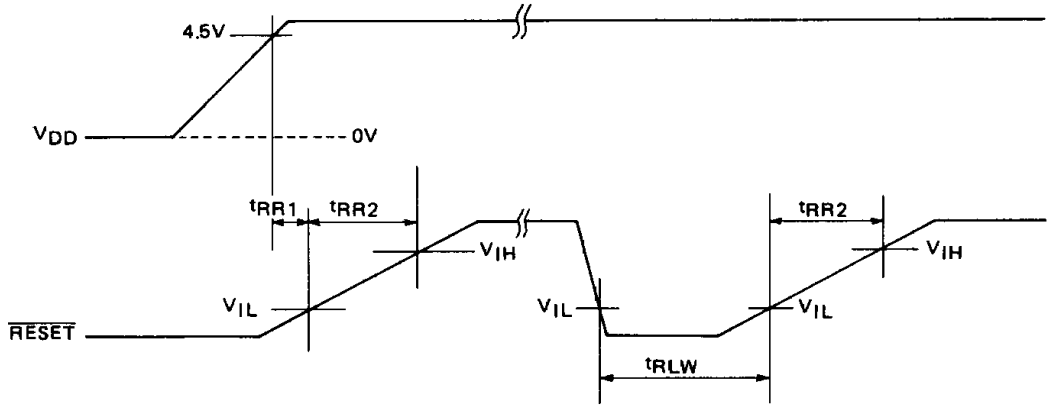


Refer to the chapter of DC CHARACTERISTICS for the definition of V_{IH}, V_{IL}, V_{OH} and V_{OL}.

Interface with Segment Driver



Reset Wave Form



Refer to the DC CHARACTERISTICS for the definition of V_{IH}, V_{IL}, V_{OH} and V_{OL}

Interface with 80 series CPU

(V_{DD} = 4.5 ~ 5.5V, ta = −20 ~ +75°C)

Parameter	Symbol	MIN.	MAX.	Unit
Address set-up time	t_{SA_1}	110	–	ns
$\overline{CS}$ set-up time	t_{SA_2}	100	–	ns
$\overline{WR}$ "L" pulse width	t_{WWR}	320	–	ns
$\overline{RD}$ "L" pulse width	t_{WRD}	320	–	ns
$\overline{WR}$, $\overline{RD}$ "H" pulse width	t_{WH}	210	–	ns
Address hold time	t_{HA_1}	25	–	ns
$\overline{CS}$ hold time	t_{HA_2}	25	–	ns
Data set-up time	t_{SWD}	300	–	ns
Data hold time (write operation)	t_{HWD}	20	–	ns
$\overline{WR}$, $\overline{RD}$ falling time	tf	–	25	ns
$\overline{WR}$, $\overline{RD}$ rising time	tr	–	25	ns
Data delay time	t_{SRD}	–	190	ns
Data hold time (Reading operation)	tHRD	0	–	ns
Busy output delay time	t_{BD}	–	410	ns

Interface with 68 series CPU

(V_{DD} = 4.5 ~ 5.5V, ta = −20 ~ +75°C)

Parameter	Symbol	MIN.	MAX.	Unit
Cycle time	t_C	500	–	ns
Address, R/W set-up time	t_{B_1}	100	–	ns
$\overline{CS}$ set-up time	t_{B_2}	90	–	ns
E signal "H" pulse width	t_W	220	–	ns
E signal "L" pulse width	t_L	210	–	ns
Address, R/W hold time	t_{A_1}	20	–	ns
$\overline{CS}$ hold time	t_{A_2}	20	–	ns
Data set-up time	t_I	225	–	ns
Data hold time (Write operation)	t_H	30	–	ns
E signal rising time	tr	–	25	ns
E signal falling time	tf	–	25	ns
Data delay time	t_D	–	180	ns
Data hold time (Read operation)	t_O	10	–	ns
Busy output delay time	t_{BD}	–	410	ns

Interface with segment driver

(V_{DD} = 4.5 ~ 5.5V, ta=−20 ~ +75°C, f_{OSC} = 500 kHz)

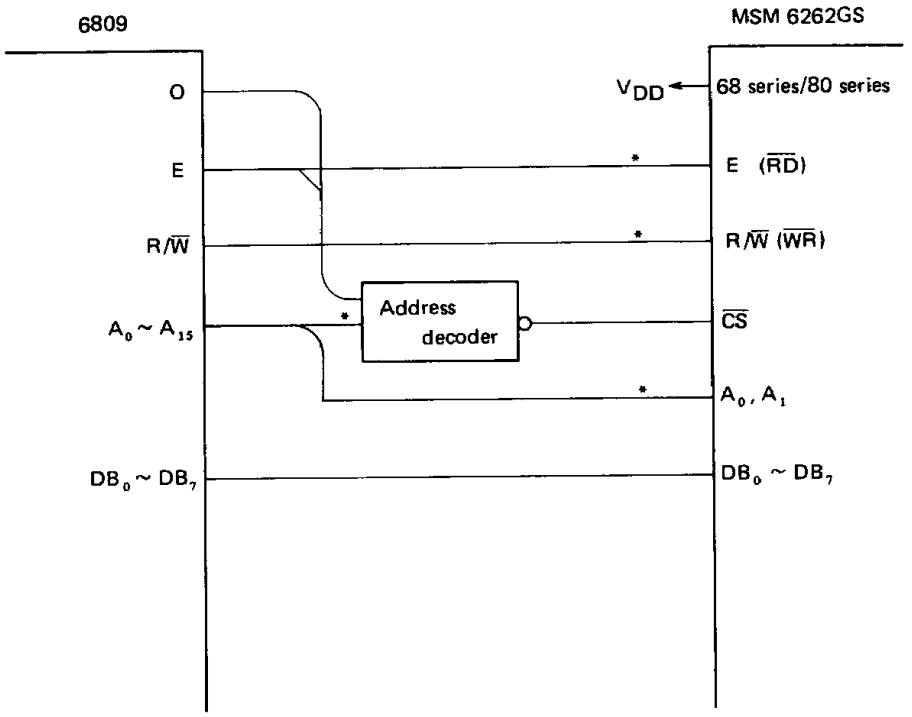
Parameter	Symbol	MIN.	MAX.	Unit
Clock "L" pulse width	t_{LW}(CP)	400	—	ns
Clock "H" pulse width	t_{HW}(CP)	400	—	ns
Do set-up time	t setup	200	—	ns
Do hold time	t hold	200	—	ns
LOAD, Clock set-up time	t_{CL}	200	—	ns
LOAD, Clock hold time	t_{LC}	100	—	ns
LOAD, "H" pulse width	t_{HW}(L)	400	—	ns
DF delay time	t_M	−500	500	ns

Reset waveform

(V_{DD} = 4.5 ~ 5.5V, ta = −20 ~ +75°C)

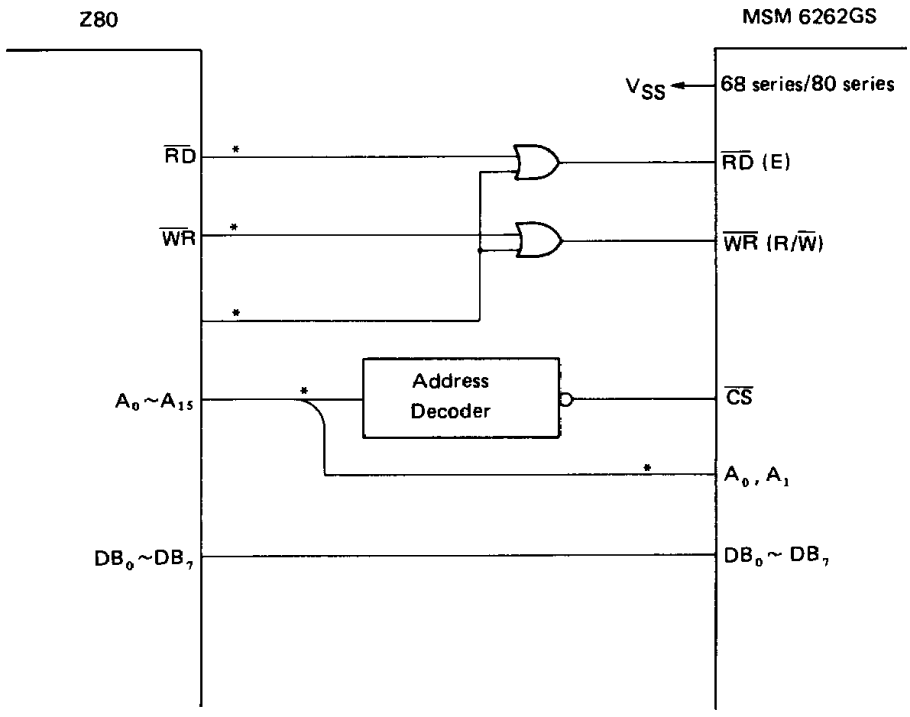
Parameter	Symbol	MIN.	MAX.	Unit
"L" input time when power is on	tRR_1	0.25	—	ms
"L" input width when in operation	tRLW	0.5	—	ms
Rising time	tRR_2	0.5	—	ms

Interface with 6809



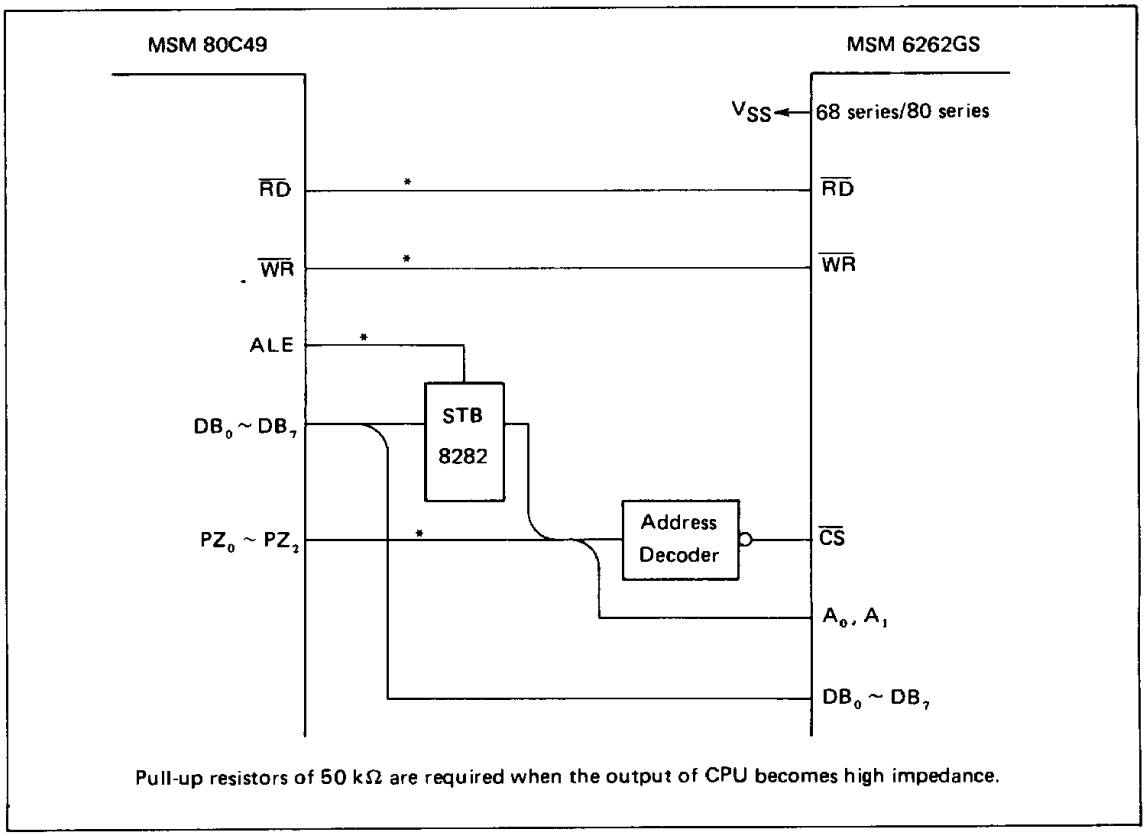
Pull-up resistors of 50 kΩ are required when the output of CPU becomes high impedance.

Interface with Z80



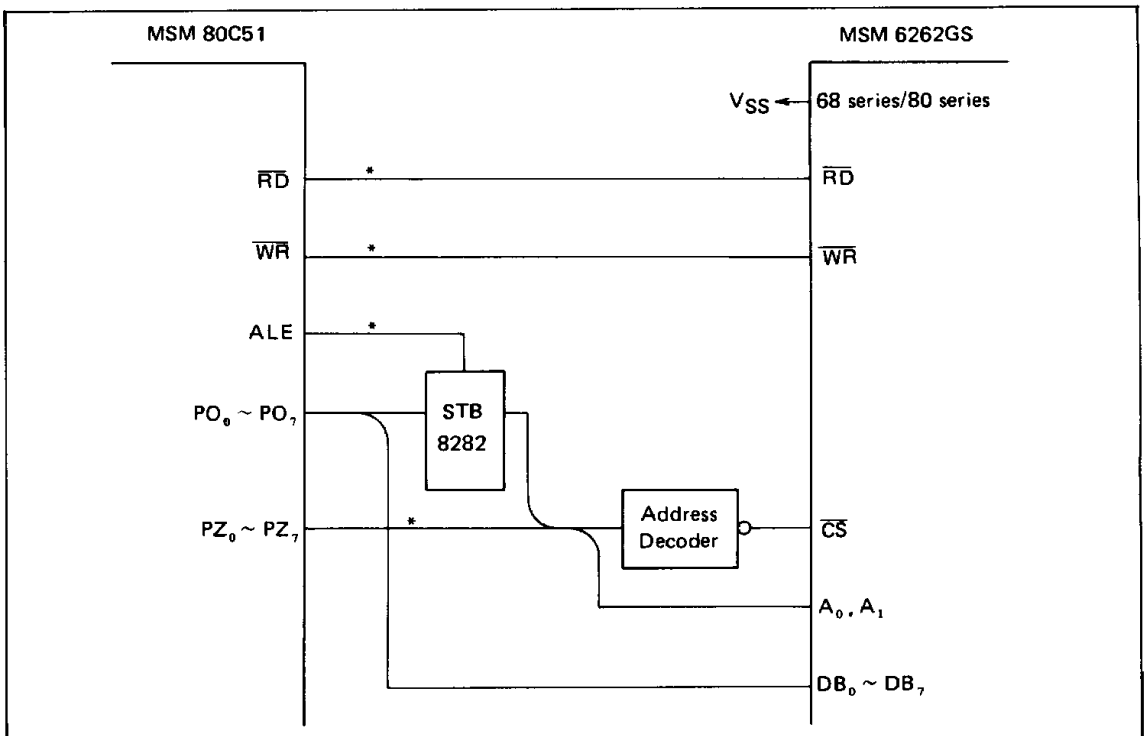
Pull-up resistors of 50 kΩ are required when the output of CPU becomes high impedance.

Interface with 80C49



Pull-up resistors of 50 kΩ are required when the output of CPU becomes high impedance.

Interface with 80C51

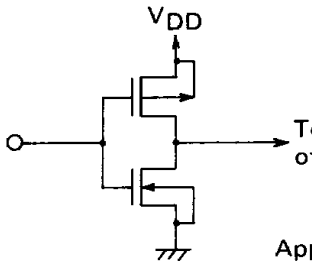


Pull-up resistors of 50 kΩ are required when the output of CPU becomes high impedance.

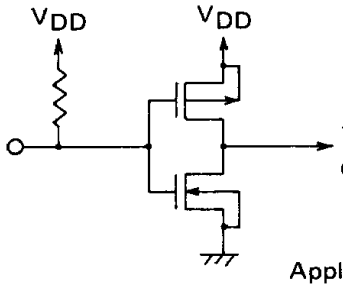
PIN DESCRIPTION

Pin Name	Input/Output	Function
OSC1 OSC2, OSC3	I, I/O	Oscillation connection pin.
$\overline{RESET}$	I	Reset pin.
68 series/80 series	I	Selection pin for either 68 series CPU or 80 series CPU.
$\overline{CS}$	I	Chip select pin. By setting CS at "L" level, MSM6262GS is set at selecting condition.
R/W ($\overline{WR}$)	I	R/$\overline{W}$ pin of 68 series CPU shall be connected to this pin, while $\overline{WR}$ pin shall be connected to this pin in case of 80 series CPU.
E ($\overline{RD}$)	I	E pin of 68 series CPU shall be connected to this pin, while $\overline{RD}$ pin shall be connected to this pin in case of 80 series CPU.
A_0, A_1	I	The address bus of CPU shall be connected to this pin. Instruction code is set by this pin.
DB_0 ~ DB_7	I/O	The data bus of CPU shall be connected to this pin. This pin is used to set the data of the instruction or to read the internal data.
TEST1 ~ TEST 3	I	Test pin. Normally these pins should be set at V_{SS} or open.
V_{DD}, V_{SS}		Voltage supply pin. V_{DD} is also used for the common bias voltage level to drive the LCD.
V_1, V_4, V_5		Common bias voltage input pin to drive the LCD.
DO	O	Serial data output pin for SEGMENT drivers.
CP	O	Clock pulse output pin. The clock output from this pin enables the character pattern data, which is output from DO, to input to the SEGMENT drivers.
LOAD	O	Load signal output pin. The character pattern data to the SEGMENT drivers, which was output from DO and CP, is loaded to the LCD output of the SEGMENT drivers, synchronized with the COMMON signal.
DF	O	B-type AC signal output pin to drive the LCD.
COM1 ~ COM48	O	COMMON signal output pin to drive the LCD.
BUSY1 OUT	O	This pin shows the internal condition of MSM6262GS. "H" shows that MSM6262GS is in internal operation, while "L" shows that MSM6262GS is ready to receive the instruction from the CPU.
BUSY2 OUT	O	This pin shows that MSM6262GS is in internal operation based on the instruction from the CPU, or MSM-6262GS is in display rivising operation based on the instruction from the CPU. "H" shows that MSM6262GS is in internal operation, while "L" shows that the display on the LCD has been established and the MSM6262GS is ready to receive an instruction.

○ **Input pin**

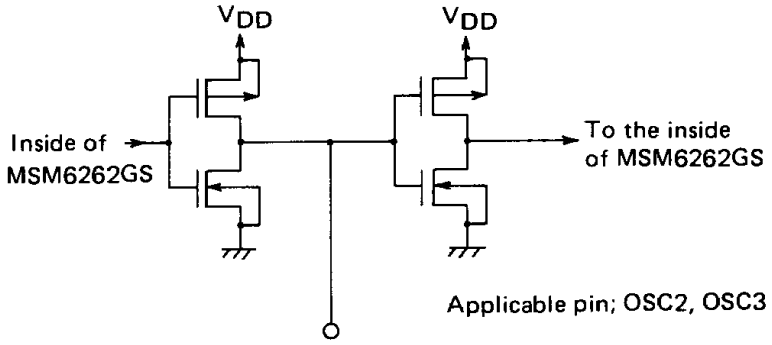


Applicable pin; OSC1, 68 series/80 series, $\overline{CS}$
R/$\overline{W}$ ($\overline{WR}$), E ($\overline{RD}$)
A0, A1

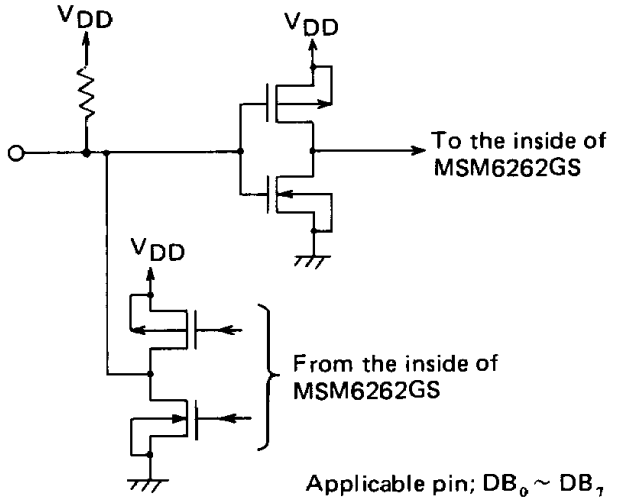


Applicable pin; $\overline{RESET}$

○ **Input/Output pin**

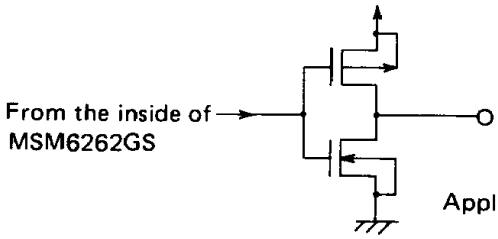


Applicable pin; OSC2, OSC3



Applicable pin; $DB_0 \sim DB_7$

○ **Output pin**



Applicable pin; CP, L, DF, DO,
BUSY1 OUT, BUSY2 OUT

FUNCTIONAL DESCRIPTION

1. Instruction Registor (IR) and Data Registor (DR)

The MSM62626S has two registors, instruction registor (IR) and data registor (DR).
IR is used to store the address code or instruction code of display data RAM (DD RAM) or character generator RAM (CG RAM).
This resistor can be written by the CPU, but can not be read out by the CPU but for some cases.
DR is used to store the data to write into (or read out) the data to/from DD RAM or CG RAM.
The data written into DR by the CPU is automatically written into the DD RAM or CG RAM.
When an address code is written into IR, the data of the specified address is automatically transferred to the DR from either DD RAM or CG RAM. By having the CPU subsequently read the DR (from the DR data), it is possible to verify DD RAM or CG RAM data.
After the writing of DR by the CPU, the DD RAM or CG RAM of the next address is selected to be ready for the next CPU writing.
Likewise, after the reading operation of the CPU, DD RAM or CG RAM data of the next address is transferred to the DR, when CPU is ready for the next reading operation.

2. Busy Flag (BF)

When the output of BUSY1 OUT is "H", MSM6262GS is engaged in internal operation.
When the output of BUSY2 OUT is "H", it indicates that MSM6262GS is engaged in internal operation or MSM6262GS is engaged in the revising of the display of the first line on the LCD. (Refer to the instruction table.)
When the output of BUSY1 OUT is "H", any input of new instruction is ignored. So, before setting a new instruction, it is necessary to check whether BUSY1 OUT and BUSY2 OUT are at "L".

3. Address Counter (ADC)

The address counter (ADC) allocates the address for the DDRAM and CG RAM write/read and also for the cursor display.
When the instruction code for a DD RAM address or CG RAM address setting is input to IR, after deciding whether it is DD RAM or CG RAM, the address counter code is transferred from IR to ADC. After writing (reading) the display data to (from) the DD RAM or CG RAM, the ADC increments (or decrements) by 1 automatically as its internal operation.

4. Timing Generator Circuit

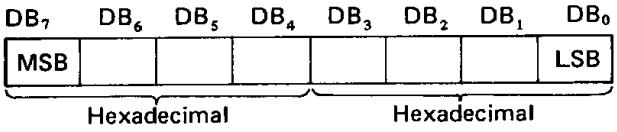
This circuit generates the timing signal for the internal operation by CPU's instruction as well as to operate the internal circuit of DD RAM, CG RAM, CG ROM and so forth. It also generates the transfer signal to the SEGMENT driver (MSM5839CGS or MSM5259GS).
The internal operation accessed by the CPU and internal operation for LCD display is independent. So, blinking on the LCD, other than the corresponding display of the newly written data, does not occur even when the data is written from the CPU to the DD RAM.

5. Display Data RAM (DD RAM)

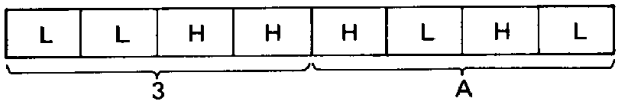
DD RAM is used to store the 8-bits character code (refer to Table 2) and 1-bit under-line data.
The address of DD RAM corresponds to the display position on the LCD. The correspondence is described below.

DD RAM address (set to ADC) is described as hexadecimal.

ADC



Example: When DD RAM address is 3A



(1) Relation between DD RAM and display position in 2-lines display mode

	Digit 1	2	3	4	5	~	79	80 ← Display position
1st line	00	01	02	03	04	~	4E	4F ← DD RAM address (hexadecimal)
2nd line	80	81	82	83	84	~	CE	CF

Note: The address of the last digit of the first line and the first digit of the second line does not have any continuity.

When 2 pieces of MSM5839CGS (or MSM5259GS) are connected to MSM6262GS, 32 characters can be displayed from the first digit to the 16th digit.

	Digit 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1st line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
2nd line	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F

MSM5839CGS (1) or MSM5259GS (1) — MSM5839CGS (2) MSM5259GS (2)

When the display is shifted by an instruction, the relation between the DD RAM address and the display position becomes as follows.

(Shift to right direction)

Digit	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1st line	4F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E
2nd line	CF	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E

MSM5839CGS (1) or MSM5259GS (1) — MSM5839CGS (2) MSM5259GS (2)

1st line	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
2nd line	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90

(Shift to left direction)

The maximum DD RAM capacity of MSM6262GS is for 160 characters. So, maximum 10 pieces of MSM5839CGS (or MSM5259GS) can be connected in case of 2-lines display mode.

Digit	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	~	73	74	75	76	77	78	79	80
1st line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	~	48	49	4A	4B	4C	4D	4E	4F
2nd line	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90	91	~	C8	C9	CA	CB	CC	CD	CE	CF

MSM5839CGS (1) or MSM5259GS (1) — MSM5839CGS (2) MSM5259GS (2) — MSM5839CGS (3)~(9) MSM5259GS (3)~(9) — MSM5839CGS (10) MSM5259GS (10)

(2) Relation between the DD RAM and display position in 4-lines display mode

Digit	1	2	3	4	5	~	39	40	← Display position
1st line	00	01	02	03	04	~	26	27	
2nd line	40	41	42	43	44	~	66	67	DD RAM address (hexadecimal)
3rd line	80	81	82	83	84	~	A6	A7	
4th line	C0	C1	C2	C3	C4	~	E6	E7	

Note: The address of the previous line and the first address of the next line does not have any continuity.

When 2 pieces of MSM5839CGS (or MSM5259GS) are connected to MSM6262GS, 64 characters can be displayed from the first digit to the 16th digit.

Digit	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1st line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
2nd line	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F
3rd line	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F
4th line	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CB	CF

MSM5839CGS (1) or MSM5259GS (1) — MSM5839CGS (2) MSM5259GS (2)

When the display is shifted by an instruction, the relation between the DD RAM address and the display position becomes as follows.

(shift to right direction)

Digit	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1st line	27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E
2nd line	67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E
3rd line	A7	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E
4th line	E7	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE

MSM5839CGS (1) MSM5259GS (1) — MSM5839CGS (2) MSM5259GS (2)

1st line	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
2nd line	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50
3rd line	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90
4th line	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0

(shift to left direction)

The maximum DD RAM capacity of MSM6262GS is for 160 characters. So, maximum 5 pieces of MSM5839CGS (or MSM5259GS) can be connected in case of 4-lines display mode.

Digit	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	~	33	34	35	36	37	38	39	40
1st line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	~	20	21	22	23	24	25	26	27
2nd line	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	~	60	61	62	63	64	65	66	67
3td line	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90	91	~	A0	A1	A2	A3	A4	A5	A6	A7
4th line	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	~	E0	E1	E2	E3	E4	E5	E6	E7

MSM5839CGS (1) or MSM5259GS (1) — MSM5839CGS (2) MSM5259GS (2) — MSM5839CGS (3), (4) MSM5259GS (3), (4) — MSM5839CGS (5) MSM5259GS (5)

6. Cursor/Blink Control Circuit

This is the circuit to control the generation of cursor and its blinking. This circuit is controlled by the program of the CPU.
The position of the cursor and its blink appears on the position according to the ADC contents, which corresponds to the address of DD RAM, For example, when the ADC is set as 07, the position of cursor and its blinking become as follows.

	DB7			~				DB0
ADC	0	0	0	0	0	1	1	1
	0				7			

2-lines display

Cursor and its blinking position

Digit 1	2	3	4	5	6	7	8	9	~	79	80
00	01	02	03	04	05	06	07	08	~	4E	4F
80	81	83	83	84	85	86	87	88	~	CE	CF

4-lines display

Cursor and its blinking position

Digit 1	2	3	4	5	6	7	8	9	~	39	40
00	01	02	03	04	05	06	07	08	~	26	27
40	41	42	43	44	45	46	47	48	~	66	67
80	81	82	83	84	85	86	87	88	~	A6	A7
C0	C1	C2	C3	C4	C5	C6	C7	C8	~	E6	E7

Note: Cursor display and blinking can be performed even when the CG RAM address is set in the ADC. So, it is necessary to disable the cursor display and blinking when the CG RAM address is set in the ADC.

7. Underline Control Circuit

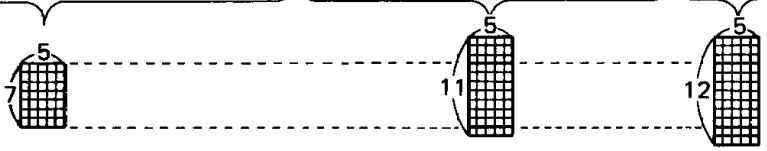
First, whether underline display mode or underline blinking mode has to be set by the CPU.
When an instruction to enable the underline function is input from the CPU, the cursor display shifts to the right direction (increment) or left direction (decrement). Display of underline appears (or disappears) on the same position where cursor was displayed.
An input of "H" data enables the underline display, while an input of "L" data enables to disappear the display of underline.

8. Character Generator ROM (CG ROM)

CG ROM stores the character pattern. MSM6262GS has 128 kinds of 5 x 7 dots pattern, 96 kinds of 5 x 11 dots pattern and 32 kinds of 5 x 12 dots pattern. The character pattern corresponds to the character code which is written into the DD RAM.
The relation between 8-bits character code and character pattern is described in Table 2.
When the 8-bits character code of CG ROM is written into the DD RAM, the character pattern of the corresponding character code of the CG ROM is displayed on the LCD position corresponding to the DD RAM address.
When all of the upper 4-bits of CR ROM code is "L", CG ROM can be switched to CG RAM.

Table 2 Relation between character code and character pattern

Upper / Lower 4-bit	0000 (0)	0001 (1)	0010 (2)	0011 (3)	0100 (4)	0101 (5)	0110 (6)	0111 (7)	1000 (8)	1001 (9)	1010 (A)	1011 (B)	1100 (C)	1101 (D)	1110 (E)	1111 (F)
0000 (0)	a	α		0	@	P	`	p	à	ó		−	タ	ミ	Å	Ó
0001 (1)	O	β	!	1	A	Q	a	q	ä	ö	。	ア	チ	ム	À	Ö
0010 (2)	↑	γ	"	2	B	R	b	r	á	ō	「	イ	ツ	メ	Á	Ō
0011 (3)	↓	δ	#	3	C	S	c	s	ä	œ	」	ウ	テ	モ	Ä	Œ
0100 (4)	±	ε	$	4	D	T	d	t	ā	æ	、	エ	ト	ヤ	Ā	Æ
0101 (5)	£	θ	%	5	E	U	e	u	è	ù	。	オ	ナ	ユ	È	Ù
0110 (6)	\	λ	&	6	F	V	f	v	é	ú	ヲ	カ	ニ	ヨ	É	Ú
0111 (7)		μ	'	7	G	W	g	w	ë	ü	ァ	キ	ヌ	ラ	Ë	Ü
1000 (8)	~	ν	(	8	H	X	h	x	ē	ū	ィ	ク	ネ	リ	E	Ū
1001 (9)	φ	π	)	9	I	Y	i	y	ì	ç	ゥ	ケ	ノ	ル	ì	ÿ
1010 (A)	ō	ρ	*	:	J	Z	j	z	í	≠	ェ	コ	ハ	レ	í	√
1011 (B)	F_r	σ	+	;	K	[	k	{	ï	千	ォ	サ	ヒ	ロ	ï	≅
1100 (C)	¢	Σ	,	<	L	¥	ℓ	|	ī	万	ャ	シ	フ	ワ	ī	§
1101 (D)	!!	÷	−	=	M	]	m	}	ì	²	ュ	ス	ヘ	ン	¿	n
1110 (E)	ω	φ	.	>	N	^	n	→	ñ	½	ョ	セ	ホ	:	Ñ	¼
1111 (F)	Ω	∞	/	?	O	_	o	←	ò	¾	ッ	ソ	マ	°	ò	
Configuration	5 x 7 dots								5 x 11 dots						5 x 12 dots	



8. Character Generator RAM (CG RAM)

The CG RAM is used to display user's original character pattern other than CG ROM.
The CG RAM has capacity (32 byte = 256 bits) to write 4 kinds of 5 x 8 dots and 2 kinds of 5 x 12 dots.
In displaying the character pattern stored in the CG RAM, CG RAM has to be enabled by an instruction. When CG RAM is enabled, CG ROM code for 16 characters cannot be read out as the character code with all "L" on the upper 4-bits is used as CG RAM code.
The following describes how to write and read the character pattern to and from the CG RAM.

(1) When the character pattern is 5 x 8 dots (See Table 3-1)

- **A method to write character pattern into the CG RAM by the CPU**

  3 bits of the CG RAM address (0 ~ 2) correspond to the line position of the character pattern. 2 bits of the CG RAM address (3, 4) correspond to the lower 2-bits of the character code.
  First, set increment or decrement by the CPU, and then input the CG RAM address. After this, write character pattern codes into CG RAM through DB_0 ~ DB_7 line by line.
  DB_0 to DB_7 correspond to CG RAM data 0 ~ 7 in Table 3-1.
  It is displayed when "H" is set as input data and is not display when "L" is set as input data.
  Since the ADC is automatically incremented or decremented by 1 after the writing of data to the CG RAM, it is not necessary to set the CG RAM address again.
  The line, the CG RAM address 0 ~ 2 of which are all "H" ("7" in hexadecimal notation), is the cursor position. It is ORed with the cursor at the cursor position and displayed to LCD.
  For this reason, it is necessary to set all input data that become cursor positions to "L".
  Although CG RAM data 0 ~ 4 bit are output to the LCD as display data, CG RAM data bit 5 ~ 7 are not. The latter can be written and read to and from the RAM, it is therefore allowed to be used as data RAM.
  Accordingly, it is necessary to set all input data which become cursor positions to "H". 0 ~ 4 bit of CG RAM data are output to the LCD as the display data, however, 5 ~ 7 bit of CG RAM data are not. But it can be used as RAM because data can be written/read into/from it.

- **A method to display the CG RAM character pattern to the LCD**

  First, an instruction to enable the CG RAM has to be input from the CPU. CG RAM is selected only when the upper 4 bits are all "L".
  So, the character pattern of CG RAM is displayed on the LCD position, corresponds to the CG RAM, when a character code shown in Table 3-1 is written into DD RAM. Since the 2 and 3 bit of the character code is regarded as invalid, "K" is displayed when the character code is "01", "05", "09", and "0D".

(2) When the character pattern ◆ 5 x 12 dots (See Table 3-2)

- **A method to write character pattern into the CG RAM by the CPU**

  4 bits of CG RAM address (0 ~ 3) correspond to the line position of the character pattern. CG RAM address bit 4 corresponds to the bit 1 of the character code.
  First, set increment or decrement by the CPU, and then input the address of the CG RAM.
  After this, write the character pattern code into the CG RAM, line by line from DB_0 ~ DB_7.
  DB_0 to DB_7 correspond to CG RAM data, bit 0 ~ 7, in Table 3-2.
  It is displayed when "H" is set as the input data, while it is not displayed when "L" is set as the input data.
  As the ADC is automatically incremented or decremented by 1 after the writing of data to the CG RAM, it is not necessary to set the CG RAM address again.
  The line, the CG RAM address of which is "0B" or "1B" (hexadecimal), is the position of the cursor. It is ORed with cursor at the cursor position and is displayed on the LCD. So,

all of the input data for the position of the cursor have to be "L" when cursor display is required.
When the CG RAM data, bit 0 ~ 4, CG RAM address, bit 0 ~ 4, is "0" ~ "B", it is displayed on the LCD as the display data. When the CG RAM data, bit of 5 ~ 7, and CG RAM, bit data is 0 ~ 4 and CG RAM address data is "C" ~ "F", it is not output to the LCD.
But in this case, CG RAM can be used as RAM and it can be written into/read out. So, it can be used as the data RAM.

- **A method to display the CG RAM character pattern on the LCD.**

  First, an instruction to enable the CG RAM has to be input from the CPU. CG RAM is selected only when all of upper 4 bits data of the character code is Table 2 is "L" So, CG RAM character pattern is displayed on the LCD position corresponding to the DD RAM address when the character code is Table 3-2 is written into the DD RAM.
  Since the address bit of 0, 2 and 3 are regarded as invalid, the character of " " is display when the character code is "00", "01", "04", "05", "08", "09", "0C" and "0D."

(3) A method to read out the CG RAM data

First, set the CG RAM address by inputting a CG RAM address set instruction from the CPU. Then, execute the CG RAM/DD RAM data read instruction. The set data of CG RAM address is output to the DB_0 ~ DB_7. The 8-bits data, read out from the MSM6262GS, corresponds to the data which is written into the CG RAM. Since the CG RAM address is automatically incremented or decremented by +1 (or −1), the CG RAM read out instruction can be successfully input. It is necessary, however, to set the DD RAM at data transferring condition by executing the DD RAM address set instruction after all of CG RAM data are read out.

Table 3-1.

CG RAM	CG RAM	DD RAM CHARACTER CODE
4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
LSB	MSB LSB	MSB LSB
L L L L L	X X X L H H H L	
L L H	H L L L H	
L H L	H L L L H	
L H H	H L L L H	L L L L X X L L
H L L	H L L L H	
H L H	H L L L H	
H H L	L H H H L	
H H H	L L L L L	
L H L L L	X X X H L L L H	
L L H	H L L H L	
L H L	H L H L L	
L H H	H H L L L	
H L L	H L H L L	L L L L X X L H
H L H	H L L H L	
H H L	H L L L H	
H H H	L L L L L	
H H L L L	X X X L H H H L	
L L H	L L H L L	
L H L	L L H L L	
L H H	L L H L L	L L L L X X H
H L L	L L H L L	
H L H	L L H L L	
H H L	L H H H L	
H H H	L L L L L	

X: DON'T CARE

Table 3-2.

CG RAM ADDRESS					CG RAM DATA								DD RAM CHARACTER CODE							
4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
				LSB	MSB							LSB	MSB							LSB
L	L	L	L	L	X	X	X	L	L	L	L	L								
	L	L	L	H				L	L	L	L	L								
	L	L	H	L				L	L	L	L	L								
	L	L	H	H				L	H	L	L	L								
	L	H	L	L				L	H	H	H	H								
	L	H	L	H				H	L	L	H	L								
	L	H	H	L				L	H	H	H	H								
	L	H	H	H				L	H	L	H	L								
	H	L	L	L				H	H	H	H	H								
	H	L	L	H				L	L	L	H	L								
	H	L	H	L				L	L	L	L	L								
	H	L	H	H				L	L	L	L	L								
	H	H	L	L																
	H	H	L	H																
	H	H	H	L																
	H	H	H	H																
H	L	L	L	L	X	X	X	L	L	L	L	L								
	L	L	L	H				L	L	L	L	L								
	L	L	H	L				L	L	L	L	L								
	L	L	H	H				L	L	L	L	L								
	L	H	L	L				L	L	L	L	L								
	L	H	L	H				H	L	L	L	H	L	L	L	L	X	X	H	X
	L	H	H	L				H	L	L	L	H								
	L	H	H	H				L	H	L	H	L								
	H	L	L	L				L	L	H	L	L								
	H	L	L	H				L	H	L	L	L								
	H	L	H	L				H	L	L	L	L								
	H	L	H	H				L	L	L	L	L								
	H	H	L	L				X	X	X	X	X								
	H	H	L	H																
	H	H	H	L																
	H	H	H	H																

X: DON'T CARE

9. LCD Display Circuit (COM1 ~ COM48, DO, CP, LOAD, DF)

The MSM6262GS is provided with COMMON signal output. So, maximum 160 characters can be displayed when it is used together with SEGMENT drivers (MSM5259GS or MSM5839CGS).
Interface between MSM6262GS and SEGMENT drivers can be done by using DO, CP, LOAD and DF.
The SEGMENT data is serially input to the SEGMENT driver from DO terminal, synchronized with the pulse which is output from the CP signal.
This data, input to the SEGMENT driver, is converted from serial data to parallel data by the latch pulse which is output from the LOAD terminal of MSM6262 and this converted data is used as the display data. This parallel/serial conversion is performed synchronized with the COMMON signal of MSM6262GS and LCD display AC signal which is output from DF terminal. So, this signal can drive dot matrix LCD panel.

10. Reset Circuit

Power-on-reset is required for MSM6262GS when it is powered-on. So, a condensor has to be connected between $\overline{\text{RESET}}$ terminal and V_{SS} terminal.
It is also advisable to connect a diode between $\overline{\text{RESET}}$ terminal and V_{SS} terminal when it is required to connect a condensor of more than 3.3 μF to $\overline{\text{RESET}}$ terminal.
When the power-on reset circuit normally operate, the busy flag 1 and 2 becomes at "H" level for about 10 ms after the power-on. During this period, a initialization of MSM6262GS is performed by following procedures.

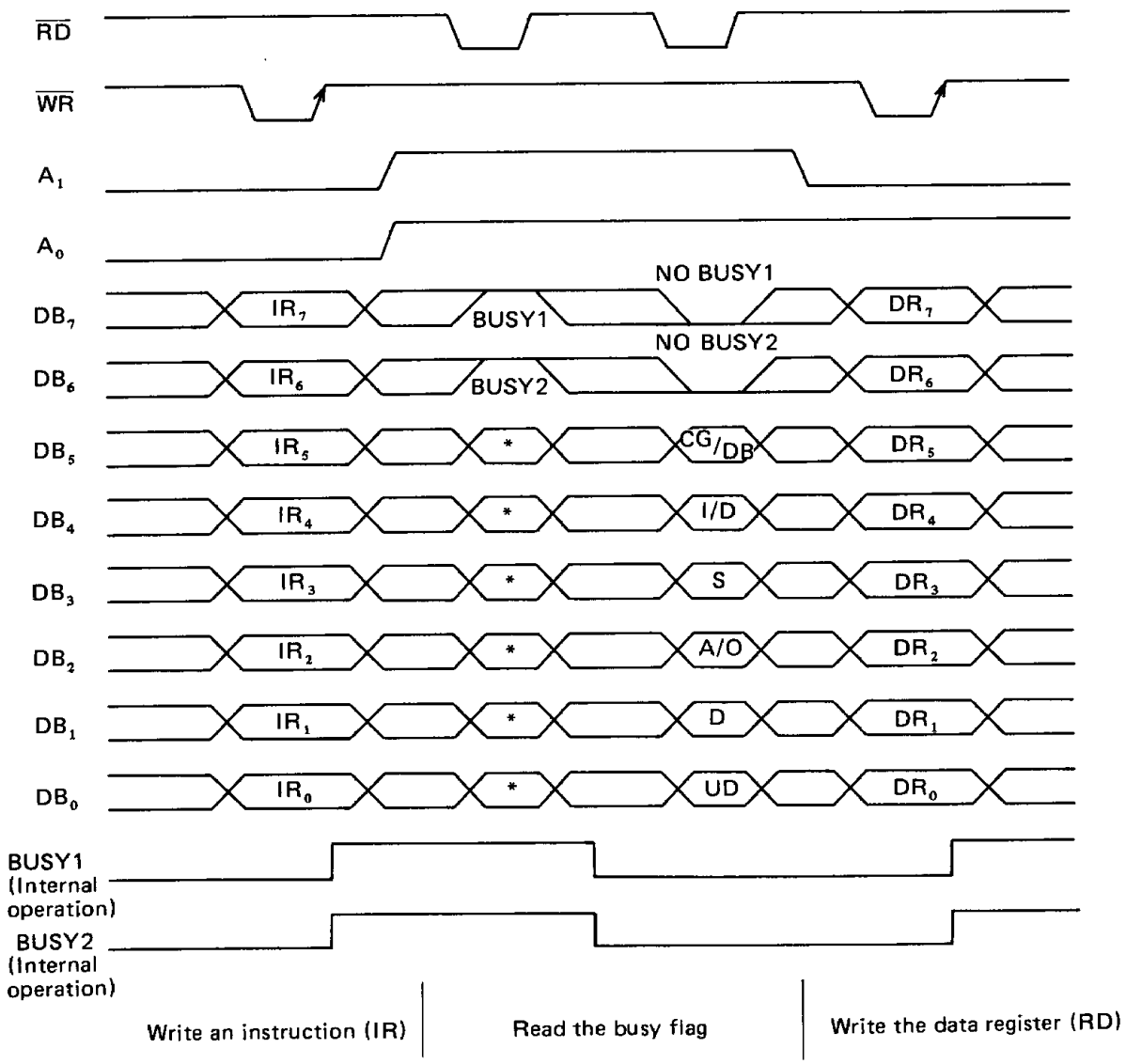
1 Display clear
2 CG ROM becomes ENABLE
3 No display shift
4 Increment of ADC
5 2-line display mode
6 5 x 8 dots font configuration
7 No display shift for "g", "j", "p", "q" and "y".
8 Display off
9 No display of cursor, blinking and underline

11. Data Bus with CPU

MSM6262GS can be interfaced with 8-bit CPU, such as 6809, Z80, 80C49 and 80C51. When MSM6262GS is connected with 6809, 68 series/80 series terminal has to be connected to V_{DD}. When MSM6262GS is connected with Z80, 80C49 or 80C51, 68 series/80 series terminal has to be connected to V_{SS}.
68 series/80 series level cannot be switched during MSM6262GS's operation. It has to be connected with either V_{DD} or V_{SS} before MSM6262GS is powered-on.

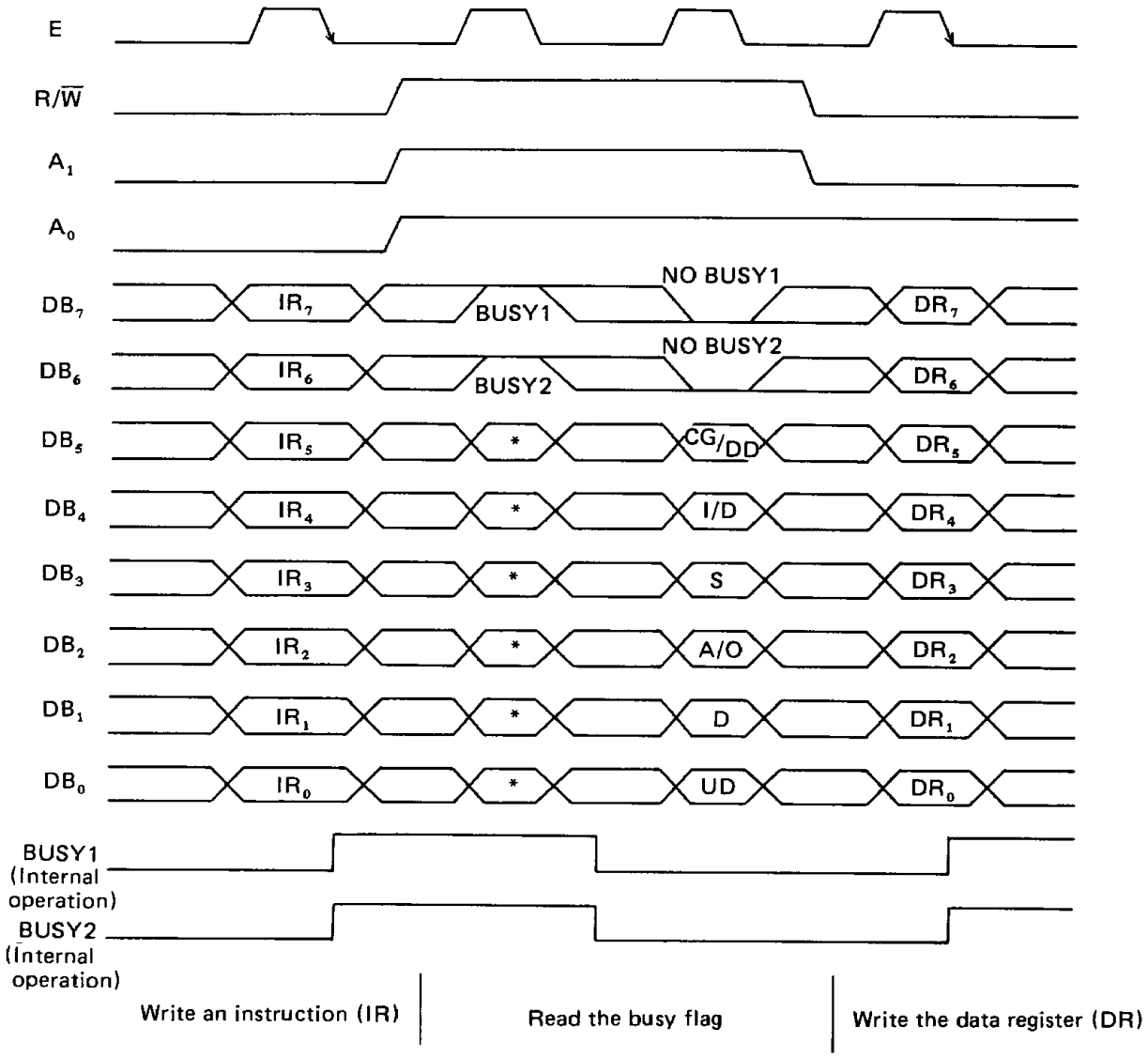
Note: When a reset signal is being input to $\overline{\text{RESET}}$ terminal, 68 series/80 series terminal's level can be switched. Since 68 series/80 series terminal does not have a switching characteristics nor V_T characteristics to have a interface with MCU nor it does not have an anti-chaterring circuit. So, this method is not a recommendable one since MSM6262GS is initialized when a reset signal is input.

80 series CPU data transfer



Note: * DON'T CARE

68 series CPU data transfer



Note: * DON'T CARE

INSTRUCTION TABLE

Note 1: In case of 80 series CPU, access to MSM6262GS is done by WR and RD. So, a bit for part of the read/write code is not required

* : DON'T CARE

80 series CPU / 68 series CPU	Note 1	A_1	A_0	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	Explanation	Execution Time (MAX) fosc-500kHz
	R/W	A_1	A_0	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0		
Display Clear	L	L	L	L	L	L	L	L	L	L	H	First, clear all of the display. Then set 0 address of DD RAM in the address counter.	3.22 ms
Return	L	L	L	L	L	L	L	L	L	H	CR/C	CR/C = L; Cursor home CR/C = H; Carriage Return	1.62 ms
Under Line	L	L	L	L	L	L	L	L	H	UL	*	UL = 1; Write the underline in the cursor part before executing this instruction. UL = 0; Erase the underline in the cursor part before executing this instruction.	20 μs
Entry Mode Set	L	L	L	L	L	L	L	H	I/D	S	A/O	This instruction (S) set whether the display of the direction of cursor (I/D) should be shifted or not. When the data is being written or read, this operation is performed. This instruction also set whether the character code of DD RAM is used as CG ROM or CG RAM. (A/O)	20 μs
Display/Cursor Shift	L	L	L	L	L	L	H	S/C	UD/RL	D_2 UR/DL	D_1 (*)	This instruction shift the cursor and display without changing the DD RAM contents. (S/C, UD/RL, UR/DL)	20 μs
CG RAM address Set	L	L	L	L	L	H	A_{CG}					This instruction set the CG RAM address. The data, which will be sent/received after the CG RAM address is set, is CG RAM data.	20 μs
Function Set	L	L	L	L	H	N	*	F_1	F_2	F_3	*	This instruction set followings. No. of lines (N), Character font (F_1), Cursor line font (F_2), Font shift of "g, j, p, q, y" (F_3)	20 μs
Display Control	L	L	L	H	D	C	B	UC	UB	*	*	This instruction set followings. All display on/off (D), Cursor display on/off (C), Character on the cursor position on/off (B), Underline display on/off (UC), Character, on the underline, blink on/off (UB)	20 μs
CG RAM/DD RAM Data Write	L	L	H	WRITE DATA								Write a data in either DD RAM or CG RAM	20 μs
DD RAM Address Set	L	H	L	A_{DD}								Set DD RAM address. The data which is sent/received after that is DD RAM data.	20 μs
Read the Underlined Data	H	L	L	ULD	RAM DATA							Read following data. Data on the underline, DD RAM or CG RAM data.	20 μs
Read the CG RAM/DD RAM Data	H	L	H	READ DATA								Read the data either from DD RAM or CG RAM.	20 μs
Read the Address Counter Content	H	H	L	A_{DC}								Read the address counter contents.	20 μs
Read Busy Flag	H	H	H	B1F	B2F	CG/DD	I/D	S	A/O	D	UD	Busy 1 flag (B1F) which shows MSM6262GS's internal operation. Busy 2 flag (B2F) which shows that the revising of display starting line is going on. CG/DD shows whether the data, being transmitted or received, is CG RAM or DD RAM. I/D shows the direction of cursor. S shows the display shift. A/O shows when the DD RAM character code is CG ROM character code or CG RAM character code. D shows the all display on/off UD shows underline display on/off	0 μs

CR/C = H : Carriage Return
UL = H : Write under line
I/D = H : Increment
S = H : Accompany display shift
A/O = L : CG ROM ENABLE
S/C = H : Display move
UD/RL = H : Up/Down move
D_2, D_1 : The bit to set the line to be displayed in the upper-most position. D_1 is LSB. D_2 is MSB.
UR/DL = H : Upper-right move
N = L : 2 lines
N = H : 4 lines
F_1 = H : 5 x 11 dot
F_1^2 = L : 5 x 12 dots or 5 x 8 dots
F_3 = H : Shift "g, j, p, q, r" to the lower position by 1-dot.
ULD = H : Underline data exist
B1F = H : Internal operation
B2F = H : Revising the display starting line or internal operation
CG/DD = H : Transmit or receive CC RAM data

CR/C = L Cursor home
UL = L : Underline erase
I/D = L : Decrement

A/O = H : CG RAM ENABLE
S/C = L : Cursor move
UD/RL = L : Left/Right move

UR/DL = L : Down-left move

F_1 = L : 5 x 7 dots
F_2 = H : 5 x 11 dots or 5 x 7 dots
F_3 = L : Character shift disable

ULD = L : No underline data
B1F = L : Ready to receive instruction
B2F = L : No revision on display starting line
CG/DD = L : Transmit/Receive of DD RAM data

DD RAM : Display data RAM
CG RAM : Character generator RAM
A_{CG} : CG RAM address
A_{DD} : DD RAM address
A_{DC} : Address counter which is used for both DD RAM and CG RAM

In case of fosc = 600 kHz, it becomes $20\mu s \times \frac{500}{600} \fallingdotseq 16.7\mu s$

12. Instruction Code

The instruction code is defined as the signal through which the MSM6262GS is accessed by the CPU. MSM6262GS starts its operation upon receipt of the instruction code.
The internal processing operation starts with a timing that does not affect the LCD display, so, the busy condition is longer than that of cycle time.
In the busy condition, MSM6262GS does not execute any instruction other than the reading of busy flag. Therefore, the CPU has to verify that busy flag is set at "L" before inputting the instruction code.

(1) Display clear

	A_1	A_0	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	L	L	L	L	L	L	L	L	L	H

When this instruction is executed, the LCD display is cleared.
When the cursor and blink is being displayed, the blinking position moves to the left end of the LCD. (In case of 2-lines or 4-lines display mode, the position is the left end of the first line)
All of the DD RAM data becomes "20" (hex), space code, while ADC data becomes "00" (hex.). If display is shifted, it returns to the normal position.
Data for underline is re-written as "L" and display turns off.

(2) Return

	A_1	A_0	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	L	L	L	L	L	L	L	L	H	CR/C

- **CR/C = L (Cursor Home)**
  When this instruction is executed, cursor and blinking position move to the left end of the LCD. (In case of 2-lines or 4-lines display mode, it moves to the left end of the first line)
  When display is being shifted, the display returns to its original position for both parallely and vertically.
  ADC becomes "00" (hex.).
- **CR/C = H (Return)**
  When this instruction is executed, cursor and blinking position moves to the left end of the line.
  If the display is being shifted when this instruction was executed, only cursor and blinking position moves to the original position before it was shifted.
  All bit other than line specifying the bit of ADC will be reset to "L".

(3) Underline

	A_1	A_0	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	L	L	L	L	L	L	L	H	UL	*

* : DON'T CARE

- **UL = H (Write underline)**
  When this instruction is executed underline appears on the cursor position. Cursor will move to the right or left if either increment or decrement is specified.
- **UL = L (Erase underline)**
  When this instruction is executed, the underline on the cursor position disappears. Cursor will move to the right or left if either increment or decrement is specified.
  When this instruction is executed, ADC will be automatically incremented by +1 or decremented by −1. Display is shifted accordingly.

(4) Entry mode set

	A_1	A_0	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	L	L	L	L	L	L	H	I/D	S	A/O

- **I/D (Increment/Decrement)**
  When this instruction is executed, the character code or underline code is written into (or read out from) the DD RAM, DD RAM address will be incremented (I/D = H) or decremented (I/D = L) by 1.
  In case of decrement, cursor moves to the right, while cursor move to the left in case of decrement.
  It is same in case of writing/erasing the data into/from CG RAM.
- **S (Display shift in case of writing)**
  When S = L in case of writing data into DD RAM, display is shifted either to the right or left. When I/D = H, all display will shift to the left, while it will shift to the right when I/D = L. So, display of cursor looks being stopped and display itself looks being shifted.
  In case of reading the data from DD RAM, display shall not be shifted. In case of reading/writing the data from/to CG RAM, display shall not be shifted.
  In case of S = L, display shall not be shifted.
- **A/O (CG RAM ENABLE/CG ROM ENABLE)**
  When A/O is L, CG ROM will be enabled, and all CG ROM contents on Table 2 becomes selectable and CG RAM cannot be selected.
  CG RAM cannot be used as character code for display. But it can be used as data RAM.
  When A/O = H, CG RAM is enabled.
  In case the upper 4-bit of the character code in Table 2 is 0 (hex.), the bit pattern of CG RAM is displayed on the LCD. (CG RAM has a RAM area for 4 kinds of 5 x 8 dots and 2 kinds of 5 x 12 dots)
  CG ROM is selected when the upper 4-bit of the character code in Table 2 is 1 ~ F (hex.).

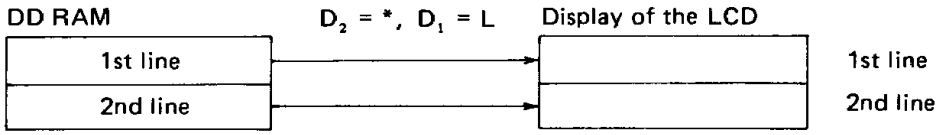
(5) Display/Cursor move

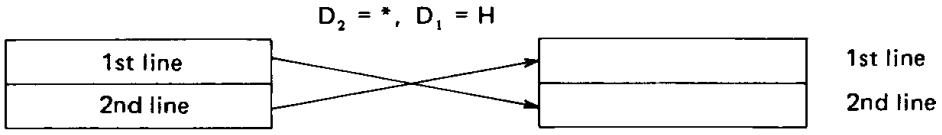
	A_1	A_0	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	L	L	L	L	L	H	S/C	UD/RL	D_2 (UR/DL)	D_1 (*)

* : DON'T CARE

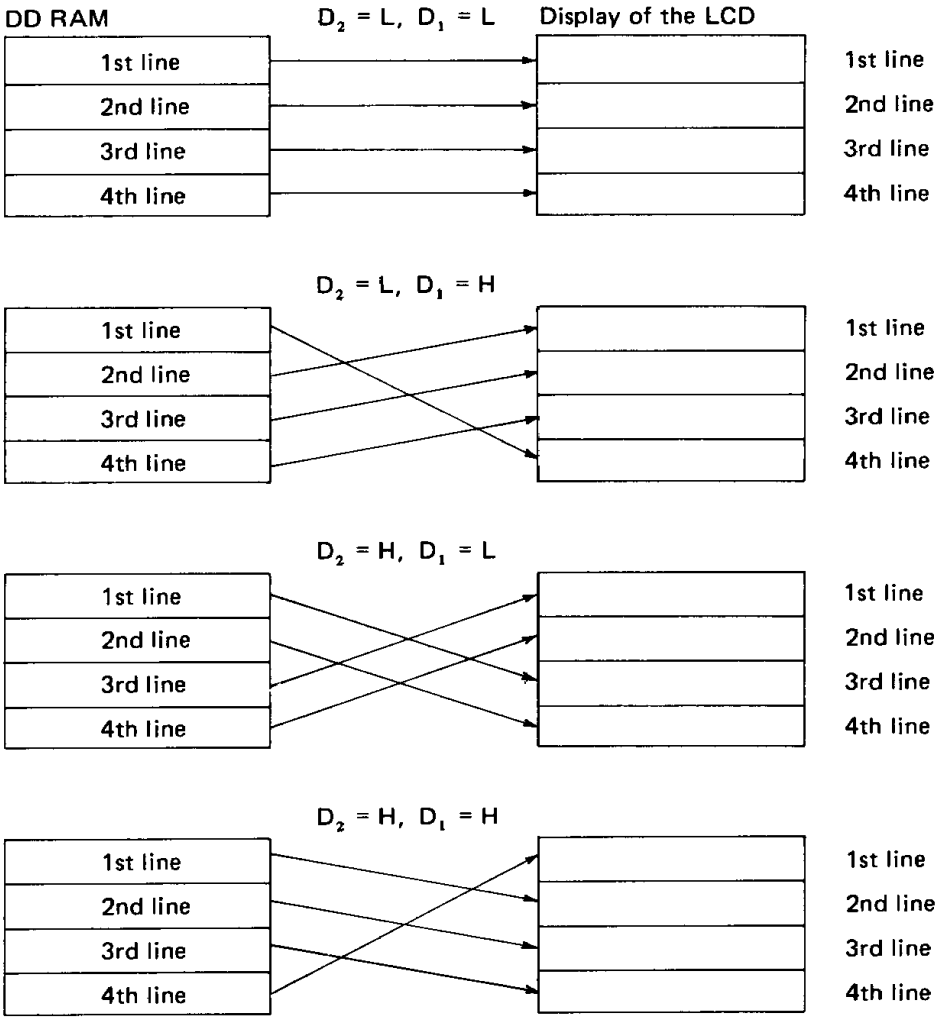
- **S/C (Display move/Corsor move)**
  This is the bit to select either display or cursor to move. S/C = H enables the display movement, while S/C = L enables the cursor movement.
- **UD/RL (Upward or Downward move/Right or left move)**
  UD/RL = H enables upward or downward move. UD/RL = L enables right or left move.
- **D_2, D_1 (Starting line of display)**
  Upward or downward movement is enabled by setting the starting line of display. D_1 is LSB and D_2 is MSB. Both D_1 and D_2 is expresed in 2-bit binary data.
  In case of 2-line mode, only D_1 is regarded as valid. Both D_1 and D_2 are regarded as valid data in case of 4-lines mode.

= 2-line mode =





= 4-line mode


DD RAM
D_2 = L, D_1 = L
Display of the LCD
1st line
2nd line
3rd line
4th line
1st line
2nd line
3rd line
4th line
D_2 = L, D_1 = H
1st line
2nd line
3rd line
4th line
1st line
2nd line
3rd line
4th line
D_2 = H, D_1 = L
1st line
2nd line
3rd line
4th line
1st line
2nd line
3rd line
4th line
D_2 = H, D_1 = H
1st line
2nd line
3rd line
4th line
1st line
2nd line
3rd line
4th line

- **UR/DL (Up-right move/Down-left move)**
  UR/DL = H enables up-right movement.
  UR/DL = L enables down-left movement.

  Combination of bit for Display/Cursor movement is as follows

S/C	UD/RL	D_2 (UR/DL)	D_1 *	Explanation
L	L	L	*	Move the cursor to the left by 1 digit
L	L	H	*	Move the cursor to the right by 1 digit
L	H	L	*	Move the cursor to the downward by 1 digit
L	H	H	*	Move the cursor to the upward by 1 digit
H	L	L	*	Move the display to the left by 1 digit
H	L	H	*	Move the display to the right by 1 digit
H	H	L	L	Set the first line as the display starting line
H	H	L	H	Set the 2nd line as the display starting line
H	H	H	L	Set the 3rd line as the display starting line ▲2
H	H	H	H	Set the 4th line as the display starting line ▲2

Note: In case of 2-line mode, ▲2 is invalid.

(6) CG RAM address set

	A_1	A_0	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	L	L	L	L	H	Ac_4	Ac_3	Ac_2	Ac_1	Ac_0

Set the CG RAM address which consists of 5-bit of $Ac_4 \sim Ac_0$. The data which will be transferred after this instruction is set shall be limited to the CG RAM data (character font data).

(7) Function set

Instruction set

A_1	A_0	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
L	L	L	H	N	*	F_1	F_2	F_3	*

* : DON'T CARE

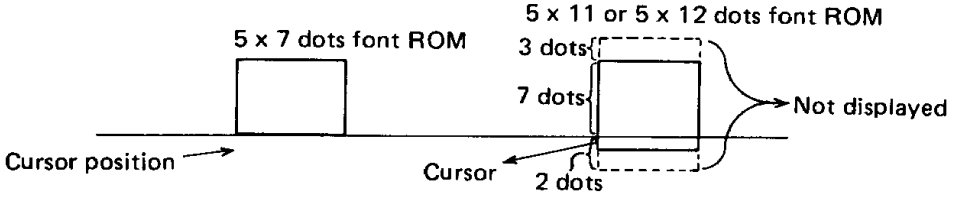
- N (4-line/2-line) LCD line selection

N	LCD lines
L	2-line mode
H	4-line mode

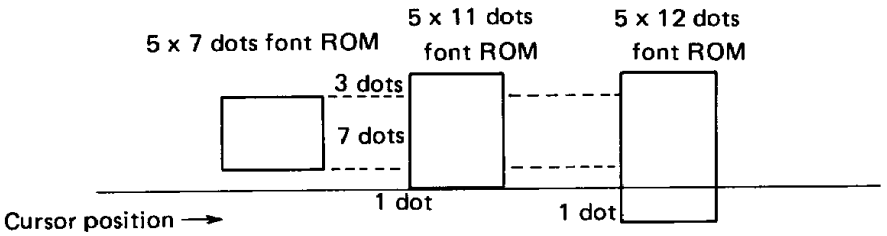
- **F_1 (5 x 11 dots/5 x 7 dots)**
  When F_1 = H, 5 x 12 dots/font is selected.
  When F_1 = L, 5 x 8 dots/font is selected.
- **F_2 (Font assignment of cursor line)**
  When F_2 = L and if character code, which has a display dot on the cursor position, is selected, it is displayed on the cursor line of LCD.
  When F_2 = H and if character code, which has a display dot on the cursor position, is selected, cursor is displayed but the bit on the cursor position is not displayed.
  In case of CG RAM, however, this function is not applicable and the bit on the cursor position is also displayed.
- **F_3 (Font shift of 'g, j, p, q, y')**
  When F_3 = H, the character font of 'g, j, p, q, y' is shifted to the downward by 1-bit.
  When F_3 = L, display is same as that described in Table 2. This bit is only valid in case of 5 x 12 dots/font.

Example

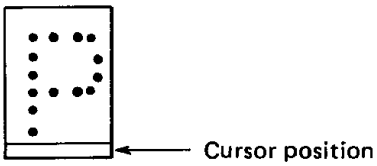
① F_1 = L (5 x 8 dots/font)



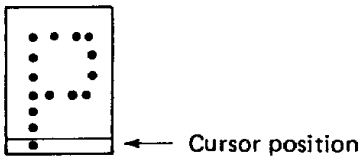
② F_1 = H (5 x 12 dots/font)



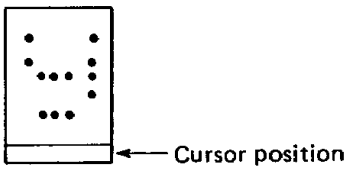
③ F_2 = H



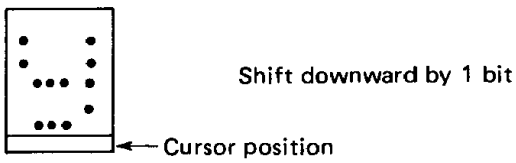
④ F_2 = L



⑤ F_3 = L



⑥ F_3 = H (5 x 12 dots/font only)



(8) Display control

Instruction code

A_1	A_0	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
L	L	H	D	C	B	UC	UB	*	*

* : DON'T CARE

- **D**
  When D = H, display on the LCD is enabled.
  When D = L, display is disabled.
  When display was disabled by setting D at L, character code is the DD RAM does not change. So, when D becomes at H again, display is enabled immediately.
- **C**
  When C = H, cursor display appears.
  When C = L cursor display disappears.
- **B**
  When B = H, blinking of character, on the position corresponding to the cursor position, starts. Blinking of all-dot's-on and character (and cursor)-on is performed alternately for every 409.6 ms in case of fosc = 500 kHz and 5 x 8 dots font configuration (every 614.4 ms in case of 5 x 12 dots font configuration)
  When B = L, blinking stops.
  Cursor and blinking can be set simultaneously.
- **UC**
  When UC = H, underline is displayed on the cursor position.
  When UC = L, underline display is disabled.
- **UB**
  When UB = H, blinking of character, on the position corresponding to the underline position, starts. Blinking of character stops when UB = L.
  Cursor, blink, underline and blinking of character on the underline can be set simultaneously.

(9) CG RAM and DD RAM data write

Instruction code

A_1	A_0	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
L	H	DI_7	DI_6	DI_5	DI_4	DI_3	DI_2	DI_1	DI_0

Write the 8-bit data (DI_7 ~ DI_0) into either CG RAM or DD RAM. Determination of either CG RAM or DD RAM is made by the CC RAM address set or DD RAM address set which shall be set in advance.
After the data was written into the RAM, it is incremented or decremented by 1 according to the entry mode of the address. Display shift will be also determined by the entry mode.

(10) DD RAM address set

	A_1	A_0	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	H	L	AI_7	AI_6	AI_5	AI_4	AI_3	AI_2	AI_1	AI_0

This instruction code set the DD RAM address, consists of 8-bit (AI_7 ~ AI_0). The data which is received after this instruction was set shall be limited to the DD RAM data (character code data).
The address code other than below shall not be input.

2-line mode : 1st line 00 ~ 4F
2nd line 80 ~ CF
4-line mode : 1st line 00 ~ 27
2nd line 40 ~ 67
3rd line 80 ~ A7
4th line C0 ~ E7

(11) Underline data read

	A_1	A_0	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	L	L	ULD	Do_6	Do_5	Do_4	Do_3	Do_2	Do_1	Do_0

This instruction read the 8-bit data (Do_7 ~ Do_0) from either CG RAM or DD RAM. Determination of CG RAM or DD RAM is made by the CG RAM address set or DD RAM set which shall be set in advance.
The first data read by this instruction is a valid data. Normal data is read out from the second instruction onward if the read instruction was executed continuously. This instruction address will be incremented or decremented by 1 according to the entry mode. Display shift is not, however, performed. Underline data is output to DB_7 as either H (when display is on) or L (when display is off).
The MSB of RAM data is not read. RAM data consists of 7-bit (DB_0 ~ DB_6)

(12) CG RAM and DD RAM data read

	A_1	A_0	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	L	H	Do_7	Do_6	Do_5	Do_4	Do_3	Do_2	Do_1	Do_0

This instruction read the 8-bit data ($Do_7 \sim Do_0$) from either CG RAM or DD RAM. Determination of CG RAM or DD RAM is made by the CG RAM address set or DD RAM address set which shall be set in advance.
CG RAM address set instruction or DD RAM address set instruction has to be input just before executing this read instruction. If it is not input, the first output of the data becomes invalid. When this read instruction is performed continuously, normal data is output from the 2nd data onward.
In case of DD RAM data read, normal data is output from the first data without inputting the address set under the condition that cursor is moved by the cursor shift instruction.
After reading the data, the address is incremented or decremented by 1 by the entry mode. The shift of the display, however, is not performed.

(13) Address counter read

	A_1	A_0	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	H	L	Ao_7	Ao_6	Ao_5	Ao_4	Ao_3	Ao_2	Ao_1	Ao_0

This instruction read the 8-bit data ($Ao_7 \sim Ao_0$). Address counter is determined by the address which shall be set in advance as it is used for both CG RAM and DD RAM.

(14) Busy flag read

	A_1	A_0	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	H	H	B1F	B2F	CG/DD	I/D	S	A/O	D	UD

- **B1F (Busy 1 flag)**
  When B1F = H, MSM6262GS is engaged in internal operation and next instruction is not accepted until when B1F becomes L. So, subsequent instruction has to be input after B1F is confirmed at L. During B1F = H, $DB_5 \sim DB_0$ cannot be determined.

- **B2F (Busy 2 flag)**
  B2F indicates that MSM6262GS is engaged in its internal operation and it also indicates that the display starting line is under being revised.
  Instruction contents of B1F and B2F is same other than when setting the starting line of display.
  B2F = H indicates that MSM6262GS is engaged in its internal operation. B2F = L indicates that MSM6262GS in ready for accepting new instruction.
  Even when B2F = H, new instruction can be accepted if B1F = L, When the starting line of display is revised under this condition, the previous set data about starting line of display becomes invalid and the newly input data about starting line becomes valid.

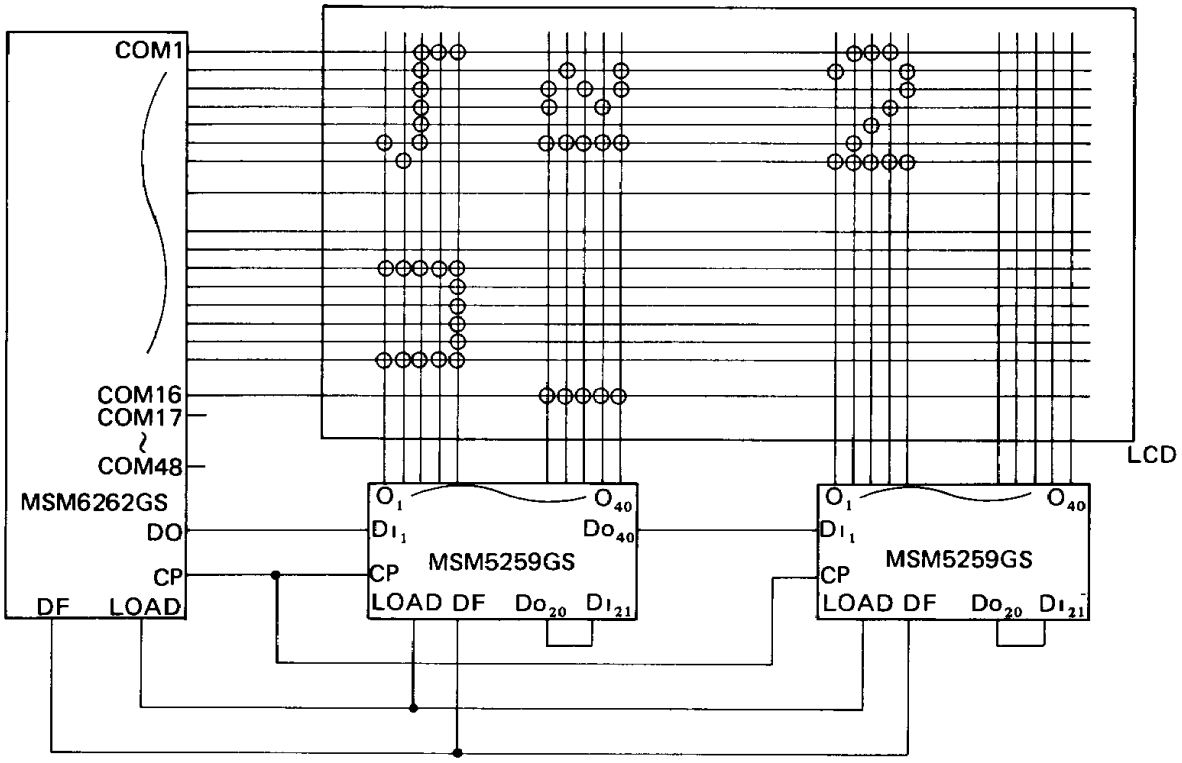
- **CG/DD (CG RAM/DD RAM)**
  This bit indicates whether the address counter contents is CG RAM or DD RAM when B1F = L. CG RAM is selected when CG/DD = H, while DD RAM is selected when CG/DD = L.
- **I/D (Increment/Decrement)**
  This is the bit to set the increment or decrement when B1F = L. Increment is selected when I/D = H, while decrement is selected when I/D = L.
- **S (Shift)**
  This is the bit to set the shift condition in the entry mode when B1F = L. Shift is set when S = H, while shift is disabled when S = L.
- **D (Display)**
  This is the bit to indicate whether the display, which was set by display control instruction, is on or off when B1F = L.
- **UD (Underline)**
  This is the bit to indicate the condition of underline or blinking on the underline, both of which were set by display control instruction, when B1F = L.
  When UD = H, either (or both of) underline display or blinking on the underline is being executed. When UD = L, it indicate neither of underline display nor blinking on the underline is performed.

1 Power on.
2 Wait for 15 msec or more after V_{DD} become at 4.5 V.
3 No busy 1 check (Check whether B1F = L or not)
4 Set No. of lines, character font by instruction. (After this stage, function set instruction cannot be input.)
5 No busy 1 check
6 Set display-off by inputting display control instruction.
7 No busy 1 check
8 Input display clear
9 No busy 1 check
10 Set entry mode
11 No busy 1 check
12 Set following functions.
Display on, Cursor, Blink, Underline Blink on the underline
13 No busy 1 check
14 Initialization complete

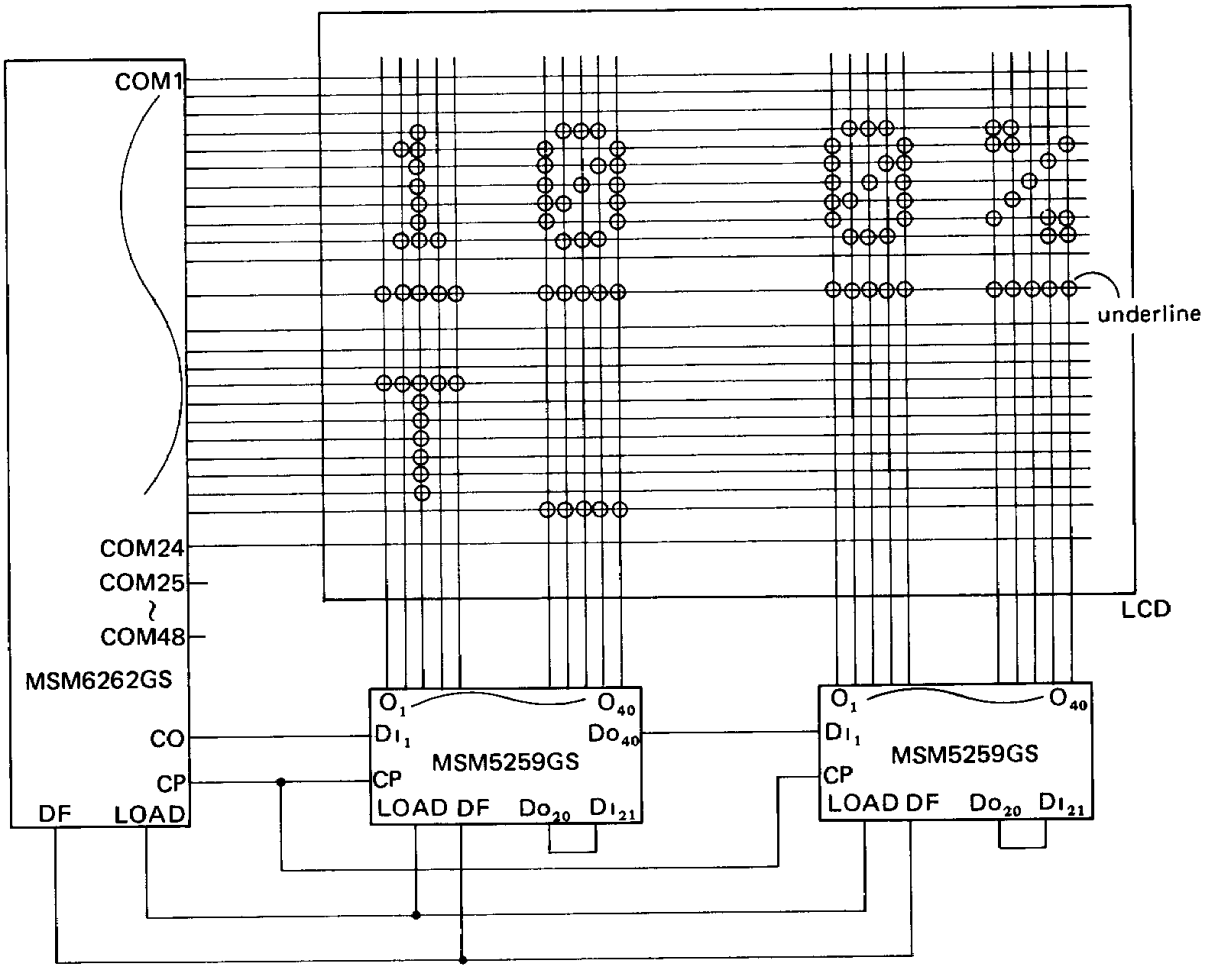
TYPICAL APPLICATION

- **Interface with MSM6262GS and LCD driver**
  When V_{LCD} is within the voltage range of $V_{DD} \sim V_{SS}$, MSM5259GS is recommendable as SEGMENT driver. When V_{LCD} is beyond the voltage range of $V_{DD} \sim V_{SS}$, MSM5839CGS is recommendable as SEGMENT driver.

1 2-line display mode
5 x 7 dots/font, 16 characters/line
(Note: COM17 ~ COM48 should be left open)



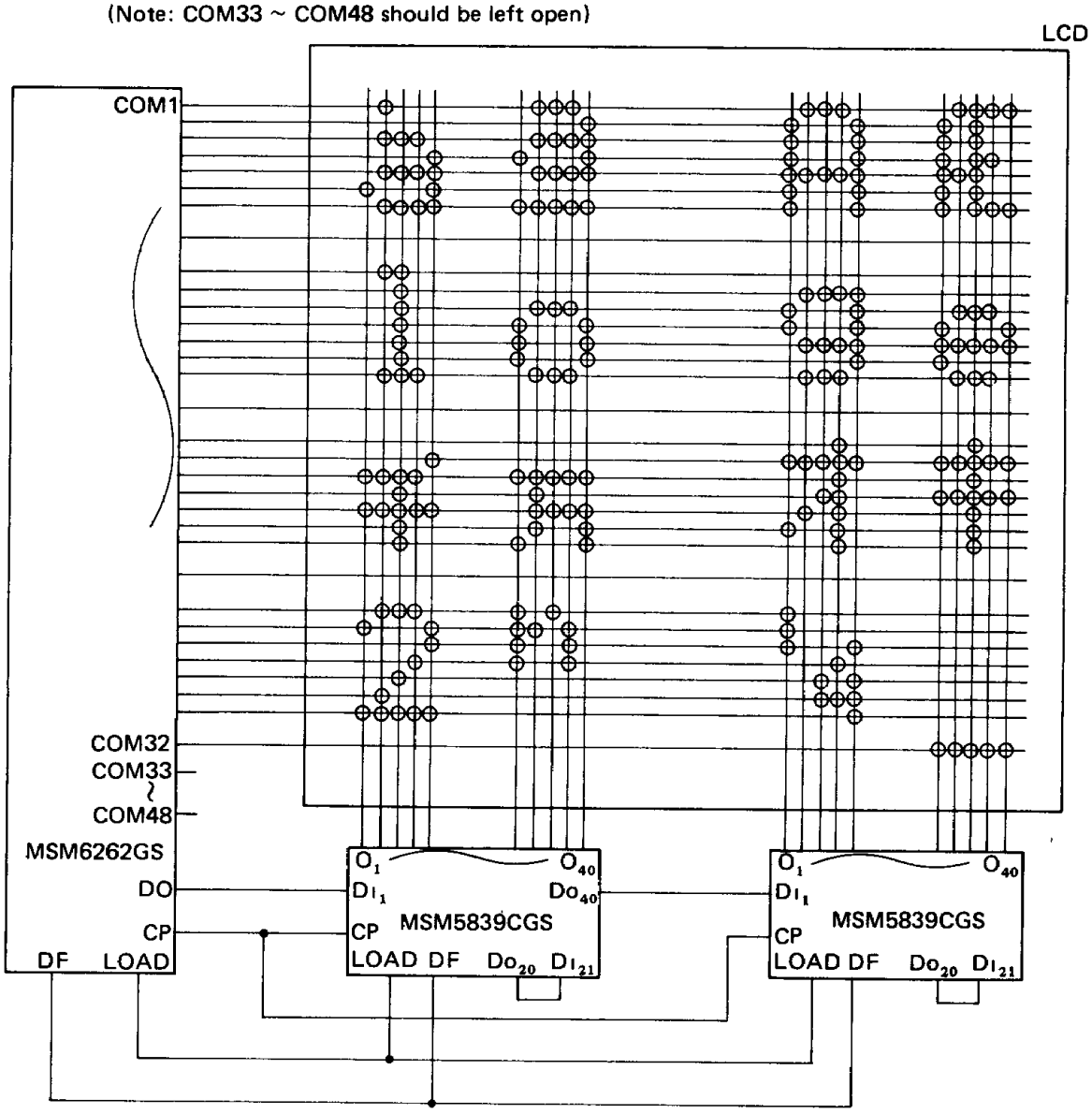
2 2-line display mode
5 x 11 dots/font, 16 characters/line
(Note: COM25 ~ COM48 should be left open)



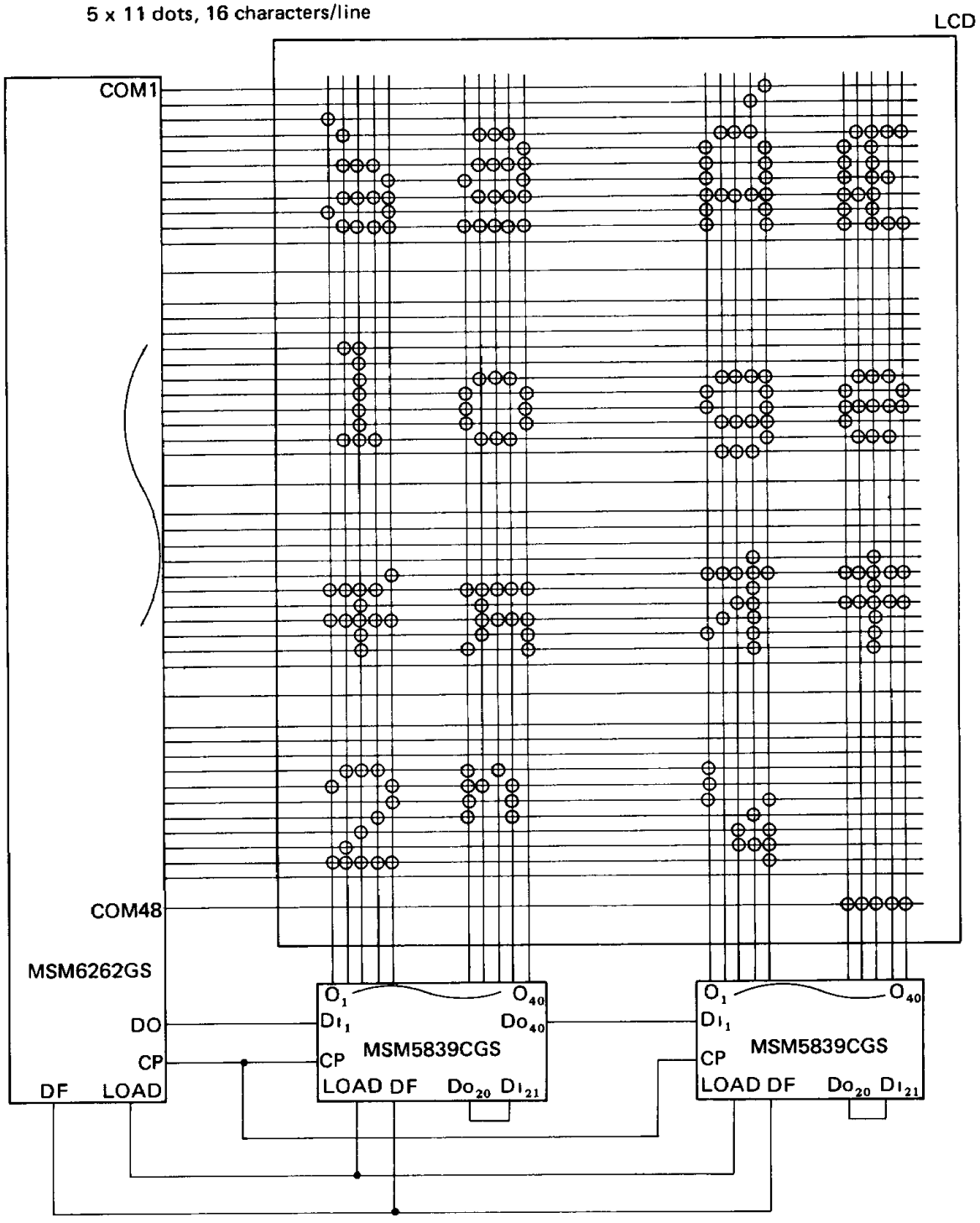
3 4-line display mode

5 x 7 dots/font, 16 characters/line

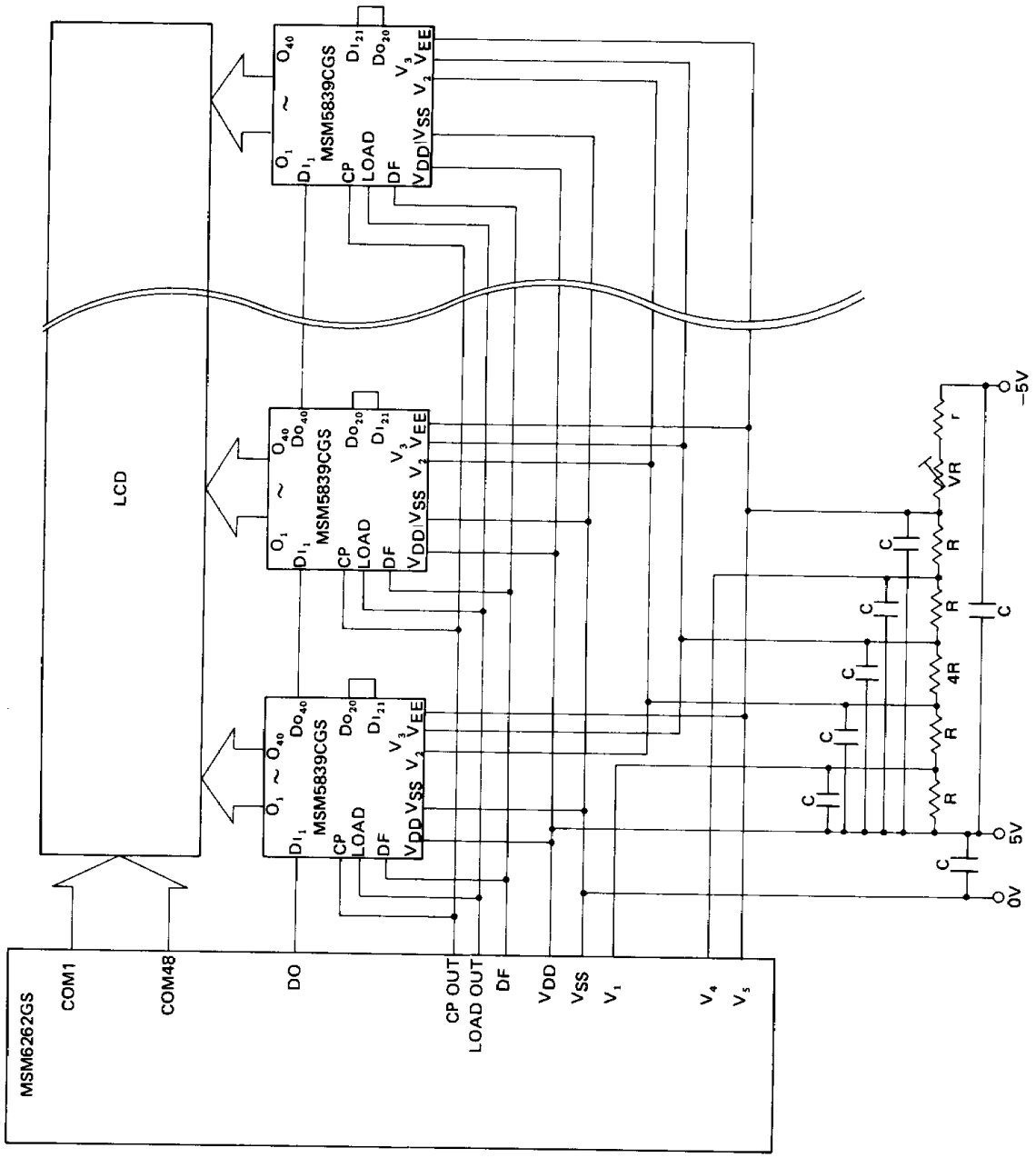
(Note: COM33 ~ COM48 should be left open)



4 4-line display mode
5 x 11 dots, 16 characters/line



MSM6262GS, MSM5839CGS, Bias circuit connection

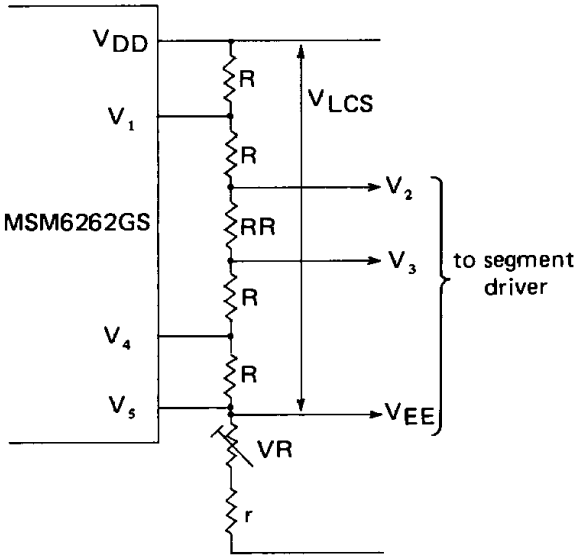


- **Example of bias circuit**

1 1/5 ~ 1/8 bias example 1.

Bias	1/5	1/6	1/7	1/8
PR	R	2R	3R	4R

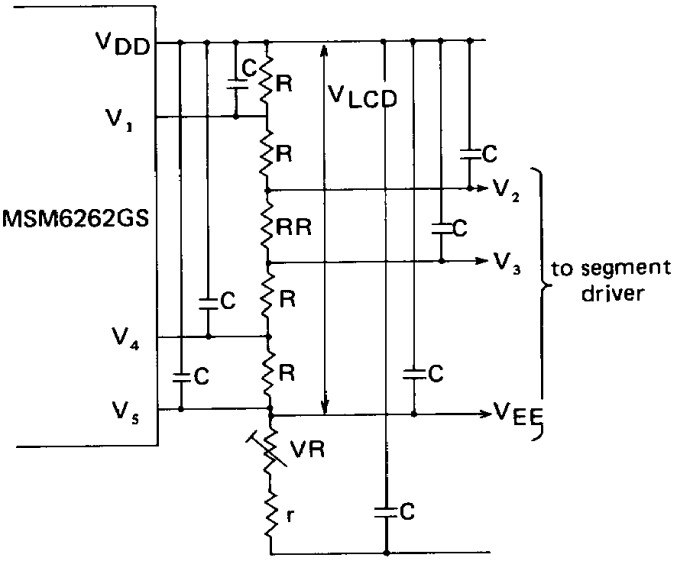
V_{LCD}; LCD driving voltage



1/5 ~ 1/8 bias example 2.

Bias	1/5	1/6	1/7	1/8
RR	R	2R	3R	4R

V_{LCD}; LCD driving voltage



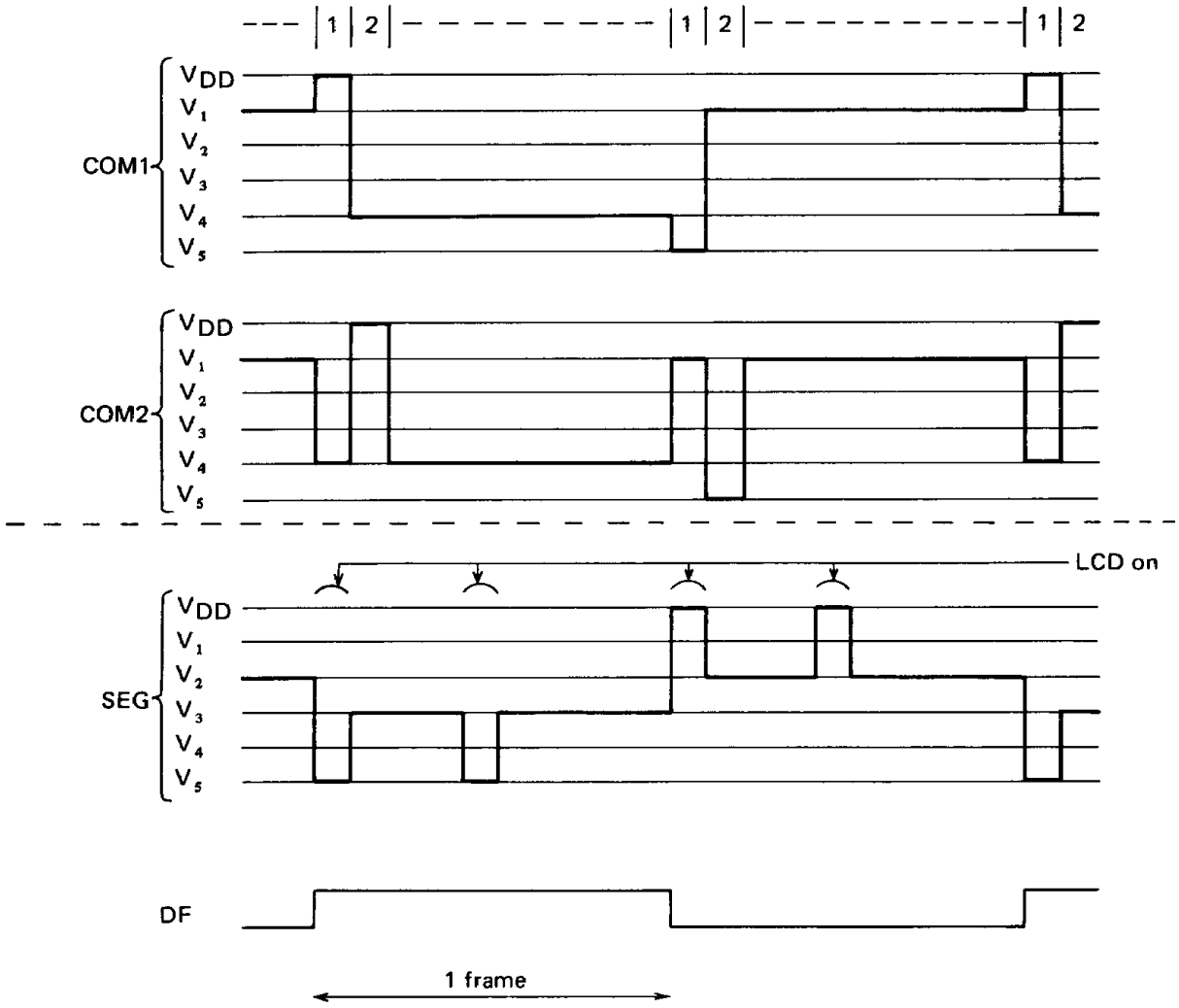
- **LCD duty and bias**

No. of line	2-line		4-line	
Duty	1/16	1/24	1/32	1/48
Bias	1/5	1/6	1/7	1/8

Above are examples of relation between LCD duty and bias. Since it is subject to change depend on the characteristics of LCD panel, please use above as a reference value.
The value of resistance on bias circuit is determined by the operational margin and power consumption. To make the power consumption lower, the value of resistance has to be bigger and this make the LCD driving output high and it causes the distortion on the LCD driving waveform.
In case of large LCD panel, the value of the resistance should be much lower as the LCD capacity increase.
To improve the distortion of LCD driving waveform, to connect bybass condensors parallely to the bias resistance, can be useful. But to connect a condensor of too big value causes the level shift of the bias voltage.
So, it has to be determined carefully after checking experimentally.
Followings are the reference value.

$R = 2 \sim 10k\Omega$
$V_R = 10 \sim 50k\Omega$
$r = 200\Omega \sim 2k\Omega$
$c = 0.0022 \sim 0.047\ \mu F$

LCD Driving Waveform



Duty	1/16	1/24	1/32	1/48
Frame frequency	78, 125 Hz	52, 08 Hz	78, 125 Hz	52, 08 Hz

Note: fosc = 500 kHz

PRODUCT LINE-UP

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