AN-6982

Power Factor Correction Converter Design with FAN6982

Introduction

The FAN6982 is a 14-pin, Continuous Conduction Mode (CCM) Power Factor Correction (PFC) controller IC, that employs leading-edge modulation for average current control and has a number of advanced features for better performance and reliability. The variable output voltage function (range function) reduces PFC output voltage at light-load and low-line conditions to improve light-load efficiency, but can be also easily disabled using EN pin. The RDY signal can be used for power-on sequence control of the downstream DC/DC converter. A TriFault Detect™ function helps reduce external components and provides full protection for feedback loops such as open, short, and over voltage. FAN6982 also includes PFC soft-start, peak current limiting, line feed-forward, and input voltage brownout protection.

This application note describes the theory of operation and step-by-step design considerations for a power factor correction power supply using the FAN6982 controller. A typical application circuit is shown in Figure 1, where the supply voltage, V_{DD}, is supplied from a standby auxiliary power supply and the supply voltage for the downstream converter is controlled by the RDY pin.

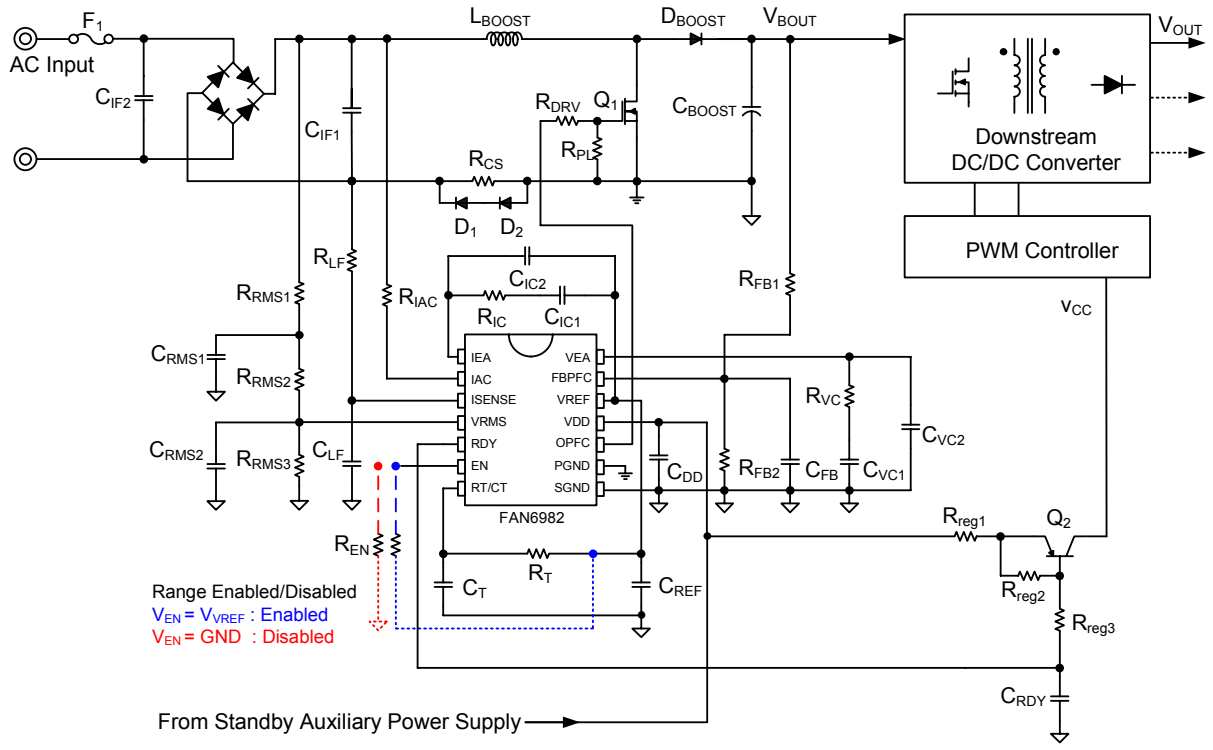

Figure 1. Typical FAN6982 Application Circuit

Functional Description

Widely used operation modes for the boost converter are continuous conduction mode (CCM) and boundary conduction mode (BCM). These two descriptive names refer to the current flowing through the energy storage inductor of the boost converter, as depicted in Figure 2. The inductor current in CCM is continuous; while in BCM, the new switching period is initiated when the inductor current returns to zero, which is at the boundary of continuous conduction and discontinuous conduction operations. CCM PFC is commonly used for high-power applications above 300W since the inductor current has a small ripple and higher power factor can be obtained than BCM operation. Due to the reverse-recovery current of the output diode, using a high-speed diode with a small reverse recovery current is crucial to achieve high efficiency and low EMI.

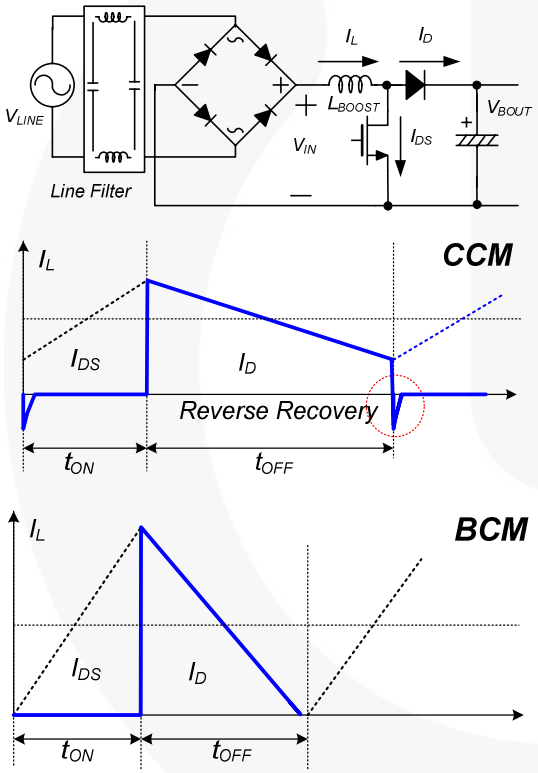

Figure 2. CCM vs. BCM Control

Current and Voltage Control of PFC

As shown in Figure 3, the FAN6982 employs two control loops for power factor correction: a current-control loop and a voltage-control loop. The current-control loop shapes inductor current, as shown in Figure 4, such that voltage drop across the internal resistor R_M should be same as the averaged voltage drop across the sensing resistor, R_{CS}, during one switching cycle:

$$\frac{1}{T_S}\int_0^{T_S}(I_L \cdot R_{CS})dt = I_{MO} \cdot R_M \qquad (1)$$

where the internal resistor R_M is typically 5.7kΩ; the output current of gain modulator, I_{MO}, is given as a function of input current of IAC pin; and voltages of the VRMS and VEA pins are calculated as:

$$I_{MO} = I_{AC} \times \frac{10.5 \times (V_{EA} - 0.7)}{V_{RMS}^{\,2}\,(V_{EA}^{\,MAX} - 0.7)} \qquad (2)$$

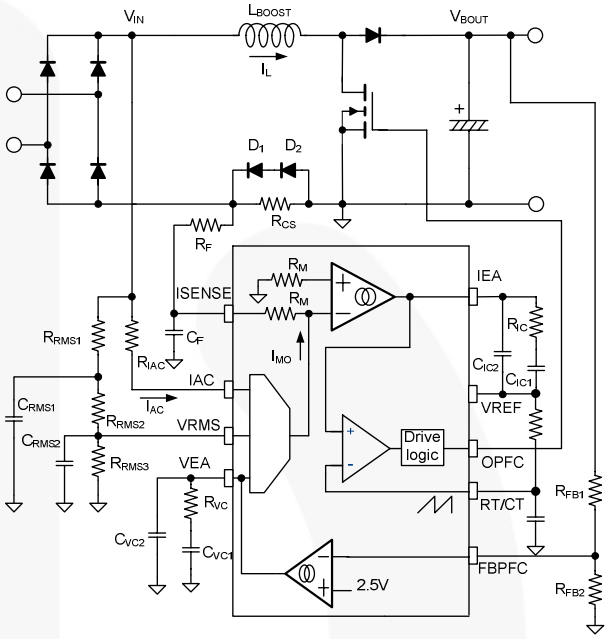

Figure 3. Current and Voltage Control Feedback Circuit

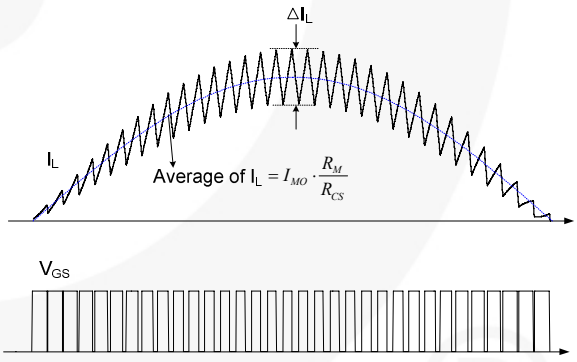

Figure 4. Operation Waveforms of CCM PFC

The voltage-control loop regulates PFC output voltage using an internal error amplifier such that the FBPFC voltage is same as the internal reference of 2.5V. Note that, from Equation (2), the voltages of V_{EA} should be almost constant to obtain pure sinusoidal reference for the input current shaping. Because there is always twice the line frequency ripple in the PFC output voltage, a narrow bandwidth should be used for the output voltage-control loop to minimize the line frequency ripple. Otherwise, the control loop tries to remove the output voltage ripple, changing the error amplifier output voltage as shown in Figure 5, which causes distortion of the input current.

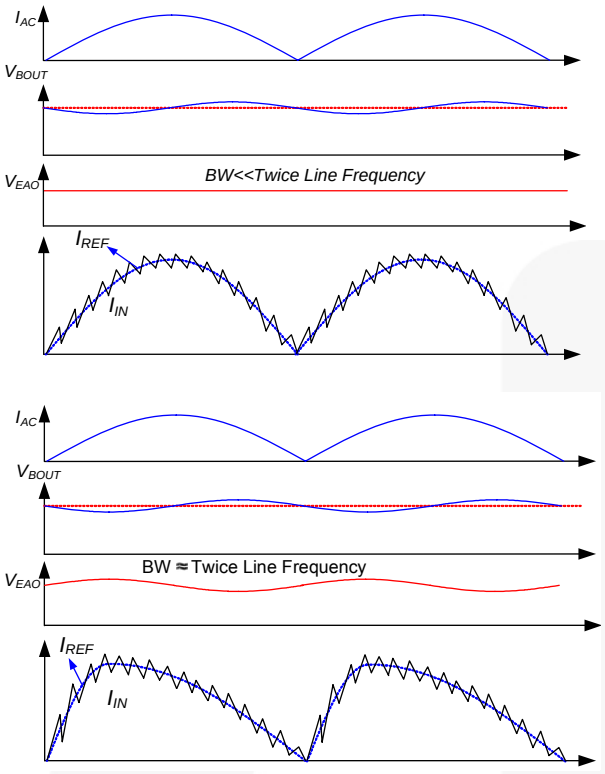

Figure 5. Control Bandwidth and Inductor Current

Line Feed-Forward

Since rectified line voltage provides the sinusoidal reference for the input current shaping of the current-control loop, the increase of the line voltage causes increase of input current. However, from an input and output power balance point of view, input current should be reduced when input voltage increases to keep input power same. When the error amplifier has adequate bandwidth, as in most DC-DC applications, it is able to maintain regulation within a tolerable output voltage range during input voltage changes. However, for PFC applications, some severe output voltage overshoot/undershoot is unavoidable during line transient due to the narrow bandwidth of output regulation control loop.

One measure to address this issue is line feed-forward, which changes the gain of the gain modulator as inversely proportional to the RMS value of line voltage, as shown in Figure 6. This **negates** the effect of input voltage variations on the output voltage and eliminates the need for any correction by the error amplifier, as shown in Figure 7.

The second benefit of line feed-forward is that the output of the error amplifier becomes directly proportional to the input power of the converter, independently of line voltage variation. This makes the control-to-output transfer function independent of line voltage and simplifies control loop design.

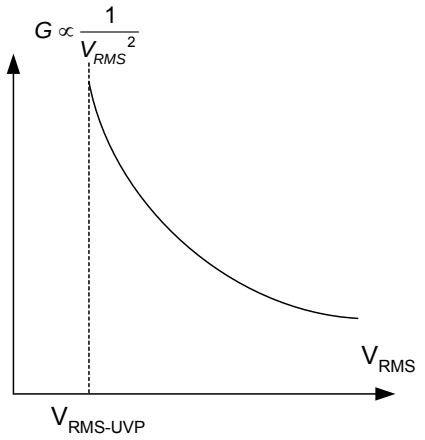

Figure 6. Modulation Gain Characteristics

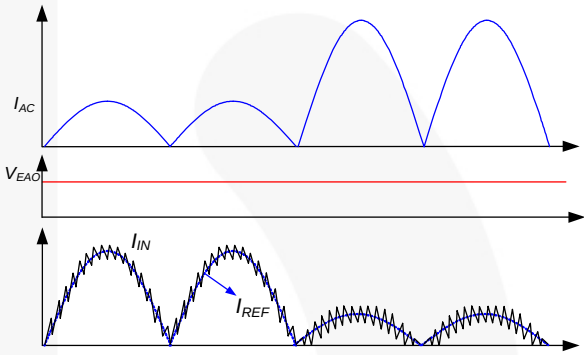

Figure 7. Effect of Line Feed-Forward

Line Voltage Sensing

Since FAN6982 uses line voltage information for line feed-forward and brownout protection, the RMS value of line voltage should be sensed. To sense the RMS value of the line voltage, an averaging circuit with two poles is typically employed, as shown in Figure 3. The voltage of VRMS pin in normal PFC operation is given as:

$$V_{RMS} = V_{LINE} \frac{\sqrt{2}R_{RMS3}}{R_{RMS1} + R_{RMS2} + R_{RMS3}} \cdot \frac{2}{\pi} \quad (3)$$

where V_{LINE} is RMS value of line voltage.

Once PFC stops switching operation, the junction capacitance of bridge diode and input bypass capacitor are not discharged and V_{IN} of Figure 3 is clamped at the peak of the line voltage as illustrated in Figure 8. Then, the voltage of VRMS pin is given by:

$$V_{RMS}^{NS} = V_{LINE} \frac{\sqrt{2}R_{RMS3}}{R_{RMS1} + R_{RMS2} + R_{RMS3}} \quad (4)$$

Therefore, the voltage divider for VRMS should be designed considering the brownout protection trip point and PFC startup threshold (1.05V/1.9V).

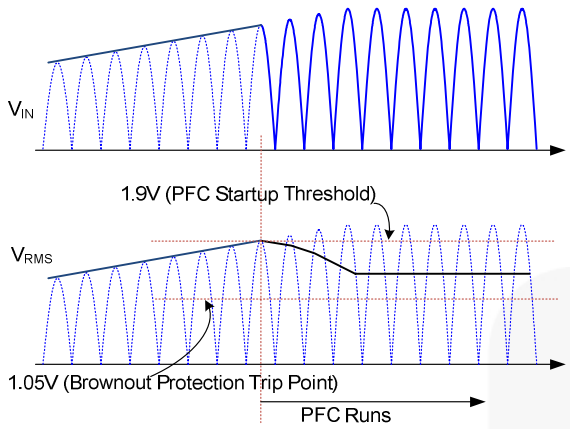

Figure 8. V_{RMS} According to the PFC Operation

Range Function

To improve system efficiency at low AC line voltage and light load condition, FAN6982 provides two-level PFC output voltage. As shown in Figure 9, FAN6982 monitors V_{EA} and V_{RMS} voltages to adjust the PFC output voltage. When V_{EA} and V_{RMS} are lower than the thresholds, an internal current source of 20μA is enabled and flows through R_{FB2}, increasing the voltage of the FBPFC pin. This causes the PFC output voltage to reduce when 20μA is enabled, calculated as:

$$V_{OPFC2} = \frac{R_{FB1} + R_{FB2}}{R_{FB2}} \times (2.5 - 20\mu A \times R_{FB2}) \quad (5)$$

It is typical to set the second boost output voltage as 340V~300V.

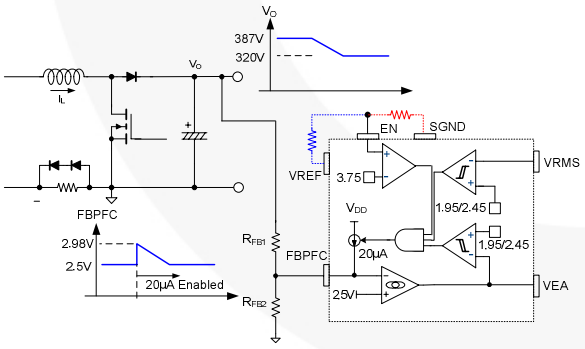

Figure 9. Two-Level PFC Output Block

Oscillator

The internal oscillator frequency is determined by the timing resistor and capacitor on the RT/CT pin. The frequency of the internal oscillator is given by:

$$f_{OSC} = \frac{1}{0.56 \cdot R_T \cdot C_T + 360 C_T} \quad (6)$$

Dead time for the PFC gate drive signal is determined by:

$$t_{DEAD} = 360 C_T \quad (7)$$

Dead time should be smaller than 2% of the switching period to minimize line current distortion around the line zero crossing.

The duty cycle is determined by comparing I_{EA} voltage with the sawtooth waveform on the RT/CT pin. Note that FAN6982 employs leading-edge modulation and the duty cycle reduces as I_{EA} voltage increases.

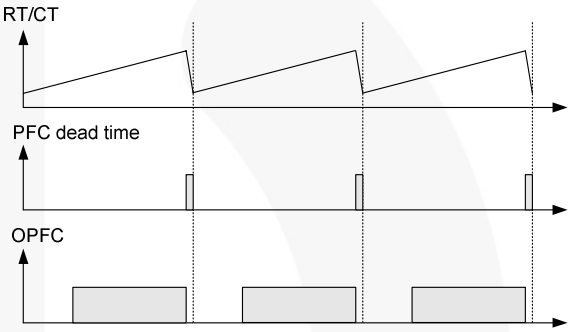

Figure 10. Timing Diagram

RDY Function

The RDY function shown in Figure 11 is controlled by the voltage of FBPFC. When the voltage of FBPFC is over than 96% of 2.5V, the RDY pin is be connected to SGND. Meanwhile, the internal MOSFET is turned off and the RDY pin is floated when FBPFC pin voltage is lower than 46% of 2.5V. This is typically used to control the startup and shutdown of downstream converter by connecting and disconnecting supply voltage of the downstream converter as shown in Figure 11. Typically, a bypass capacitor is connected across the RDY pin and ground to minimize noise interference.

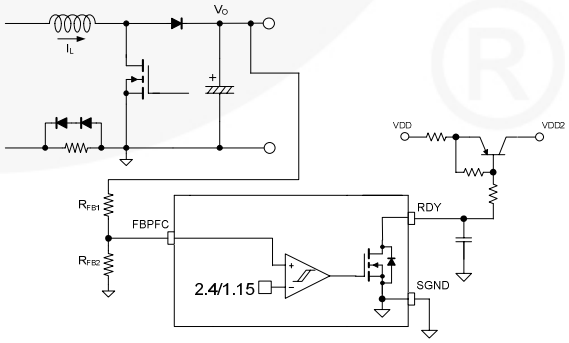

Figure 11. RDY Application Circuit

Soft-Start Function

The soft-start is combined with RDY pin operation. During startup, the RDY pin remains floating until the PFC output voltage reaches 96% of its nominal value. When the supply voltage of the downstream converter is controlled by the RDY pin, the PFC stage starts with no load since the downstream converter does not operate until the PFC output voltage is built to a certain level.

Usually the error amplifier output V_{EA} is saturated to HIGH during the startup since the actual output voltage is less than the target value. V_{EA} remains saturated to HIGH until the PFC output voltage reaches its target value. Once the PFC output reaches its target value, the error amplifier comes out of saturation. However, it takes several line cycles for V_{EA} to drop to its proper value for the output regulation, which delivers more power to the load than required, causing output voltage overshoot.

To prevent output voltage overshoot during startup caused by the saturation of error amplifier; FAN6982 clamps the error amplifier output voltage (V_{EA}) at 2.8V, which is half of its maximum value, until PFC output reaches 96% of its nominal value. Once the PFC output voltage reaches 96% of its nominal value, the clamping function of V_{EA} is disabled. Then the voltage of PFC output is regulated by voltage control loop.

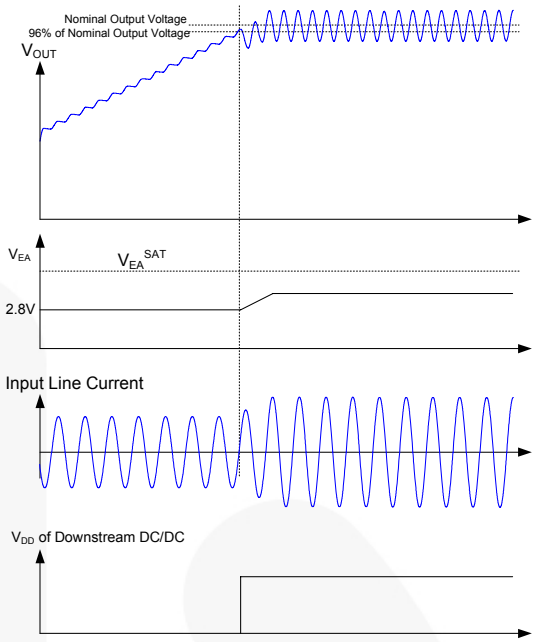

Figure 12. PFC Soft-Start

Design Considerations

In this section, a design procedure is presented using the schematic in Figure 13 as reference. A 350W PFC power supply application with universal input range is selected as a design example. The design specifications are summarized in Table 1.

Table 1. Design Specifications

Brownout Protection Line Voltage	$72V_{AC}$
Line Voltage Range	$85\sim264V_{AC}$
AC Input Voltage Frequency	f_{line} = 50 ~ 60Hz
Nominal PFC output voltage	V_{BOUT} = 387V
Minimum PFC Output Voltage During Holdup Time	310V
Hold-up Time	t_{HLD} = 20ms
Rated Output Power	P_{OUT} = 350W
Efficiency	η = 0.94
Switching Frequency	f_{SW} = 65KHz
PFC Inductor Ripple Current	Maximum ΔI_L is 50% of Average Inductor Current at Full Load
PFC Output Voltage Ripple	$12V_{PP}$

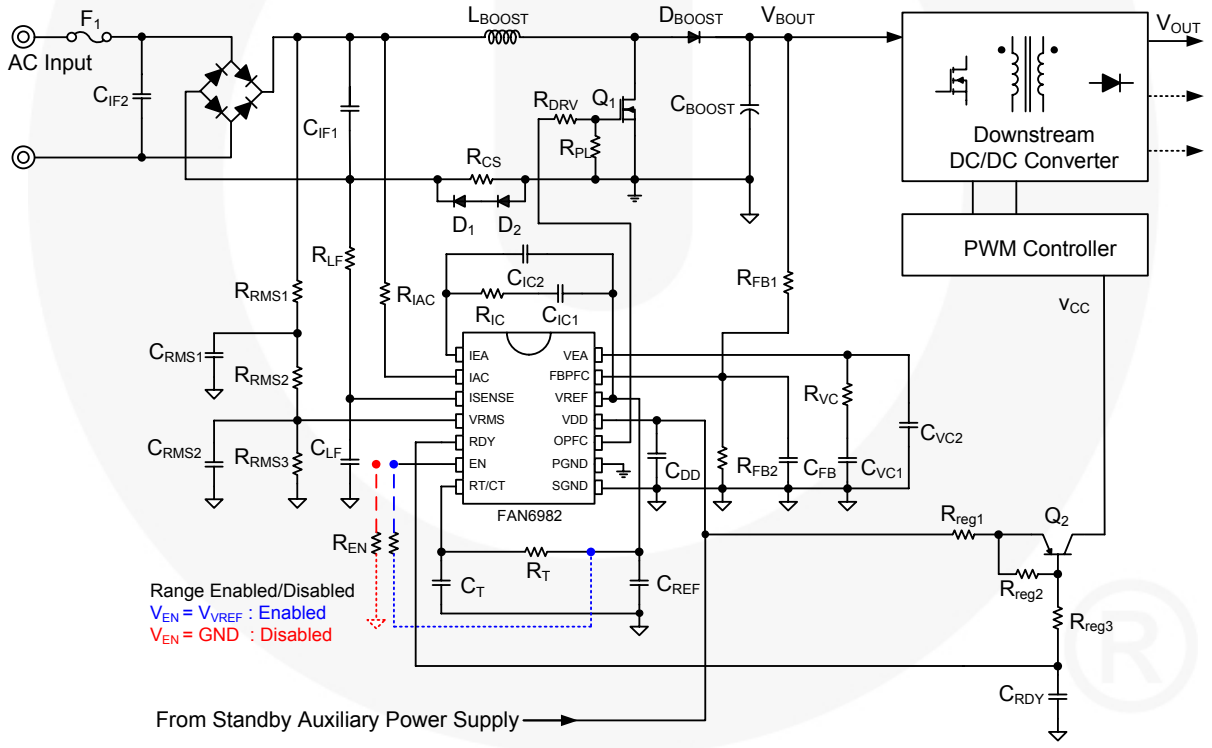

Figure 13. Reference Circuit for Design Example

[STEP-1] Frequency Setting

The switching frequency is determined by the timing resistor and capacitor (R_T and C_T) as:

$$f_{SW} \cong \frac{1}{0.56 \cdot R_T \cdot C_T} \quad (8)$$

The timing capacitor value determines the maximum duty cycle of PFC gate drive signal as:

$$D_{MAX.PFC} = 1 - \frac{t_{DEAD}}{t_{SW}} = 1 - 360 \cdot C_T \cdot f_{SW} \quad (9)$$

It is typical to use a 470pF~1nF capacitor for 50~75kHz switching frequency operation, such that maximum duty cycle of 99~98% is obtained.

(Design Example) Since the switching frequency is 65kHz, C_T is selected as 1nF to obtain maximum duty cycle as:

$$D_{MAX.PFC} = 1 - 360 \cdot C_T \cdot f_{SW} = 0.98$$

Then, the timing resistor is determined as:

$$R_T = \frac{1}{0.56 f_{SW} C_T} = 27k\Omega$$

[STEP-2] Line Sensing Circuit Design

FAN6982 senses the RMS value and instantaneous value of line voltage using the VRMS and IAC pins, respectively, as shown in Figure 14. The RMS value of the line voltage is obtained by an averaging circuit using low-pass filter with two poles. Meanwhile, the instantaneous line voltage information is obtained by sensing the current flowing into the IAC pin through R_{IAC}.

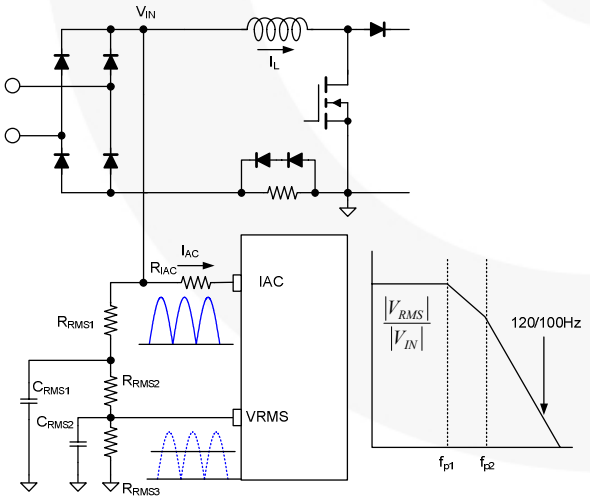

Figure 14. Line-Sensing Circuits

RMS sensing circuit should be designed considering the nominal operation range of line voltage and brownout protection trip point as:

$$V_{RMS-UVL} = V_{LINE.BO} \frac{\sqrt{2}R_{RMS3}}{R_{RMS1} + R_{RMS2} + R_{RMS3}} \cdot \frac{2}{\pi} \quad (10)$$

$$V_{RMS-UVH} < V_{LINE.MIN} \frac{\sqrt{2}R_{RMS3}}{R_{RMS1} + R_{RMS2} + R_{RMS3}} \quad (11)$$

where $V_{RMS-UVL}$ and $V_{RMS-UVH}$ are the brownout/in thresholds of V_{RMS}.

It is typical to set R_{RMS2} as 10% of R_{RMS1}. The poles of the low-pass filter are given as:

$$f_{P1} \cong \frac{1}{2\pi \cdot C_{RMS1} \cdot R_{RMS2}} \quad (12)$$

$$f_{P2} \cong \frac{1}{2\pi \cdot C_{RMS2} \cdot R_{RMS3}} \quad (13)$$

To properly attenuate the twice line frequency ripple in V_{RMS}, it is typical to set the poles around 10~20Hz.

The resistor R_{IAC} should be large enough to prevent saturation of the gain modulator as:

$$\frac{\sqrt{2}V_{LINE.BO}}{R_{IAC}} \cdot G^{MAX} < 159\mu A \quad (14)$$

where $V_{LINE.BO}$ is the brownout protection line voltage, G^{MAX} is the maximum modulator gain when V_{RMS} is 1.08V (which is typically 9 as can be found in the datasheet), and 159μA is the maximum output current of the gain modulator.

(Design Example) The brownout protection thresholds are 1.05V ($V_{RMS-UVL}$) and 1.9V ($V_{RMS-UVH}$), respectively. Then, the scaling down factor of the voltage divider is:

$$\frac{R_{RMS3}}{R_{RMS1} + R_{RMS2} + R_{RMS3}} = \frac{V_{RMS-UVL}}{V_{LINE.BO}} \cdot \frac{\pi}{2\sqrt{2}} = \frac{1.05}{72} \cdot \frac{\pi}{2\sqrt{2}} = 0.0162$$

The startup of the PFC controller at the minimum line voltage is checked as:

$$\frac{V_{LINE.MIN} \cdot \sqrt{2}R_{RMS3}}{R_{RMS1} + R_{RMS2} + R_{RMS3}} = 85 \cdot \sqrt{2} \cdot 0.0162 = 1.95 > 1.9V$$

The resistors of the voltage divider network are selected as R_{RMS1}=2MΩ, R_{RMS2}=200kΩ, and R_{RMS3}=36kΩ.

To place the poles of the low-pass filter at 15Hz and 22Hz, the capacitors are obtained as:

$$C_{RMS1} = \frac{1}{2\pi \cdot f_{P1} \cdot R_{RMS2}} = \frac{1}{2\pi \cdot 15 \cdot 200 \times 10^3} = 53nF$$

$$C_{RMS2} \cong \frac{1}{2\pi \cdot f_{P2} \cdot R_{RMS3}} = \frac{1}{2\pi \cdot 22 \cdot 36 \times 10^3} = 200nF$$

The condition for Resistor R_{IAC} is:

$$R_{IAC} > \frac{\sqrt{2}V_{LINE.BO}}{159 \times 10^{-6}} \cdot G^{MAX} = \frac{\sqrt{2} \cdot 72 \cdot 9}{159 \times 10^{-6}} = 5.8M\Omega$$

Therefore, 6MΩ resistor is selected for R_{IAC}.

[STEP-3] PFC Inductor Design

The duty cycle of boost switch at the peak of line voltage is given as:

$$D_{LP} = \frac{V_{BOUT} - \sqrt{2}V_{LINE}}{V_{BOUT}} \quad (15)$$

Then the current ripple of the boost inductor at the peak of line voltage is given as:

$$\Delta I_L = \frac{\sqrt{2}V_{LINE}}{L_{BOOST}} \cdot \frac{V_{BOUT} - \sqrt{2}V_{LINE}}{V_{BOUT}} \cdot \frac{1}{f_{SW}} \quad (16)$$

The average of boost inductor current over one switching cycle at the peak of the line voltage is given as:

$$I_{L.AVG} = \frac{\sqrt{2}P_{OUT}}{V_{LINE} \cdot \eta} \quad (17)$$

The ripple factor (K_{RF}), the ratio between the inductor current ripple and average inductor current at the peak of line voltage load is given as:

$$K_{RF} = \frac{\Delta I_L}{I_{L.AVG}} = \frac{\eta \cdot V_{LINE}^2}{P_{OUT} \cdot L_{BOOST}} \cdot \frac{V_{BOUT} - \sqrt{2}V_{LINE}}{V_{BOUT}} \cdot \frac{1}{f_{SW}} \quad (18)$$

As depicted in Figure 15, the ripple factor has the maximum value when the line voltage is:

$$V_{LINE.MRF} = \frac{\sqrt{2}V_{BOUT}}{3} \quad (19)$$

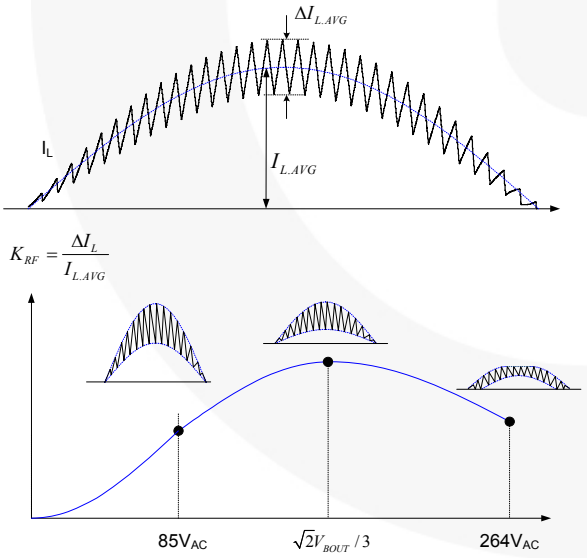

Figure 15. Ripple Factor with Different Line Voltages

Therefore, with a given current ripple factor ($K_{RF}=\Delta I_L/I_{LAVG}$), the boost inductor value is obtained as:

$$L_{BOOST} = \frac{2V_{BOUT}^2 \cdot \eta}{K_{RF} \cdot P_{OUT}} \cdot \frac{1}{27 f_{SW}} \quad (20)$$

(Design Example) The largest ripple factor is obtained at a line voltage as:

$$V_{LINE} = \frac{\sqrt{2}V_{BOUT}}{3} = \frac{\sqrt{2} \cdot 387}{3} = 182V_{AC}$$

With the ripple current specification (50%), the boost inductor is obtained as:

$$L_{BOOST} = \frac{2V_{BOUT}^2 \cdot \eta}{K_{RF} \cdot P_{OUT}} \cdot \frac{1}{27 f_{SW}} = \frac{2 \cdot 387^2 \cdot 0.94}{0.5 \cdot 350} \cdot \frac{1}{27 \cdot 65 \times 10^3} = 916\mu H$$

The inductor current ripple at low line is obtained as:

$$\Delta I_L = \frac{\sqrt{2}V_{LINE}}{L_{BOOST}} \cdot \frac{V_{BOUT} - \sqrt{2}V_{LINE}}{V_{BOUT}} \cdot \frac{1}{f_{SW}} = \frac{\sqrt{2} \cdot 85}{916 \times 10^{-6}} \cdot \frac{387 - \sqrt{2} \cdot 85}{387} \cdot \frac{1}{65 \times 10^3} = 1.39A$$

The average inductor current at the peak of the line voltage for low line is obtained as:

$$I_{L.AVG} = \frac{\sqrt{2}P_{OUT}}{V_{LINE.MIN} \cdot \eta} = \frac{\sqrt{2} \cdot 350}{85 \cdot 0.94} = 6.19A$$

The maximum of the inductor current at low line is obtained as:

$$I_L^{PK} = I_{L.AVG} + \Delta I_L / 2 = 6.19 + 1.39 / 2 = 6.89A$$

[STEP-4] PFC Output Capacitor Selection

The output voltage ripple should be considered when selecting the PFC output capacitor. Figure 16 shows the twice line frequency ripple on the output voltage. With a given specification of output ripple, the condition for the output capacitor is obtained as:

$$C_{BOUT} > \frac{I_{BOUT}}{2\pi \cdot f_{LINE} \cdot V_{BOUT,RIPPLE}} \quad (21)$$

where I_{BOUT} is nominal output current of boost PFC stage and $V_{BOUT,RIPPLE}$ is the peak-to-peak output voltage ripple specification.

The hold-up time also should be considered when determining the output capacitor as:

$$C_{BOUT} > \frac{2P_{OUT} \cdot t_{HOLD}}{V_{BOUT}^2 - V_{BOUT,MIN}^2} \quad (22)$$

where P_{OUT} is nominal output power of boost PFC stage, t_{HOLD} is the required hold-up time, and $V_{BOUT,MIN}$ is the allowable minimum PFC output voltage during hold-up time.

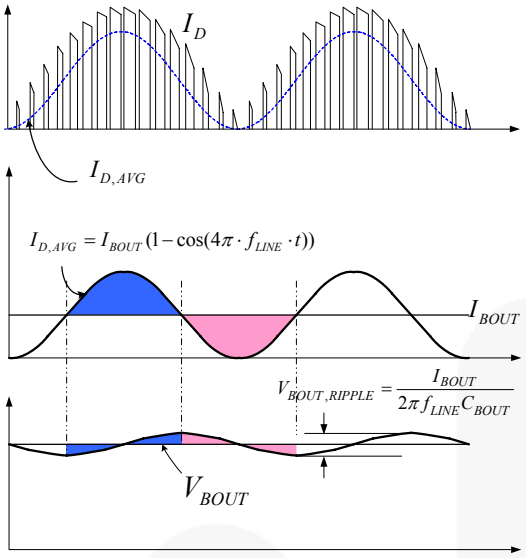

Figure 16. PFC Output Voltage Ripple

(Design Example) With the ripple specification of $12V_{PP}$, the capacitor should be:

$$C_{BOUT} > \frac{I_{BOUT}}{2\pi \cdot f_{LINE} \cdot V_{BOUT,RIPPLE}} = \frac{0.9}{2\pi \cdot 50 \cdot 12} = 239\mu F$$

Since minimum allowable output voltage during one cycle line (20ms) drop-outs is 310V, the capacitor should be:

$$C_{BOUT} > \frac{2P_{BOUT} \cdot t_{HOLD}}{V_{OUT}^2 - V_{OUT,MIN}^2} = \frac{2 \cdot 349 \cdot 20 \times 10^{-3}}{387^2 - 310^2} = 260\mu F$$

Thus, 270µF capacitor is selected for the PFC output capacitor.

[STEP-5] PFC Output Sensing Circuit

To improve system efficiency at low-line and light-load condition, FAN6982 provides two-level PFC output voltage. As shown in Figure 17, the range function can be enabled or disabled through a resistor connected to ground or VREF. FAN6982 monitors V_{EA} and V_{RMS} voltages to adjust the PFC output voltage and enables a 20µA current source.

The PFC output voltage when 20µA is enabled is given as:

$$V_{BOUT2} = V_{BOUT} \times (1 - \frac{20\mu A \times R_{FB2}}{2.5}) \quad (23)$$

It is typical to set the second boost output voltage as 340V~300V. It should be checked if the output voltage is higher than the peak of the line voltage

$$\frac{R_{RMS1} + R_{RMS2} + R_{RMS3}}{R_{RMS3}} \cdot \frac{\pi}{2} \cdot 2.45 < V_{BOUT2} \quad (24)$$

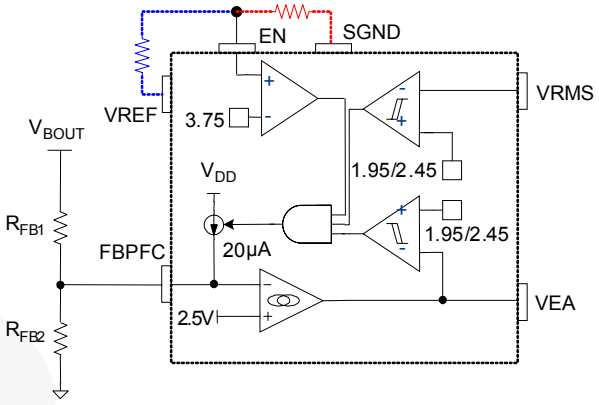

Figure 17. Block of Range Function

The voltage divider network for the PFC output voltage sensing should be designed such that FBPFC voltage is 2.5V at nominal PFC output voltage:

$$V_{BOUT} \times \frac{R_{FB2}}{R_{FB1} + R_{FB2}} = 2.5V \quad (25)$$

(Design Example) Assuming the second level of PFC output voltage is 347V:

$$R_{FB2} = (1 - \frac{V_{BOUT2}}{V_{BOUT}}) \cdot \frac{2.5}{20 \times 10^{-6}}$$

$$= (1 - \frac{347}{387}) \cdot \frac{2.5}{20 \times 10^{-6}} = 12.9k\Omega$$

13kΩ is selected for R_{FB2}.

It is checked if the output voltage is higher than the peak of the line voltage:

$$\frac{R_{RMS1} + R_{RMS2} + R_{RMS3}}{R_{RMS3}} \cdot \frac{\pi}{2} \cdot 2.45$$

$$= \frac{2 \times 10^6 + 200 \times 10^3 + 36 \times 10^3}{36 \times 10^3} \cdot \frac{\pi}{2} \cdot 2.45$$

$$= 239V < 347V$$

Then, to obtain 387V for nominal PFC output,

$$R_{FB1} = (\frac{V_{BOUT}}{2.5} - 1) \cdot R_{FB2}$$

$$= (\frac{387}{2.5} - 1) \cdot 13 \times 10^3 = 1999k\Omega$$

2MΩ is selected for R_{FB1}.

[STEP-6] PFC Current-Sensing Circuit Design

Figure 18 shows the PFC compensation circuits for the input current shaping and output voltage regulation. The first step in compensation network design is to select the current-sensing resistor of PFC converter considering the maximum power limit. Since line feed-forward is used, the output power is proportional to the voltage control error amplifier voltage as:

$$P_{OUT}(V_{EA}) = P_{OUT}^{MAX} \cdot \frac{V_{EA} - 0.6}{V_{EA}^{SAT} - 0.6} \quad (26)$$

where V_{EA}^{SAT} is 5.6V and the maximum power limit of PFC given by the maximum V_{EA} voltage is:

$$P_{OUT}^{MAX} = \frac{V_{LINE.BO}^{2} \cdot G^{MAX} \cdot R_M}{R_{IAC} R_{CS}} \quad (27)$$

where R_M is internal modulator resistor whose typical value is 5.7kΩ, R_{IAC} is a resistor connected between IAC pin, and PFC input and G_{MAX} is the maximum of ratio of IAC pin current and modulator output current (I_{MO}/I_{AC}). The typical value of G^{MAX} is 9 when VRMS pin voltage is 1.05V, which is related to the brownout protection threshold of line voltage ($V_{LINE.BO}$).

It is typical to set the maximum power limit of the PFC stage around 1.2~1.5 of its nominal output power, such that the V_{EA} is around 4~4.5V at nominal output power. By adjusting the current-sensing resistor for the PFC converter, the maximum power limit of the PFC stage can be programmed.

To filter out the current ripple of switching frequency, an RC filter is typically used for the ISENSE pin. R_{LF} should not be larger than 100Ω and the time constant of the filter should be 300~500ns to properly remove the leading-edge current spike caused by reverse recovery of output diode.

Diodes D_1 and D_2 are required to prevent over-voltage on the ISENSE pin due to the inrush current that might damage FAN6982. A fast recovery diode or ultra-fast recovery diode is recommended.

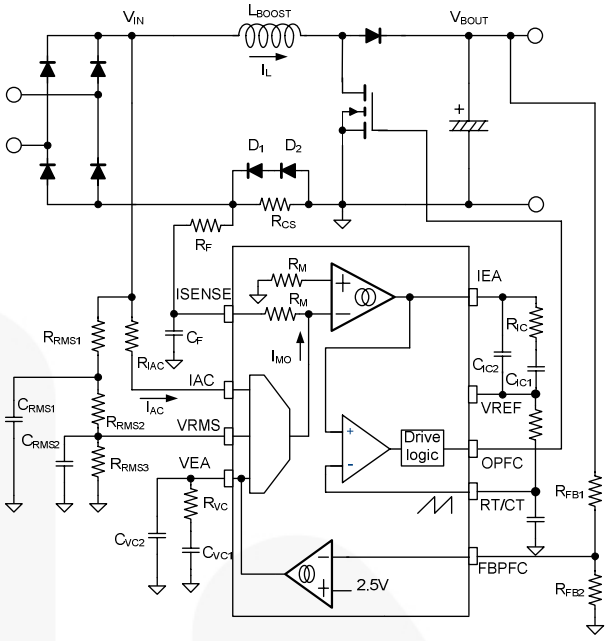

Figure 18. Gain Modulation Block

(Design Example) Setting the maximum power limit of the PFC stage as 450W (around 130% of nominal output power), the current sensing resistor is obtained as:

$$R_{CS} = \frac{V_{LINE.BO}^{2} \cdot G^{MAX} \cdot R_M}{R_{IAC} P_{BOUT}^{MAX}} = \frac{72^2 \cdot 9 \cdot 5.7 \times 10^3}{6 \times 10^6 \cdot 450} = 0.098\Omega$$

Thus, 0.1Ω resistor is selected.

[STEP-8] PFC Current Loop Design

The transfer function from duty cycle to the inductor current of boost power stage is given as:

$$\frac{\hat{i}_L}{\hat{d}} = \frac{V_{BOUT}}{sL_{BOOST}} \quad (28)$$

The transfer function from the output of the current control error amplifier to the inductor current-sensing voltage is obtained as:

$$\frac{\hat{v}_{CS}}{\hat{v}_{IEA}} = \frac{R_{CS} \cdot V_{BOUT}}{V_{RAMP} \cdot sL_{BOOST}} \quad (29)$$

where V_{RAMP} is the peak to peak voltage of ramp signal for current control PWM comparator, which is 2.55V.

The transfer function of the compensation circuit is given as:

$$\frac{\hat{v}_{IEA}}{\hat{v}_{CS}} = \frac{2\pi f_{II}}{s} \cdot \frac{1 + \frac{s}{2\pi f_{IC}}}{1 + \frac{s}{2\pi f_{IP}}} \quad (30)$$

where:

$$f_{II} = \frac{G_{MI}}{2\pi \cdot C_{IC1}},\ f_{IZ} = \frac{1}{2\pi \cdot R_{IC} \cdot C_{IC1}}\ and\ f_{IP} = \frac{1}{2\pi \cdot R_{IC} \cdot C_{IC2}} \quad (31)$$

where G_{MI} is the gain of transconductance error amplifier.

The procedure to design the feedback loop is as follows:

(a) Determine the crossover frequency (f_{IC}) around 1/10~1/6 of the switching frequency. Then calculate the gain of the transfer function of Equation (29) at crossover frequency as:

$$\left|\frac{\hat{v}_{CS}}{\hat{v}_{IEA}}\right|_{@\ f=f_{IC}} = \frac{R_{CS} \cdot V_{BOUT}}{V_{RAMP} \cdot 2\pi f_{IC} \cdot L_{BOOST}} \quad (32)$$

(b) Calculate R_{IC} that makes the closed-loop gain unity at crossover frequency:

$$R_{IC} = \frac{1}{G_{MI} \cdot \left|\frac{\hat{v}_{CS}}{\hat{v}_{IEA}}\right|_{@\ f=f_{IC}}} \quad (33)$$

(c) Since the control-to-output transfer function of power stage has -20dB/dec slope and -90° phase at the crossover frequency is 0dB, as shown in Figure 19, it is necessary to place the zero of the compensation network (f_{IZ}) around 1/3 of the crossover frequency so that more than 45° phase margin is obtained. Then the capacitor C_{IC1} is determined as:

$$C_{IC1} = \frac{1}{R_{IC} \cdot 2\pi f_C / 3} \quad (34)$$

(d) Place compensator high-frequency pole (f_{CP}) at least a decade higher than f_{IC} to ensure that it does not interfere with the phase margin of the current loop at its crossover frequency.

$$C_{IC2} = \frac{1}{2\pi \cdot f_{IP} \cdot R_{IC}} \quad (35)$$

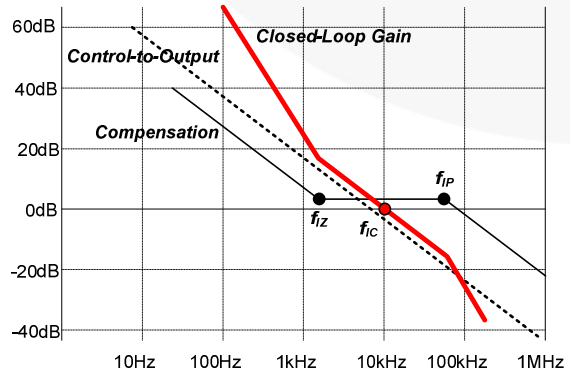

Figure 19. Current Loop Compensation

(Design Example) Setting the crossover frequency as 6kHz (around 1/10 of switching frequency):

$$\left|\frac{\hat{v}_{CS1}}{\hat{v}_{IEA}}\right|_{@\ f=f_{IC}} = \frac{R_{CS} \cdot V_{BOUT}}{V_{RAMP} \cdot 2\pi f_{IC} \cdot L_{BOOST}} = \frac{0.1 \cdot 387}{2.55 \cdot 2\pi \cdot 6\times10^{3} \cdot 916\times10^{-6}} = 0.44$$

$$R_{IC} = \frac{1}{G_{MI} \cdot \left|\frac{\hat{v}_{CS}}{\hat{v}_{IEA}}\right|_{@\ f=f_{IC}}} = \frac{1}{88\times10^{-6} \cdot 0.44} = 26k\Omega$$

$$C_{IC1} = \frac{1}{R_{IC} \cdot 2\pi f_C / 3} = \frac{1}{26\times10^{3} \cdot 2\pi \cdot 6\times10^{3} / 3} = 3.1nF$$

Setting the pole of the compensator at 60kHz,

$$C_{IC2} = \frac{1}{2\pi \cdot f_{IP} \cdot R_{IC}} = \frac{1}{2\pi \cdot 60\times10^{3} \cdot 26\times10^{3}} = 0.10nF$$

The actual components are a little changed for the off-the-shelf components as:

R_{IC}=27kΩ, C_{IC1}=3.3nF, and C_{IC2}=100pF.

[STEP-9] PFC Voltage Loop Design

Since FAN6982 employs line feed-forward, the power-stage transfer function becomes independent of the line voltage. Then the low-frequency, small-signal, control-to-output transfer function is obtained as:

$$\frac{\hat{v}_{BOUT}}{\hat{v}_{EA}} \cong \frac{I_{BOUT} \cdot K_{MAX}}{5} \cdot \frac{1}{sC_{BOUT}} \quad (36)$$

where $K_{MAX} = P_{OUT}{}^{MAX} / P_{OUT}$ and 5V is the control window of error amplifier (5.6V-0.6V=5V).

Proportional and integration (PI) control with high-frequency pole is typically used for compensation. The compensation zero (f_{VZ}) introduces phase boost, while the high-frequency compensation pole (f_{VP}) attenuates the switching ripple, as shown in Figure 20.

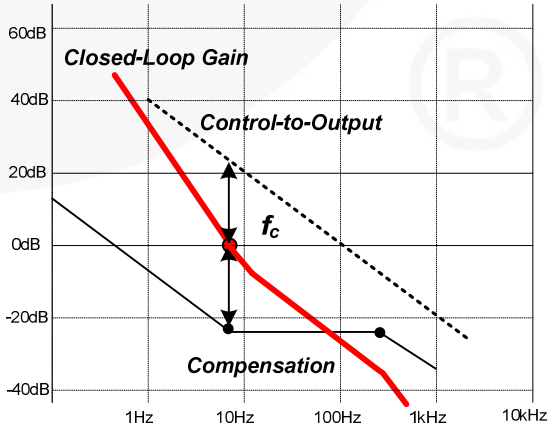

Figure 20. Voltage Loop Compensation

The transfer function of the compensation network is obtained as:

$$\frac{\hat{v}_{COMP}}{\hat{v}_{OUT}} = \frac{2\pi f_{VI}}{s} \cdot \frac{1+\frac{s}{2\pi f_{VZ}}}{1+\frac{s}{2\pi f_{VP}}} \quad (37)$$

where:

$$f_{VI} = \frac{2.5}{V_{BOUT}} \cdot \frac{G_{MV}}{2\pi \cdot C_{VC1}},\ f_{VZ} = \frac{1}{2\pi \cdot R_{VC} \cdot C_{VC1}} \quad and \quad f_{VP} = \frac{1}{2\pi \cdot R_{VC} \cdot C_{VC2}} \quad (38)$$

The procedure to design the feedback loop is as follows:

(a) Determine the crossover frequency (f_{VC}) around 1/10~1/5 of the line frequency. Since the control-to-output transfer function of power stage has -20dB/dec slope and -90° phase at the crossover frequency, as shown in Figure 20 as 0dB; it is necessary to place the zero of the compensation network (f_{VZ}) around the crossover frequency so that 45° phase margin is obtained. Then, the capacitor C_{VC1} is determined as:

$$C_{VC1} = \frac{G_{MV} \cdot I_{BOUT} \cdot K_{MAX}}{5 \cdot C_{BOUT} \cdot (2\pi f_{VC})^2} \cdot \frac{2.5}{V_{BOUT}} \quad (39)$$

where G_{MV} is the gain of the transconductance error amplifier for the output voltage regulation.

To place the compensation zero at the crossover frequency, the compensation resistor is obtained as:

$$R_{VC} = \frac{1}{2\pi \cdot f_{VC} \cdot C_{VC1}} \quad (40)$$

(b) Place compensator high-frequency pole (f_{VP}) at least a decade higher than f_C to ensure that it does not interfere with the phase margin of the voltage regulation loop at its crossover frequency. It should also be sufficiently lower than the switching frequency of the converter so noise can be effectively attenuated. Then, the capacitor C_{VC2} is determined as:

$$C_{VC2} = \frac{1}{2\pi \cdot f_{VP} \cdot R_{VC}} \quad (41)$$

(Design Example) Setting the crossover frequency as 22Hz:

$$C_{VC1} = \frac{G_{MV} \cdot I_{BOUT} \cdot K_{MAX}}{5 \cdot C_{BOUT} \cdot (2\pi f_{VC})^2} \cdot \frac{2.5}{V_{BOUT}} = \frac{70\times10^{-6} \cdot 0.9 \cdot 1.27}{5 \cdot 270\times10^{-6} \cdot (2\pi \cdot 22)^2} \cdot \frac{2.5}{387} = 20nF$$

$$R_{VC} = \frac{1}{2\pi \cdot f_{VC} \cdot C_{VC1}} = \frac{1}{2\pi \cdot 22 \cdot 20\times10^{-9}} = 362k\Omega$$

Setting the pole of the compensator at 120Hz:

$$C_{VC2} = \frac{1}{2\pi \cdot f_{VP} \cdot R_{VC}} = \frac{1}{2\pi \cdot 120 \cdot 362\times10^{3}} = 3.7nF$$

1. Design Summary

Application	Output Power	Input Voltage	Output Voltage / Output Current
PFC Power Supply	350W	85~264V_{AC}	387V/0.9A

Features

- Switch-charge technique of gain modulator provides better PF and lower THD
- Over-Voltage Protection (OVP), Under-Voltage (UVP), Open-Loop (OLP), and maximum current limit Protections
- Range function improves system efficiency at low AC line voltage and light load condition
- Ready pin function provides power-on sequence for the downstream converter

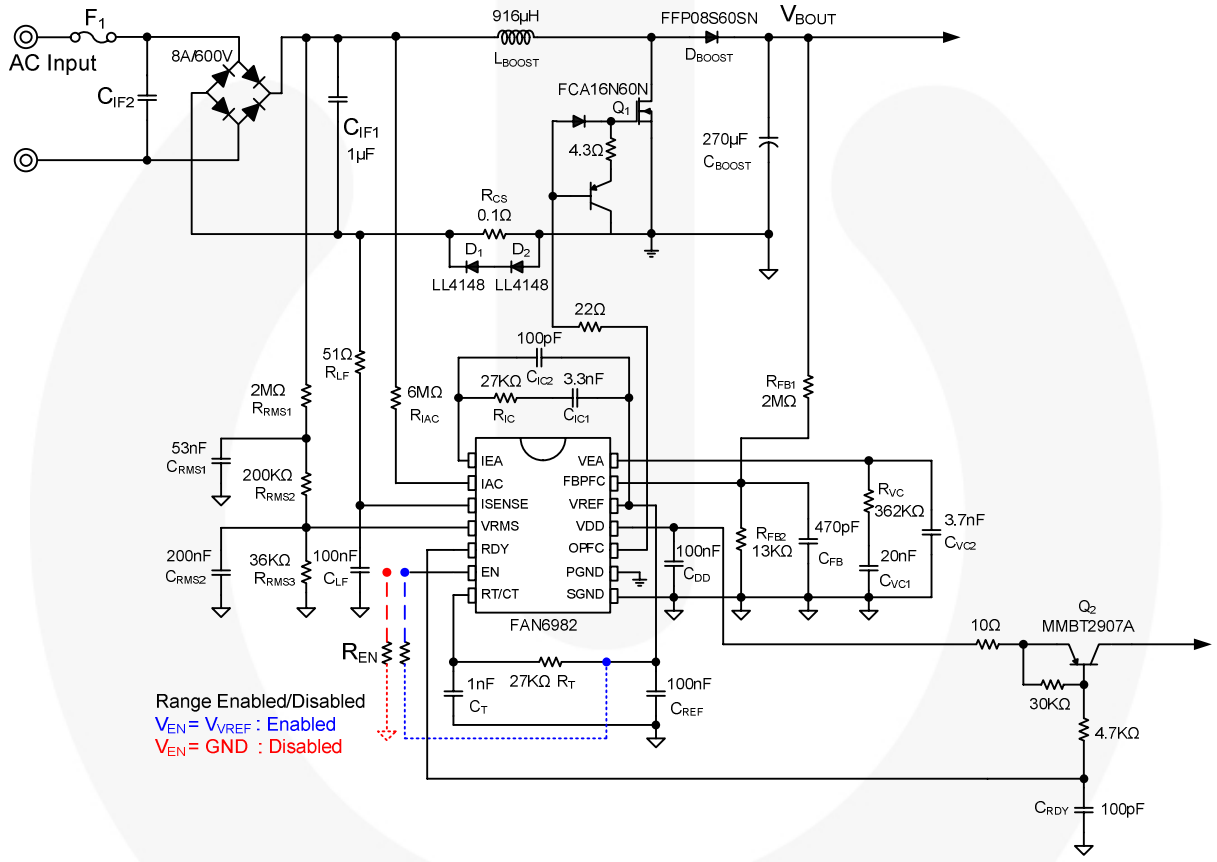

Figure 21. Final Schematic of Design Example

Appendix A

MOSFET and Diode Reference Specification

PFC MOSFETs	
Voltage Rating	**Part Number**
500V	FQP13N50C, FQPF13N50C, FDP18N50, FDPF18N50, FDA18N50, FDP20N50(T), FDPF20N50(T)
600V	FCP11N60, FCPF11N60, FCP16N60, FCPF16N60, FCP20N60S, FCPF20N60S, FCA20N60S, FCP20N60, FCPF20N60
Boost Diodes	
600V	FFP08H60S, FFPF10H60S, FFP08S60S, FPF08S60SN, BYC10600

References

FAN6982 — CCM Power Factor Correction Controller

AN-8027 — FAN480X PFC+PWM Combo Controller Application

AN-6004 — 500W Power Factor Corrected (PFC) Design with FAN4810

AN-6032 — FAN4800 Combo Controller Applications

AN-42009 — ML4824 Combo Controller Applications

ATX 350W Evaluation Board of FAN6982+FSBH0F70A