AK2305

Dual PCM CODEC for ISDN TERMINAL ADAPTER

GENERAL DESCRIPTION

AK2305 is a dual PCM CODEC-Filter most suitable for ISDN Terminal Adapter. A-law/u-law is selected by the internal register. In addition to CODEC, this device has dual DTMF receiver and External Tone Input pin.

Input/output operational amplifiers included in this device are used for transmit/receive gain adjustment. AK2305 has internal volume control to attenuate signal from 0dB to –12dB by 3dB step control which is defined by an internal register written through the serial interface.

PCM interface of AK2305 accepts several clock formats, which are Long Frame, Short Frame, GCI, IDL. 64k-4096kHz clock input is available for PCM interface.

FEATURE

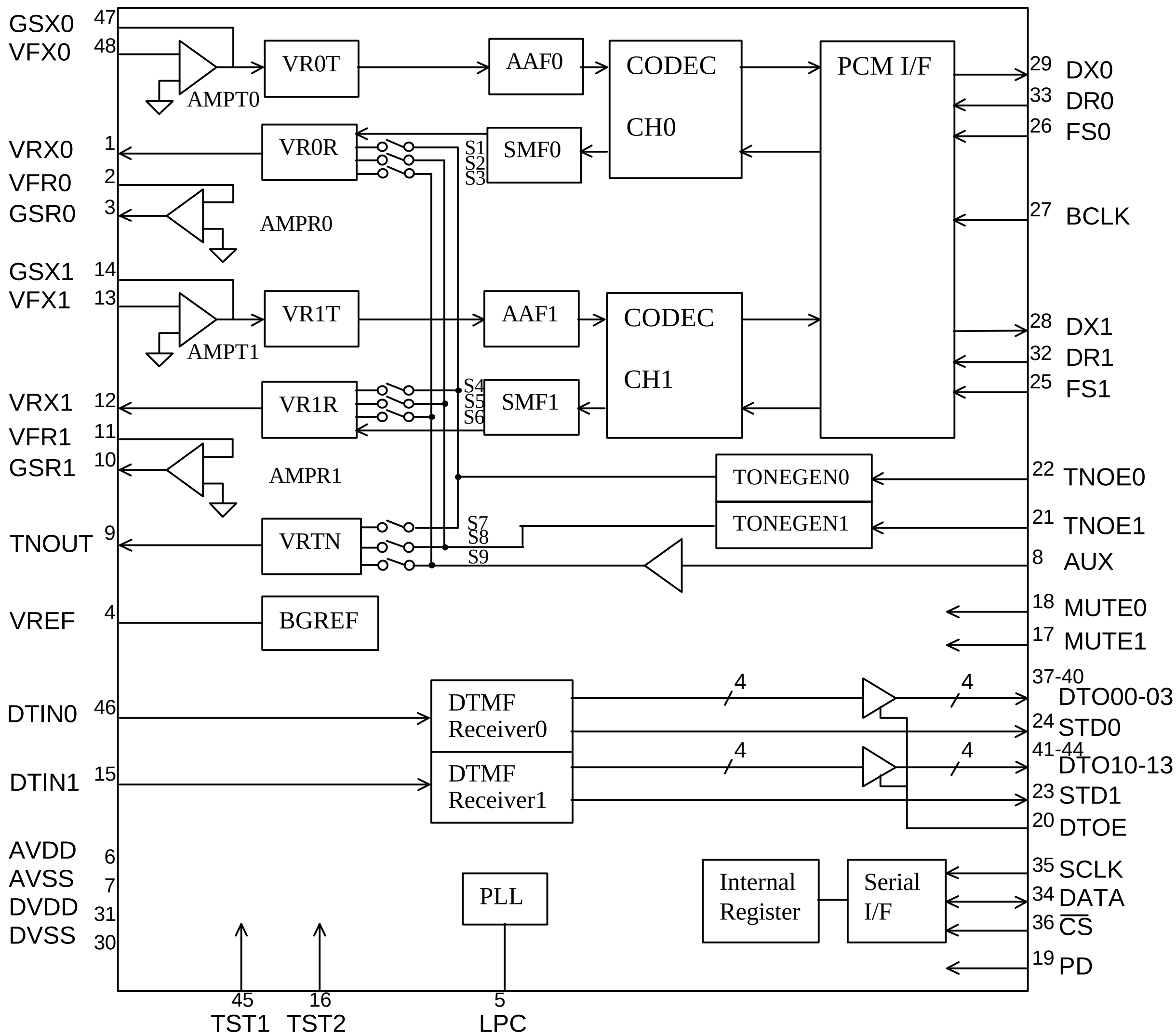
- **Dual PCM CODEC and Filtering systems for ISDN Terminal Adapter**
- **Dual DTMF Receiver**
- **External Tone Input(AUX)**
- **Independent functions on each channel**
  - **Frame Sync Signal(8kHz)**
  - **Power Down Mode(Pin/Register operation)**
  - **Mute(Pin/Register operation)**
  - **Gain Adjustment: 0 to -12dB (3dB step)**
- **Selectable PCM Data Interface Timing: Long Frame / Short Frame / GCI / IDL**
- **Variable PCM Data Rate: 64k x N [Hz] (64k - 4.096MHz)**
- **Operational Amplifier for Gain Adjustment**
- **A-law/u-law Register Selectable**
- **Serial Interface**
- **Power on Reset**
- **Single +5V ± 5% CMOS technology**
- **Low Power Consumption (85mW typ)**

PACKAGE

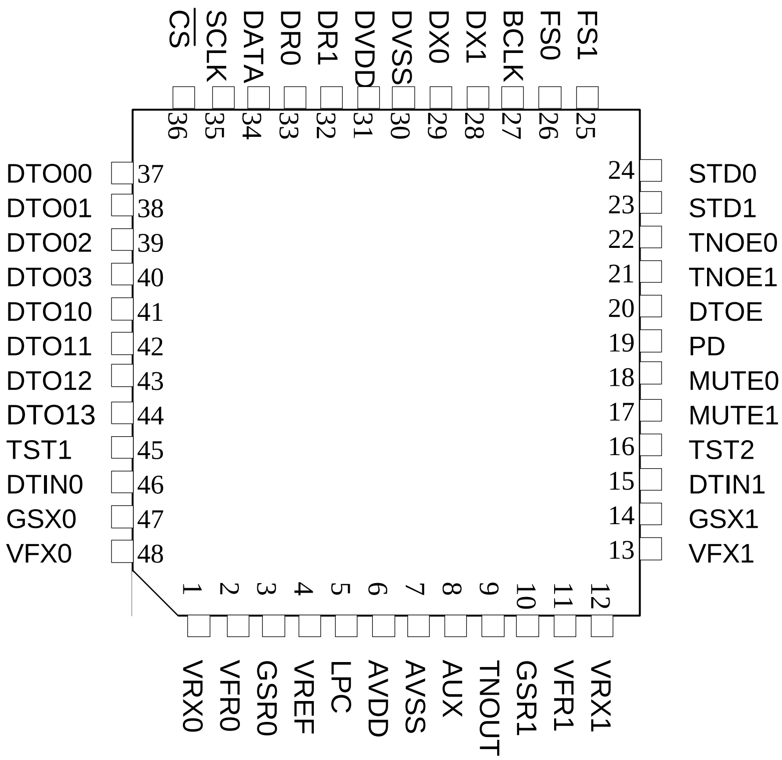
- **48LQFP**
  9.0 x 9.0 mm (0.5mm pin pitch)

CONTENTS

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN CONDITION

Pin#	Name	I/O	Pin type	AC load (MAX.)	DC load (MIN.)	Outout status (Power down mode)	Output status (Reset)	Remarks
1	VRX0	O	Analog	50pF	10kΩ	Hi-Z	Hi-Z	
2	VFR0	I	Analog					
3	GSR0	O	Analog	50pF	10kΩ (*1)	Hi-Z	Hi-Z	
4	VREF	O	Analog					external cap
5	LPC	O	Analog					external cap
6	AVDD	-						
7	AVSS	-						
8	AUX	I	Analog					
9	TNOUT	O	Analog	50pF	10kΩ	Hi-Z	Hi-Z	
10	GSR1	O	Analog	50pF	10kΩ (*1)	Hi-Z	Hi-Z	
11	VFR1	I	Analog					
12	VRX1	O	Analog	50pF	10kΩ	Hi-Z	Hi-Z	
13	VFX1	I	Analog					
14	GSX1	O	Analog	50pF	10kΩ (*1)	Hi-Z	Hi-Z	
15	DTIN1	I	Analog					
16	TST2	I	TTL					Factory use only
17	MUTE1	I	TTL					
18	MUTE0	I	TTL					
19	PD	I	TTL					
20	DTOE	I	TTL					
21	TNOE1	I	TTL					
22	TNOE0	I	TTL					
23	STD1	O	CMOS	15pF		L	L	
24	STD0	O	CMOS	15pF		L	L	
25	FS1	I	TTL					(*2)
26	FS0	I	TTL					
27	BCLK	I	TTL					
28	DX1	O	CMOS	15pF		Hi-Z	Hi-Z	
29	DX0	O	CMOS	15pF		Hi-Z	Hi-Z	
30	DVSS	-						
31	DVDD	-						
32	DR1	I	TTL					(*3)
33	DR0	I	TTL					
34	DATA	I/O	TTL/CMOS	15pF		Input	Input	
35	SCLK	I	TTL					
36	CSN	I	TTL					
37	DTO00	O	CMOS	15pF		Hi-Z	Hi-Z	
38	DTO01	O	CMOS	15pF		Hi-Z	Hi-Z	
39	DTO02	O	CMOS	15pF		Hi-Z	Hi-Z	
40	DTO03	O	CMOS	15pF		Hi-Z	Hi-Z	
41	DTO10	O	CMOS	15pF		Hi-Z	Hi-Z	
42	DTO11	O	CMOS	15pF		Hi-Z	Hi-Z	
43	DTO12	O	CMOS	15pF		Hi-Z	Hi-Z	
44	DTO13	O	CMOS	15pF		Hi-Z	Hi-Z	
45	TST1	I	TTL					Factory use only
46	DTIN0	I	Analog					
47	GSX0	O	Analog	50pF	10kΩ (*1)	Hi-Z	Hi-Z	
48	VFX0	I	Analog					

*1) DC load(MIN.) includes a feedback resistance of input/output op-amp. *2) Pulled down to VSS in GCI/IDL mode.
*3) Pulled down to VSS in 2ch Multiplex mode.

PIN FUNCTION

Pin#	Name	I/O	Function
48	VFX0	I	Transmit analog input. Inverting input of transmit gain adjustment amplifier for channel 0.
47	GSX0	O	Output of transmit gain adjustment amplifier for channel 0.
1	VRX0	O	Receive analog output of SMF for channel 0. This output can drive 10kΩ and 50pF.
2	VFX0	I	Transmit analog input. Inverting input of transmit gain adjustment amplifier for channel 0.
3	GSR0	O	Output of receive gain adjustment amplifier for channel 0.
10	GSR1	O	Output of receive gain adjustment amplifier for channel 1.
11	VFR1	I	Inverting input of receive gain adjustment amplifier for channel 1.
12	VRX1	O	Receive analog output of SMF for channel 1. This output can drive 10kΩ and 50pF.
14	GSX1	O	Output of transmit gain adjustment amplifier for channel 1.
13	VFX1	I	Transmit analog input. Inverting input of transmit gain adjustment amplifier for channel 1.
29	DX0	O	Serial output of PCM data of ch0. In Long Frame / Short Frame mode, output PCM data of ch0. In GCI / IDL mode, output PCM data of ch0 is multiplexed with ch1. The PCM data rate is synchronized with BCLK. See “PCM INTERFACE” from page 9. This output remains in the high impedance state except for the period of transmitting PCM data.
33	DR0	I	Serial input of PCM data of ch0. In Long Frame / Short Frame mode, input PCM data of ch0. In GCI / IDL mode, input PCM data of ch0 is multiplexed with ch1. The PCM data rate is synchronized with BCLK. See “PCM INTERFACE” from page 9.
28	DX1	O	Serial output of PCM data of ch1. In Long Frame / Short Frame mode, output PCM data of ch1. The PCM data rate is synchronized with BCLK. See “PCM INTERFACE” from page 9. This output remains in the high impedance state except for the period of transmitting PCM data. In 2ch multiplexd mode, this pin remains in the high impedance state.
32	DR1	O	Serial input of PCM data of ch1. In Long Frame / Short Frame mode, input PCM data of ch1. The PCM data rate is synchronized with BCLK. See “PCM INTERFACE” from page 9. In GCI / IDL mode, this pin is pulled down to VSS.
26	FS0	I	Frame sync input for channel 0. FS0 must be 8KHz clock synchronized in BCLK.

Pin#	Name	I/O	Function
25	FS1	I	Frame sync input for channel 1. FS1 must be 8KHz clock synchronized in BCLK. In GCI / IDL mode, this pin is pulled down to VSS.
27	BCLK	I	Bit clock of PCM data interface. This clock is apply for both ch0 and ch1. BCLK should be synchoronized with 8 x N kHz(FSn x N kHz).
46	DTIN0	I	DTMF tone input of ch 0.
37	DTO00	O	Output of DTMF receiver 0. DTO00 is LSB.
38	DTO01	O	
39	DTO02	O	
40	DTO03	O	
24	STD0	O	Steering to delay output of ch0. After the DTMF decoding, the output latch is renewed and this output alters to high level.
15	DTIN1	I	DTMF tone input.
41	DTO10	O	Output of DTMF receiver 1. DTO10 is LSB.
42	DTO11	O	
43	DTO12	O	
44	DTO13	O	
23	STD1	O	Steering to delay output of ch0. After the DTMF decoding, the output latch is renewed and this output alters to high level.
20	DTOE	I	Output enable pin for the DTMF receiver.
22	TNOE0	I	Output enable pin for the tone generator 0.
21	TNOE1	I	Output enable pin for the tone generator 1.
8	AUX	I	External tone input pin. Input signal should be through more than 0.1uF of an external capacitance.
9	TNOUT	O	Tone output pin.
34	DATA	I/O	Data input of serial interface.
35	SCLK	I	Clock input of serial interface.
36	$\overline{CS}$	I	Read and write enable of serial interface.
18	MUTE0	I	Active high input for ch0 mute.
17	MUTE1	I	Active high input for ch0 mute.
19	PD	I	Active high input for all power down.
5	LPC	O	Pin for PLL loop filter. Connect to AVSS with 0.22uF or larger.
4	VREF	O	Analog ground output. To stabilize the analog ground, connect to AVSS with 0.1uF or larger.
31	DVDD	-	Digital positive supply voltage. System digital +5V supply.
30	DVSS	-	Digital negative supply voltage. System digital ground.
6	AVDD	-	Analog positive supply voltage. Systems analog +5V supply.
7	AVSS	-	Analog negative supply voltage. System analog ground.
45	TST1	I	Only for factory use. Should to be fixed to DVSS.
16	TST2	I	

CIRCUIT DESCRIPTION

Block	Function
AMPT0,1	Op-amp for input gain adjustment. This op-amp is used as an inverting amplifier. Adjusting the gain with external resistors. The resistor larger than 10kΩ is recommended for the feedback resistor. <NOTE> AMP0(1) becomes automatically power down, when both CODEC ch0(1) and DTMFR0(1) are power down.
AMPR0,1	Op-amp for output gain adjustment. This op-amp is used as an inverting amplifier. Adjusting the gain with external resistors. The resistor larger than 10kΩ is recommended for the feedback resistor.
AAF	Integrated anti-aliasing filter which prevents signals around the sampling rate from folding back into the voice band. AAF is a 2nd order RC low-pass filter.
A/D	Converts analog signal to 8bit PCM data according to the companding schemes of ITU recommendation G.711; A-law or u-law. The band limiting filter is also integrated. The selection of companding schemes is set by ALAWN register as follows: "H": u-Law "L": A-Law
D/A	Expands 8bit PCM data according to A-law or u-law. The selection of companding schemes is set by ALAWN register as follows: "H": u-Law "L": A-Law
SMF	Extracts the inband signal from D/A output. It also corrects the sinx/x effect of D/A output.
BGREF	Provides the stable analog ground voltage (2.4V) using an on-chip band-gap reference circuit which is temperature compensated.
TONE GEN 0 TONE GEN 1	Generates two kinds of tone; 400Hz and 1300Hz. Tone selection is defined by registers. ON/OFF of tone output is controlled by TNOE0/1.
SWITCH Sn(n=1-9)	Controls output signals from VRX0, VRX1, TNOUT pins. Each switch is controlled by register.
DTMF Receiver0,1	Detects and decodes the DTMF tone. ON/OFF of decoded output is controlled by DTOE.
VR0T/R VR1T/R VRTN	Gain selects of analog I/O signals. It is posibble to select gain from 0dB to -12dB (3dB/step* 5steps). Gain is defined by register.
SERIAL I/F	Interface to internal register by using SCLK, DATA, and $\overline{\text{CS}}$ pins. 1word=14bit; Instruction code: 2bit, address: 3bit, data: 9bit(1dummy bit included).
PLL	PLL generates system clock of AK2305. Reference clock is FSn (8KHz). More than 0.22uF of an external capacitance should be connected between LPC and AVSS.
PCM I/F	PCM data rate is available for 64xN(N = 1 to 64)kHz which synchronizes with BCLK. Data format is selected in four types(Long Frame, Short Frame, GCI, IDL). 2ch PCM data are interfaced through DR0,1 and DX0,1 in non multiplexed mode or DR0 and Dx0 in multiplexed mode.

FUNCTIONAL DESCRIPTION

PCM INTERFACE

AK2305 supports the following types of format.
One of those is selected by PCMIF0 and PCMIF1 registers.

- **Long Frame Sync(LF)**
- **Short Frame Sync(SF)**
- **GCI**
- **IDL**

PCM data of both channels are multiplexed and interfaced through the common pins (DR0, DX0) in 2ch Multiplex I/F mode. But in 2ch Independent I/F mode of LF or SF, it is also available to interface through the independent pin(DR0/1,DX0/1) by channel.

Register of PCM interface mode selection

PCMIF1	PCMIF0	Interface	Frame sync	Input pin	Output pin	Remarks
0	0	LF/SF (Non multiplex)	FS0,FS1	DR0,DR1	DX0, DX1	Reset
0	1	LF/SF (2ch multiplex)	FS0,FS1	DR0	DX0	
1	0	GCI (2ch multiplex)	FS0	DR0	DX0	
1	1	IDL (2ch multiplex)	FS0	DR0	DX0	

FRAME SYNC SIGNAL(Frame Sync : FS)

Frame sync signal should be 8kHz clock. 8bits PCM data is accommodated in 1 frame (125us).
Though only FS0 is required (FS1 isn't required) in the mode of GCI or IDL, both FS0 and FS1 are required in the mode of LF or SF.

FIRST FS

It is used as the input clock of PLL. PLL generates all timing in this IC from this signal.
FS0 is assigned as First FS in the mode of GCI or IDL, and in the mode of LF or SF, it is assigned by the first FS register.

1stFS register	First FS	Remarks
0	FS0	Reset
1	FS1	

Note

Keep supplying the first FS except for the state of all power down(PD="H"). If the first FS is not supplied, AK2305 loses timing; at a result, DTMFR and TONE GEN become not guaranteed to work normally.

BCLK

This clock decides the PCM data rate. See the following table of the relation between BCLK and PCM data rate.

PCM I/F mode	BCLK	Rate of PCM data
LF/SF/IDL	F	F
GCI	2F	F

Long Frame Sync(LF) Short Frame Sync(SF)

AK2305 automatically decides whether Long Frame or Short Frame should be selected, by monitoring the high level period of First FS.

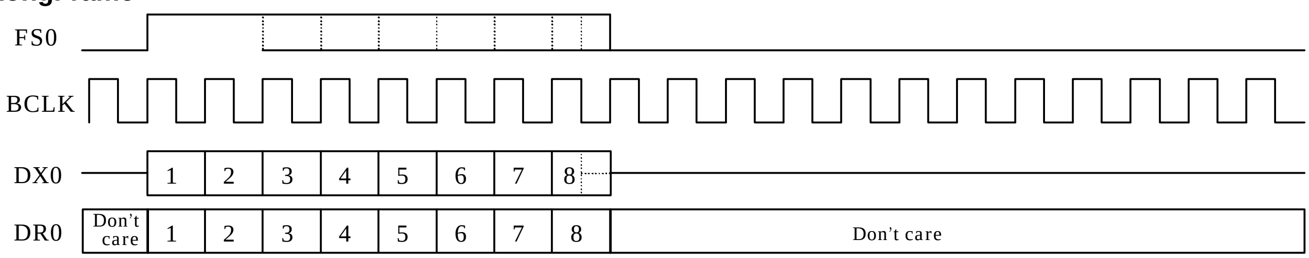
Period of First FS =”H”	Frame type
more than 2 clock of BCLK	LF
1 clock of BCLK	SF

INTERFACE TIMING

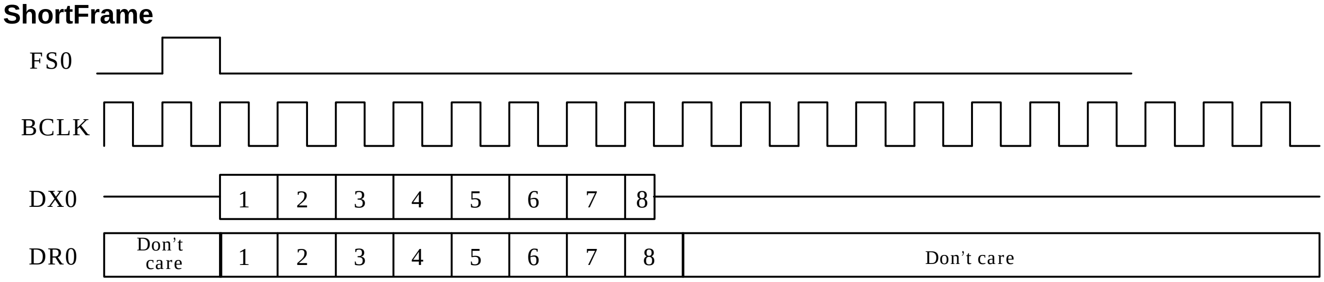
<2ch Multiplex>

PCM data of both channel are interfaced by the DX0 and DR0(DX1 and DR1 are not used) at the format of 8bits in the period of 1 frame(125us) which synchronizes with the FSn(n=0,1). In the period of 1frame, 64 time slots can be assigned at the maximum (in case of BCLK=4.096MHz). The number of the time slots is BCLK/64k. The time slot assignment of CH0 and CH1 is decided by FS0 and FS1. In the mode of LF and SF, second FS(not first FS) must be delayed or fast at least (8/BCLK) x n: (n=1 - 63) from the first FS.

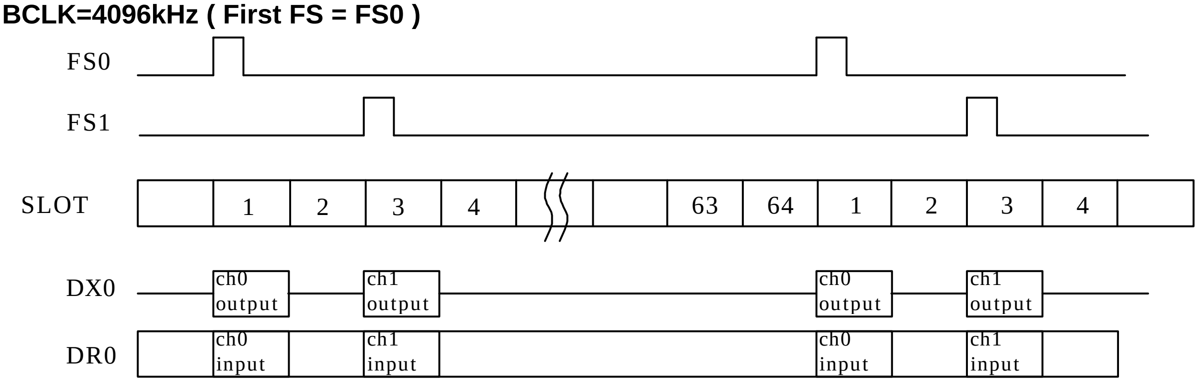
LongFrame



ShortFrame



BCLK=4096kHz (First FS = FS0)



INTERFACE TIMING

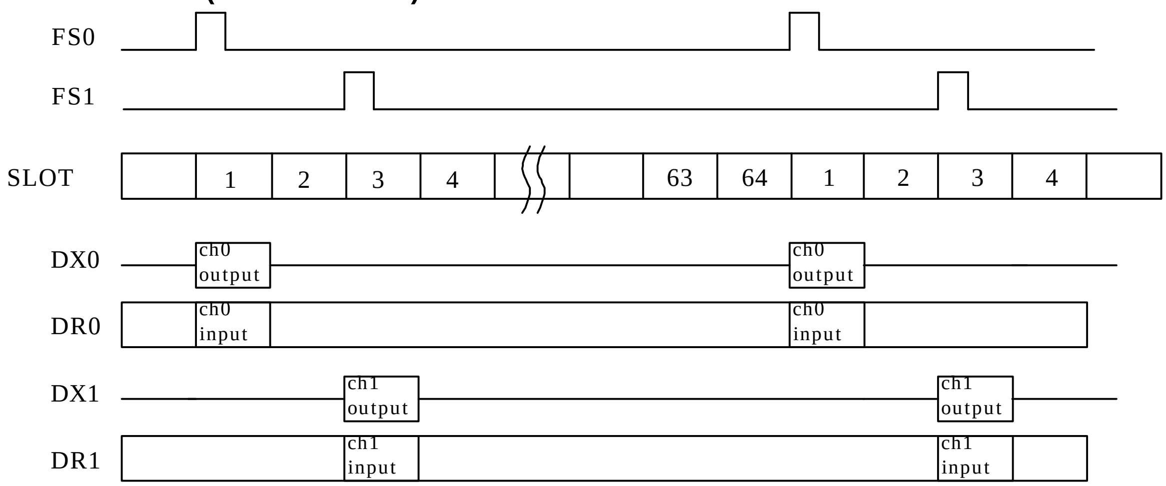
<Non Multiplex>

PCM data of each channel are interfaced by each I/O pins(DX0 and DR0/DX1 and DR1) at the format of 8bits in the period of 1 frame(125us) which synchronizes with the FSn(n=0,1). The timing of FS0 and FS1 can be set at optionally as far as they synchronize with BCLK.

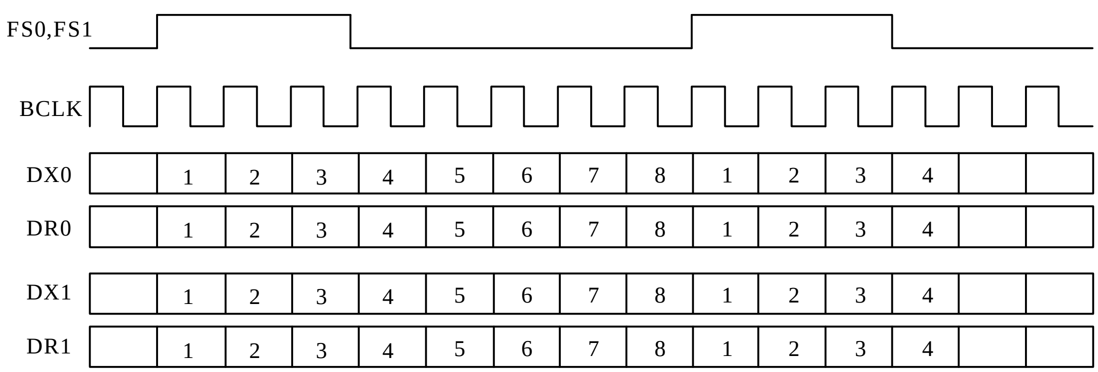
NOTE) First FS and Second FS

Only when BCLK=64kHz, it is possible to input the same clock to the first FS and the second FS. Except for 64kHz BCLK, 8 clock of BCLK x n (n=1-63 integral numbers) intervals of n slots are needed.

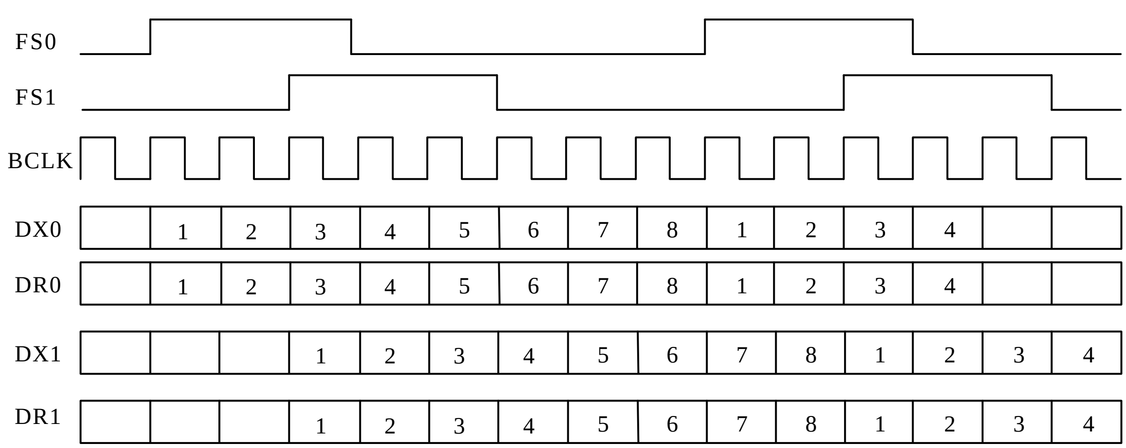
BCLK=4096kHz (First FS = FS0)



BCLK=64kHz(LF) (FS0 and FS1 at the same timing, First FS = FS0)



BCLK=64kHz(LF) (First FS = FS0)



GCI(General Circuit Interface)

Interface used for ISDN. This data format is as below.
PCM data channel assignment for B1 and B2 is defined by SEL2B register.

CH0,1selection

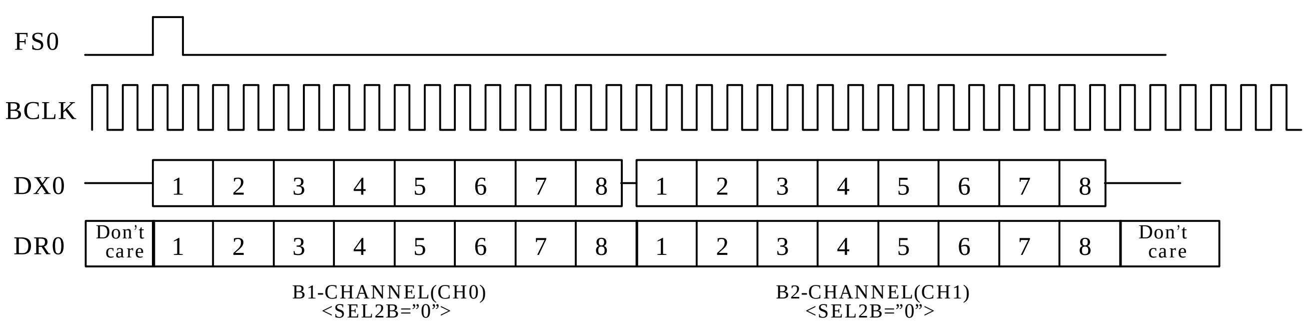
SEL2B	CH0	CH1	Remarks
0	B1	B2	Reset
1	B2	B1	

Note: BCLK is twice the PCM data rate.
BCLK is acceptable from 512kHz to 4096kHz.

INTERFACE TIMING

<2ch Multiplex>

PCM data of each channel is interfaced through DR0/DX0 pin in 8bits format.
They are accommodated in 1 frame(125us) which synchronizes with FS0.



<Non Multiplex>

Not supported.

IDL(Interchip Digital Link)

Interface used for ISDN. This data format is as below.
PCM data channel assignment for B1 and B2 channel is defined by SEL2B register.

CH0,1selection

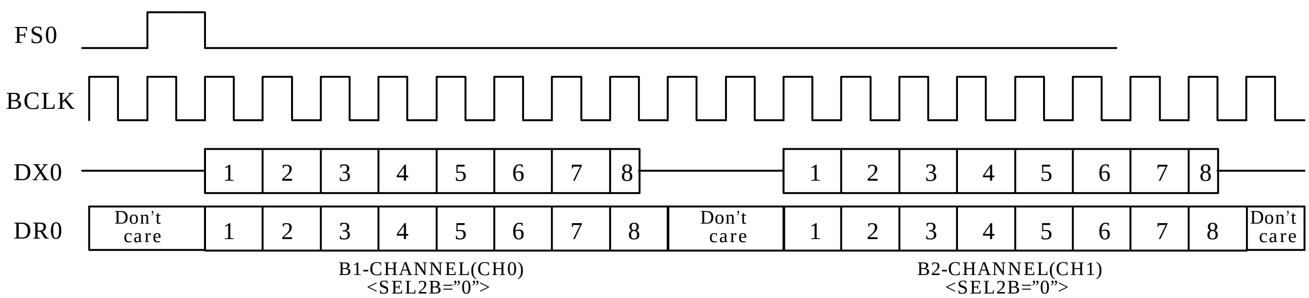
SEL2B	CH0	CH1	Remarks
0	B1	B2	Reset
1	B2	B1	

Note: BCLK is same as the PCM data rate.
BCLK is acceptable from 256kHz to 4096kHz.

INTERFACE TIMING

<2ch Multiplex>

PCM data of each channel is interfaced through DR0/DX0 pin in 8bits format.
They are accommodated in 1 frame(125us) which synchronizes with FS0.



<Non Multiplex>

Not supported.

RESET

POWER ON RESET

AK2305 automatically generates the internal reset pulse at the time of power on. Then all circuits are reset and internal registers are initialized.

After reset operation, CODEC CH0/CH1 circuits start to be initialized. It takes 150ms(typ.), 330ms(max) from power on to completion of initialization.

*)Output pins remain Hi-Z during the period in which the internal reset pulse is high(See page 5).
The period of the reset pulse is about 20ms(typ), 200ms(max).

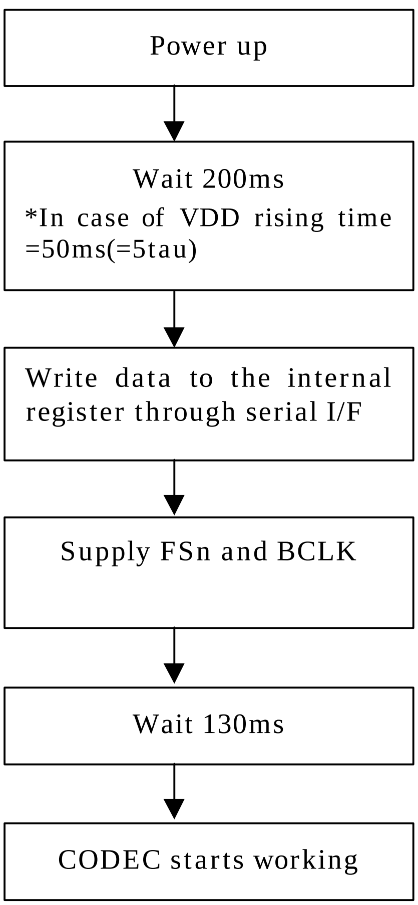
POWER-UP TIME FOR POWER ON RESET

When power-up time is no longer than 50ms(=5tau:tau is time constant), Power On Reset works normally.

When the time is longer than 50ms, Power On Reset is not available and no internal registers are initialized. All registers must be written.

RECOMMENDED START UP PROCEDURE

The following start up procedure is recommended when AK2305 is going to power up.



- TNOE0,1=" L"
- FSn=" L"
- BCLK=" L"

When 1stFS and BCLK are set to " L", CODEC ch0,ch1 dose not interface with external devices.

- Write data to the internal register before CODEC starts working.

- CODEC Initialization starts.

- CODEC Initialization complete.

POWER DOWN

Power consumption is reduced in power down mode.
In the power down mode, supply of current for analog circuits and clock for digital circuits, is stopped, and relating circuits are halted.

There are two power down modes.

- **Power down for all circuits**
- **Power down by block**

* In the power down mode, output pins of corresponded blocks turn to Hi-Z.(See page 4)

POWER DOWN MODE SETTING

Mode	Circuits	Pin/Registers		Operation for "0"/"1"	Note
All circuits	All	Pin	PD	"0" : Normal "1" : Power down	- Registers are not reset. **- Serial I/F is available.** - No need to supply FSn(n=0,1),BCLK.
Block	CODEC CH0	Registers	PDCH0	"0" : Normal "1" : Power down	- Keep supplying first FS, even when CODEC CH0,1 are in power down mode (see page8). - Even when CODEC CHn(n=0,1) is in power down mode, the functions below are available: (1) AMPTn(n=0,1) Input/Output (2) TONEGEN0,1 Output From VRXn(n=0,1), TNOUT - Even when all these blocks are in power down mode; AMPT0/1, VR0/1R, AMPR0/1, VRTN, TONEGEN0/1, BGREF, Serial IF, PLL operate normally at all the time.
	CODEC CH1		PDCH1		
	DTMF Receiver0		PDDT0		
	DTMF Receiver1		PDDT1		

Note) Initial value of PDCHn, PDDTn(n=0,1) are "0".

CANCELLATION OF POWER DOWN : CODEC

When power down mode for CODEC CH0/CH1 is cancelled, CODEC starts to be initialized.
It takes 130mS(typ.).

POWER DOWN MODE SETTING and POWER DOWN BLOCK

POWER DOWN BLOCK		ALL BLOCK	CODEC CH0	CODEC CH1	CODEC CH0&1	DTMFR0	DTMFR1	CODEC CH0, DTMFR0	CODEC CH1, DTMFR1
PIN REGISTER		PD	PDCH0	PDCH1	PDCH0 PDCH1	PDDT0	PDDT1	PDCH0 PDDT0	PDCH1 PDDT1
Channel 0	AMPT0	OFF						OFF	
	VR0T	OFF	OFF		OFF			OFF	
	AAF0	OFF	OFF		OFF			OFF	
	CODEC CH0	OFF	OFF		OFF			OFF	
	SMF0	OFF	OFF		OFF			OFF	
	VR0R	OFF							
	AMPR0	OFF							
Channel 1	AMPT1	OFF							OFF
	VR1T	OFF		OFF	OFF				OFF
	AAF1	OFF		OFF	OFF				OFF
	CODEC CH1	OFF		OFF	OFF				OFF
	SMF1	OFF		OFF	OFF				OFF
	VR1R	OFF							
	AMPR1	OFF							
PCM I/F		OFF			OFF				
TONEGEN 0		OFF							
TONEGEN 1		OFF							
VRTN		OFF							
DTMFR 0		OFF				OFF		OFF	
DTMFR 1		OFF					OFF		OFF
PLL		OFF							
BGREF		OFF							
SERIAL I/F									

MUTE

PIN CONTROL

The output on each channel can be muted independently by pin control.

MUTEn (n=0,1)	Operation	DXn pin (n=0,1)	VRXn pin (n=0,1)	Remarks
0	Normal	PCM data output	CODEC analog output	
1	Mute	High-Impedance	AGND*	*)TONE circuits are avialable even if the mute operates.

REGISTER CONTROL

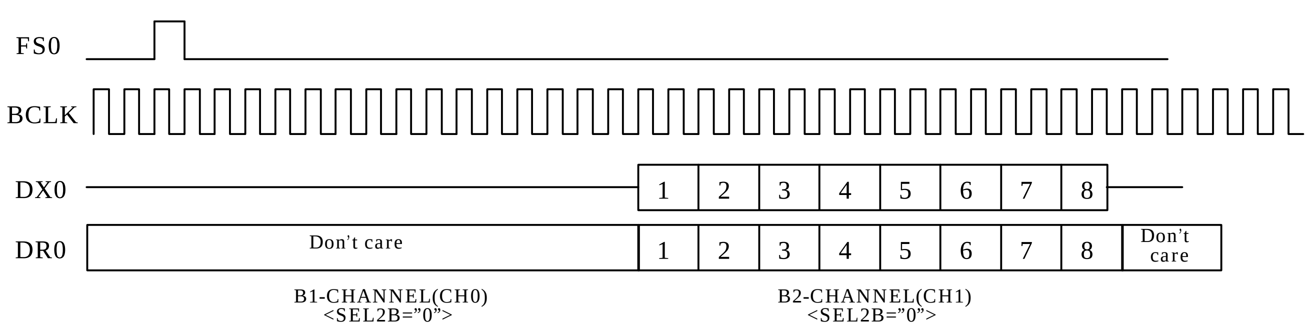
The output on each channel can be muted independently by register control.

MTDXn (n=0,1)	Operation	DXn pin (n=0,1)	VRXn pin (n=0,1)	Remarks
0	Normal	PCM data output	CODEC analog output* (MUTE0,1pin="0")	Reset
1	Mute	High-Impedance		

*) MUTEn is given priority over MTDXn. Therefore, for instance, even when MTDXn is "1," output of VRXn is AGND if MUTEn="1."

<Example>

CH0 muted (MUTE0="1," MUTE1="0," MTDX0,1="0" : GCI mode)



VRX0 : CODEC CH0 analog output is always at AGND level.
TONEGEN0,1output can be controlled by TNOE0,1 pin.

VRX1 : CODEC CH1 analog output is the signal converted from the PCM data of CH1 input through DR0 pin.
TONEGEN0,1 output can be controlled by TNOE0,1 pin.

GAIN ADJUSTMENT

Analog input/output gain can be adjusted at the range from0 to -12dB (3dB/step*5steps) by register.

VR register

VRnT2 VRnR2 VRTN2	VRnT1 VRnR1 VRTN1	VRnT0 VRnR0 VRTN0	Gain	Remarks
0	0	0	0 dB	Reset
0	0	1	-3 dB	
0	1	0	-6 dB	
0	1	1	-9 dB	
1	-	-	-12 dB	

*) This table is applicable to VR0T,VR0R,VR1T, VR1R ,and VRTN registers.

DTMF RECEIVER

This circuit detects and decodes the DTMF signal and outputs the 4bits code.
See the following table.

Output code table (n=0,1)

Low Tone [Hz]	High Tone [Hz]	KEY	DTO n3	DTO n2	DTO n1	DTO n0
697	1209	1	0	0	0	1
	1336	2	0	0	1	0
	1477	3	0	0	1	1
770	1209	4	0	1	0	0
	1336	5	0	1	0	1
	1477	6	0	1	1	0
852	1209	7	0	1	1	1
	1336	8	1	0	0	0
	1477	9	1	0	0	1
941	1336	0	1	0	1	0
	1209	*	1	0	1	1
	1477	#	1	1	0	0
697	1633	A	1	1	0	1
770	1633	B	1	1	1	0
852	1633	C	1	1	1	1
941	1633	D	0	0	0	0

DECODED OUTPUT

Decoded DTMF signals are output at DTO00-03,10-13 pins through tri-state buffers.
The outputs are enabled by DTOE pin.

DTOE Input	DTO00-03, DTO10-13 Output
0	Hi-Impedance
1	Decoded Output

GUARD TIME SETTING

Input Signal Available Time(t_{REC}) and Inter Digit Pause Time(t_{ID}) can be settled by adjusting Guard Time as follows. Guard Time is adjusted by GTPn, GTAn(n=0-3.)

Input Signal Available Time(t_{REC}) = Detecting Signal Time(t_{DP}) + Guard Time(t_{GTP})
Inter Digit Pause Time(t_{ID}) = Detecting Signal-stop Time(t_{DA}) + Guard Time(t_{GTA})

Range of adjusting Guard Time(t_{GTP}, t_{GTA})	1ms - 121 ms
Step of adjusting Guard Time(t_{GTP}, t_{GTA})	8ms

Regarding the relation between GTPn / GTAn(n=0-3) and Guard Time, see the next page.
Also the relation between Input Signal Available Time(t_{REC}) and Inter Digit Pause Time(t_{ID}) is shown.

Relation between GTPn(n=0- 3) Register and
GUARD TIME(t_{GTP}) / Input Signal Available Time(t_{REC})

GTP Register				tGTP[ms]	tREC[ms]=tGTP+tDP			
3	2	1	0	typ	min	typ	max	
0	0	0	0	1	6	12	15	
0	0	0	1	9	14	20	23	
0	0	1	0	17	22	28	31	
0	0	1	1	25	30	36	39	
0	1	0	0	33	38	44	47	← tGTP default
0	1	0	1	41	46	52	55	
0	1	1	0	49	54	60	63	
0	1	1	1	57	62	68	71	
1	0	0	0	65	70	76	79	
1	0	0	1	73	78	84	87	
1	0	1	0	81	86	92	95	
1	0	1	1	89	94	100	103	
1	1	0	0	97	102	108	111	
1	1	0	1	105	110	116	119	
1	1	1	0	113	118	124	127	
1	1	1	1	121	126	132	135	

tDP[ms]		
min	typ	max
5	11	14

Relation between GTAn(n=0- 3) Register and
GUARD TIME(t_{GTA}) / Inter Digit Pause Time(t_{ID})

GTA Register				tGTA[ms]	tID[ms]=tGTA+tDA			
3	2	1	0	typ	min	typ	max	
0	0	0	0	1	1.5	5	9.5	
0	0	0	1	9	9.5	13	17.5	
0	0	1	0	17	17.5	21	25.5	← tGTA default
0	0	1	1	25	25.5	29	33.5	
0	1	0	0	33	33.5	37	41.5	
0	1	0	1	41	41.5	45	49.5	
0	1	1	0	49	49.5	53	57.5	
0	1	1	1	57	57.5	61	65.5	
1	0	0	0	65	65.5	69	73.5	
1	0	0	1	73	73.5	77	81.5	
1	0	1	0	81	81.5	85	89.5	
1	0	1	1	89	89.5	93	97.5	
1	1	0	0	97	97.5	101	105.5	
1	1	0	1	105	105.5	109	113.5	
1	1	1	0	113	113.5	117	121.5	
1	1	1	1	121	121.5	125	129.5	

tDA[ms]		
min	typ	max
0.5	4	8.5

NOTE
tGTA in tables above are typical value. Regard the margin of ±1ms.

TONE GENERATOR

Generates two kinds of tone, 400Hz and 1300Hz.
One of them is selected by TMDn register.

SELECTION OF TONE

Selects 1 tone from 400Hz/1300Hz by TMDn register.

Tone selection register

TMDn	Tone frequency	Remarks
0	400Hz	Reset
1	1300Hz	

(n=0,1)

SELECTION OF OUTPUT PIN

VRX0, VRX1, TNOUT is available for Tone output pin by S1-S9 switch.
S1-S9 switch is controlled by each register.

Tone output by switch controlling

Output circuits	VRX0	VRX1	TNOUT	Register setting	Remarks
TONEGEN0	S1	S4	S7	"0" : OFF "1" : ON	All "0" when reset
TONEGEN1	S2	S5	S8		
AUX	S3	S6	S9		

TONE OUTPUT ENABLE

Inputting "1" to TNOEn, defined tone is output.

Tone Output Enable

TONEn	Output States
0	AGND
1	Tone

AUX INPUT

Input signal from external CPU/Tone generators.
Signals are output on VRXn, TNOUT via VRnR, VRTN.
Output signals are switched onto each pin by S3, S6, and S9 which are controlled by registers.
(See "SELECTION OF OUTPUT PIN" above.)

Must input with an external cap(>0.1uF.)
Input impedance is 200kΩ±25%.

SERIAL INTERFACE

The internal registers can be read/written with SCLK, DATA, and $\overline{CS}$ pins.

1word consists of 14bits. The first 2bits are the instruction code which specifies read/write.
The following 3bits specify the address. The rest of 8bits are for setting registers.

B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
I1	I0	A2	A1	A0	*	D7	D6	D5	D4	D3	D2	D1	D0
Instruction code (2bit)		Address (3bit)			*	Data for setting internal registers (8bit)							

*)Dummy bit for adjusting the I/O timing when reading data.

INSTRUCTION CODE

I1	I0	Read/Write
1	0	Read
1	1	Write
Other codes		No action

SCLK and WRITE / READ

(1) Input data are loaded into the internal shift register at the rising edge of SCLK.
(2) The rising edge of SCLK is counted after the falling edge of $\overline{CS}$.
(3) When $\overline{CS}$ is "L" and more than 14 SCLK pulses:
[WRITE] Data are loaded into the internal register at the rising edge of the SCLK 14th pulse.
[READ] DATA pin is switched to an input pin at the falling edge of the SCLK 14th pulse.

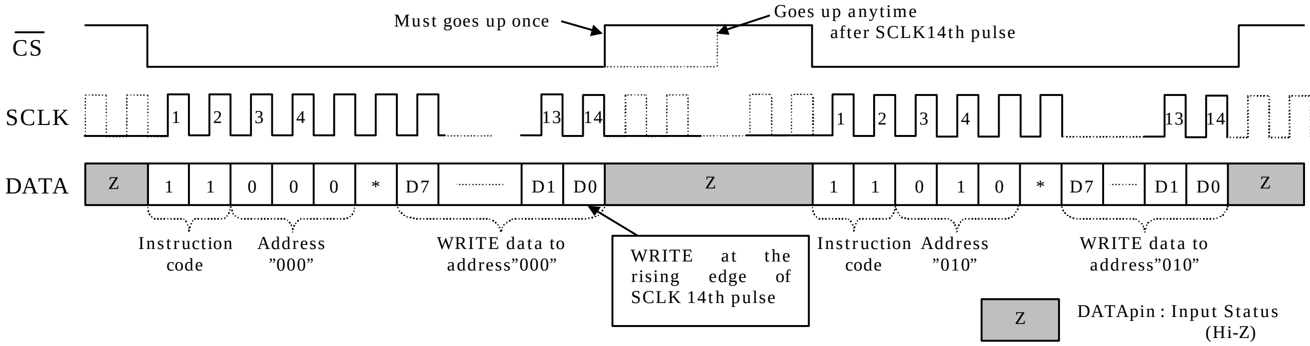
$\overline{CS}$ and WRITE / READ CANCELLATION

(1) WRITE is cancelled when $\overline{CS}$ goes up before the rising edge of the SCLK 14th pulse.
(2) READ is cancelled when $\overline{CS}$ goes up before the falling edge of the SCLK 14th pulse.

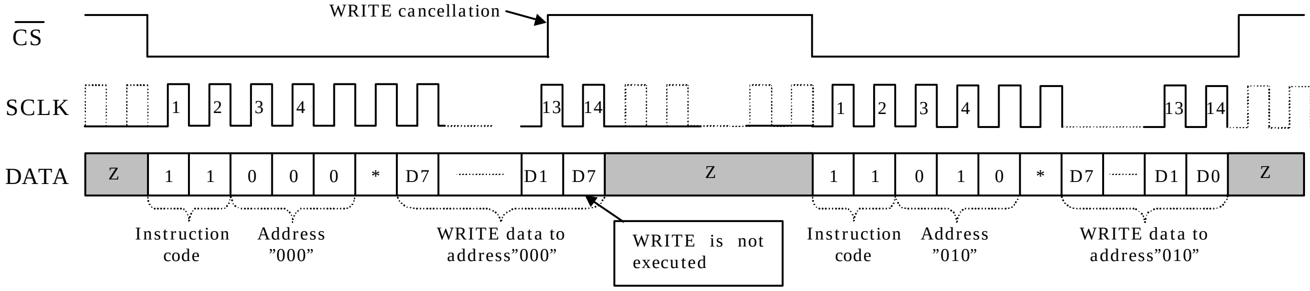
SERIAL WRITE / READ (SERIAL ACCESS)

(1) $\overline{CS}$ must go up to "H" before the next access in successive access.
(2) When the next access is going to be done , if $\overline{CS}$ remains to be "L", successive access can not be done.

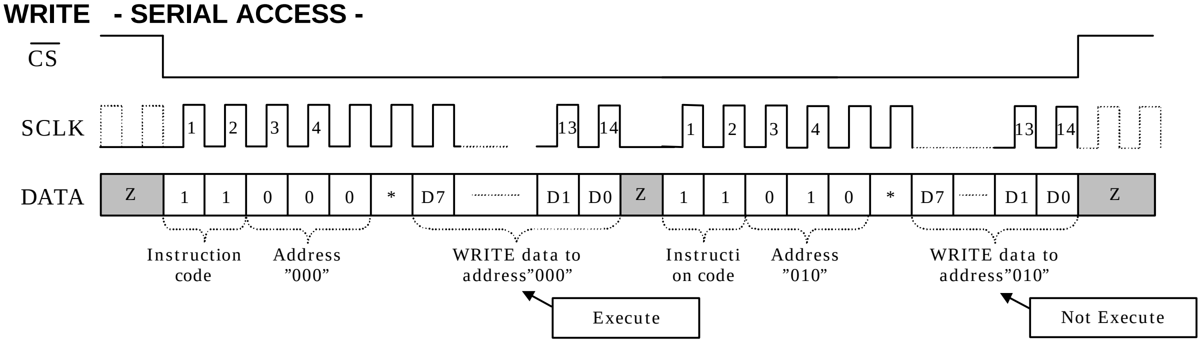
WRITE



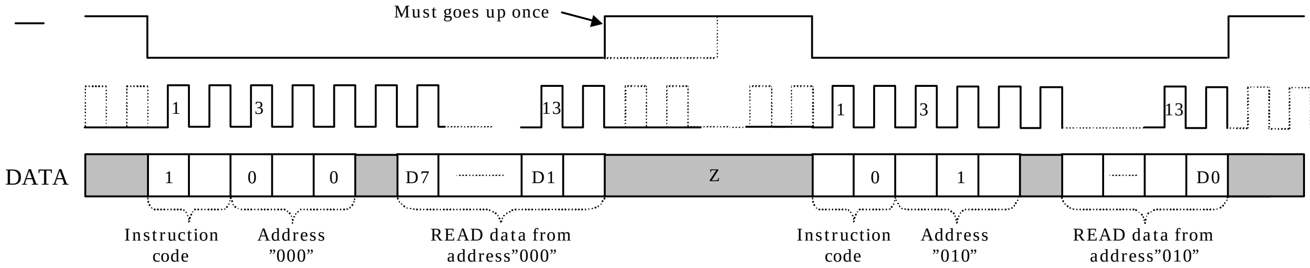
WRITE - CANCELLATION -



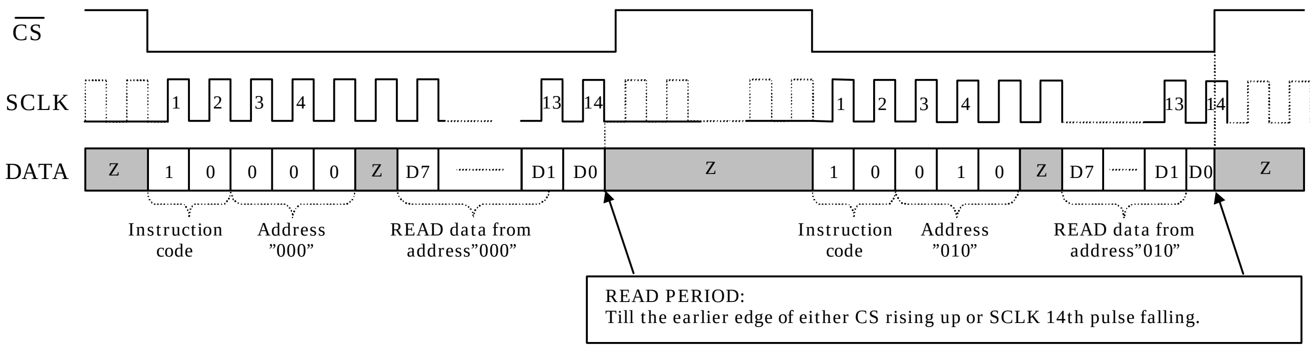
WRITE - SERIAL ACCESS -



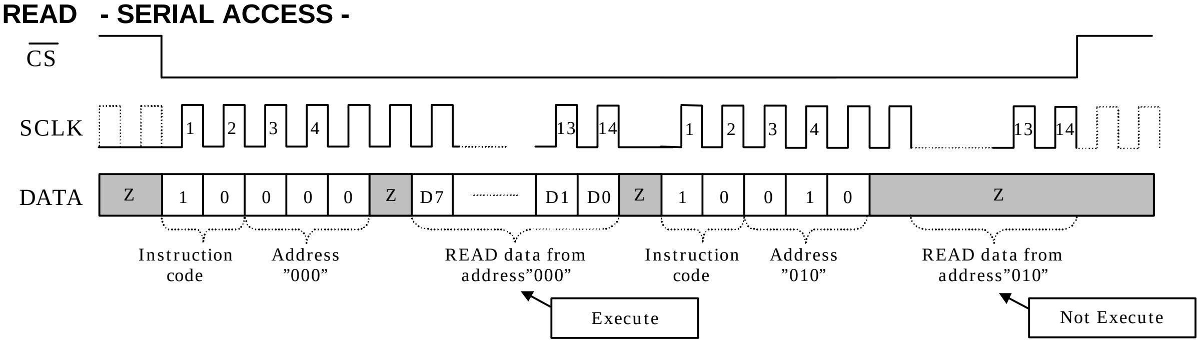
READ



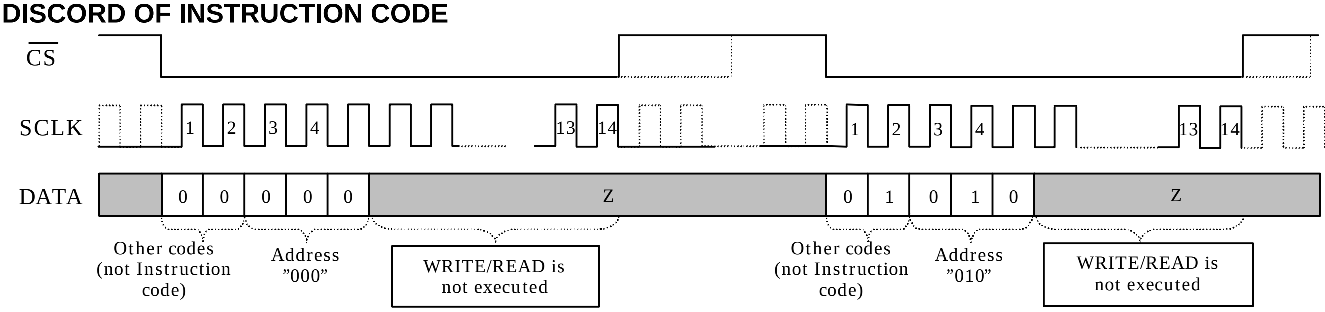
READ - OUTPUT PERIOD OF DATA PIN -



READ - SERIAL ACCESS -



DISCORD OF INSTRUCTION CODE



REGISTER

REGISTER MAP

Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
A2	A1	A0	*	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	*	-	VR0T2	VR0T1	VR0T0	-	VR0R2	VR0R1	VR0R0
0	0	1	*	-	VR1T2	VR1T1	VR1T0	-	VR1R2	VR1R1	VR1R0
0	1	0	*	-	S9	S8	S7	-	VRTN2	VRTN1	VRTN0
0	1	1	*	-	S6	S5	S4	-	S3	S2	S1
1	0	0	*	PCMIF1	PCMIF0	SEL2B	1stFS	PDDT1	PDDT0	PDCH1	PDCH0
1	0	1	*	-	-	-	ALAWN	MTDX1	MTDX0	TMD1	TMD0
1	1	0	*	GTA3	GTA2	GTA1	GTA0	GTP3	GTP2	GTP1	GTP0

*) Dummy Bit
Note) All registers are available for write/read.

INITIALIZATION OF REGISTERS

Only at POWER ON RESET, registers are initialized.
When POWER ON RESET is not used, all registers should be set through a serial interface.

FUNCTION OF REGISTER

Address	Bit	Name	Default	Function	Refer to
000	0	VR0R0	0	**Receive gain adjustment on ch0** 0 to -12dB by 3dBstep 000: 0dB 1xx: -12dB	18
	1	VR0R1	0		
	2	VR0R2	0		
	3	-	0	Not used	
	4	VR0T0	0	**Transmit gain adjustment on ch0** 0 to -12dB by 3dBstep 000: 0dB 1xx: -12dB	
	5	VR0T1	0		
	6	VR0T2	0		
	7	-	0	Not used	
	8	-	-	Dummy bit	
001	0	VR1R0	0	**Receive gain adjustment on ch1** 0 to -12dB by 3dBstep 000: 0dB 1xx: -12dB	
	1	VR1R1	0		
	2	VR1R2	0		
	3	-	0	Not used	
	4	VR1T0	0	**Transmit gain adjustment on ch1** 0 to -12dB by 3dBstep 000: 0dB 1xx: -12dB	
	5	VR1T1	0		
	6	VR1T2	0		
	7	-	0	Not used	
	8	-	-	Dummy bit	
010	0	VRTN0	0	**Gain adjustment of tone output** 0 to -12dB by 3dBstep 000: 0dB 1xx: -12dB	18
	1	VRTN1	0		
	2	VRTN2	0		
	3	-	0	Not used	
	4	S7	0	**Switch regulation for tone output** 0: Tone OFF 1: Tone ON	21
	5	S8	0		
	6	S9	0		
	7	-	0	Not used	
	8	-	-	Dummy bit	
011	0	S1	0	**Switch regulation for tone output** 0: Tone OFF 1: Tone ON	
	1	S2	0		
	2	S3	0		
	3	-	0	Not used	
	4	S4	0	**Switch regulation for tone output** 0: Tone OFF 1: Tone ON	
	5	S5	0		
	6	S6	0		
	7	-	0	Not used	
	8	-	-	Dummy bit	

Address	Bit	Name	Default	Function	Refer to
100	0	PDCH0	0	**CODEC ch0,1 Power down control**	15
	1	PDCH1	0	0: Power ON 1: Power OFF	
	2	PDDT0	0	**DTMF Receiver 0,1 Power down control**	
	3	PDDT1	0	0: Power ON 1: Power OFF	
	4	1stFS	0	**First FS select** 0: FS0 1: FS1	9
	5	SEL2B	0	**PCM data channel assignment** 0: CH0->B1	12
	6	PCMIF0	0	**PCM interface select**	9
	7	PCMIF1	0	Multiplex/Non Multiplex	
	8	-	-	Dummy bit	
101	0	TMD0	0	**TONEGEN 0,1 tone frequency select**	21
	1	TMD1	0	0: 400Hz 1: 1300Hz	
	2	MTDX0	0	**PCM output(DX0,1pin) Mute**	17
	3	MTDX1	0	0: PCM OUT 1: PCM MUTE	
	4	ALAWN	1	**A-law/u-law select** 0:A-law 1:u-law	8
	5	-	0	Not used	
	6	-	0		
	7	-	0		
	8	-	-	Dummy bit	
110	0	GTP0	0	**DTMF Receiver** **Guard Time t_{GTP} setting**	20
	1	GTP1	0		
	2	GTP2	0		
	3	GTP3	0		
	4	GTA0	0	**DTMF Receiver** **Guard Time t_{GTA} setting**	20
	5	GTA1	0		
	6	GTA2	0		
	7	GTA3	0		
	8	-	-	Dummy bit	

BSOLUTE MAXIMUM RATINGS

Parameter		Min	Max	
Power Supply Voltages Digital Power Supply	 DVDD AVDD	 -0.3	 6.5	 V V
	DVSS	-0.1		V
Digital Input Voltage	TD	-0.3		V
Analog Input Voltage	TA	-0.3		V
Input current (except power supply pins)	IN		10	
Storage Temperature	Tstg		125	C

Note 1) All voltages with respect to ground. AVSS= =0V

Normal operation is not guaranteed at these extremes.

R OPERATING ONDITIONS

Parameter		Min	Typ		Units
Power Supplies Analog power supply Digital power supply	 DVDD	 4.75	 5.0 5.0	 AVDD	 V
Ambient Operating Temperature	Ta			85	C
Frame Sync Frequency	FS0,FS1		8		

Note 1) If DVDD is greater than AVDD, then IDD will increase

) All voltages reference to ground AVSS= =0V

LECTRICAL C

Unless otherwise noted, guaranteed for AVDD=DVDD=+5V +/– 5%, Ta = – ~ +85 o , FS0,FS1=8kHz

DC Characteristics

Parameter		Conditions	Min		Max	Units
Power Consumption	DD1	All outp unloaded			105	
	PDD	PDCH0,1 PDDT0,1=1,0 All o ut unload		60	78.8	
Output High Voltage1	VOH	IOH mA Except for DTOn0-n3(n=0,1)				V
Output Low Voltage (CMOS level)	V 1	I =1.6mA			0.4	V
(TTL level)	V		2.0			V
(TTL level)	V				0.8	V
	Ii		10		+10	A
Input Capacitance					5	pF
Current	Io		-10		+10	A

CODEC

Absolute Gain

	Conditions		Typ		Units
	Input: 0dBm0@1020Hz				Vrms
		-0.6	-		dB
	Input: 0dBm0@1020Hz				Vrms
		-0.6	-		dB
	3.14dBm0				Vrms

Parameter			Min		Max	
Transmit Gain Tracking Error		-55dBm0 ~	-1.2	-		
		-50dBm0　-40dBm0			0.4	
	1020Hz Tone	~	-0.2	-		
Receive Gain Tracking Error		-55dBm0　-50dBm0			1.2	
	-10dBm0	~	-0.4	-		dB
		-40dBm0　3dBm0			0.2	

Parameter			Min		Max	
Transmit Frequency Response		0.05kHz	-	-		
					-26	
		0.2kHz		-		
		0.3　3.0kHz			0.15	
		3.4kHz			0	
					-14	
	Relative to:	~	-0.15	-		
		3.4kHz			0	
		4.0kHz	-	-		

Distortion

	Conditions			Typ		Units
	1020Hz Tone	~	25	-	-	
		-30dBm0　-40dBm0				dB
		~	36	-	-	
	1020Hz Tone	~	25	-	-	
		-30dBm0　-40dBm0				dB
		~	36	-	-	
Transmit			-	-		dB
Receive			-	-		dB
	-6dBm@860Hz,1380Hz		-	-		dB

-Law, Psophometric Weighted for A-Law

Parameter	Conditions		Typ	Max	
Transmit Delay, Absolute	f =1600Hz		-	560	
Transmit Delay, Relative	f =500Hz 600Hz	-		220	us
	f =600Hz 1000Hz	-		145	
	f =1000Hz 2600Hz	-		75	
	f =2600Hz ~	-	-		
	f =2800Hz 3000Hz	-		155	
Receive Delay, Absolute				450	us
Relative to f=1600Hz	f =500Hz ~	-40	-		us
	f =1000Hz ~	-30	-		
	f =1600Hz ~	-	-		
	~2800Hz		-	125	
	~3000Hz		-	175	

Parameter	Conditions			Typ	Max	
Idle Channel Noise	u		-		10	dBrnC0
→	A-law, Psophometric		-		-80	
Idle Channel Noise 2)	u			5		dBrnC0
→	A-law, Psophometric		-		-80	
Noise, Single Frequency	f=0 100kHz		-		-53	
PSRR, Transmit	± f=0 50kHz					dB
	AVDD=DVDD=5V 100mVop ~		40	-	-	
Spurious Out-of-Band Signal at VRX Output	0.3 3.4kHz	4.6 7.6kHz	-	-		dB
		~			-	
		8.4 100kHz	-	-		

Note 1) Analog Input = Analog Ground

Note 3) Not tested in production. Parameters guaranteed by design.

Parameter		Min		Max	
Transmit to Receive		-		-75	
Receive to Transmit		-		-75	
Transmit to Transmit		-		-75	
Receive to Receive		-		-75	

Intrachannel Crosstalk

	Conditions		Typ		Units
	0dBm0@VFXIN, Idle PCM code		-		dB
	0dBm0 code level, VFXIN = 0 Vrms		-		dB

Parameter		Min		Max	
Input Leakage Current		-100		+100	
Input Resistance			-		MΩ
Load Resistance			-		k
Load Capacitance			-		pF
		-		-	
Output		-		10	Ω

Parameter		Min		Max	
Output Voltage		2.3		2.5	
Load Resistance					k
Load Capacitance					pF
			3.6		
Output				10	Ω

Parameter		Min		Max	
Input Leakage Current		-100		+100	
Input Resistance			-		M
Load Resistance			-		k
Load Capacitance			-		pF
		-		-	
Output		-		10	Ω

Volume VR0T,VR0R,VR1T,VR1R,VRTN

	Pin		Min		max	
Step margin			-0.5			dB

Parameter		Conditions		typ		Unit
	TNOUT	VRTN=0dB				dBm
	AUX			200		k
Abcolute gain	TNOUT	VRTN=0dB		0		dB
(Relative to output signal 1kHz input)	TNOUT	VRTN=0dB		0		dB

Tone Generator

		Conditions		typ		Units
Signal			381		419	
	1300Hz			1300		Hz
			-11		-9	
Out of band noize level		4k-8kHz				dB
					P-40	
					P-60	

Note) dBm = decibels above or below a reference power of 1mW into a 600
P = output level of in band transmit signal.

Parameter		min		Max	
Valid Input Signal Levels signal)		-19			dBm
	Note3,6,8		10		
Frequecy Deviation accept				± ±	
Frequecy Deviation Reject		±			
Third Tone Tolerance			-16		
Noise Tolerance			-12		
Dial Tone Tolerance			-17		
Input Impeedance		500			Ω

Note2)Both tones of the composite signal have equal amplitudes.
± ±
Note4)Bandwidth limited to 3kHz Gaussian noise.
± ±
Note6)For error rate of better than 1 in 10,000.

Note8)Twist = high tone / low tone
dBm = decibels above or below a reference power of 1mW into a 600

Parameters		Condition		Typ		Units	s
	t		5		14		
Tone Absent Detection Time	DA			4		ms	
	t		48		-		
Tone Duration Reject(*1)	R		-		37		
Interdigit Pause Accept(*1)	ID			-		ms	
	t O			-		ms	
	t	DTOE=5V,unloaded		-		us	
	t	DTOE=5V,unloaded		-		us	
	t	DTOE=5V,unloaded		-		us	
	t	R =10k, C =50pF			40		
Output Data Disable(DTOE to DTO)	PTD	L L		10		ns	

GTPn, (n=0-3) are default. Adjustable by setting GPAn

See p.19 & p.20.

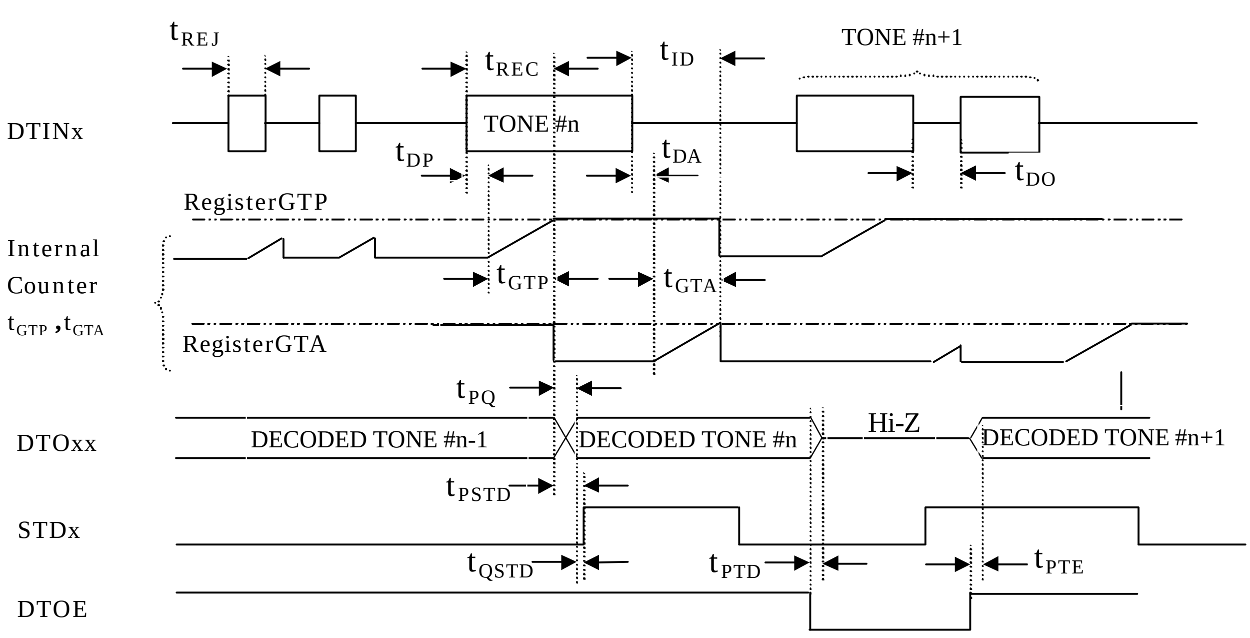


Figure 1 : DTMF Receiver Timing

Timing Specification

Unless otherwise noted, the specification applies for TA = -40 to +85°C, DVDD = AVDD = 5V±5%,DVSS = AVSS = 0V and FS0,FS1 = 8kHz. All timing parameters are measured at VOH = 2.0V and VOL =0.7V.

Lomg Frame,Short Frame,GCI, IDL Timing

Parameter	Symbol	Min	Typ	Max	Unit	Ref fig
FS Frequency	$1/t_{PF}$	-	8	-	kHz	Fig.2 Fig.3 Fig.4 Fig.5
BCLK Frequency	$1/t_{PB}$	64		4096	kHz	
BCLK Pulse Width High	t_{WBH}	80			ns	
BCLK Pulse Width Low	t_{WBL}	80			ns	
Rising Time: (BCLK,FS0,FS1,DX0,DX1,DR0,DR1)	t_R			40	ns	
Falling Time: (BCLK,FS0,FS1,DX0,DX1,DR0,DR1)	t_F			40	ns	
Hold Time: BCLK Low to FS High	t_{HBF}	40			ns	
Setup Time: FS High to BCLK Low	t_{SFB}	70			ns	
Setup Time: DR to BCLK Low	t_{SDB}	40			ns	
Hold Time: BCLK Low to DR	t_{HBD}	40			ns	
Delay Time: BCLK High to DX valid (Note1)	t_{DBD}			60	ns	
Long Frame						
Hold Time: 2nd period of BCLK Low to FS Low	t_{HBFL}	40			ns	Fig.2
Delay Time: FS or BCLK High, whichever is later,to DX valid (Note1)	t_{DZFL}			60	ns	
Delay Time: FS or BCLK Low, whichever is later, to DX High-Z (Note1)	t_{DZCL}	10		60	ns	
FS Pulse Width Low	t_{WFSL}	1			BCLK	
Short Frame						
Hold Time: BCLK Low to FS Low	t_{HBFS}	40			ns	Fig.3
Setup Time: FS Low to BCLK Low	t_{SFBS}	40			ns	
Delay Time: BCLK Low to DX High-Z (Note1)	t_{DZCS}	10		60	ns	
GCI						
BCLK Frequency	$1/t_{PB}$	512		4096	kHz	Fig.4
Delax Time: Second BCLK Low to DX High-Z	t_{DZCG}	10		60	ns	
Setup Time: DR to Second BCLK High	t_{SDBG}	40			ns	
Hold Time: Second BCLK High to DR	t_{HBDG}	40			ns	
IDL						
BCLK Frequency	$1/t_{PB}$	256		4096	kHz	Fig.5

Note1) When with 150pF cap, and two LSTTL operating.

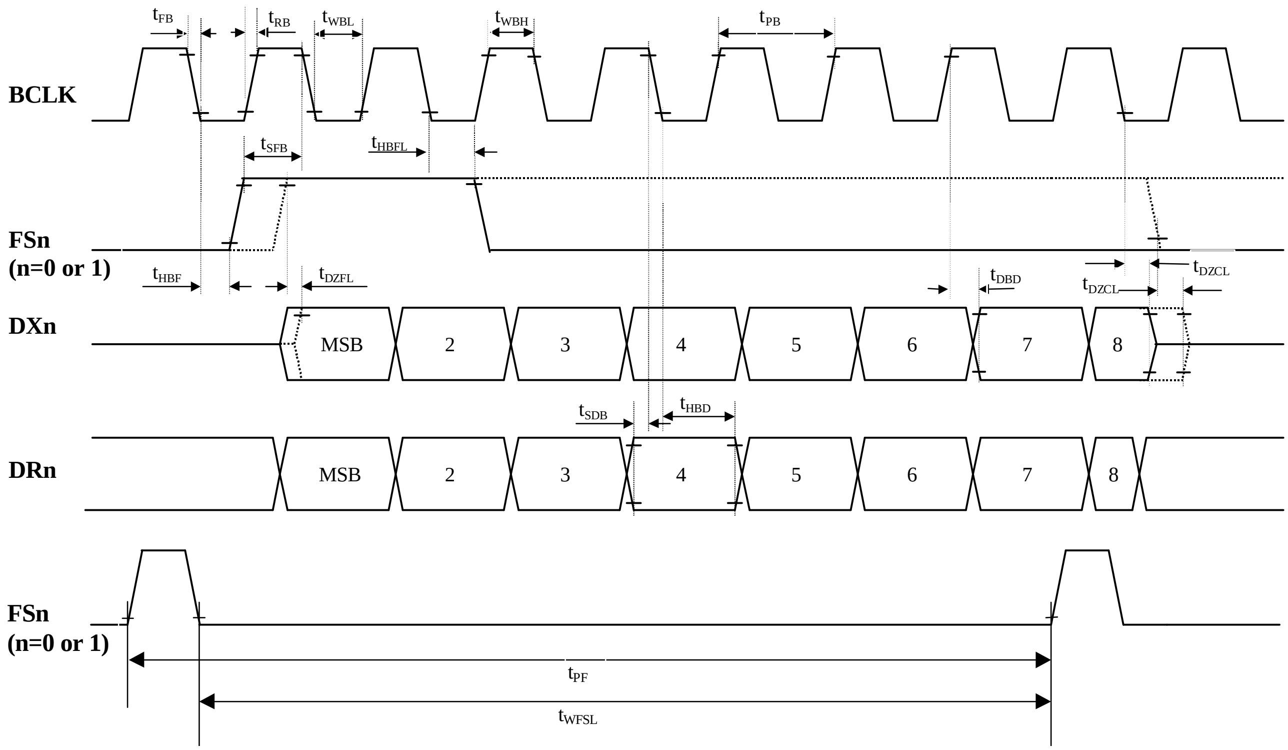


Figure2 : PCM Interface Timing < Long Frame >

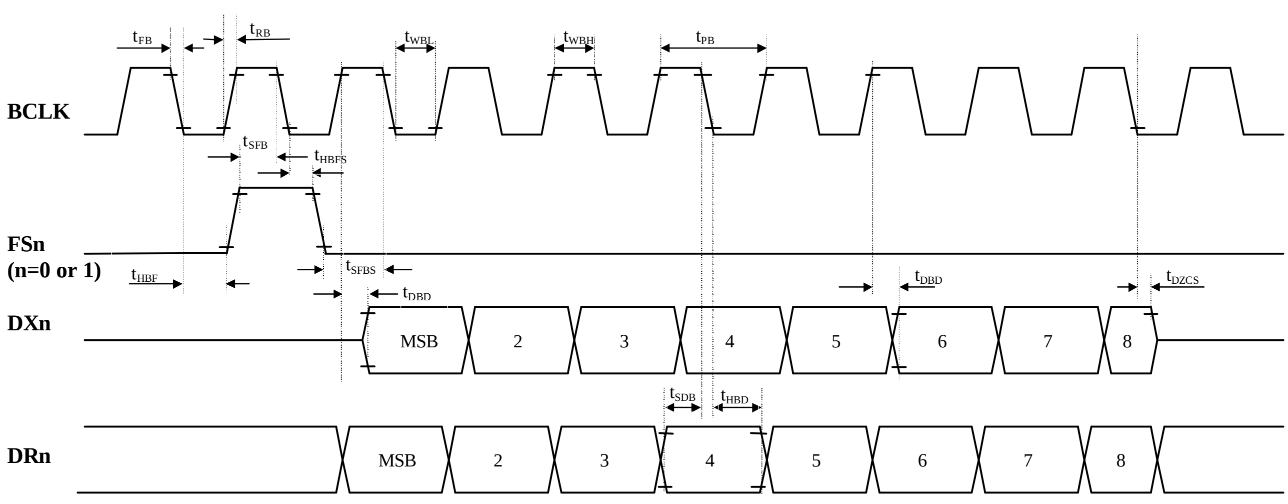


Figure3 : PCM Interface Timing < Short Frame >

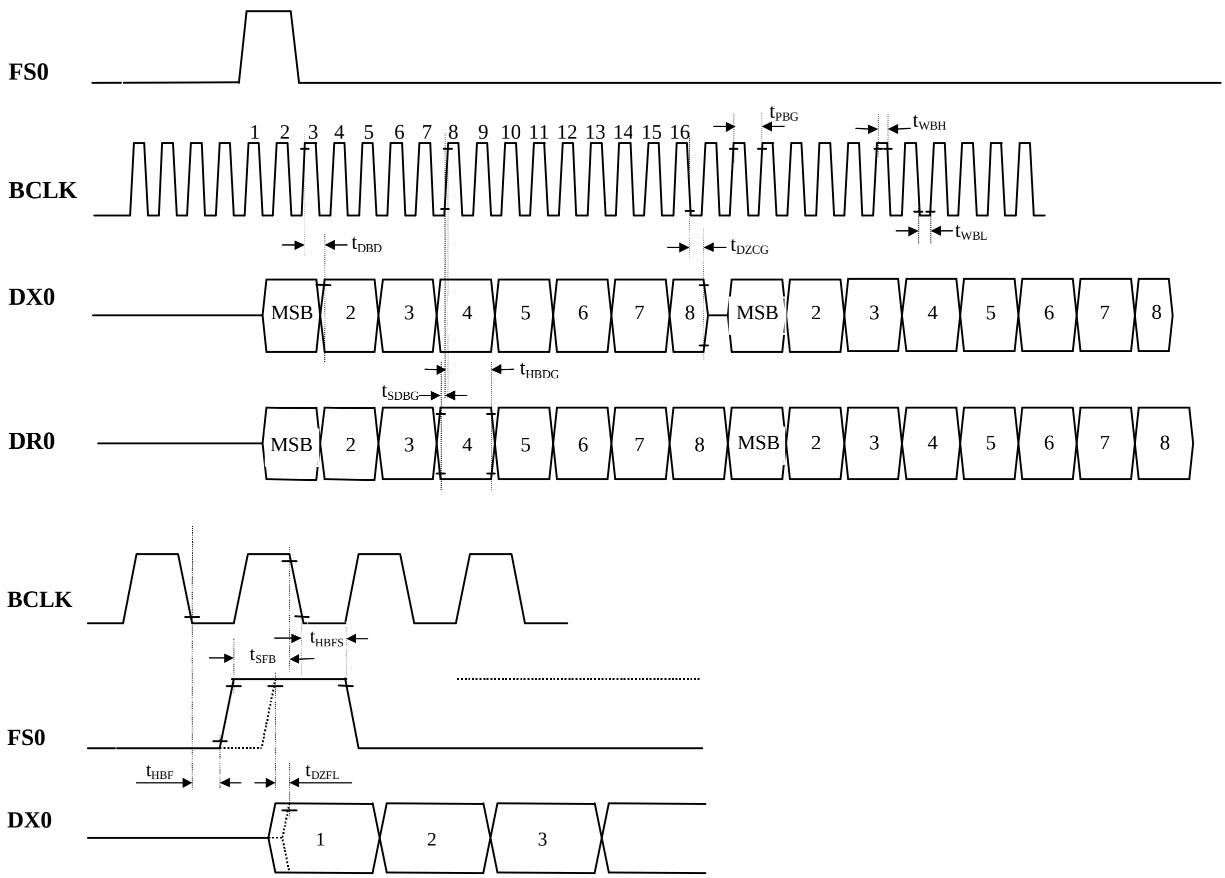


Figure4 : PCM Interface Timing < GCI >

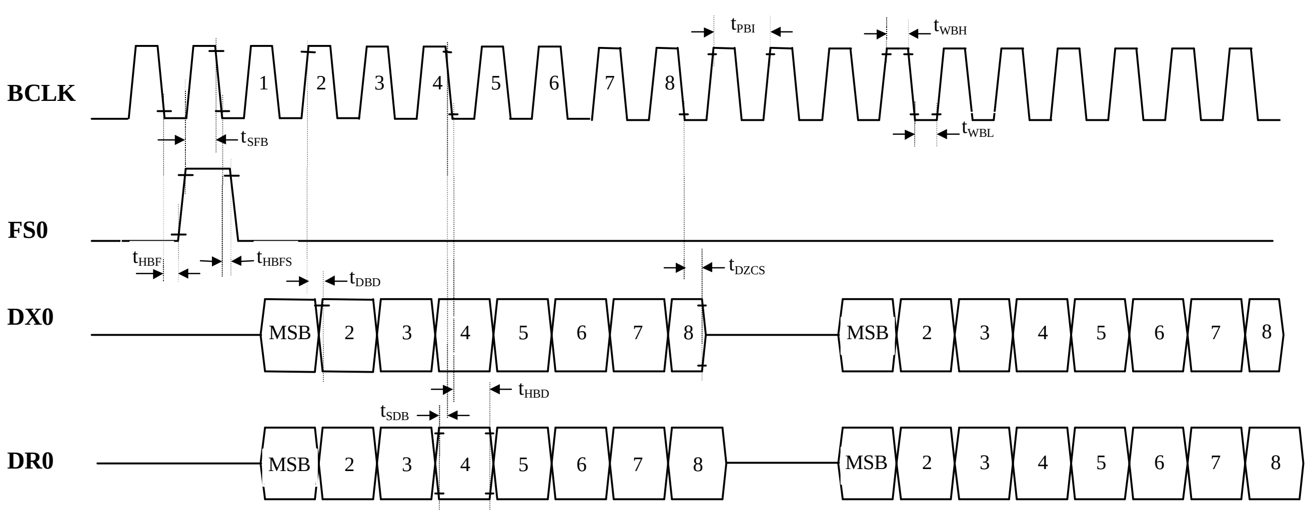


Figure5 : PCM Interface Timing < IDL >

Serial Interface Timing

Parameter	Symbol	Min	Typ	Max	Unit	Ref fig
SCLK Frequency	$1/t_{PSCLK}$			4	MHz	Fig.6
SCLK Pulse Width High	t_{WSH}	40			ns	
SCLK Pulse Width Low	t_{WSL}	40			ns	
$\overline{CS}$ Pulse Width Low	t_{WCL}	14			SCLK	
Hold Time: SCLK High to $\overline{CS}$ Low	t_{HCS}	80			ns	
Setup Time: $\overline{CS}$ Low to SCLK High	t_{SCS}	40			ns	
Rising Time: $\overline{CS}$,SCLK	t_R			100	ns	
Falling Time: $\overline{CS}$,SCLK	t_F			100	ns	
W R I T E						
Setup Time: DATA to SCLK High	t_{SDC}	40			ns	Fig.6
Hold Time: SCLK High to DATA	t_{HDC}	40			ns	
Hold Time: SCLK Low to $\overline{CS}$ High	t_{HCS2}	0			ns	
R E A D						
Delay Time: SCLK Low to DATA pin drive	t_{DVD}	0			ns	Fig.7
Delay Time: SCLK Low to DATA valid	t_{DDD}			60	ns	
Delay Time: SCLK Low to DATA High-Z	t_{DZSD}	0		60	ns	Fig.8
Delay Time: $\overline{CS}$ High to DATA High-Z	t_{DZCD}	0		60	ns	
$\overline{CS}$ Pulse Width High	t_{WCH}	40			ns	

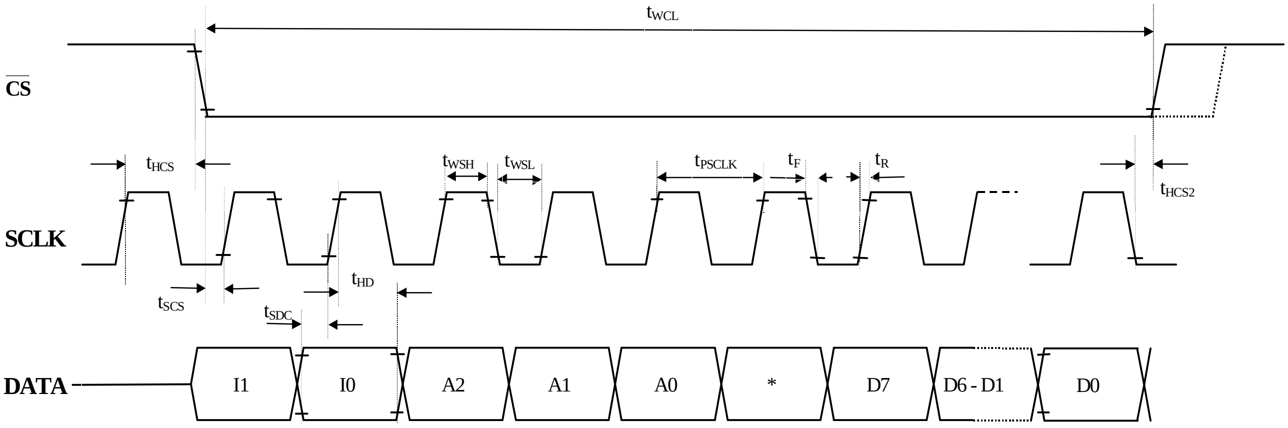


Figure6 : Serial Interface Timing < WRITE >

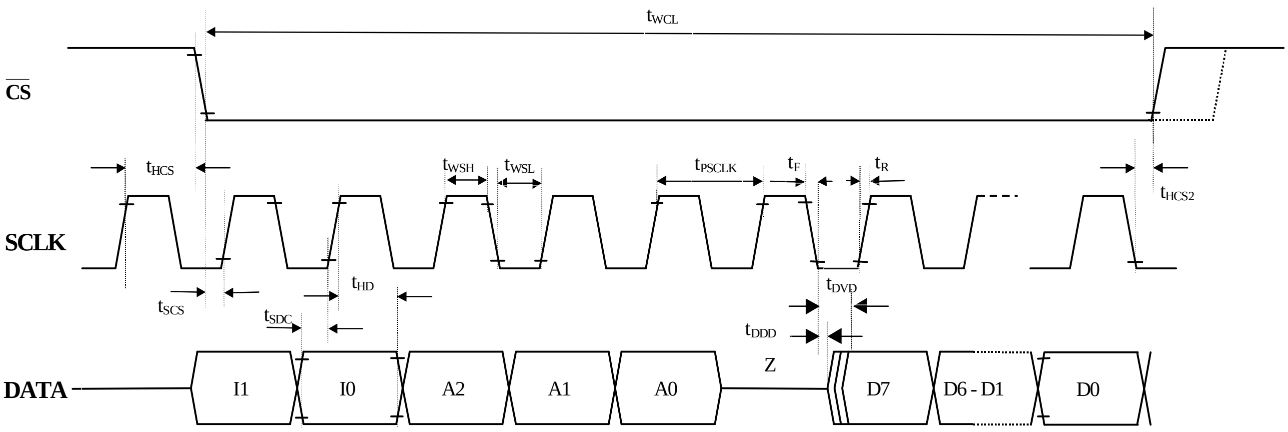


Figure7 : Serial Interface Timing < READ >

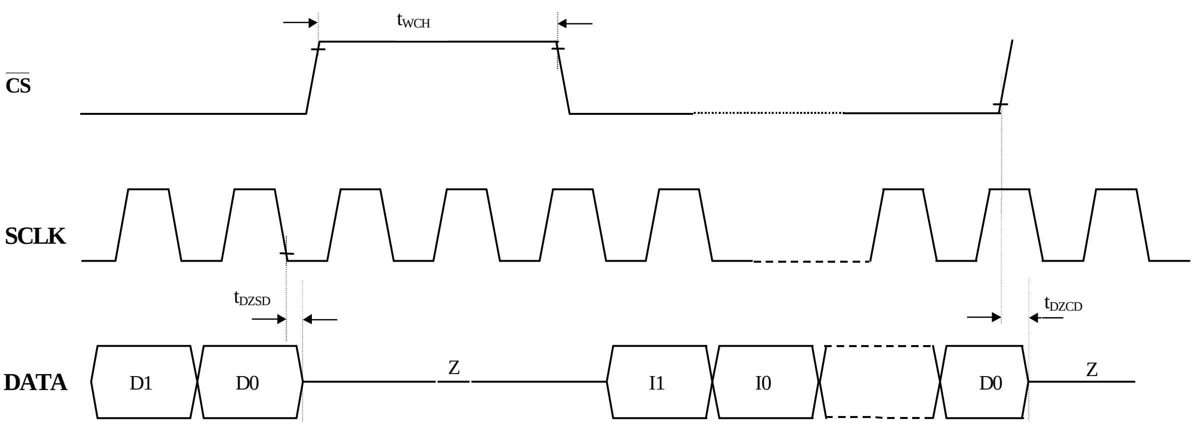
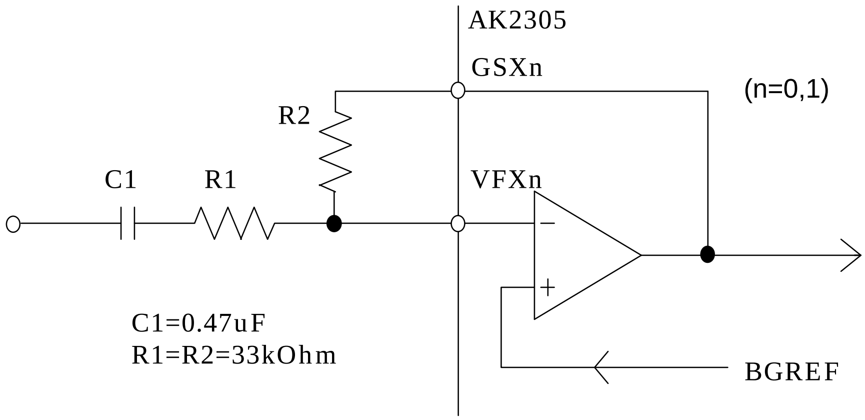


Figure8 : Serial Interface Timing < READ >

APPLICATION CIRCUIT EXAMPLE

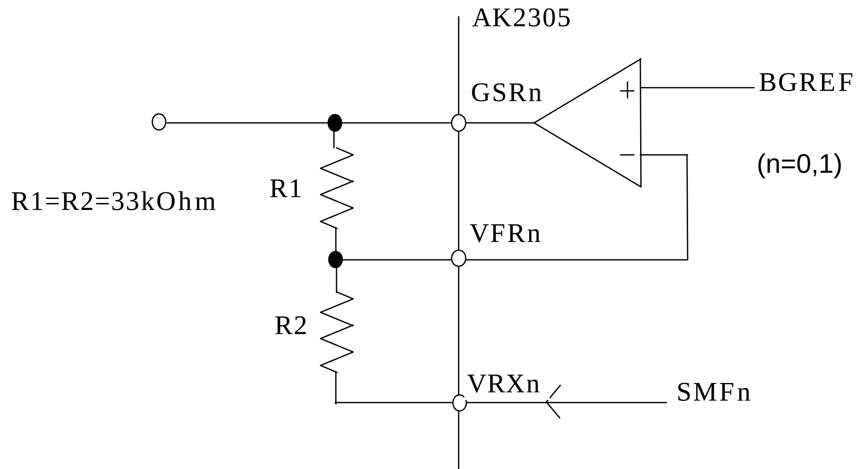
Analog input circuit(AMPT0,1)

AK2305 has an op-amp at analog input of each channel. Each op-amp can be used as a gain adjustment. Op-amp can be used as an inverting amplifier. Feedback resistor must be 10kΩ or larger.



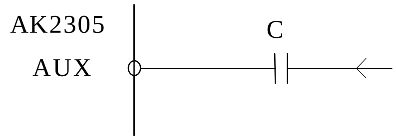
Analog output circuit(AMPR0,1)

AK2305 has an op-amp at analog input of each channel. Each op-amp can be used as a gain adjustment. Op-amp can be used as an inverting amplifier. Feedback resistor must be 10kΩ or larger.



AUX INPUT

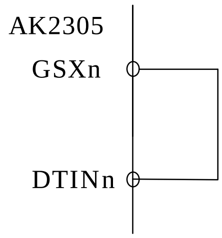
An external tone is input to AUX through an external capacitance of more than 0.1uF.



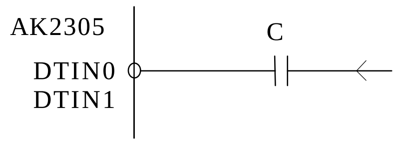
DTIN0, DTIN1 INPUT

There are the following 2 cases in case of that DTMF tone is input through DTIN0,DTIN1.

(1)DTMF tone is output from AMPT0,AMPT1 included AK2305
Connect GSXn with DTINn directly.

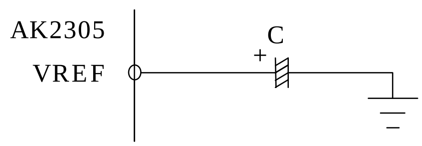


(2) DTMF tone is output from an external amplifier
DTMF tone is input to DTIN0,DTIN1 through an external capacitance of more than 0.1uF.



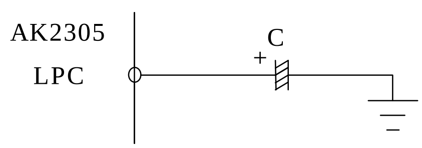
Analog ground stabilization capacitor

An external capacitor of more than 0.1uF should be connected between VREF and AVSS to stabilize analog ground (VREF).



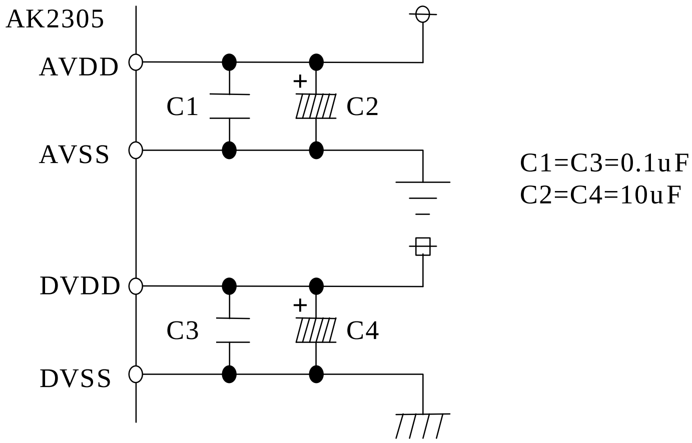
PLL Loop filter capcitor

An external capacitor of more than 0.22uF should be connected between LPC and AVSS.

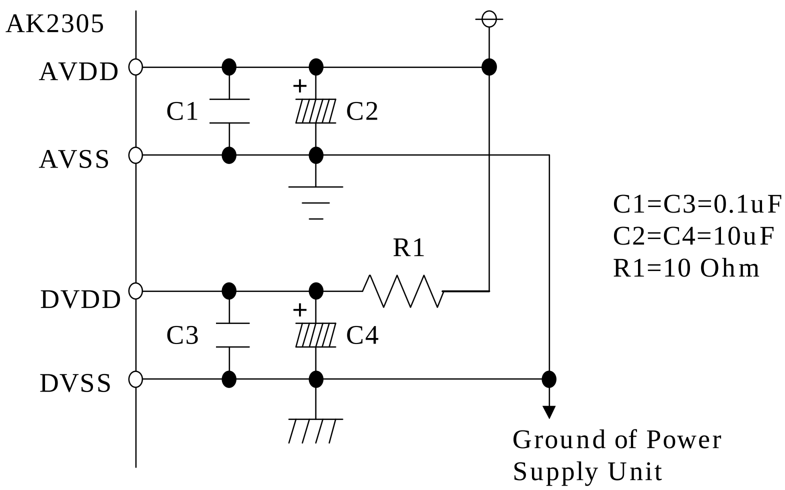


Power Supply

To attenuate the power supply noise, connect capacitors between AVDD and AVSS, and DVDD and DVSS, as shown below.



To use the same supply for both digital and analog power supply (DVDD and AVDD), insert 10Ω resistor between AVDD and DVDD. AVSS and DVSS must be separated on the board, and connected them at power supply unit.

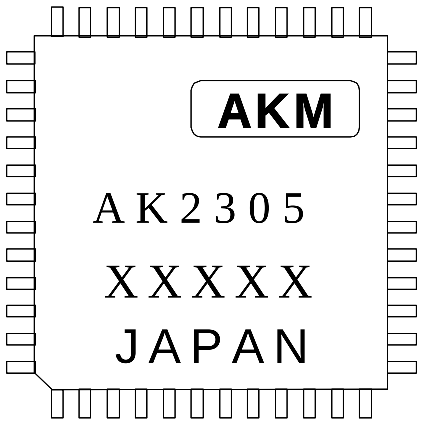


PACKAGING INFOMATION

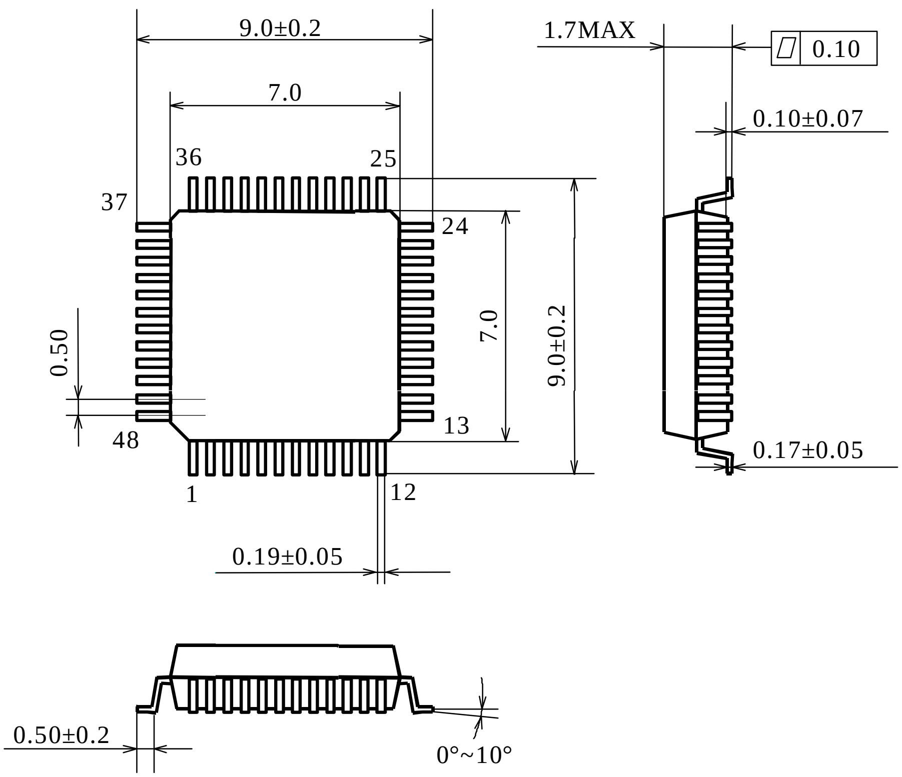
- 48pin LQFP

Marking

(1) Pin#1 indication
(2) Date Code: 5 digit XXXXX
(3) Marketing Code: AK2305
(4) AKM Logo



Outline Dimensions



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  (b) A critical component is one whose failure to function or perform may reasonably be expected to result, whether directly or indirectly, in the loss of the safety or effectiveness of the device or system containing it, and which must therefore meet very high standards of performance and reliability.
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