AN-6047 FIN324C Reset and Standby

Summary

The FIN324C is designed with both a reset and a standby pin. These two pins are similar in function, but allow versatility in the system design. This application note discusses the differences between the two pins, system implementation, and how to debug issues.

Reset vs. Standby

Although very similar, the reset and standby pins function differently. Unlike the standby pin, both the serializer and deserializer have the reset pin. When reset is in LOW state, the device is in a power-down mode. The power-down mode consumes less than 10µA of power. When reset is asserted HIGH, all registers and outputs are reset to initial states. The reset is designed with an input filter, which delays the internal reset by 15µs to ensure that voltage transients do not cause an unwanted reset of the device.

Only the serializer is designed with the standby pin. The deserializer monitors the level of the CTL lines to enter or exit standby. When the serializer's standby pin is in the LOW state, the serializer pulls all four CTL lines to the rail. This CTL voltage level puts the deserializer into standby mode. When the serializer's standby pin is asserted HIGH, the serializer drives all four CTL lines to ground. This LOW state enables the deserializer (see Figure 1). Unlike reset, standby does not reset the register and outputs; they remain in their last-known state.

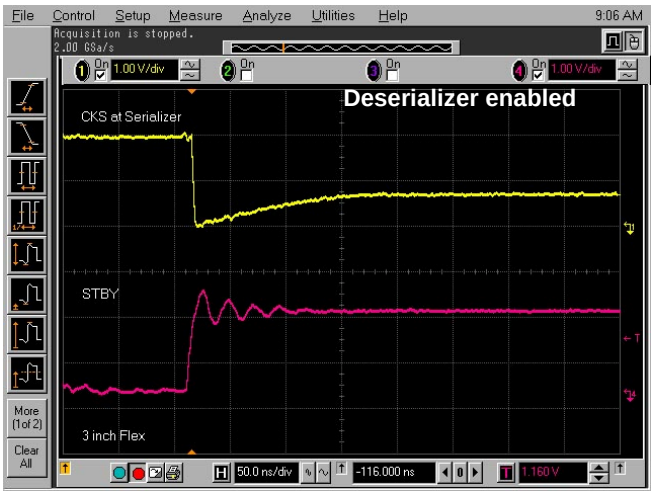

Figure 1 – CTL Enable Pulse

To assert the serializer and deserializer into reset or standby, only one of the pins must be pulled LOW. For example, if reset is LOW on both the serializer and deserializer and standby is HIGH, the devices are reset. To enable the device, both reset and standby must be HIGH. To enable the serializer and deserializer, the deserializer's reset pin must be HIGH and the serializer's reset and standby pins must be HIGH. See Tables 1&2 for serializer and deserializer comparisons.

/RES	/STBY	Serializer M/S=1					Deserializer M/S=1				
		DP (a,c)	CNTL (a,b)	STRBn (a)	Sys Cntr (a,e)	CKS/DS (d)	DP (b,c)	CNTL (b,c)	WCLKn (b,c)	Sys Cntl (a,e)	CKS/DS (a,c,d)
0	x	Inputs Disabled	Inputs Disabled	Inputs Disabled	Inputs Enabled	Output "Standby"	Output "LOW"	Output "LOW"	Output "HIGH"	Inputs Enabled	Input Disabled
1	0	Inputs Disabled	Inputs Disabled	Inputs Disabled	Inputs Enabled	Output "Standby"	Output "Last"	Output "Last"	Output "HIGH"	Inputs Enabled	Input Standby
1	1	I/O Active	Inputs Enabled	Inputs Enabled	Inputs Enabled	Output "Normal"	I/O Active	Output Active	Output "Active"	Inputs Enabled	I/O "Active"

Table 1 - Reset and Standby Table

Function	Current	Deserializer Output Levels	Internal Registers	Serializer Pin	Deserializer Pin	Input Filter
Reset	10µA	DP, CNTL = Low WCLK = High	Resets All Registers	BGA = G2 MLP = 8	BGA = G2 MLP = 9	15µs
Stanby	10µA	Outputs remain at last known state	Registers remain in last known state	BGA = G3 MLP = 11	BGA = NA MLP = NA	No

Table 2 - Reset vs Standby Comparison Table

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System Implementation

The combination of the reset and standby pins offer the system designer versatility.

In a mobile phone with a clam shell form factor, the reset pins can be pulled LOW every time the flip is closed. This allows a full reset of the registers and parallel outputs when the flip is opened. The standby pin can be pulled LOW to save power between writes to the display. This allows the micro serializer / deserializer (µSerDes) to be in a power-down state and keep the last-known states of the registers and parallel outputs. These two pins allow the µSerDes pair and the system to operate efficiently, depending on the systems status. For example, a typical phone call may consist of:

- Opening the flip
- Dialing a number
- Making the call
- Hanging up and closing the flip

During each one of these states, the µSerDes pair can be enabled and disabled to save the maximum amount of power (please see Figure 2).

Per Figure 2, the reset and standby (STBY) status during the phone call would be:

- Flip Closed, Reset = L, STBY = L
- Open Flip, Reset = H, STBY = H
- Dialing Number, Reset = H, STBY = H
- Making Call, Reset = H, STBY = L
- Closing Flip, Reset = L, STBY = L

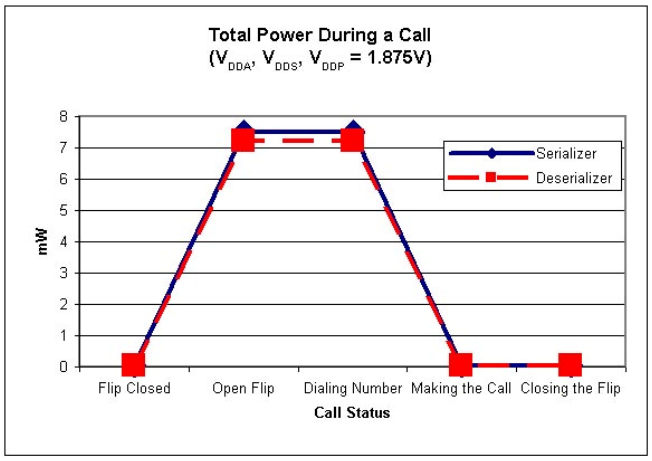

Figure 2 – Power Consumed During a Call

When powering on the µSerDes pair, it is recommended that the standby pin is delayed by 20µs to the reset pin transitioning HIGH (see Figure 3). Although this delay is not required for full functionality, it is recommended to ensure that the deserializer's reset pin is fully HIGH and the device is ready to be enabled by the LOW pulse on the CTL lines. If the deserializer's power is still transitioning when the CTL lines transition LOW, the deserializer does not enable.

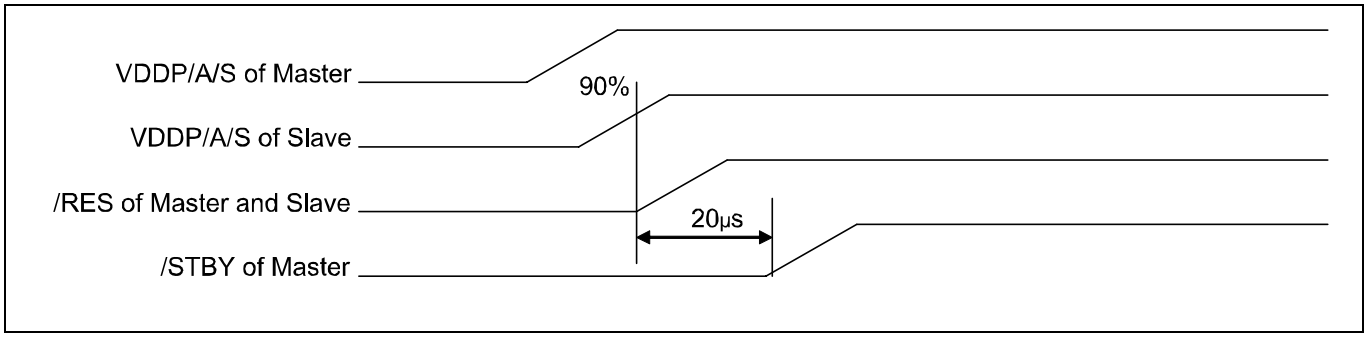

Figure 3 – Power-up Sequencing

Debugging the System

Below are key points if the deserializer is not responding.

Issue: The deserializer is not responding and all outputs including WCLK are LOW.

Solution: The deserializer's reset pin is not HIGH. Transition the deserializer's reset pin to a HIGH state.

Issue: The deserializer is not responding; the WCLK outputs remain HIGH while there is an input on the serializer's STBY.

Solution: The deserializer is not fully enabled.

- Confirm that the reset pin is HIGH on both the serializer and deserializer.
- Probe all four of the CTL lines at the deserializer and confirm that the CTL lines transition LOW when the STBY pin is asserted HIGH. Use a high-impedance probe with a load capacitance below 1pF.
- Probe one of the CTL lines after the LOW enable pulse; the voltage level transitions the voltage offset of 600-800mV. If the voltage offset returns to the rail, the deserializer did not enable. If the CTL voltage offset equals 600-800mV and the WCLK output is not transitioning with an input on STBY, there is a different issue. In this case, the deserializer is enabled; please verify all connections and states of control pins.
- Review the timing between the reset pin of the deserializer transitioning HIGH and the standby pin transitioning HIGH of the serializer. Fairchild recommends a 20µs delay between the two.

Note: While measuring any CTL line please use high-impedance probes (<1pF). Lower impedance probes roll the edges and induce skew onto the CTL.

Resources

For questions not addressed here, visit Fairchild's website at http://www.fairchildsemi.com/products/interface/userdes.html or contact Fairchild via email interface@fairchildsemi.com.

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