AKM

AKD4394
Evaluation board Rev.C for AK4394

General Description

The AKD4394 is an evaluation board for AK4394, which is 192kHz sampling 24Bit $\Delta\Sigma$ DAC. The AKD4394 includes a LPF which can add differential analog outputs from the AK4394 and also has a digital interface with AKM's wave generator using ROM data and AKM's ADC evaluation boards. Therefore, it is easy to evaluate the AK4394.

■ **Ordering Guide**

   AKD4394 Rev.C   --- Evaluation board Rev.C for AK4394: differential output

Function

■ On-board differential output buffer circuit

■ On-board clock generator

■ BNC connector for an external clock input

■ Compatible with 3types of interface

1. Direct interface with evaluation boards for AKM's A/D converter (AKD539X, AKD535X)
2. Interface with a signal generator (AKD43XX)
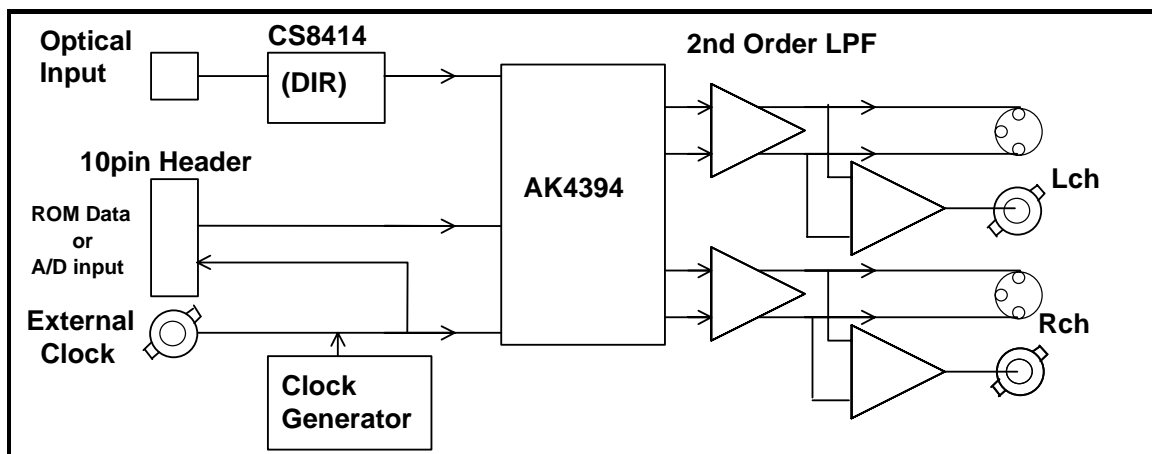3. On-board CS8414 as DIR which accepts optical input.

Fig.1 Block diagram

* Circuit diagram and PCB layout are attached at the end of this manual.

(AKD4394 Rev.C is same as AKD4393 Rev.C.)

■ External Analog Circuit (Rev.C)

The differential output circuit and LPF is implemented on board. The differential outputs of AK4394 is buffered by non-inverted circuit and output via Cannon connector(differential output). LPF adds differential outputs. NJM5534D is used for op-amp on this board that has low noise and high voltage torelance characteristics. Analog signal is output via Cannon and BNC connectors on the board. The output level is about 2.94Vrms(typ@VREF=5.0V) by Cannon and 2Vrms(typ@VREF=5.0V) by BNC.
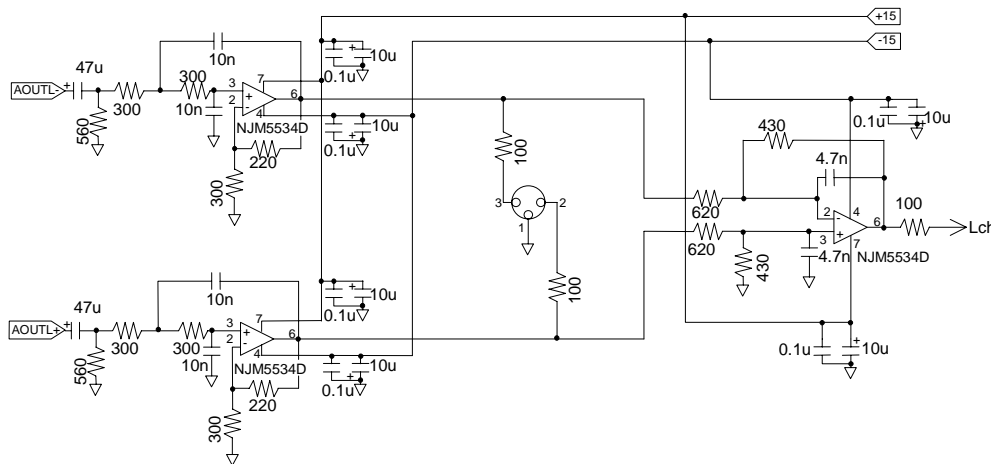

Fig.2   External Analog Filter

■ Operation sequence

1. Set up the jumpers for power supply.

    [JP15(REG)] selects power supply for AVDD pin of AK4394.

        short: 5V is supplied from regulator. (default)

                    Nothing should be connected to A5V jack.

        open: 5V is supplied from A5V.

2. Set up the power supply lines.

        +15V=15V, -15V=-15V: Power supply for op-amp. AVDD of AK4394 is supplied from "+15V" through regulator (JP15: short).

        A5V=5V: This jack is used when AVDD of AK4394 is supplied from this. In this case, JP15 should be open.

        DVDD=5V: Power supply for logic circuit on this board.

        VP=3V~5.25V: Digital (set JP10 to VP),

        AGND=DGND=0V .

        Each supply line should be distributed from the power unit.

3. Set up the evaluation modes by jumper pins and DIP switches.(See next item.)

4. Power on.(The AK4394 should be reset once by bringing PD "L" upon power-up.)

    *SW1 resets the AK4394 during operation.

     The AK4394 is reset at SW1="L" and exits resetting at SW1="H".

■ The evaluation modes and corresponding jumper pins setting

1. Evaluation Modes

●Applicable Evaluation Mode

        (1) DIR(Optical Link)

        (2) Ideal sine wave generated by ROM data

        (3) Using AD converted data

        (4)All interface signals including master clock are fed externally.

(1) DIR(Optical Link) (default)

    PORT2 is used for the evaluation using such as CD test disk. The DIR generates MCLK, BICK and LRCK SDATAfrom the received data through optical connector(PORT2: TORX176).
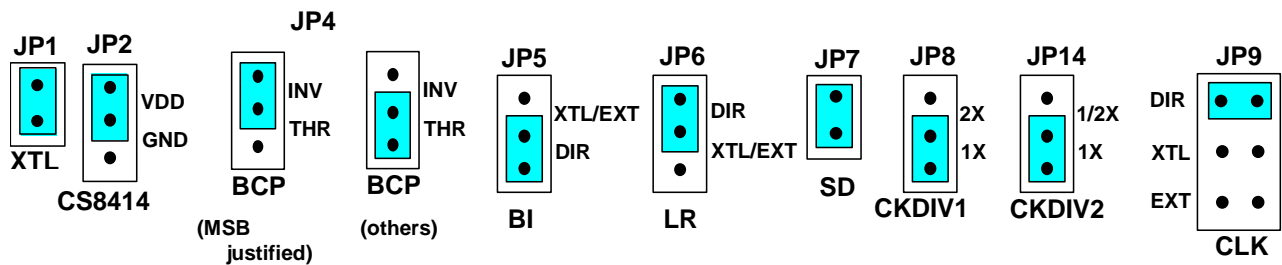
Fig.3   Jumper set-up (DIR)

(2) Ideal sine wave generated by ROM data

    Digital signal generated by AKD43XX are used. PORT1 is used for the interface with AKD43XX. Master clock is sent from AKD4394 to AKD43XX then LRCK, BICK and SDATA are sent from AKD43XX to AKD4394.
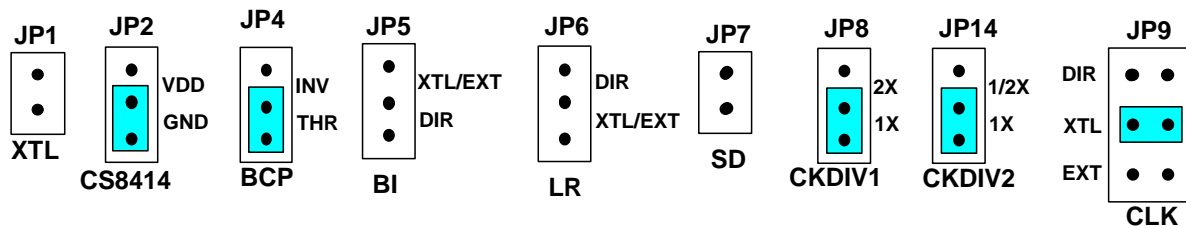

Fig.4   Jumper set-up (ROM data)

(3) Using AD converted data

AD converted data from AKM's AD evaluation boards(AKD539X, AKD535X) is used through PORT1.

* In case of using external clock through a BNC connector, select EXT of JP9 and short JP1.

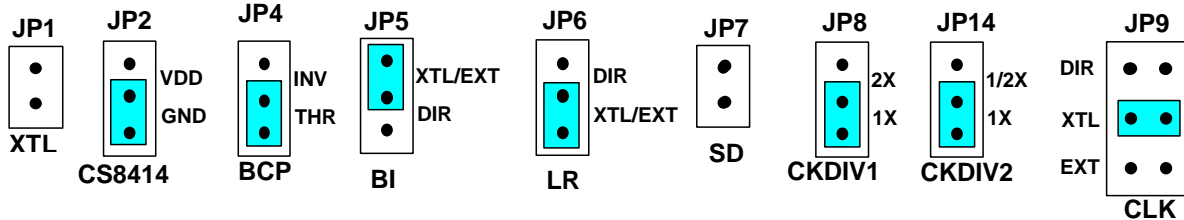* In case of using the double speed sampling mode, select 1/2X of JP8 and set S2-2(DFS) on.

Fig.5   Jumper set-up (A/D)

(4) All interface signals including master clock are fed externally.

Under the following set-up, MCLK, LRCK and SCLK signals needed for the D/A to operate could be fed through PORT1.
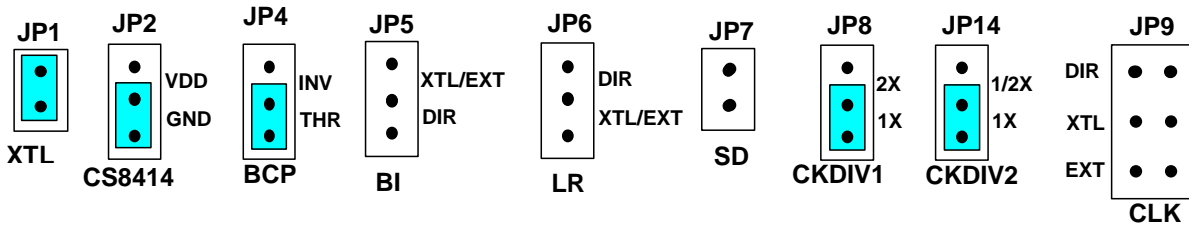
Fig.6   Jumper set-up (ext.)

2.   MCLK set-up

When the LRCK is fed from the 74HC4040 on the board, The ratio of MCLK to LRCK can be selected by JP8 and JP14.

JP14	JP8	X'tal	MCLK	fs	MCLK/LRCK
1X	1X	12.288MHz	12.288MHz	48kHz	256
1X	2X	24.576MHz	24.576MHz	48kHz	512
1/2X	1X	24.576MHz	12.288MHz	96kHz	128
1/2X	2X	49.152MHz	12.288MHz	96kHz	128

Table.1   set-up example

3.   BICK set-up

When BICK is supplied from U1(74HC4040), either 32fs or 64fs could be selected. Fig.8 shows 64fs mode. 64fs mode is recommended.

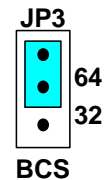*Only mode 0(LSB justified 16bit mode) can correspond to 32fs.

Fig.7   Jumper Set-up (BCS)

4. DIP switch set-up

Confirm the set-up of the DIP switch before the operation. "ON" means "H" and "OFF" means "L".

4-1.   Set-up of SW3, SW4(Mode set-up of AK4394: see the data sheet of AK4394)

DIF2	DIF1	DIF0	Mode	BICK	
OFF	OFF	OFF	0: LSB justified, 16bit	≥32fs	
OFF	OFF	ON	1: LSB justified, 20bit	≥40fs	
OFF	ON	OFF	2: LSB justified, 24bit	≥48fs	
OFF	ON	ON	3: I^{2}S	≥48fs	(default)
ON	OFF	OFF	4: MSB justified, 24bit	≥48fs	

Table 2   Audio Serial Interface Format Select Pins (SW3-5,6,7)

4-2. Set-up of SW6 (Mode set-up of CS8414. About details, see the data-sheet of CS8414)

 Adjust the audio data format of CS8414 (DIR) to AK4394. CS8414 does not match the LSB justified 20bit/24bit mode of AK4394.

M3 (SW6-2)	M2 (SW6-3)	M1 (SW6-4)	M0 (SW6-5)	Data format	JP4	
OFF	OFF	OFF	OFF	MSB justified, 24bit	INV	
OFF	OFF	ON	OFF	I^{2}S	THR	(default)
OFF	ON	OFF	ON	LSB justified, 16bit	THR	

Table 3 Set-up of SW6

SW6-1(SEL) :Usually ON.

SW6-6(CS12): Select the channel for indicating the channel status.

ON: Rch (default), OFF: Lch

5.   Parallel/Serial Control

SW5: set up P/S pin of AK4394.

H: parallel mode. PORT3 is used JP11, 12 and 13 should be open.

L: serial mode. PORT3 is used. JP11, 12 and 13 should be open.

6.   Other set-up

SW1: Reset of AK4394. Select "H" during operation.

SW2: Soft-mute of AK4394. The soft-mute is executed during SW2 pushed.

LE1 : This LED shows pre-emphasis status. It turns on when the data is pre-emphasized.

LE2 : This LED shows the output of VERF pin in CS8414. It turns on when the error is occured in CS8414.

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Control Software Manual
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■ Set-up of evaluation board and control software

1. Set up the AKD4394 according to previous term.

2. Connect IBM-AT compatible PC with AKD4394 by 10-line type flat cable (packed with AKD4394). Take care of the direction of 10pin header. (Please install the driver in the CD-ROM when this control software is used on Windows 2000/XP. Please refer "Installation Manual of Control Software Driver by AKM device control software". In case of Windows95/98/ME, this installation is not needed. This control software does not operate on Windows NT.)

3. Insert the CD-ROM labeled "AKD4394 Evaluation Kit" into the CD-ROM drive.

4. Access the CD-ROM drive and double-click the icon of "akd4394.exe" to set up the control program.

5. Then please evaluate according to the follows.

■ Operation flow

Keep the following flow.

1. Set up the control program according to explanation above.
2. Click "Port Reset" button.

■ Explanation of each buttons

1. [Port Reset]:   Set up the USB interface board (AKDUSBIF-A).
2. [Write default]:   Initialize the register of AK4394.
3. [All Write]:   Write all registers that is currently displayed.
4. [Function1]:   Dialog to write data by keyboard operation.
5. [Function3]:   The sequence of register setting can be set and executed.
6. [Function4]:   The sequence that is created on [Function3] can be assigned to buttons and executed.
7. [Function5]:   The register setting that is created by [SAVE] function on main window can be assigned to buttons and executed.
8. [SAVE]:   Save the current register setting.
9. [OPEN]:   Write the saved values to all register.
10. [Write]:   Dialog to write data by mouse operation.

■ Indication of data

Input data is indicated on the register map. Red letter indicates "H" or "1" and blue one indicates "L" or "0". Blank is the part that is not defined in the datasheet.

■ **Explanation of each dialog**

1. [Write Dialog]: Dialog to write data by mouse operation

There are dialogs corresponding to each register.

Click the [Write] button corresponding to each register to set up the dialog. If you check the check box, data becomes "H" or "1". If   not, "L" or "0".

When writing the input data to AK4394, click [OK] button. If not, click [Cancel] button.

2. [Function1 Dialog]: Dialog to write data by keyboard operation

Address Box:	Input registers address in 2 figures of hexadecimal.
Data Box:	Input registers data in 2 figures of hexadecimal.

When writing the input data to AK4394, click [OK] button. If not, click [Cancel] button.

3. [Save] and [Open]

3-1. [Save]

Save the current register setting data. The extension of file name is "akr".

(Operation flow)
Click [Save] Button.
Set the file name and push [Save] Button. The extension of file name is "akr".

3-2. [Open]

The register setting data saved by [Save] is written to AK4394. The file type is the same as [Save].

(Operation flow)
(1)   Click [Open] Button.
(2)   Select the file (*.akr) and Click [Open] Button.

4. [Function3 Dialog]

The sequence of register setting can be set and executed.

(1) Click [F3] Button.

(2) Set the control sequence.
   Set the address, Data and Interval time. Set "-1" to the address of the step where the sequence should be paused.

(3) Click [Start] button. Then this sequence is executed.
   The sequence is paused at the step of Interval="-1". Click [START] button, the sequence restarts from
   the paused step.

This sequence can be saved and opened by [Save] and [Open] button on the [Function3] window. The extension of file
name is "aks".
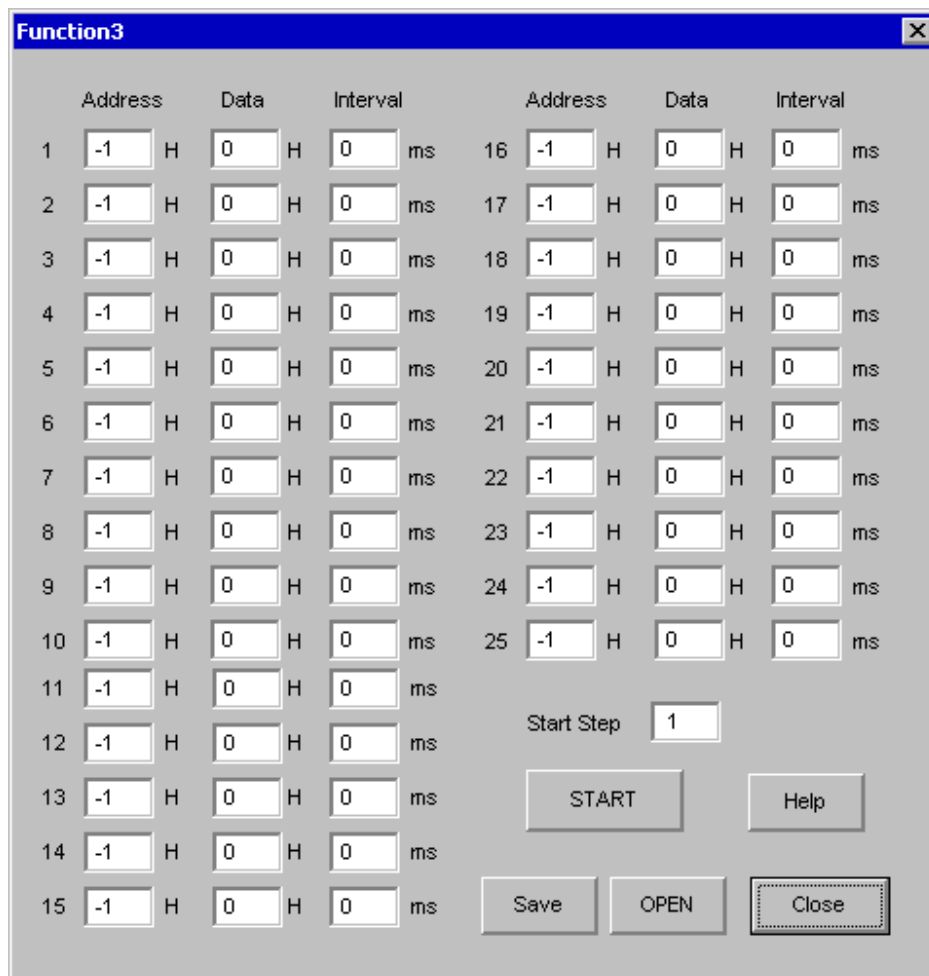
Figure 1. Window of [F3]

5. [Function4 Dialog]

The sequence that is created on [Function3] can be assigned to buttons and executed. When [F4] button is clicked, the window as shown in **Figure 2** opens.
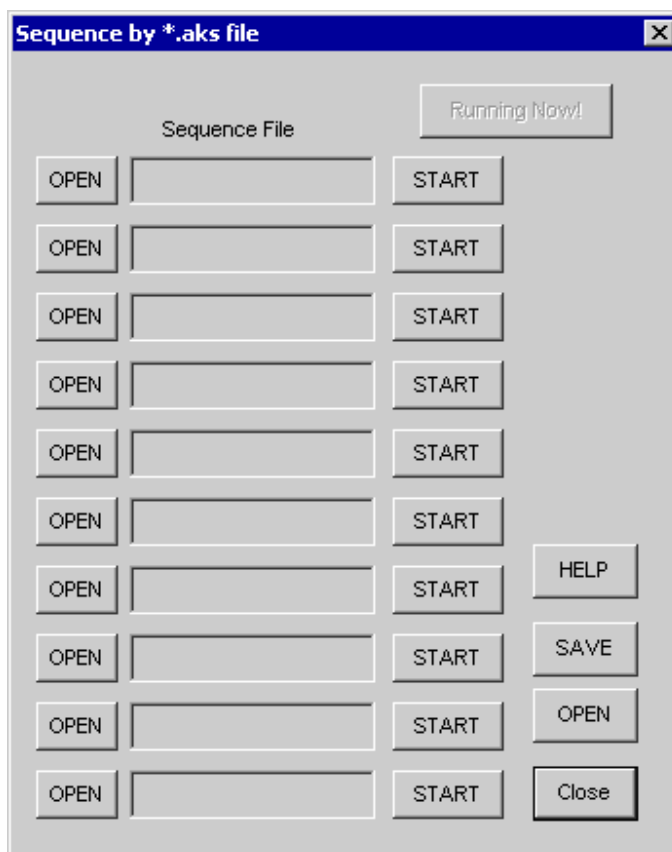
Figure 2. [F4] window

5-1. [OPEN] buttons on left side and [START] buttons

(1) Click [OPEN] button and select the sequence file (*.aks).

The sequence file name is displayed as shown in Figure 3.
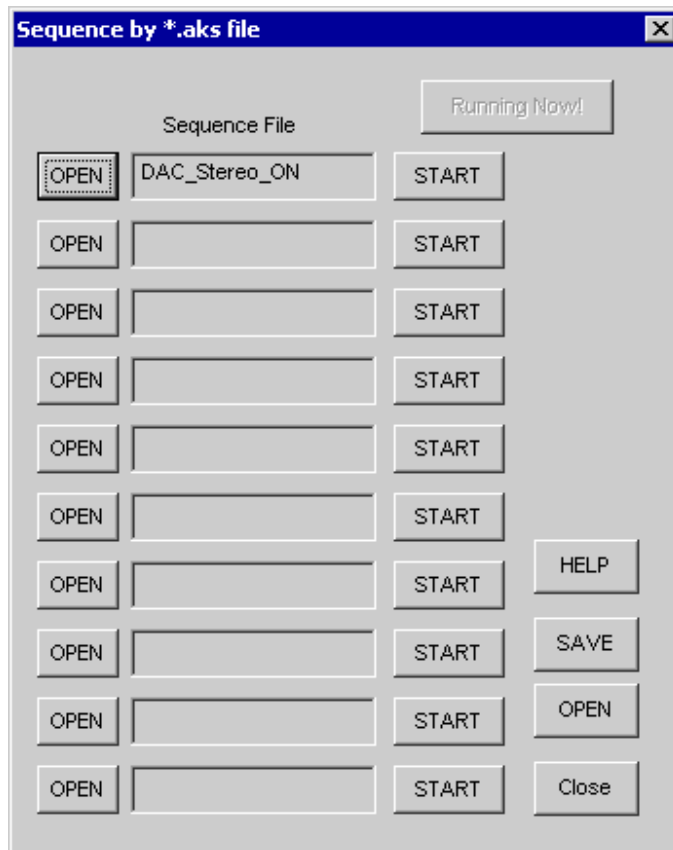
Figure 3. [F4] window(2)

(2) Click [START] button, then the sequence is executed.

5-2. [SAVE] and [OPEN] buttons on right side

[SAVE]: The sequence file names can assign be saved. The file name is *.ak4.

[OPEN]: The sequence file names assign that are saved in *.ak4 are loaded.

5-3. Note

(1) [Function4] doesn't support the pause function of sequence function.

(2) All files need to be in same folder used by [SAVE] and [OPEN] function on right side.

(3) When the sequence is changed in [Function3], the file should be loaded again in order to reflect the change.

6. [Function5 Dialog]

The register setting that is created by [SAVE] function on main window can be assigned to buttons and executed.
When [F5] button is clicked, the following window as shown in **Figure 4** opens.
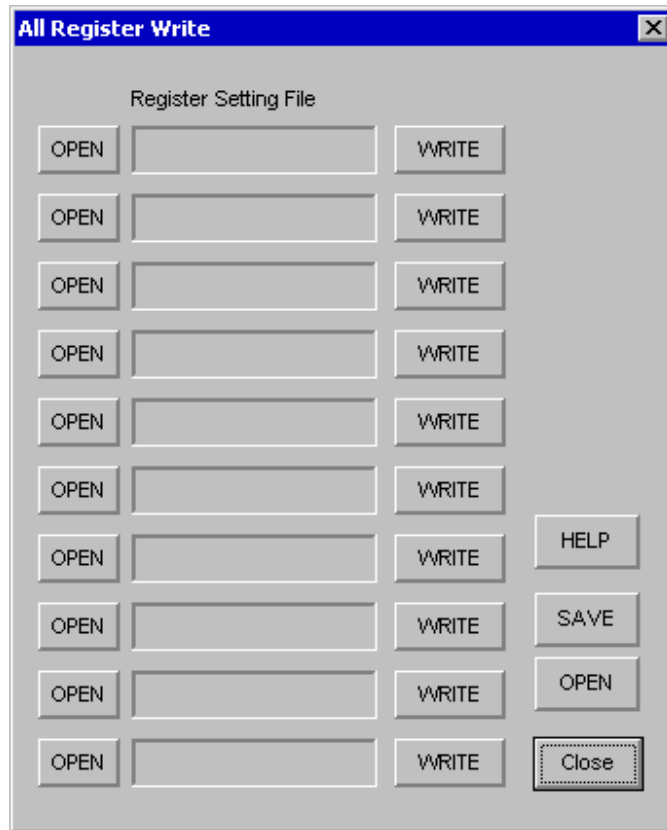
Figure 4. [F5] window

6-1. [OPEN] buttons on left side and [WRITE] button

(1) Click [OPEN] button and select the register setting file (*.akr).

(2) Click [WRITE] button, then the register setting is executed.

6-2. [SAVE] and [OPEN] buttons on right side

[SAVE]: The register setting file names assign can be saved. The file name is *.ak5.

[OPEN]: The register setting file names assign that are saved in *.ak5 are loaded.

6-3. Note

(1) All files need to be in same folder used by [SAVE] and [OPEN] function on right side.

(2) When the register setting is changed by [Save] Button in main window, the file should be loaded again in order to reflect the change.

■ AK4394 Measurement Example

Conditions:

AVDD =DVDD= 5.0V

Interface = DIR (44.1kHz, 96kHz)

MCLK = 256fs(fs=44.1kHz, 96kHz)

BICK = 64fs

fs = 44.1kHz, 96kHz,

Input data = 24bit

Measurement unit: Audio Precision System Two Cascade (fs=44.1kHz, 96kHz)

(AKD4394 Rev.C: differential output)

fs		Result	
44.1kHz	THD+N	100.3	20kLPF
	DR	120.1	22kLPF + A-weighted
	S/N	120.2	22kLPF + A-weighted
96kHz	THD+N	99.6	40kLPF
	DR	119.2	80kLPF + A-weighted
	S/N	119.8	80kLPF + A-weighted

Plot:

FFT Point: 16384

Window: Equiripple

Averages: 4

(fs=44.1kHz)

AK4394 FFT(Input Level=0dBFS,fin=1kHz)
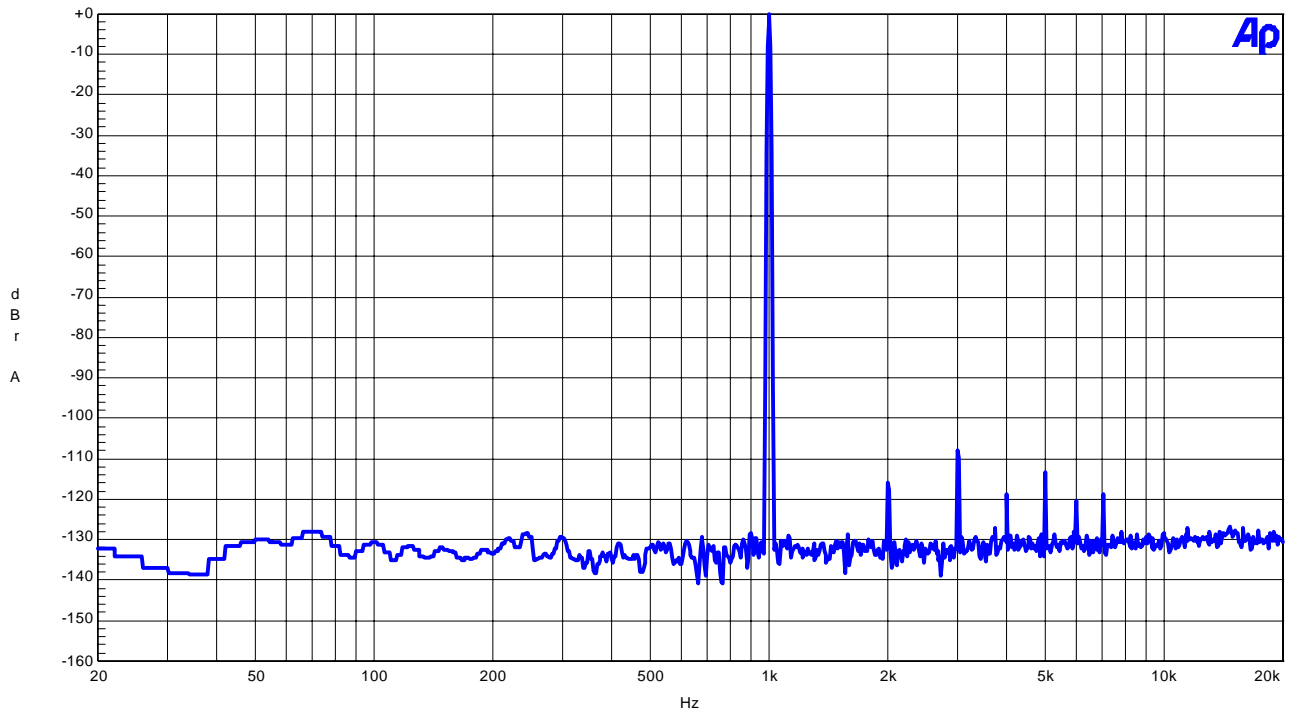
FFT (Input Level=0dBFS, fin=1kHz)
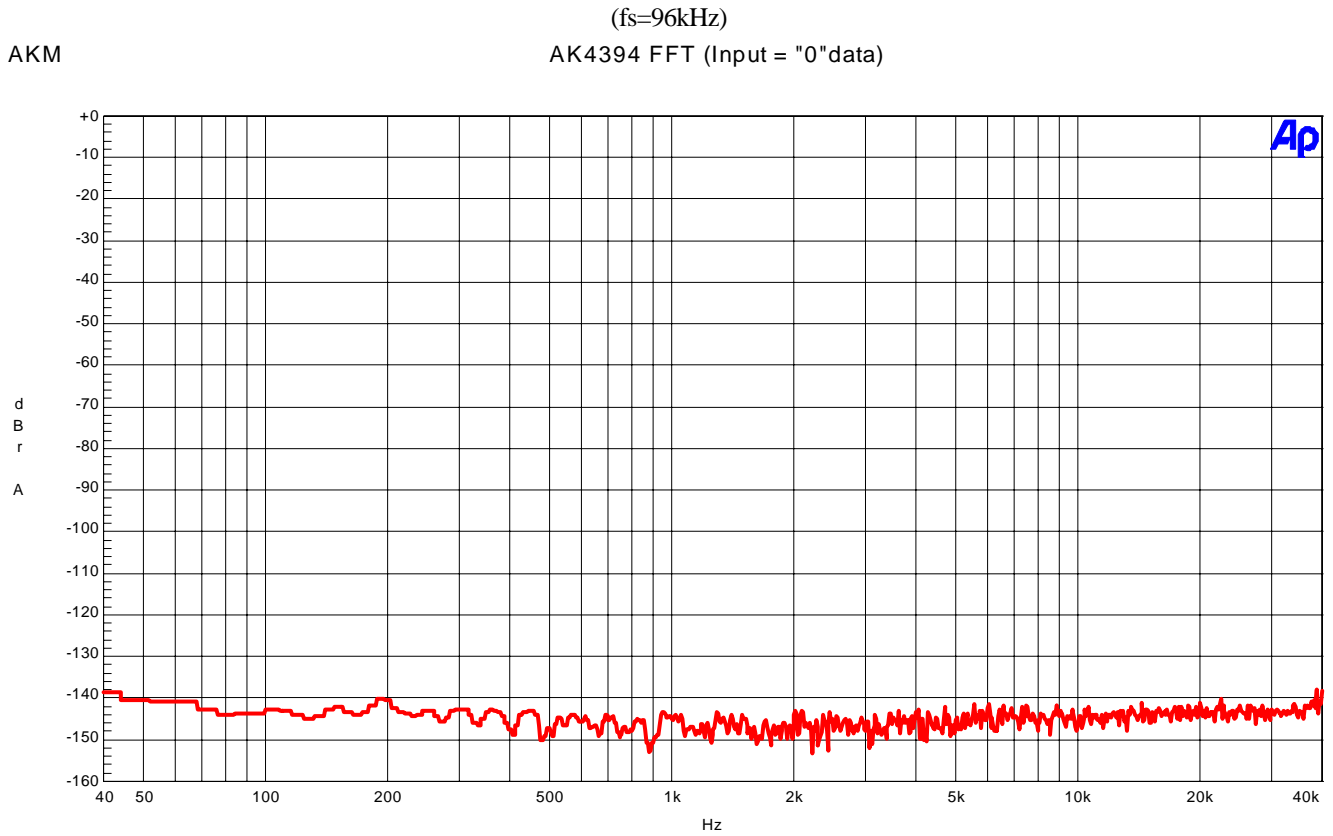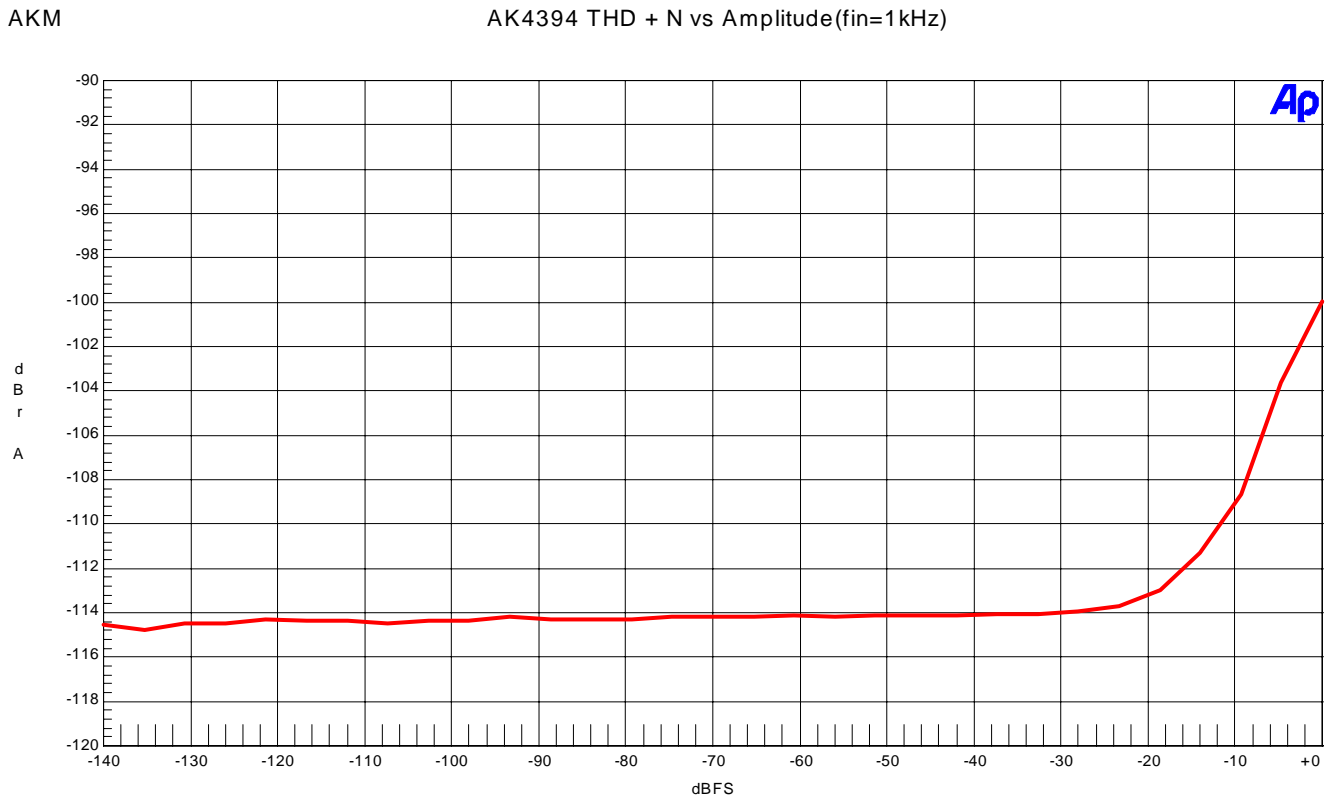
AKM   AK4394 FFT(Input Level=-60dBFS,fin=1kHz)
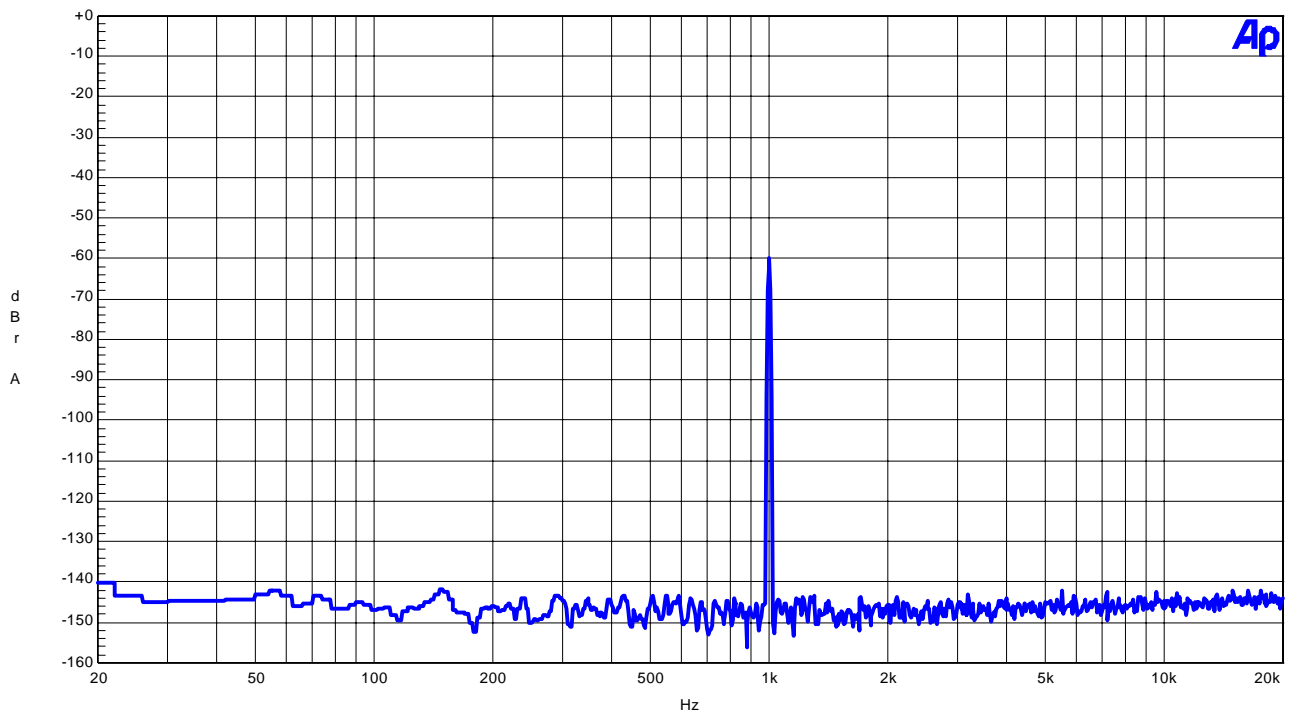
FFT (Input Level=-60dBFS, fin=1kHz)


(fs=44.1kHz)

AKM   AK4394 FFT(Input="0"data)
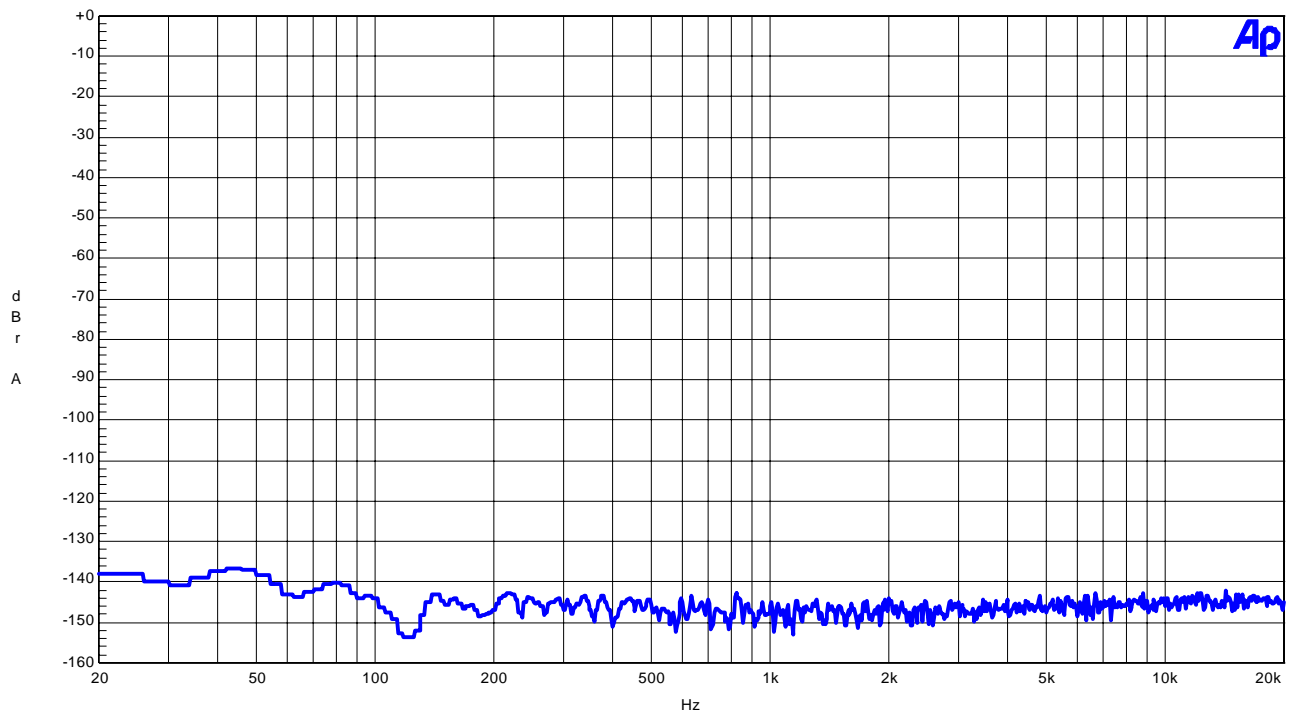
FFT (noise floor)

AKM   AK4394 FFT(Input = "0"data, out-of band)
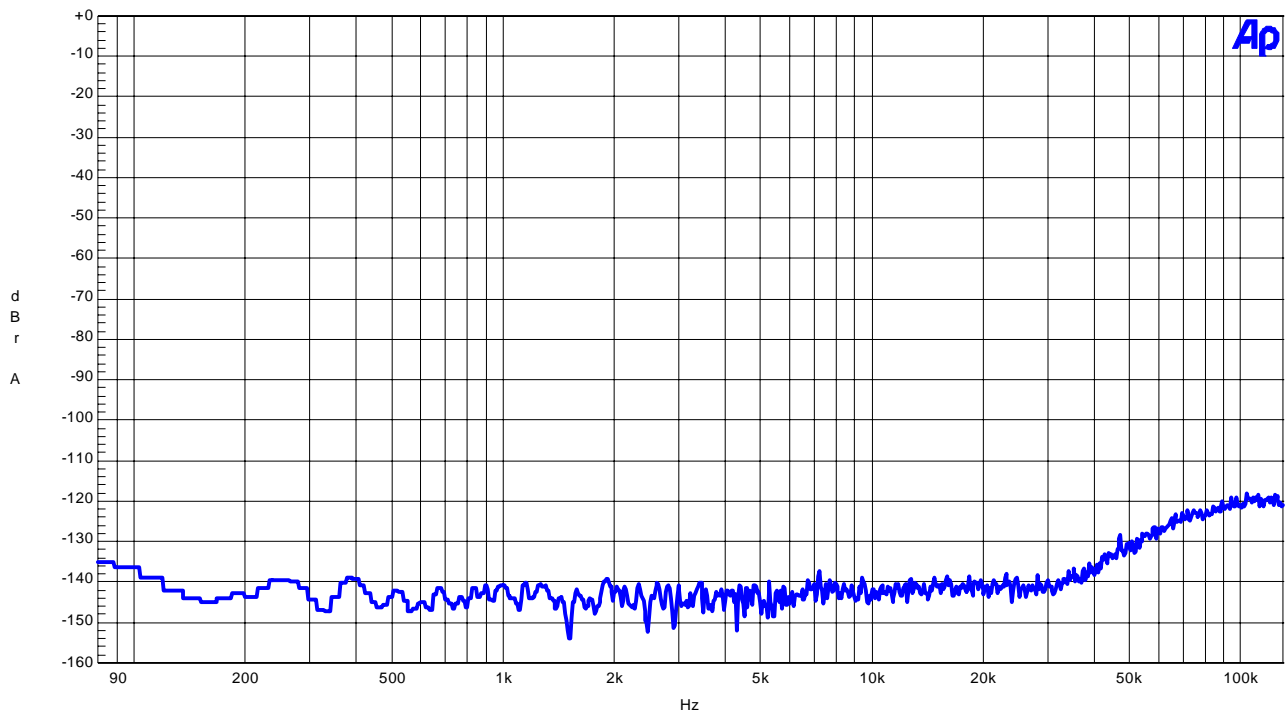
FFT (noise floor, out-of band)

(fs=44.1kHz)

AKM   AK4394 THD + N vs Amplitude(fin=1kHz)
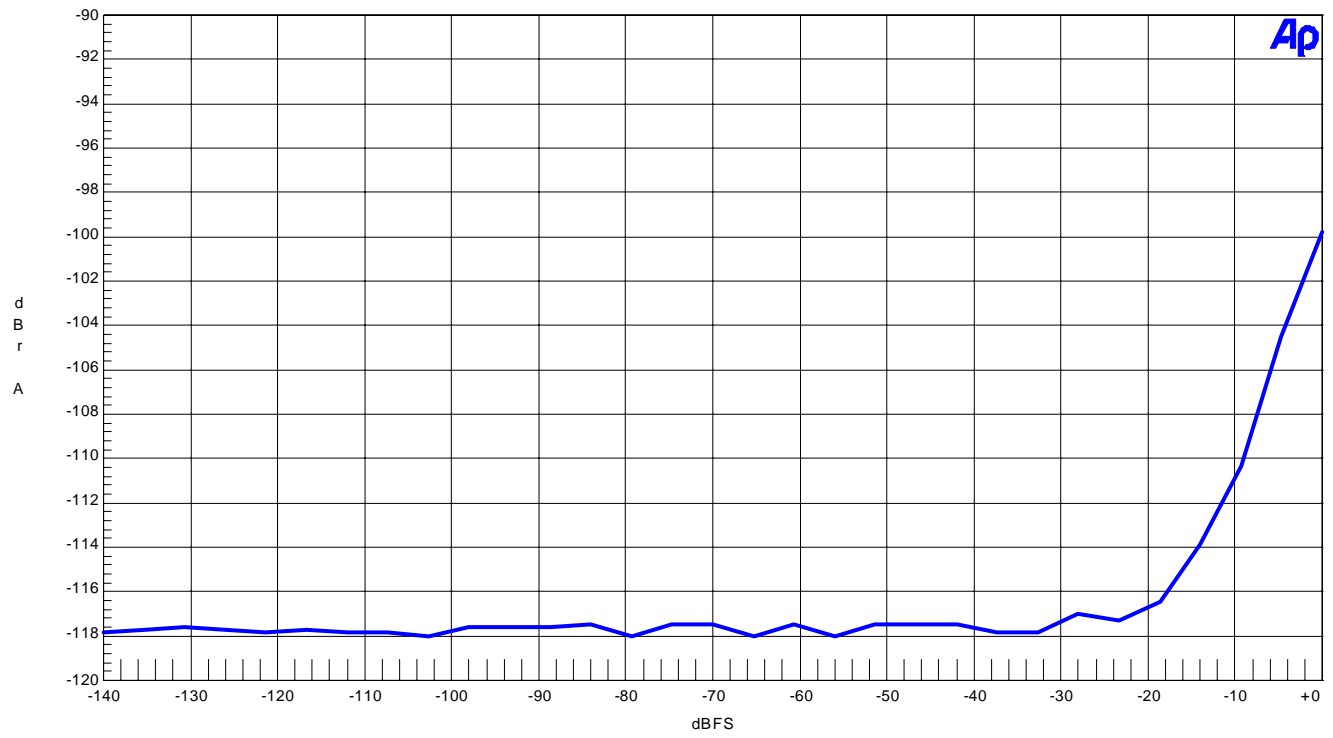
THD + N vs Amplitude (fin=1kHz)

AKM   AK4394 THD + N vs Input Frequency(Input Level=0dBFS)
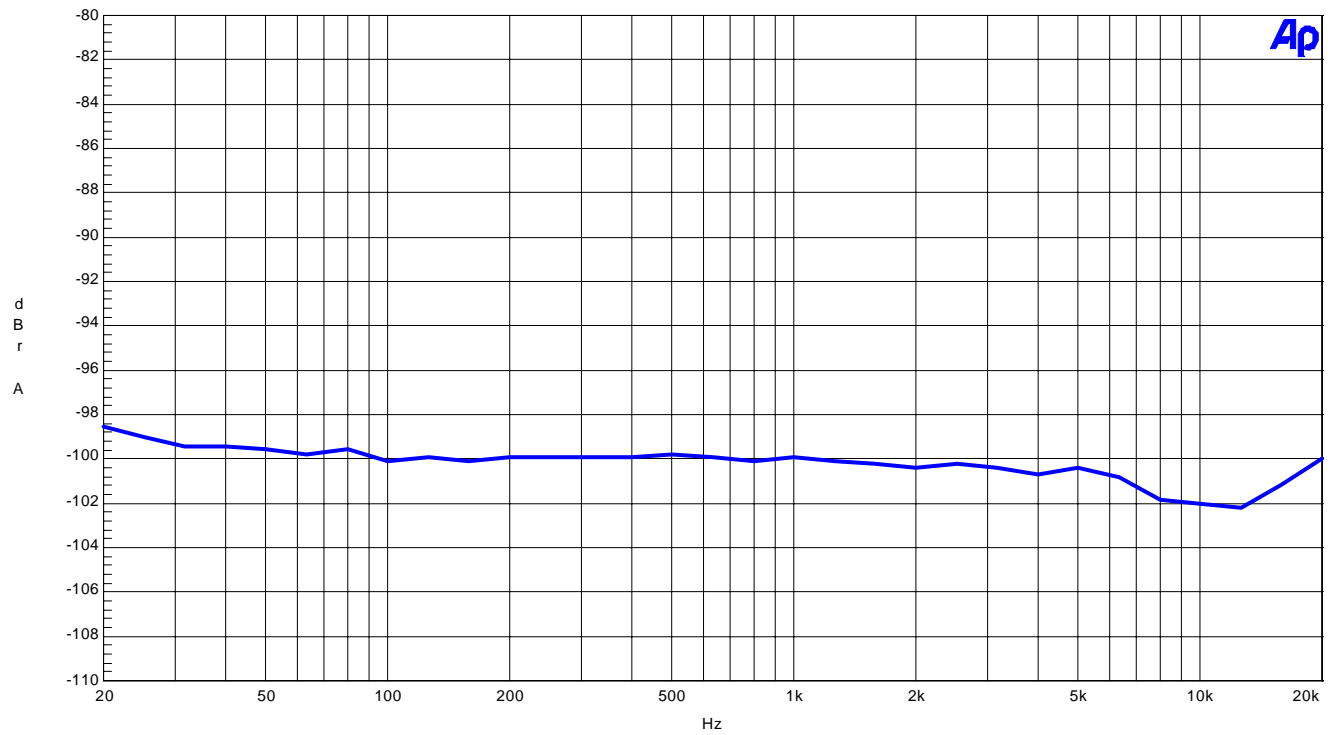
THD +N vs Input Frequency (Input Level=0dBFS)

(fs=44.1kHz)

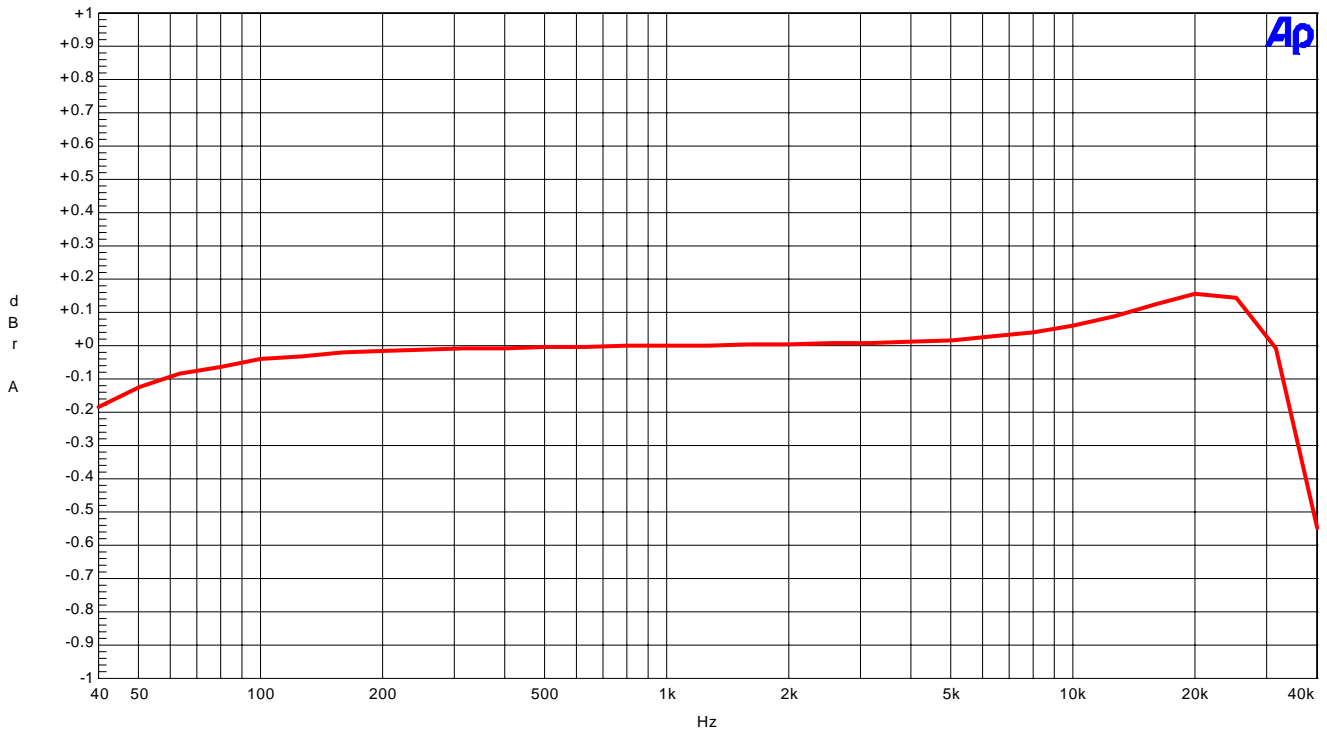AKM   AK4394 Linearity
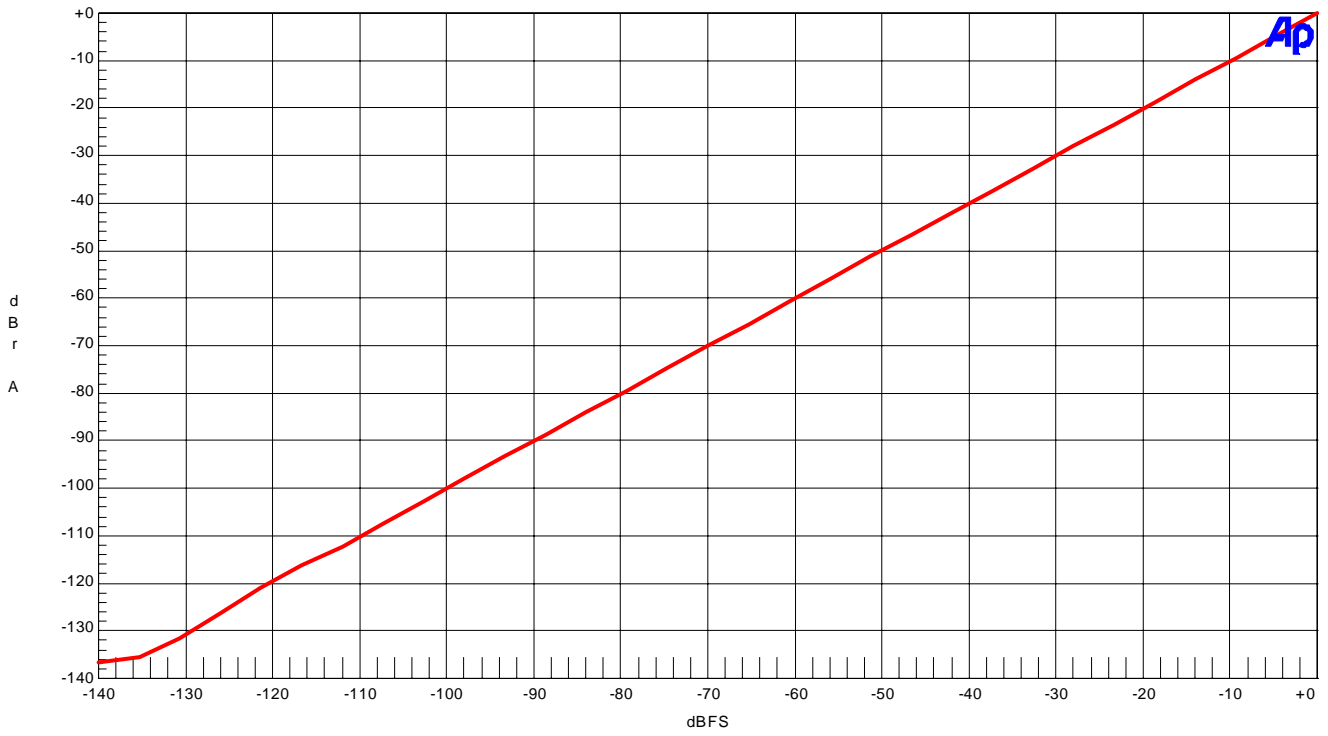
Linearity (fin=1kHz)

AKM   AK4394 Frequency Response
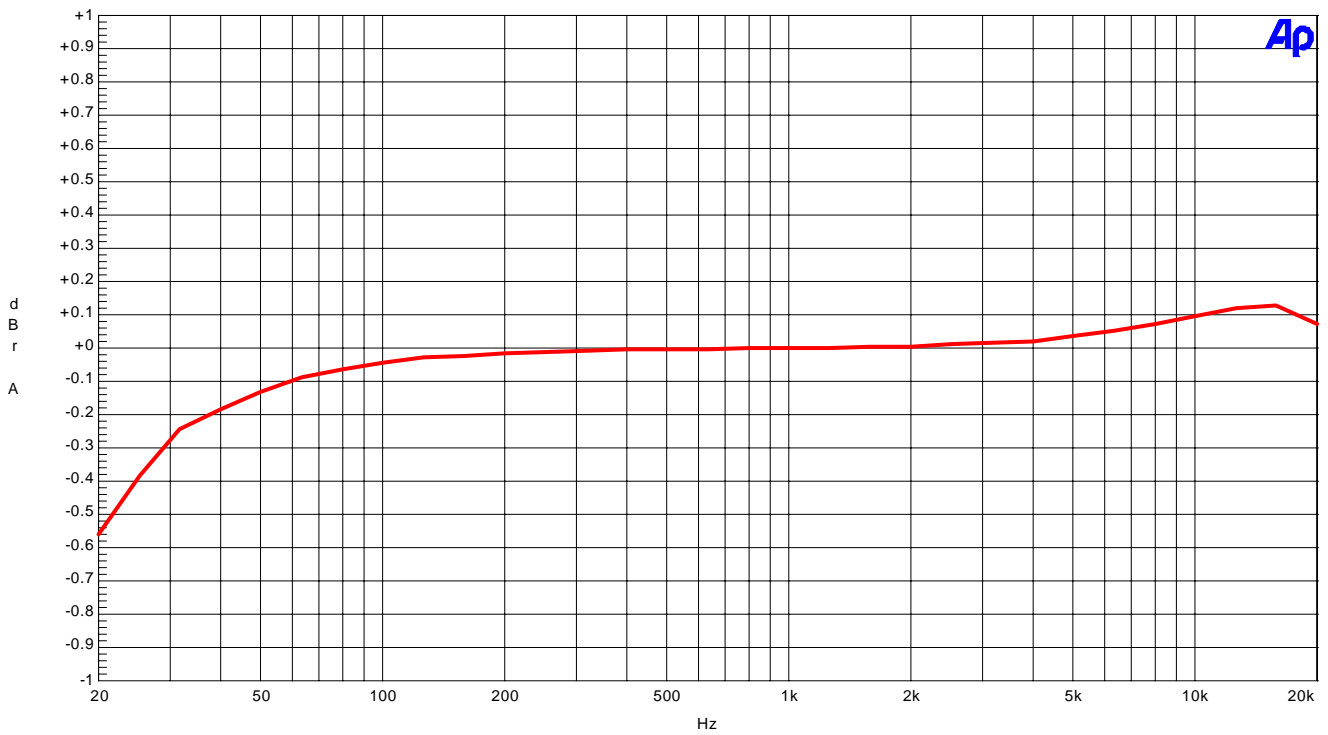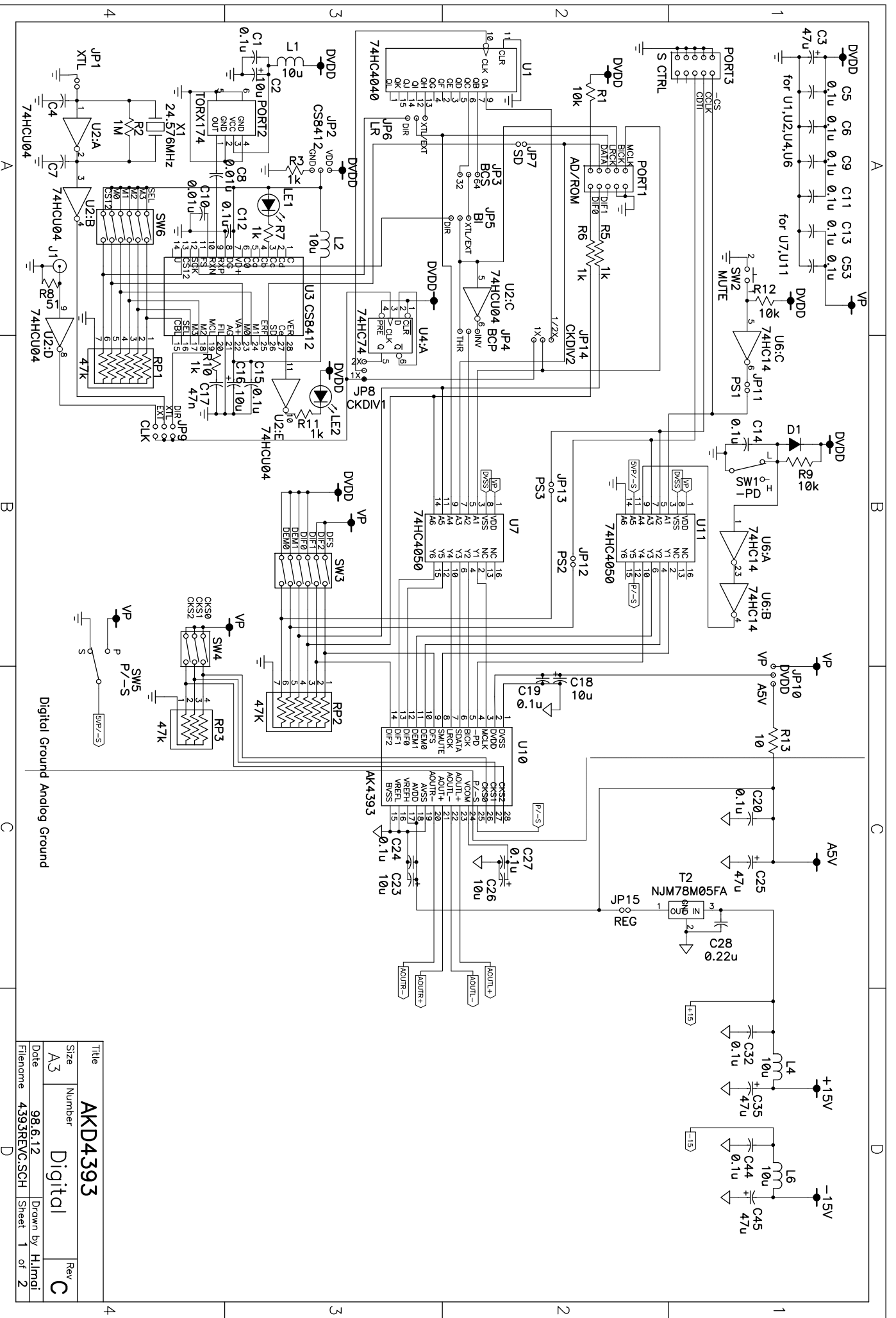

Frequency Response (Input Level=0dBFS)

(fs=44.1kHz)

AKM   AK4394 Crosstalk
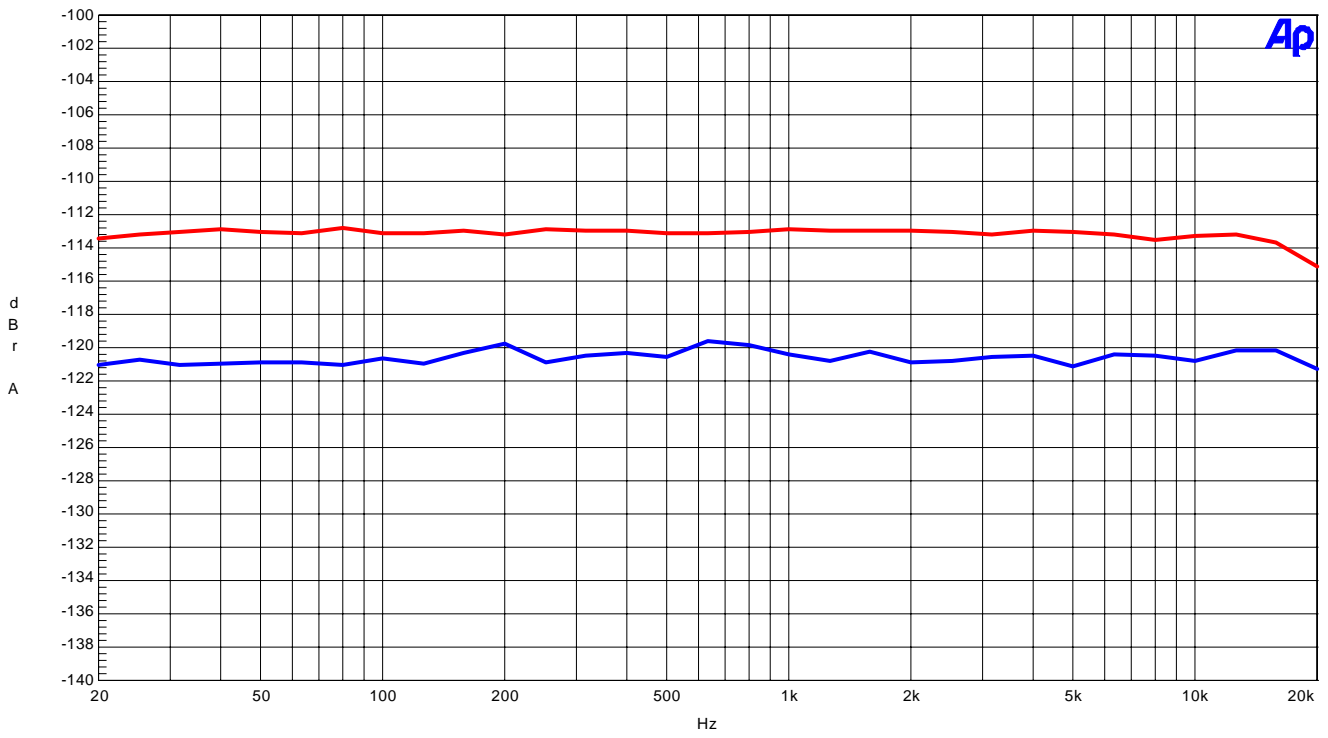
Crosstalk (upper = Rch, Lower = Lch)

(fs=96kHz)

AKM   AK4394 FFT (Input Leve=0dBFS, fin=1kHz, Notch)
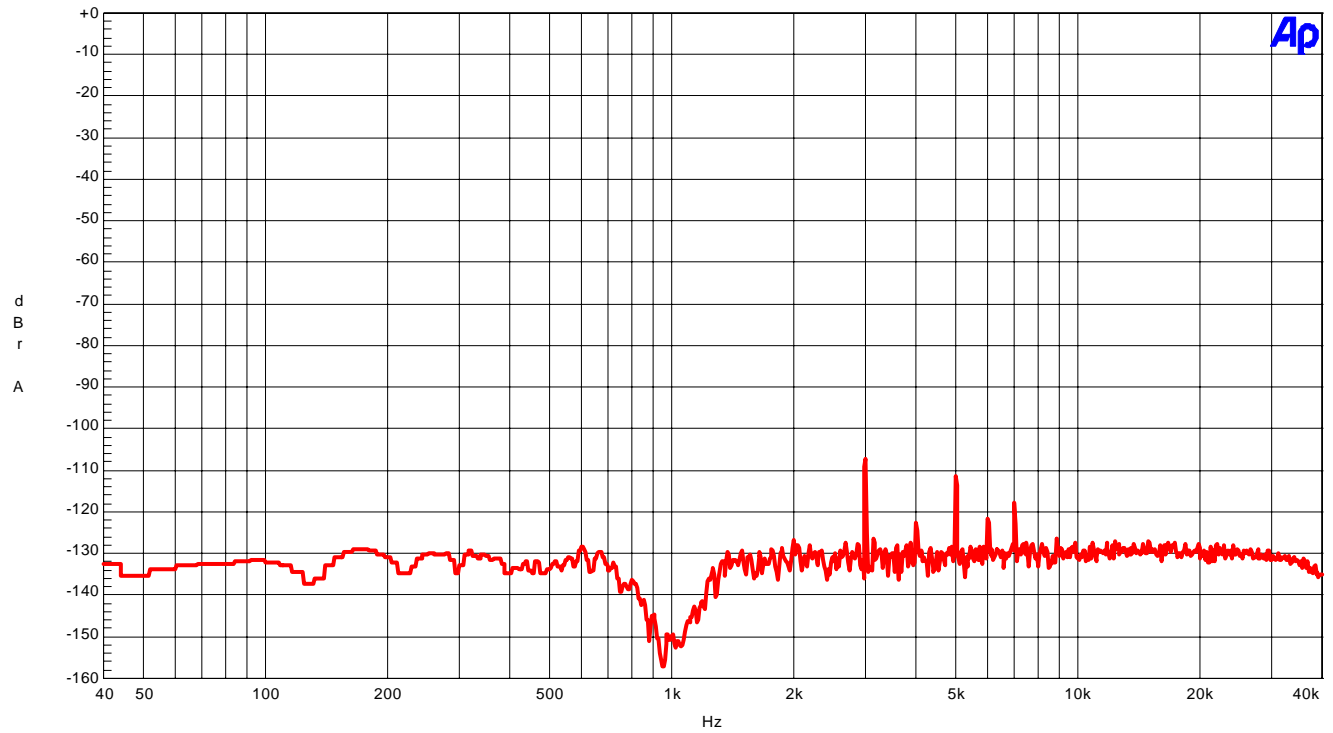
FFT (Input Level=0dBFS, fin=1kHz, notch)

AKM   AK4394 FFT (Input Leve=-60dBFS, fin=1kHz)
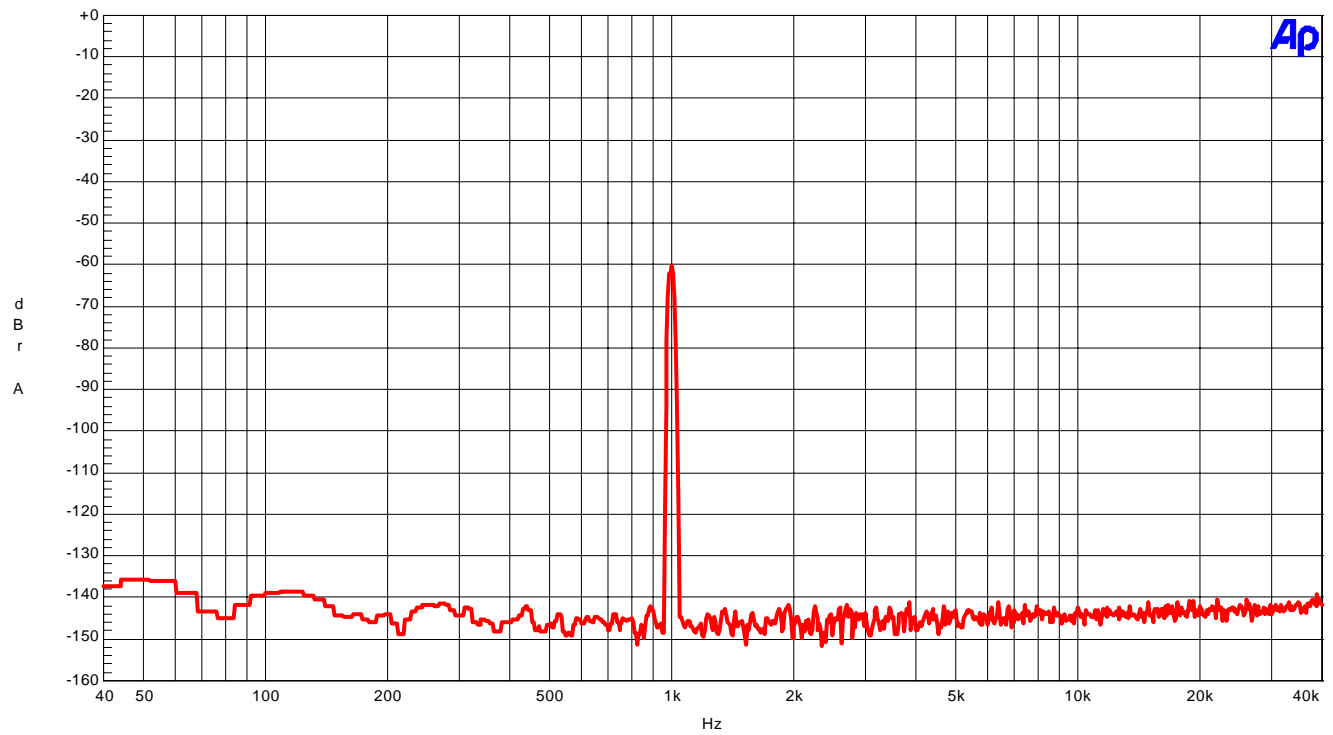
FFT (Input Level=-60dBFS, fin=1kHz)

(fs=96kHz)

AKM   AK4394 FFT (Input = "0"data)

FFT (noise floor)

AKM   AK4394 THD + N vs Amplitude(fin=1kHz)

THD + N vs Amplitude (fin=1kHz)

AKM

(fs=96kHz)

AK4394 THD + N vs Input Frequency(Input Level=0dBFS)
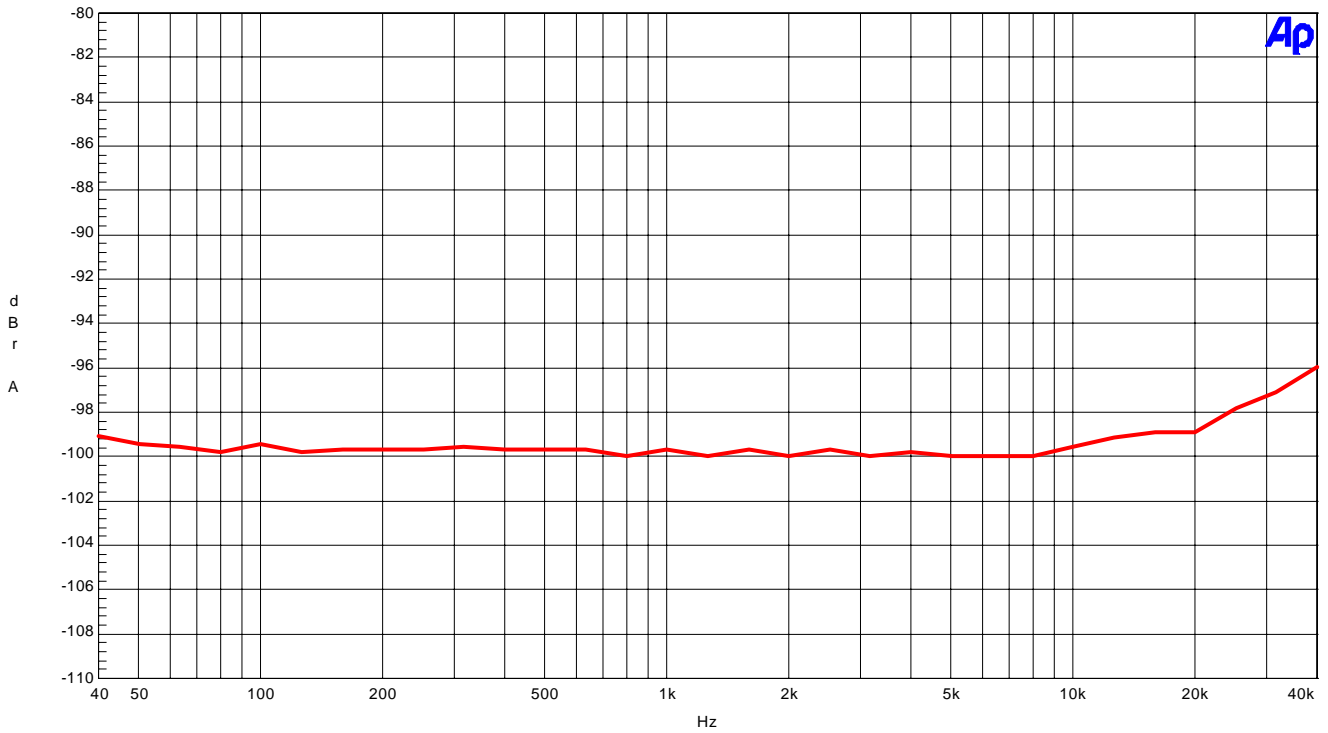
THD + N vs Input Frequency (Input Level=0dBFS)

AKM

AK4394 Linearity
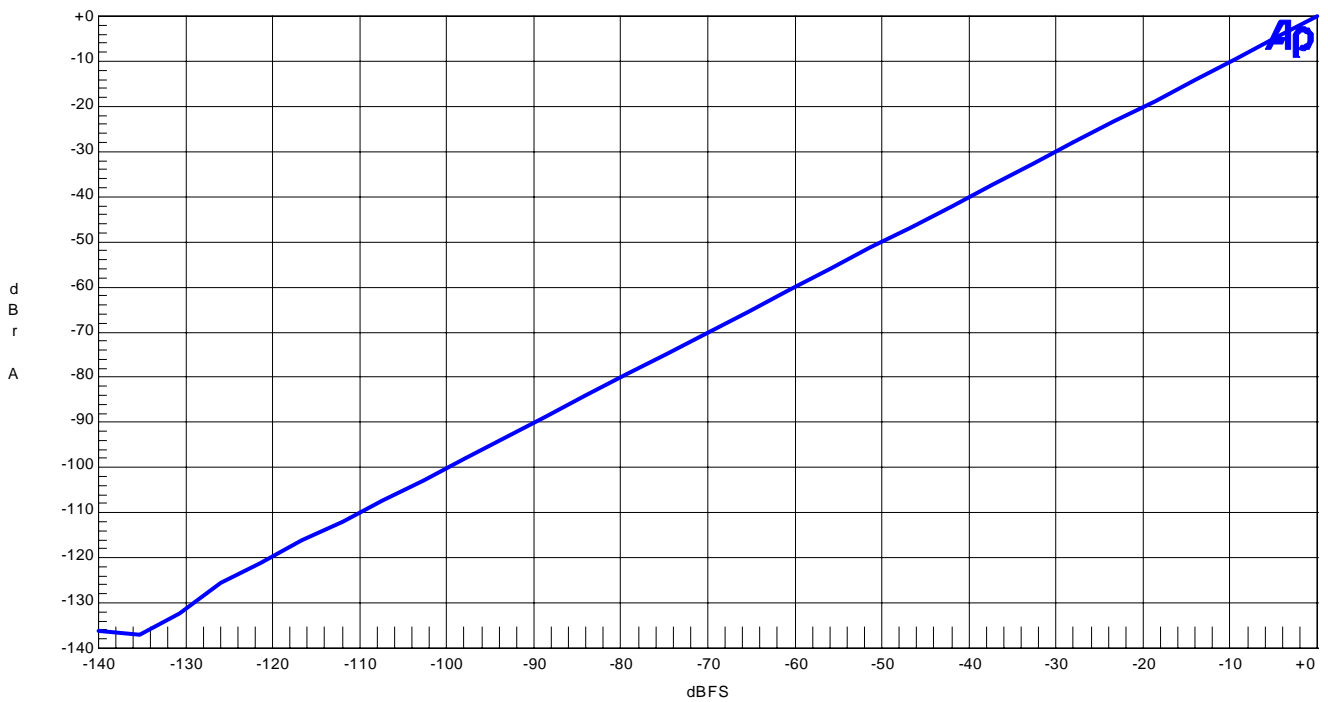
Linearity (fin=1kHz)

(fs=96kHz)

AKM   AK4394 Frequency Response

Frequency Response (Input Level=0dBFS)

AKM   AK4394 Crosstalk
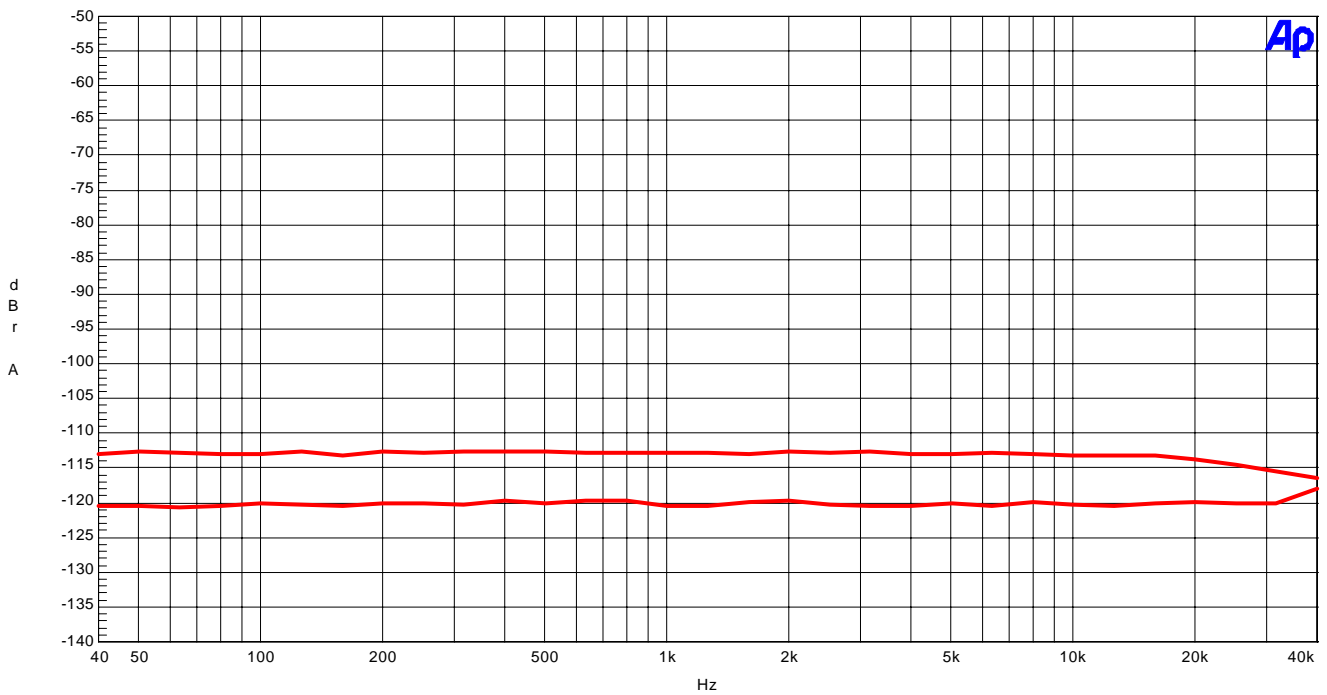
Crosstalk (upper = Rch, Lower = Lch)

Revision History

Date (YY/MM/DD)	Manual Revision	Board Revision	Reason	Contents
07/01/23	KM063002	C	Control Soft Manual	Control Soft Manual addition

Title		
AKD4393 Digital		
Size	Number	Rev
A3		C
Date	98.6.12	
Filename	4393REVC.SCH	
	Drawn by H.Imai	
	Sheet 1 of 2	

Digital Ground Analog Ground

AKD4393

Title: AKD4393
Analog
Size: A3   Number   Rev: C
Date: 98.6.12
Filename: 4393REVC.SCH
Drawn by: H.Imai
Sheet 2 of 2

AOUTR+
AOUTR−
AOUTL+
AOUTL−

C96 47u
R70 560
R61 300
R60 300
C94 10n
C95 10n
R59 300
R62 220
U15 NJM5534D
C104 0.1u
C103 10u

C93 47u
R68 560
R57 300
R56 300
C91 10n
C92 10n
R55 300
R58 220
U14 NJM5534D
C106 0.1u
C101 0.1u
C102 10u
C105 10u
C100 10u
C99 0.1u

C78 47u
R67 560
R53 300
R52 300
C71 10n
C75 10n
R51 300
R54 220
U13 NJM5534D
C108 0.1u
C97 0.1u
C107 10u
C98 10u

C68 47u
R69 560
R32 300
R33 300
C70 10n
C69 10n
R36 300
R35 220
U12 NJM5534D
C110 0.1u
C79 0.1u
C109 10u
C80 10u

R63 100
R64 100
J4
R65 100
R66 100
J2

R46 620
R47 620
R34 620
R31 620

R43 430
C81 (open)
R44 (short)
C82 4.7n
R45 (short)
C83 4.7n
R41 430
U17 NJM5534D
C74 0.1u
C90 10u
R48 (open)
C84 (open)
R50 100
C89 (short)
C85 0.1u
C86 10u

R42 430
C64 (open)
R39 (short)
C77 4.7n
R38 (short)
C63 4.7n
R37 430
U16 NJM5534D
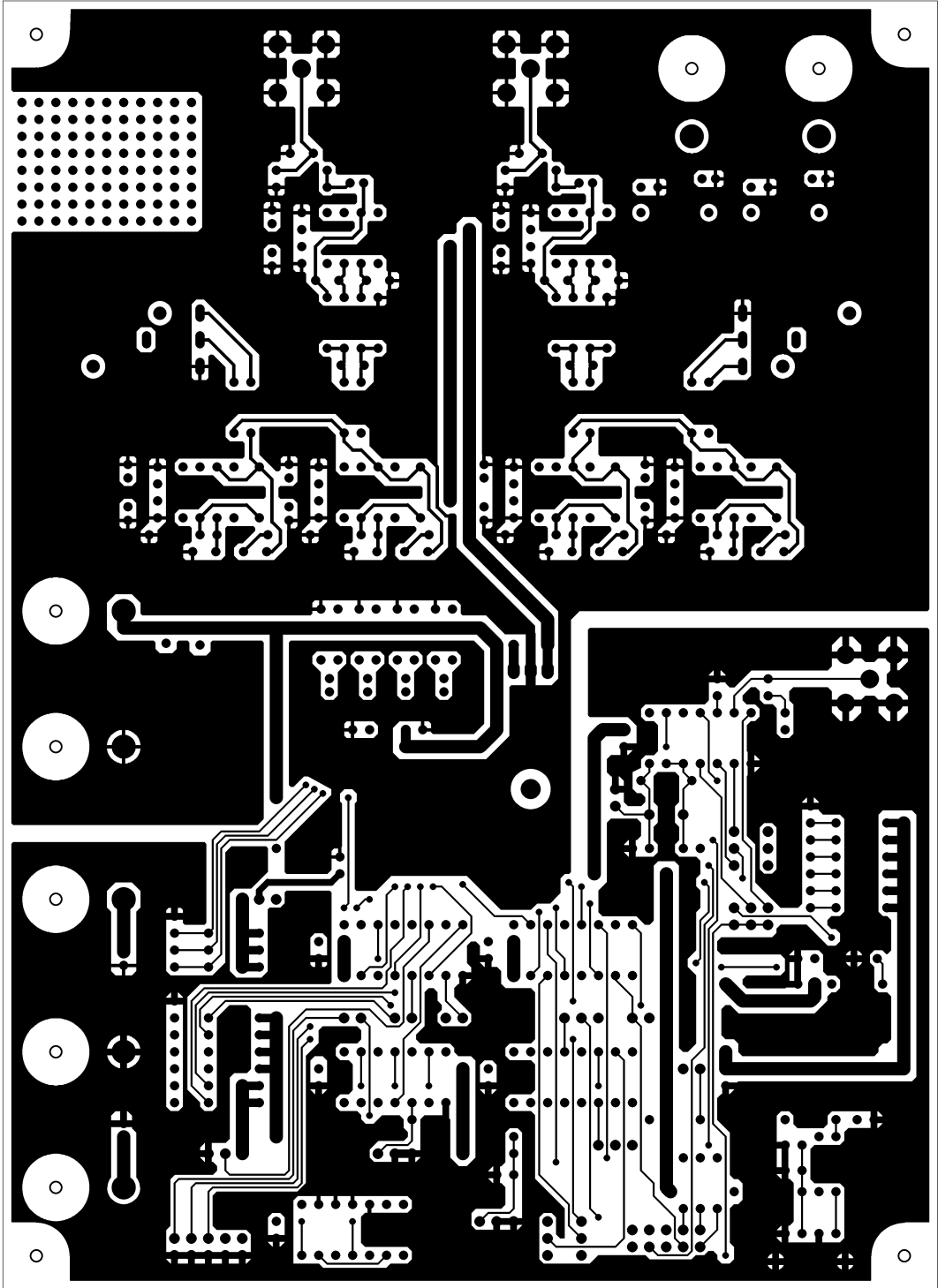C76 0.1u
C87 10u
R49 (open)
C88 (open)
R40 100
C73 (short)
C67 0.1u
C72 10u

J5 Rch
J3 Lch

−15
+15

4393C L1 SR SILK

4393C L1

4393C L2