FEATURES

- Two matched-delay outputs:
  - Bank A: undivided pass-through (QA)
  - Bank B: programmable divide by 2, 4, 8, 16 (QB0, QB1)
- Matched delay: all outputs have matched delay, independent of divider setting
- Guaranteed AC performance:
  - >2.5GHz f_{MAX}
  - <250ps t_r/t_f
  - <670ps t_{pd} (matched delay)
  - <15ps within-device skew
- Low jitter design
  - <1ps$_{RMS}$ cycle-to-cycle jitter
  - <10ps$_{PP}$ total jitter
- Power supply 3.3V or 2.5V
- Unique patent-pending input termination and VT pin for DC- and AC-coupled inputs: any differential inputs (LVPECL, LVDS, CML, HSTL)
- TTL/CMOS inputs for select and reset
- 100K EP compatible LVPECL outputs
- Parallel programming capability
- Wide operating temperature range: –40°C to +85°C
- Available in 16-pin (3mm x 3mm) MLF® package

APPLICATIONS

- OC-3 to OC-192 SONET/SDH applications
- Transponders
- Oscillators
- SONET/SDH line cards

Precision Edge®

DESCRIPTION

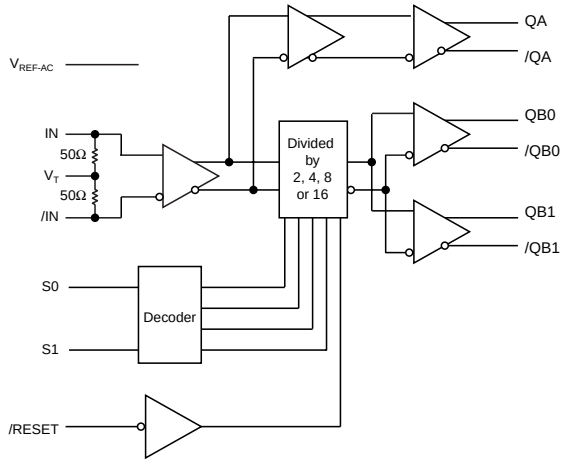
The SY89871U is a 2.5V/3.3V LVPECL output precision clock divider capable of accepting a high-speed differential clock input (AC or DC-coupled) CML, LVPECL, HSTL or LVDS clock input signal and dividing down the frequency using a programmable divider ratio to create a frequency-locked lower speed version of the input clock (Bank B). Available divider ratios are 2, 4, 8 and 16. In a typical 622MHz clock system this would provide availability of 311MHz, 155MHz, 77MHz, or 38MHz auxiliary clock components.

The differential input buffer has a unique internal termination design that allows access to the termination network through a VT pin. This feature allows the device to easily interface to different logic standards. A V_{REF-AC} reference is included for AC-coupled applications.

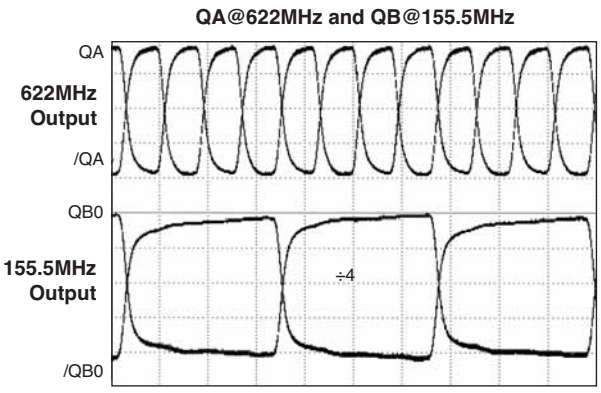
The SY89871U includes two phase-matched output banks. Bank A (QA) is a frequency-matched copy of the input. Bank B (QB0, QB1) is a divided down output of the input frequency. Bank A and Bank B maintain a matched delay independent of the divider setting.

All support documentation can be found on Micrel's web site at: www.micrel.com.

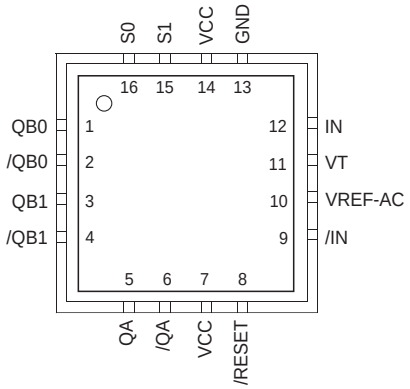
FUNCTIONAL BLOCK DIAGRAM



TYPICAL PERFORMANCE



PACKAGE/ORDERING INFORMATION



16-Pin MLF® (MLF-16)

Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89871UMI	MLF-16	Industrial	871U	Sn-Pb
SY89871UMITR[1]	MLF-16	Industrial	871U	Sn-Pb
SY89871UMG[2]	MLF-16	Industrial	871U with Pb-Free bar line indicator	NiPdAu Pb-Free
SY89871UMGTR[1, 2]	MLF-16	Industrial	871U with Pb-Free bar line indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

PIN DESCRIPTION

Pin Number	Pin Name	Pin Function
1, 2, 3, 4	QB0, /QB0 QB1, /QB1	Differential Buffered Output Clocks: This differential output is a divided-down version of the input frequency and has a matched output delay with Bank A. Divided by 2, 4, 8, or 16. See “Truth Table.” Unused output pairs may be left floating.
5, 6	QA, /QA	Differential Buffered Undivided Output Clock.
7, 14	VCC	Positive Power Supply: Bypass with 0.1µF™™0.01µF low ESR capacitors.
8	/RESET	Output Reset: Internal 25ký pull-up. Logic LOW will reset the divider select. See “Truth Table.” Input threshold is V_{CC}/2.
12, 9	IN, /IN	Differential Input: Internal 50ý termination resistors to VT input. See “Input Interface Applications” section.
10	VREF-AC	Reference Voltage: Equal to V_{CC}–1.4V (approx.), and used for AC-coupled applications. For DC-coupled applications, VREF-AC is normally left floating. Maximum sink/source current is 0.5mA. See “Input Interface Applications” section.
11	VT	Input Termination Center-Tap: Each side of differential input pair terminates to this pin. The VT pin provides a center tap to a termination network for maximum interface flexibilty. For CML and LVDS inputs, leave this pin floating. See “Input Interface Application” section.
13	GND	Ground.
15, 16	S1, S0	Select Pins: See “Truth Table.” LVTTL/CMOS logic levels. Internal 25ký pull-up resistor. Logic HIGH if left unconnected (divided by 16 mode). S0 = LSB. Input threshold is V_{CC}/2.

TRUTH TABLE

/RESET	S1	S0	Bank A Output	Bank B Outputs
1	0	0	Input Clock	Input Clock ÷2
1	0	1	Input Clock	Input Clock ÷4
1	1	0	Input Clock	Input Clock ÷8
1	1	1	Input Clock	Input Clock ÷16
0	X	X	Input Clock	QB = LOW, /QB = HIGH

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC} +0.3V
PECL Output Current (I_{OUT})
  Continuous 50mA
  Surge 100mA
V_T Current (I_{VT}) ..... ±100mA
Input Current IN, /IN (I_{IN}) ..... ±50mA
V_{REF-AC} Sink/Source Current ($I_{VREF-AC}$) ..... ±2mA
Lead Temperature (soldering, 20 sec.) ..... 260°C
Storage Temperature (T_S) ..... –65°C to +150°C

Operating Ratings[2]

Supply Voltage (V_{CC}) ..... +2.375V to +3.63V
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance[3]
  MLF® (θ_{JA})
    Still-Air ..... 60°C/W
    500lfpm ..... 54°C/W
  MLF® (ψ_{JB})
    Junction-to-board ..... 38°C/W

DC ELECTRICAL CHARACTERISTICS[4]

T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply Voltage		2.37		3.60	V
I_{CC}	Power Supply Current	No load, max V_{CC}.		50	75	mA
R_{IN}	Differential Input Resistance, (IN-to-/IN)		90	100	110	ý
V_{IH}	Input HIGH Voltage, (IN, /IN)		0.1		V_{CC}+0.3	V
V_{IL}	Input LOW Voltage, (IN, /IN)		–0.3		V_{IH}–0.1	V
V_{IN}	Input Voltage Swing	**Notes 5**	0.1		V_{CC}	V
V_{DIFF_IN}	Differential Input Voltage Swing	**Notes 5, 6**	0.2			V
$\|I_{IN}\|$	Input Current, (IN, /IN)	**Note 7**			45	mA
V_{REF-AC}	Reference Voltage		V_{CC}–1.525	V_{CC}–1.425	V_{CC}–1.325	V

Notes:

1. Permanent device damage may occur if ratings in the “Absolute Maximum Ratings” section are exceeded. This is a stress rating only and functional operation is not implied for conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Junction-to-board resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB.
4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
5. See “Timing Diagram” for V_{IN} definition. V_{IN} (max.) is specified when V_T is floating.
6. See “Typical Operating Characteristics” section for V_{DIFF} definition.
7. Due to the internal termination (see "Input Buffer Structure" section) the input current depends on the applied voltages at IN, /IN and VT inputs. Do not apply a combination of voltages that causes the input current to exceed the maximum limit!

(100KEP) LVPECL DC ELECTRICAL CHARACTERISTICS[8]

V_{CC} = 3.3V ±10% or 2.5V ±5%; T_A = –40°C to +85°C, R_L = 50ý to V_{CC} –2V, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage		V_{CC}–1.145	V_{CC}–1.020	V_{CC}–0.895	V
V_{OL}	Output LOW Voltage		V_{CC}–1.945	V_{CC}–1.820	V_{CC}–1.695	V
V_{OUT}	Output Voltage Swing		550	800	1050	mV
V_{DIFF_OUT}	Differential Output Voltage Swing		1.10	1.6	2.1	V

LVTTL/LVCMOS DC ELECTRICAL CHARACTERISTICS[8]

V_{CC} = 3.3V ±10% or 2.5V ±5%; T_A = –40°C to +85°C.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current		–125		20	µA
I_{IL}	Input LOW Current				–300	µA

Note:

8. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. Parameters are for V_{CC} = 2.5V. They vary 1:1 with V_{CC}.

AC ELECTRICAL CHARACTERISTICS[9]

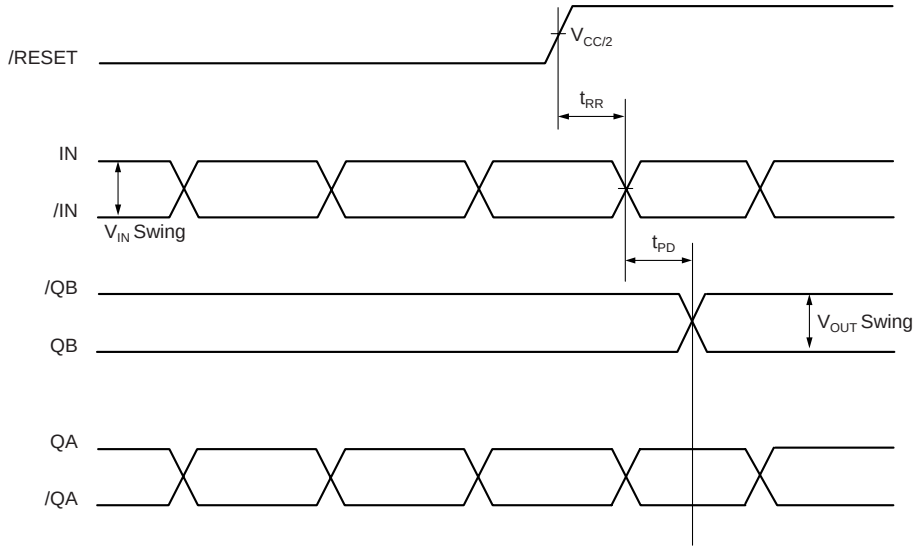
V_{CC} = 3.3V ±10% or 2.5V ±5%; T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Output Toggle Frequency	Output Swing ž 400mV	2.5			GHz
	Maximum Input Frequency	**Note 10**	3.2			GHz
t_{PD}	Differential Propagation Delay	Input Swing < 400mV	460	580	710	ps
	IN-to-QA or QB	Input Swing ž 400mV	420	550	670	ps
t_{SKEW}	Within-Device Skew (Differential) QB0-to-QB1	**Note 11**		7	15	ps
	Within-Device Skew (Differential) QA-to-QB	**Note 11**		12	30	ps
	Part-to-Part Skew (Differential)	**Note 11**			250	ps
t_{JITTER}	Cycle-to-Cycle Jitter	**Note 12**			1	ps_{RMS}
	Total Jitter	**Note 13**			10	ps_{PP}
t_{RR}	Reset Recovery Time		600			ps
t_r, t_f	Output Rise/Fall Times (20% to 80%)		70	150	250	ps

Notes:

9. Measured with 400mV input signal, 50% duty cycle, all loading with 50ý to V_{CC}–2V, unless otherwise stated.
10. Bank A (pass-through) maximum frequency is limited by the output stage. Bank B (input-to-output ÷2, ÷4, ÷8, ÷16) can accept an input frequency >3GHz, while Bank A will be slew rate limited.
11. Skew is measured between outputs under identical transitions.
12. Cycle-to-cycle jitter definition: the variation in period between adjacent cycles over a random sample of adjacent cycle pairs. $t_{JITTER\_cc} = T_n - T_{n+1}$, where T is the time between rising edges of the output signal.
13. Total jitter definition: with an ideal clock input, of frequency - f_{MAX} (device), no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.

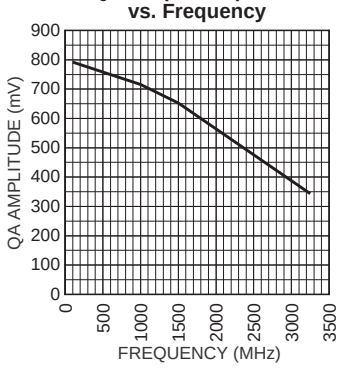
TIMING DIAGRAM



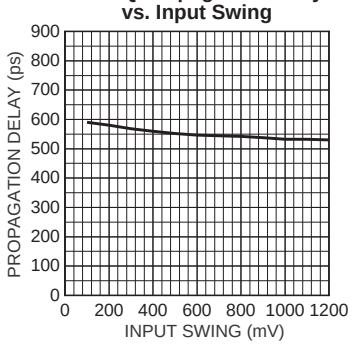
TYPICAL OPERATING CHARACTERISTICS

V_{CC} = 3.3V, V_{IN} = 400mV, T_A = 25°C, R_L = 50ý to V_{CC}–2V, unless otherwise stated.

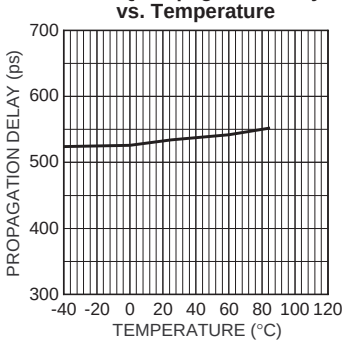
QA Output Amplitude vs. Frequency



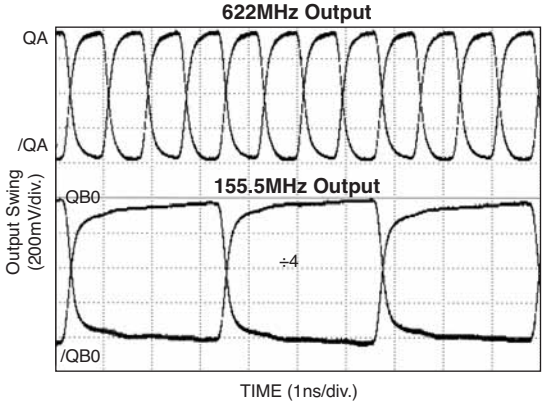
IN to Q Propagation Delay vs. Input Swing



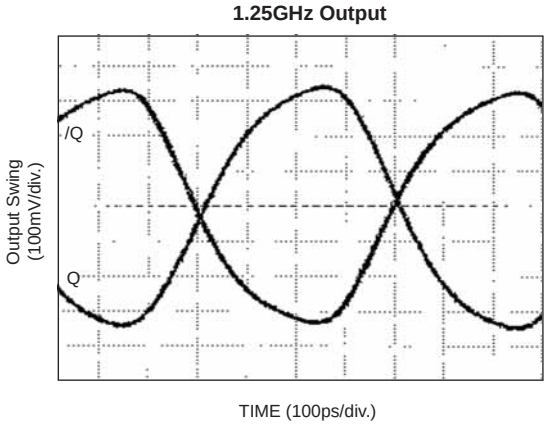
IN to Q Propagation Delay vs. Temperature



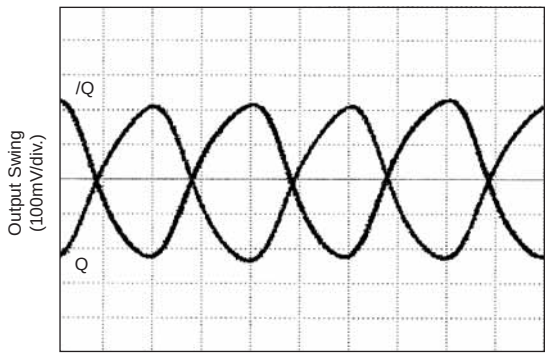
QA@622MHz and QB@155.5MHz 622MHz Output



1.25GHz Output



2.5GHz Output



DEFINITION OF SINGLE-ENDED AND DIFFERENTIAL SWING

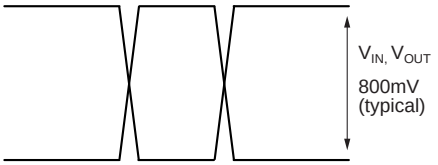


Figure 1a. Single-Ended Swing

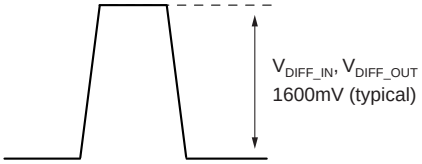


Figure 1b. Differential Swing

INPUT BUFFER STRUCTURE

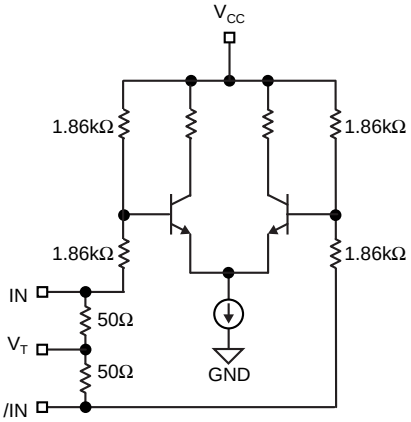


Figure 2a. Simplified Differential Input Buffer

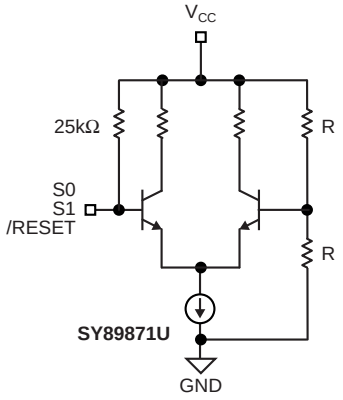


Figure 2b. Simplified TTL/CMOS Input Buffer

INPUT INTERFACE APPLICATIONS

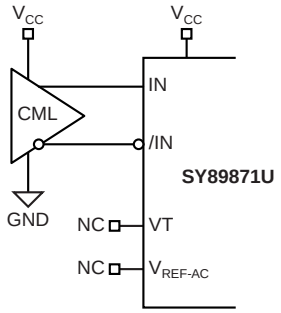


Figure 3a. DC-Coupled CML Input Interface

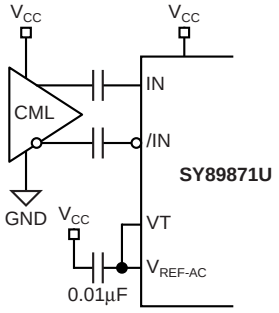


Figure 3b. AC-Coupled CML Input Interface

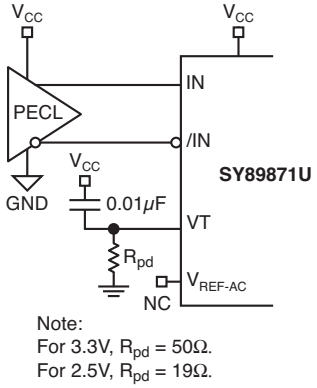


Figure 3c. DC-Coupled PECL Input Interface

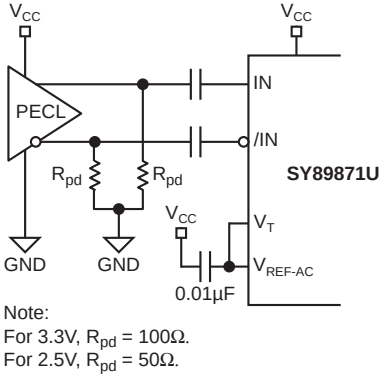


Figure 3d. AC-Coupled PECL Input Interface

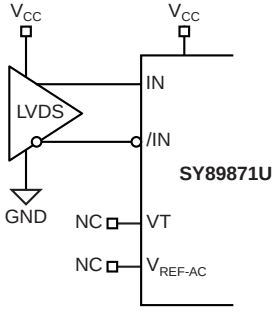


Figure 3e. LVDS Input Interface

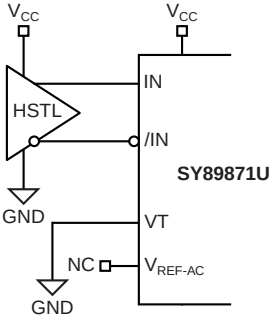


Figure 3f. HSTL Input Interface

RELATED PRODUCT AND SUPPORT DOCUMENTATION

Part Number	Function	Data Sheet Link
SY89874U	2.5GHz Any Diff. In-to-LVPECL Programmable Clock Divider and 1:2 Fanout Buffer w/Internal Termination	http://www.micrel.com/product-info/products/sy89874u.shtml
	MLF® Application Note	http://www.amkor.com/products/notes_papers/mlf_appnote.pdf
HBW Solutions	New Products and Applications	http://www.micrel.com/product-info/products/solutions.shtml

LVPECL OUTPUT TERMINATION RECOMMENDATIONS

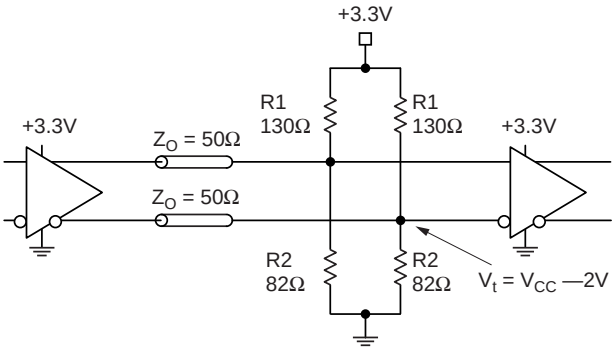


Figure 4a. Parallel Termination–Thevenin Equivalent

Note:

1. For +2.5V systems: R1 = 250ý, R2 = 62.5ý.

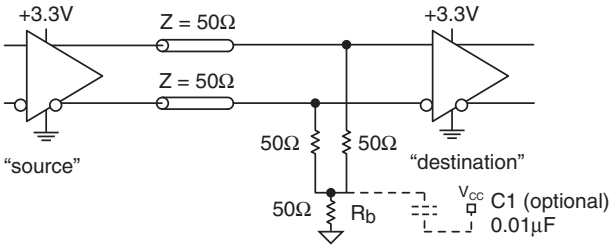


Figure 4b. Three-Resistor "Y–Termination"

Notes:

1. Power-saving alternative to Thevenin termination.
2. Place termination resistors as close to destination inputs as possible.
3. R_b resistor sets the DC bias voltage, equal to V_T. For +3.3V systems R_b = 46ý to 50ý. For +2.5V systems R_b = 19ý.
4. C1 is an optional bypass capacitor intended to compensate for any t_r/t_f mismatches.

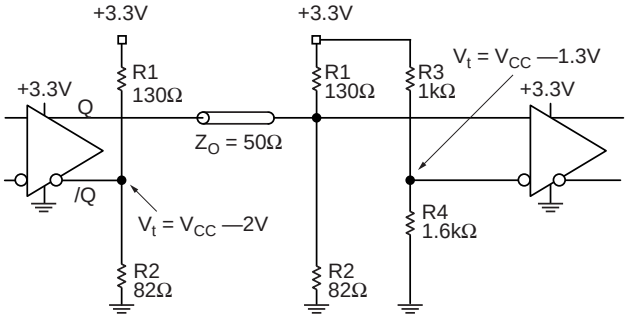
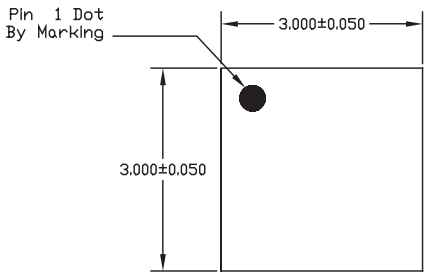


Figure 4d. Terminating Unused I/O

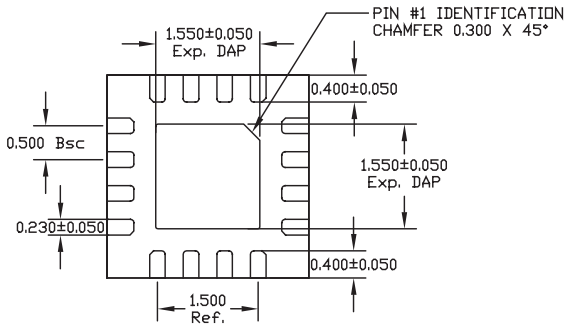
Notes:

1. Unused output (/Q) must be terminated to balance the output.
2. For +2.5V systems: R1 = 250ý, R2 = 62.5ý, R3 = 1.25ký, R4 = 1.2ký.

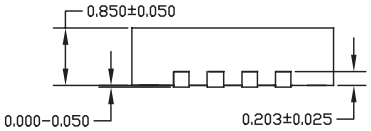
16-PIN *Micro*LeadFrame® (MLF-16)



TOP VIEW

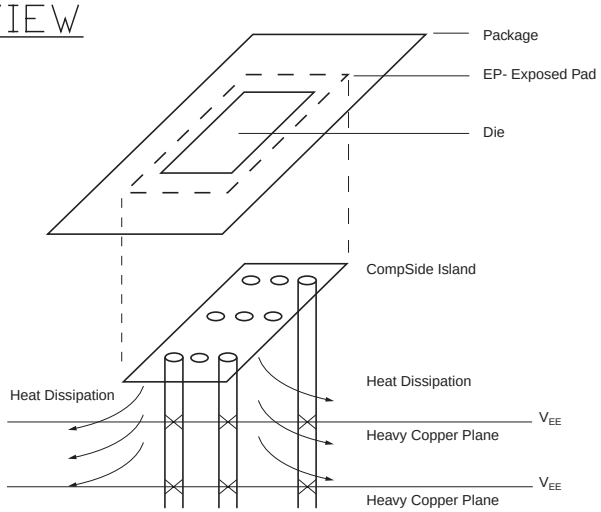


BOTTOM VIEW



SIDE VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.



PCB Thermal Consideration for 16-Pin MLF® Package
(Always solder, or equivalent, the exposed pad to the PCB)

Package Notes:

1. Package meets Level 2 moisture sensitivity classification, and is shipped in dry-pack form.
2. Exposed pads must be soldered to a ground for proper thermal management.

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA

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