8192 BIT BIPOLAR TTL

PROGRAMMABLE READ ONLY MEMORY

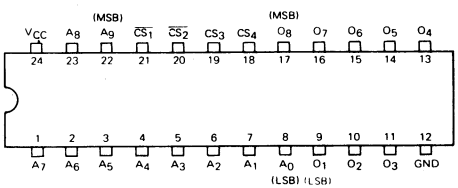
Description

The μPB408C, μPB408D, μPB428C and μPB428D are high speed, electrically programmable, fully decoded 8192 bit TTL read only memories. On-chip address decoding, four chip select inputs and open-collector/three-state outputs allow easy expansion of memory capacity. The μPB408C, μPB408D, μPB428C and μ428D are fabricated with logic level zero (low); logic level one (high) can be electrically programmed into the selected bit locations. The same address inputs are used for both programming and reading.

Features

- 1024 WORDS x 8 BITS organization (Fully decoded)
- TTL Interface
- Fast read access time : 50 ns MAX. (μPB408-1, μPB428-1)
- Medium power consumption : 500 mW TYP.
- Four chip select inputs for memory expansion
- Open-Collector outputs (μPB408C, μ408D)/Three-state outputs (μPB428C, μPB428D)
- Cerdip 24-Lead Dual In-Line Package (μPB408D, μPB428D)
- Plastic 24-Lead Dual In-Line Package (μPB408C, μPB428C)
- Fast Programming time : 200 μs/bit TYP.
- Replaceable with : Signetics' 82S180/181, Harris' HM 7680/7681 and equivalent devices (as a ROM)

Connection Diagram (Top View)



Pin names

$A_0 - A_9$	: Address Inputs
$O_1 - O_8$	: Data Outputs
$\overline{CS}_1$, $\overline{CS}_2$, CS_3, CS_4	: Chip Select Inputs
V_{CC}	: Power Supply (+5V)
GND	: Ground

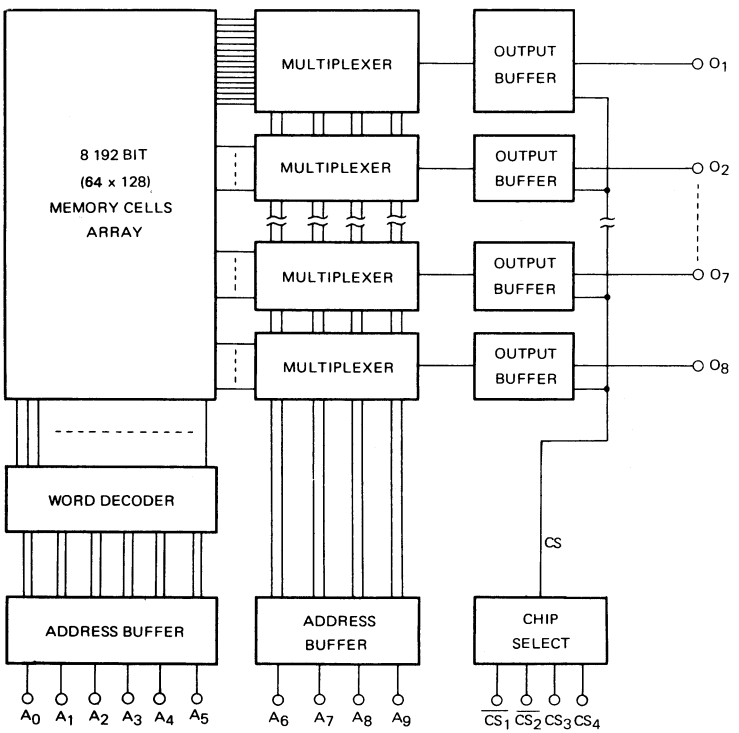
Operation

First we define an internal Chip Select logic by four Chip Select inputs:
$CS' = \overline{CS_1} + \overline{CS_2} + \overline{CS_3} \cdot \overline{CS_4}$
That is, CS' is a logical zero (low) if and only if $\overline{CS_1} = \overline{CS_2} = 0$ and $CS_3 = CS_4 = 1$. While CS' is a logical one (high) in all the other cases.

1. Programming
A logic one can be permanently programmed into a selected bit location by using special equipment (programmer). First, the desired word is selected by the ten address inputs in TTL levels. The four Chip Select inputs must be set so that CS' is a logical one. Secondly, a train of high current programming pulses is applied to the desired output. After the sensed voltage indicates that the selected bit is in the logic one state, an additional pulse train is applied, then is stopped.

2. Reading
To read the memory, The four Chip Select inputs must be set so that CS' is a logical zero. The outputs then correspond to the data programmed in the selected words. When the four Chip Select inputs are set so that CS' becomes a logical one, all the outputs will be high (floating).

Logic Diagram



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_I	−0.5 to +5.5	V
Output Voltage	V_O	−0.5 to +5.5	V
Output Current	I_O	50	mA
Operating Temperature	T_{opt}	−25 to +75	°C
Storage Temperature			
Cerdip Package	T_{stg}	−65 to +150	°C
Plastic Package	T_{stg}	−55 to +125	°C

D.C. CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, T_a = 0 to 75 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Input High Voltage	V_{IH}	2.0			V	
Input Low Voltage	V_{IL}			0.85	V	
Input High Current	I_{IH}			40	μA	V_I=5.5 V V_{CC}=5.5 V
Input Low Current	$-I_{IL}$			0.25	mA	V_I=0.4 V V_{CC}=5.5 V
Output Low Voltage	V_{OL}			0.45	V	I_O=16 mA V_{CC}=4.5 V
Output Leakage Current	I_{OFF1}			40	μA	V_O=5.5 V V_{CC}=5.5 V
Output Leakage Current	$-I_{OFF2}$			40	μA	V_O=0.4 V V_{CC}=5.5 V
Input Clamp Voltage	$-V_{IC}$			1.2	V	I_I=−18 mA V_{CC}=4.5 V
Power Supply Current	I_{CC}		100	160	mA	All Inputs Grounded V_{CC}=5.5 V
Output High Voltage	V_{OH}	2.4			V	I_O=−2.4 mA V_{CC}=4.5 V
Output Short Circuit Current *	$-I_{SC}$	20		70	mA	V_O=0 V

* Note: Applicable to μPB428C and μPB428D.

CAPACITANCE (V_{CC} = 5 V, f = 1 MHz, T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	MAX.	UNIT	TEST CONDITION
Input Capacitance	C_{IN}		8	pF	V_{IN} = 2.5 V
Output Capacitance	C_{OUT}		10	pF	V_{OUT} = 2.5 V

A.C. CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, T_a = 0 to 75 °C)

CHARACTERISTIC	SYMBOL	μPB408C-1, μPB428C-1 μPB408D-1, μPB428D-1		μPB408C, μPB428C μPB408D, μPB428D		UNIT
		MIN.	MAX.	MIN.	MAX.	
Address Access Time	t_{AA}		50		60	ns
Chip Select Access Time	t_{ACS}		30		40	ns
Chip Select Disable Time	t_{DCS}		30		40	ns

Note 1. Output Load: See Fig. 1.
Note 2. Input Waveform: 0.0 V for low level and 3.0 V for high level, less than 10 ns for both rise and fall times.
Note 3. Measurement References: 1.5 V for both inputs and outputs.
Note 4. C_L in Fig. 1 includes jig and probe stray capacitances.

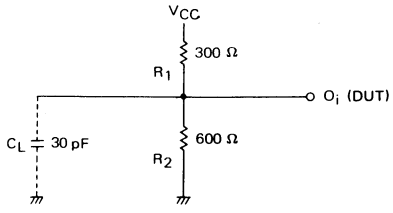


Fig. 1

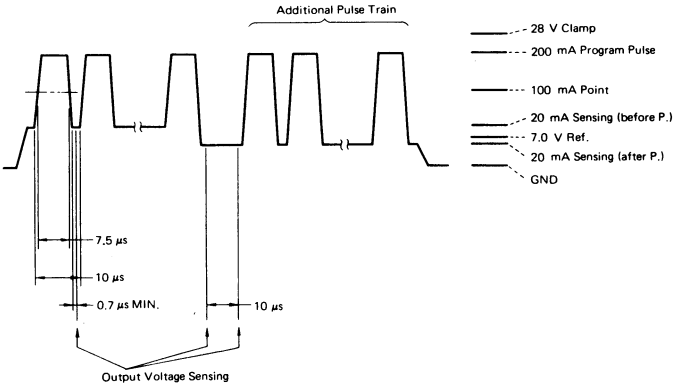
Programming Specification

It is imperative that this specification be rigorously observed in order to correctly program the μPB408C, μPB408D, μPB428C and μPB428D. NEC will not accept responsibility for any device found to be defective if it were not programmed according to this specification.

CHARACTERISTIC	LIMIT	UNIT	NOTES
Ambient Temperature	25 ±5	°C	
Programming Pulse			
Amplitude	200 ±5 %	mA	
Clamp Voltage	28 +0 % −2 %	V	
Ramp Rate (Both in Rise and in Fall)	70 MAX.	V/μs	
Pulse Width	7.5 ±5 %	μs	15 V point/150 Ω load.
Duty Cycle	70 % MIN.		
Sense Current			
Amplitude	20 ±0.5	mA	
Clamp Voltage	28 +0 % −2 %	V	
Ramp Rate	70 MAX.	V/μs	15 V point/150 Ω load.
Sense Current Interruption before and after address change	10 MIN.	μs	
Programming V_{CC}	5.0 +5 % −0 %	V	
Maximum Sensed Voltage* for programmed "1"	7.0 ±0.1	V	
Delay from trailing edge of programming pulse before sensing output voltage	0.7 MIN.	μs	

* A bit is judged to be programmed when two successive sense readings 10 μs apart with no intervening programming pulse, pass the limit. When this condition has been met, four additional pulses are applied and the pulse train, then the sense current is terminated.

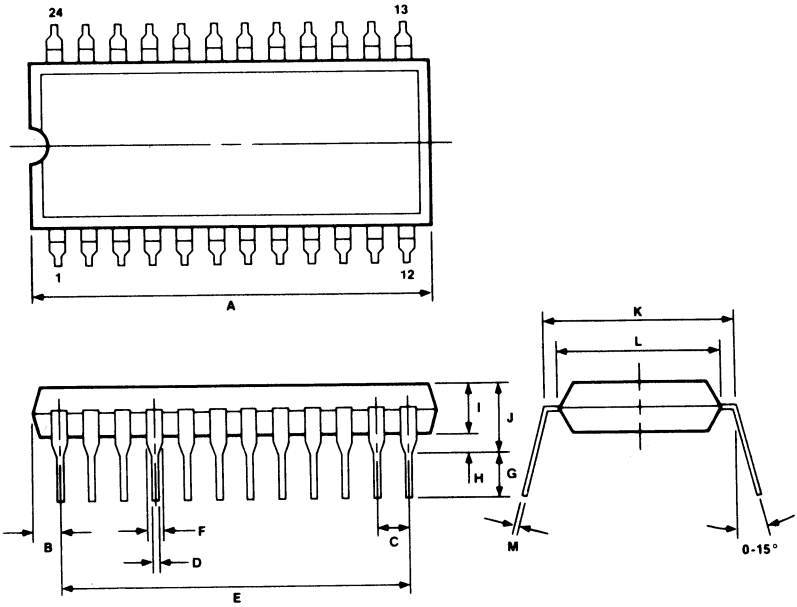
Fig. 2 Typical Output Voltage Waveform.



Package Dimensions

24PIN Plastic DIP

Item	Millimeters
A	33.02 max
B	2.54 max
C	2.54 [TP]
D	.50 ± .10
E	27.94
F	1.2 min
G	3.5 ± 0.3
H	.51 min
I	4.31 max
J	5.72 max
K	15.24 [TP]
L	13.2
M	.25 $^{+.10}_{-.05}$



24PIN Cerdip

Item	Millimeters
A	33.02 max
B	2.54 max
C	2.54 [TP]
D	.50 ± .010
E	27.94
F	1.2 min
G	3.0 ± .3
H	.51 min
I	3.80
J	5.08 max
K	15.24 [TP]
L	13.21
M	.25 ± .05