SPECTRALINEAR

SL15300

Programmable Spread Spectrum Clock Generator (SSCG)

Key Features

- Low power dissipation
  - 7.9mA-typ at 66MHz and VDD=3.3V
  - 7.0mA-typ at 66MHz and VDD=2.5V
- Wide 2.5V to 3.3V +/-10% power supply range
- Programmable 4 outputs from 3 to 200MHz
- Low Jitter
  - TBDps at 66MHz
- Programmable Center or Down Spread Modulation from 0.25 to 5.0%
- 8 to 48 MHz external crystal range
- 3 to 166 MHz external clock range
- Integrated internal voltage regulator
- Programmable PD#/OE/SSON#/FS functions
- Programmable CL at XIN and XOUT pins
- Programmable output rise and fall times
- Programmable modulation frequency from 25 to 120 kHz

Applications

- Printers, MFPs
- Digital Copiers
- NBPCs and LCD Monitors
- Routers, Servers and Switchers
- HDTV and DVD-R/W

Description

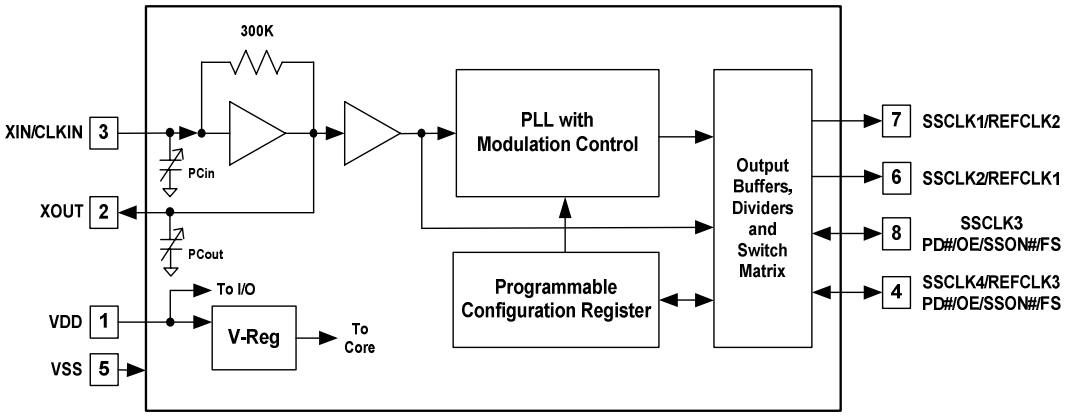
The SL15300 a programmable low power Spread Spectrum Clock Generator (SSCG) used for reducing Electromagnetic Interference (EMI). The product is designed using SpectraLinear proprietary programmable **EProClock™** phase-locked loop (PLL) and Spread Spectrum Clock (SSC) technology to synthesize and modulate the input clock. The modulated clock can significantly reduce the measured EMI levels, and leading to the compliance with regulatory agency requirements.

Up to 4 output clock frequencies, Spread %, output rise and fall times, crystal load, modulation frequency and PD#/OE/SSON#/FS functions can be programmed to meet the needs of wide range of applications. The SL15300 operates from 2.5V to 3.3V power supply voltage range. The product is offered in 8-pin TSSOP package with commercial and industrial grades.

Benefits

- Peak EMI reduction of 8 to 16 dB
- Fast time-to-market
- Cost Reduction
- Reduction of PCB layers
- Eleminates the need for higher order crystals (Xtals) and crystal oscillators (XOs)

Block Diagram



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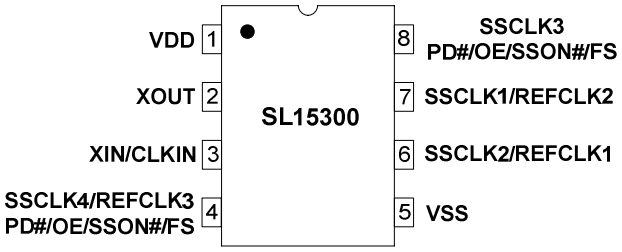
Pin Configuration



8-Pin TSSOP

Pin Description

Pin Number	Pin Name	Pin Type	Pin Description
1	VDD	Power	Positive power supply.
2	XOUT	Output	Crystal or ceramic resonator output pin. Leave this pin unconnected (floating) if external clock is used at Pin-3.
3	XIN/CLKIN	Input	Crystal, ceramic resonator or external clock input pin.
4	SSCLK4, REFCLK3, PD#, OE, SSON# or FS	Output or Input	Multi function Programmable SSCLK4 or REFOUT3 clock pin or PD#, OE, SSON#, or FS control pin. Power Down (PD#-Active Low): If PD#=0(Low) and Output Enable (OE-Active High). If PD# or OE is programmed, the pin is weakly pulled high to VDD. If SSON# or FS is programmed, the pin is weakly pulled low to VSS.
5	VSS	Power	Power supply ground.
6	SSCLK2, REFCLK1	Output	This pin can be programmed as SSCLK2 or REFCLK1 clock pin.
7	SSCLK1 or REFCLK2	Output	This pin can be programmed as SSCLK2 or REFCLK2.
8	SSCLK4, REFCLK3, PD#, OE, SSON# or FS	Input or Output	Multi function Programmable SSCLK4 or REFOUT3 clock pin or PD#, OE, SSON# or FS control pin. Power Down (PD#-Active Low): If PD#=0(Low) and Output Enable (OE-Active High). If PD# or OE is programmed, the pin is weakly pulled high to VDD. If SSON# or FS is programmed, the pin is weakly pulled low to VSS.

Notes:

1. Pull-down/up resisters can be programmed to VDD or VSS as required. The above programming values are default values.
2. Refer to DC electrical specifications tables for pull-down/up resistor values.

General Description

The primary source of EMI from digital circuits is the system clock and all the other synchronous clocks and control signals derived from the system clock. The well know techniques of filtering (suppression) and shielding (containment), while effective, can cost money, board space and longer development time.

A more effective and efficient technique to reduce EMI is Spread Spectrum Clock Generator (SSCG) technique. Instead of using constant clock frequency, the SSCG technique modulates (spreads) the system clock with a much smaller frequency, to reduce EMI emissions at its source: The System Clock.

The SL15300 is designed using SpectraLinear proprietary programmable **EProClock™** phase-locked loop (PLL) and Spread Spectrum Technologies (SST) to synthesize and modulate (spread) the system clock such that the energy is spread out over a wider bandwidth. This reduces the peak value of the radiated emissions at the fundamental and the harmonics. This reduction in radiated energy can significantly reduce the cost of complying with regulatory agency requirements and improve time-to-market without degrading system performance.

The SL15300 operates from 3.3V to 2.5V power supply range. Refer to SL15L101 for 1.8V power supply operation.

The SL15300 is available in 8-pin TSSOP package with Commercial Temperature range of 0 to 70°C and Industrial Temperature range of –40 to 85°C.

Input Frequency Range

The input frequency range is from 8.0 to 48.0 MHz for crystals and ceramic resonators. If an external clock is used, the input frequency range is from 8 to 166 MHz.

Output Frequency Range and Outputs

Up to four (4) outputs can be programmed as SSCLK or REFCLK. SSCLK output can be synthesized to any value from 3 to 200 MHz with spread based on valid input frequency. The spread at SSCLK pins can be stopped by SSON# input control pin, If SSON# pin is HIGH (VDD), the frequency at this pin is the synthesized to the nominal value of the input frequency and there is no spread.

REFOUT is the buffered output of the oscillator and is the same frequency as the input frequency without spread. However, REFOUT value can also be divided by using the output dividers from 2 to 32. The SSCLK is the programmed and synthesized value of the input clock. The remaining SSCLKs could be the same value providing fanout of up to 4 or the frequency can be divided from also 2 to 32. In this case, the spread % value is the same as the original programmed spread % value. By using only first order crystals, SL15300 can synthesize output frequency up to 200 MHz, eliminating the need for higher order Crystals (Xtals) and Crystal Oscillators (XOs). This reduces the cost while improving the system clock accuracy, performance and reliability.

Programmable CL (Crystal Load)

The SL15300 provides programmable on-chip capacitors at XIN/CLKIN (Pin-3) and XOUT (Pin-2). The resolution of this programmable capacitor is 6-bits with LSB value of 0.5pF. When all bits are off the pin capacitance is CXIN=CXOUT =7pF (minimum value). When all bits are on the pin capacitance is CXIN=CXOUT=38pF (maximum value). The values of C_{XIN} and C_{XOUT} based on the C_L (Crystal Load Capacitor) can be calculated as: $C_{XIN}=C_{XOUT}=2C_L-C_{PCB}$. Refer to the Page-13 for additional information on crystal load (C_L).
In addition, if an external clock is used, the capacitance at Pin-3 (CLKIN) can programmed to control the edge rate of this input clock, providing additional EMI control.

Programmable Modulation Frequency

The Spread Spectrum Clock (SSC) modulation default value is 31.5 kHz. The higher values of up to 120 kHz can also be programmed. Less than 25 kHz modulation frequency is not recommended to stay out of the range audio frequency bandwidth since this frequency could be detected as a noise by the audio receivers within the vicinity.

Programmable Spread Percent (%)

The spread percent (%) value is programmable from +/-0.25% to +/-2.5% (center spread) or -0.5% to -5.0% (down spread) for all SSCLK frequencies. It is possible to program smaller or larger non-standard values of spread percent. Contact SLI if these non-standard spread percent values are required in the application.

SSON# or Function Select (FS)

The SL15300 Pin-8 can also be programmed as either SSON# to enable or disable the programmed spread percent value or as Function Select (FS). If SSON# is used, when this pin is pulled high (VDD), the spread is stopped and the frequency is the nominal value without spread. If low (GND), the frequency is the nominal value with the spread.

If FS function is used, the output pins can be programmed for different set of frequencies or spread % as selected by FS. SSCLK value can be any frequency from 3 to 200MHz, but the spread % is the same percent value. REFOUT is the same frequency as the input reference clock or divide by from 2 to 32 without spread. The set of frequencies in Table 1 is given as en example, using 48MHz crystal.
The SL15300 also allows a fan-out of up to 4, meaning that Pins 4, 6, 7 and 8 can be programmed to the same frequencies with or without spread.

FS (Pin-8)	SSCLK1/2 (Pins-6/7)	REFCLK4 (Pin-4)
0	66MHz, +/-2%	48MHz
1	33MHz, +/-2%	24MHz

Table 1. Frequency Selection (FS)

Power Down (PD#) or Output Enable (OE)

The SL15300 Pin-4 can be programmed as either PD# or OE. PD# powers down the entire chip whereas OE only disables the output buffers to Hi-Z.

Absolute Maximum Ratings

Description	Condition	Min	Max	Unit
Supply voltage, VDD		-0.5	4.6	V
All Inputs and Outputs		-0.5	VDD+0.5	V
Ambient Operating Temperature	In operation, C-Grade	0	70	°C
Ambient Operating Temperature	In operation, I-Grade	-40	85	°C
Storage Temperature	No power is applied	-65	150	°C
Junction Temperature	In operation, power is applied	-	125	°C
Soldering Temperature		-	260	°C
ESD Rating (Human Body Model)	JEDEC22-A114D	-4,000	4,000	V
ESD Rating (Charge Device Model)	JEDEC22-C101C	-1,500	1,500	V
ESD Rating (Machine Model)	JEDEC22-A115D	-250	250	V
Latch-up	125°C	-200	200	mA

DC Electrical Characteristics (C-Grade)

Unless otherwise stated VDD= 3.3V+/- 10%, CL=15pF and Ambient Temperature range 0 to +70 Deg C

Description	Symbol	Condition	Min	Typ	Max	Unit
Operating Voltage	VDD	VDD+/-10%	2.97	3.3	3.63	V
Input Low Voltage	VIL	CMOS Level, if Pins 4 and 8 programmed as PD#, OE, SSON# or FS	0	-	0.3VDD	V
Input High Voltage	VIH	CMOS Level, if Pins 4 and 8 programmed as PD#, OE, SSON# or FS.	0.7VDD	-	VDD	V
Output High Voltage	VOH1	IOH=10mA , If Pins 4, 6, 7 and 8 are programmed as SSCLK/REFCLK	VDD-0.5	-	-	V
Output Low Voltage	VOL1	IOL=10mA, If Pins 4, 6, 7 and 8 are programmed as SSCLK/REFCLK	-	-	0.5	V
Input High Current	IIH	VIN=VDD, Pins 4 and 8. If outputs are programmed as PD#, OE, SSON# or FS and no pull-up/down resister used	-10	-	10	µA
Input Low Current	IIL	VIN=GND, Pins 4 and 8. If outputs are programmed as PD#, OE, SSON# or FS and no pull-up/down resister used	-10	-	10	µA
Pull-up or Down Resistors	RPU/D	CMOS Level, if Pins 4 and 8 programmed as PD#, OE, SSON# or FS	100	150	250	kΩ

Operating Supply Current	IDD	FIN=30MHz and all 4 clocks are at 66MHz and +/-2.0% Spread and CL=0	-	7.9	9.4	mA
Standby Current	ISBC	PD#=GND	-	70	90	µA
Output Leakage Current	IOL	Pins 4, 6, 7 and 8 if programmed as SSCLK or REFOUT	-10	-	10	µA
Programmable Input Capacitance at Pins 2 and 3	PCin PCout	Minimum setting value	-	7	-	pF
		Maximum setting value	-	38	-	pF
		Resolution (programming steps)	-	0.5	-	pF
Input Capacitance	CIN2	Pins 4 and 8 if programmed as PD#, OE, SSON or FS	-	4	6	pF
Load Capacitance	CL	Pins 4, 6, 7 and 8 If programmed as SSCLK or REFCLK	-	-	15	pF

AC Electrical Characteristics (C-Grade)

Unless otherwise stated VDD= 3.3V+/- 10%, CL=15pF and Ambient Temperature range 0 to +70 Deg C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Frequency Range	FIN1	Crystal or Ceramic Resonator	8	-	48	MHz
Input Frequency Range	FIN2	External Clock	3	-	166	MHz
Output Frequency Range	FOUT1	SSCLK	3	-	200	MHz
Output Frequency Range	FOUT2	REFCLK, crystal or resonator input	0.25	-	48	MHz
Output Frequency Range	FOUT3	REFCLK, clock input	0.25	-	166	MHz
Output Duty Cycle	DC1	SSCLK	45	50	55	%
Output Duty Cycle	DC2	REFCLK , Xtal input	45	50	55	%
Output Duty Cycle	DC3	REFCLK, clock input	40	50	60	%
Input Duty Cycle	DCIN	Clock Input, Pin 3	40	50	60	%
Output Rise/Fall Time	tr/f1	Programmable, VDD=3.3V, CL=15pF, 20 to 80% of VDD	-	4.00	4.80	ns
Output Rise/Fall Time	tr/f2	Programmable, VDD=3.3V, CL=15pF, 20 to 80% of VDD	-	2.00	2.40	ns
Output Rise/Fall Time	tr/f3	Programmable, VDD=3.3V, CL=15pF, 20 to 80% of VDD	-	1.40	1.70	ns
Output Rise/Fall Time	tr/f4	Programmable, VDD=3.3V, CL=15pF, 20 to 80% of VDD	-	1.10	1.35	ns
Output Rise/Fall Time	tr/f5	Programmable, VDD=3.3V, CL=15pF, 20 to 80% of VDD	-	0.85	1.00	ns
Output Rise/Fall Time	tr/f6	Programmable, VDD=3.3V, CL=15pF, 20 to 80% of VDD	-	0.70	0.85	ns
Output Rise/Fall Time	tr/f7	Programmable, VDD=3.3V, CL=15pF, 20 to 80% of VDD	-	0.55	0.67	ns

Cycle-to-Cycle Jitter (SSCLK – Pins 4/6/7/8)	CCJ1	FIN=30MHz, all 4 clocks are at 33MHz, +/-2.0% Spread. CL=15pF	-	TBD	TBD	ps
Cycle-to-Cycle Jitter (SSCLK – Pins 4/6/7/8)	CCJ2	FIN=30MHz, all 4 clocks are at 33MHz, +/-2.0% Spread. CL=15pF	-	TBD	TBD	ps
Power-down Time	tPD	Time from PD# falling edge to Hi-Z at outputs (Asynchronous)	-	150	350	ns
Power-up Time (Crystal or Clock)	tPU	Time from PD# rising edge to valid frequency at outputs (Asynchronous)	-	3.5	5.0	ms
Power Supply Ramp Time	tPSR	Time for VDD reaching minimum specified value and monolithic power supply ramp	-	-	12	ms
Output Enable Time	tOE	Time from OE falling edge to Hi-Z at outputs (Asynchronous)	-	180	350	ns
Output Disable Time	tOD	Time from OE falling edge to Hi-Z at outputs (Asynchronous)	-	180	350	ns
Spread Percent Range	SPR-1	Center Spread, SSCLK-1/2/3/4	+/-0.125	-	+/-2.5	%
Spread Percent Range	SPR-2	Down Spread, SSCLK-1/2/3/4	-5.0	-	-0.25	%
Spread Percent Variation	ΔSS%	Variation of programmed Spread %	-15	-	15	%
Modulation Frequency	FMOD	Programmable, 31.5 kHz standard	25	31.5	120	kHz

DC Electrical Characteristics (C-Grade)

Unless otherwise stated VDD= 2.5V+/- 10%, CL=15pF and Ambient Temperature range 0 to +70 Deg C

Description	Symbol	Condition	Min	Typ	Max	Unit
Operating Voltage	VDD	VDD+/-10%	2.25	2.5	2.75	V
Input Low Voltage	VIL	CMOS Level, if Pins 4 and 8 programmed as PD#, OE, SSON# or FS	0	-	0.3VDD	V
Input High Voltage	VIH	CMOS Level, if Pins 4 and 8 programmed as PD#, OE, SSON# or FS.	0.7VDD	-	VDD	V
Output High Voltage	VOH1	IOH=10mA , If Pins 4, 6, 7 and 8 are programmed as SSCLK/REFCLK	VDD-0.4	-	-	V
Output Low Voltage	VOL1	IOL=10mA, If Pins 4, 6, 7 and 8 are programmed as SSCLK/REFCLK	-	-	0.4	V
Input High Current	IIH	VIN=VDD, Pins 4 and 8. If outputs are programmed as PD#, OE, SSON# or FS and no pull-up/down resister used	-10	-	10	µA
Input Low Current	IIL	VIN=GND, Pins 4 and 8. If outputs are programmed as PD#, OE, SSON# or FS and no pull-up/down resister used	-10	-	10	µA

Pull-up or Down Resistors	RPU/D	CMOS Level, if Pins 4 and 8 programmed as PD#, OE, SSON# or FS	100	150	250	kΩ
Operating Supply Current	IDD	FIN=30MHz and all 4 clocks are at 66MHz and +/-2.0% Spread and CL=0	-	7.0	8.3	mA
Standby Current	ISBC	PD#=GND	-	70	90	µA
Output Leakage Current	IOL	Pins 4, 6, 7 and 8. If programmed as SSCLK or REFCLK	-10	-	10	µA
Programmable Input Capacitance at Pins 2 and 3	PCin PCout	Minimum setting value	-	7	-	pF
		Maximum setting value	-	38	-	pF
		Resolution (programming steps)	-	0.5	-	pF
Input Capacitance	CIN2	Pins 4 and 8 If programmed as PD#, OE, SSON or FS	-	4	6	pF
Load Capacitance	CL	Pins 4, 6, 7 and 8. If programmed as SSCLK or REFCLK	-	-	15	pF

AC Electrical Characteristics (C-Grade)

Unless otherwise stated VDD= 2.5V+/- 10%, CL=15pF and Ambient Temperature range 0 to +70 Deg C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Frequency Range	FIN1	Crystal or Ceramic Resonator	8	-	48	MHz
Input Frequency Range	FIN2	External Clock	3	-	166	MHz
Output Frequency Range	FOUT1	SSCLK	3	-	200	MHz
Output Frequency Range	FOUT2	REFCLK, crystal or resonator input	0.25	-	48	MHz
Output Frequency Range	FOUT3	REFCLK, clock input	0.25	-	166	MHz
Output Duty Cycle	DC1	SSCLK	45	50	55	%
Output Duty Cycle	DC2	REFCLK, Xtal input	45	50	55	%
Output Duty Cycle	DC3	REFCLK, clock input	40	50	60	%
Input Duty Cycle	DCIN	Clock Input, Pin 3	40	50	60	%
Output Rise/Fall Time	tr/f1	Programmable, VDD=2.5 CL=15pF, 20 to 80% of VDD	-	4.80	5.80	ns
Output Rise/Fall Time	tr/f2	Programmable, VDD=2.5 CL=15pF, 20 to 80% of VDD	-	2.60	3.10	ns
Output Rise/Fall Time	tr/f3	Programmable, VDD=2.5 CL=15pF, 20 to 80% of VDD	-	1.80	2.20	ns
Output Rise/Fall Time	tr/f4	Programmable, VDD=2.5 CL=15pF, 20 to 80% of VDD	-	1.40	1.70	ns

Output Rise/Fall Time	tr/f5	Programmable, VDD=2.5 CL=15pF, 20 to 80% of VDD	-	1.10	1.35	ns
Output Rise/Fall Time	tr/f6	Programmable, VDD=2.5 CL=15pF, 20 to 80% of VDD	-	0.90	1.10	ns
Output Rise/Fall Time	tr/f7	Programmable, VDD=2.5 CL=15pF, 20 to 80% of VDD	-	0.70	0.85	ns
Cycle-to-Cycle Jitter (SSCLK – Pins 4/6/7/8)	CCJ1	FIN=30MHz, all 4 clocks are at 33MHz, +/-2.0% Spread. CL=15pF	-	TBD	TBD	ps
Cycle-to-Cycle Jitter (SSCLK – Pins 4/6/7/8)	CCJ2	FIN=30MHz, all 4 clocks are at 33MHz, +/-2.0% Spread. CL=15pF	-	TBD	TBD	ps
Power-down Time	tPD	Time from PD# falling edge to Hi-Z at outputs (Asynchronous)	-	150	350	ns
Power-up Time (Crystal or Clock)	tPU	Time from PD# rising edge to valid frequency at outputs (Asynchronous)	-	3.5	5.0	ms
Power Supply Ramp Time	tPSR	Time for VDD reaching minimum specified value and monolithic power supply ramp	-	-	12	ms
Output Enable Time	tOE	Time from OE falling edge to Hi-Z at outputs (Asynchronous)	-	180	350	ns
Output Disable Time	tOD	Time from OE falling edge to Hi-Z at outputs (Asynchronous)	-	180	350	ns
Spread Percent Range	SPR-1	Center Spread, SSCLK-1/2/3/4	+/-0.125	-	+/-2.5	%
Spread Percent Range	SPR-2	Down Spread, SSCLK-1/2/3/4	-5.0	-	-0.25	%
Spread Percent Variation	ΔSS%	Variation of programmed Spread %	-15	-	15	%
Modulation Frequency	FMOD	Programmable, 31.5 kHz standard	25	31.5	120	kHz

DC Electrical Characteristics (I-Grade)

Unless otherwise stated VDD= 3.3V+/- 10%, CL=15pF and Ambient Temperature range -40 to +85 Deg C

Description	Symbol	Condition	Min	Typ	Max	Unit
Operating Voltage	VDD	VDD+/-10%	2.97	3.3	3.63	V
Input Low Voltage	VIL	CMOS Level, if Pins 4 and 8 programmed as PD#, OE, SSON# or FS	0	-	0.3VDD	V
Input High Voltage	VIH	CMOS Level, if Pins 4 and 8 programmed as PD#, OE, SSON# or FS.	0.7VDD	-	VDD	V
Output High Voltage	VOH1	IOH=10mA , If Pins 4, 6, 7 and 8 are programmed as SSCLK/REFCLK	VDD-0.5	-	-	V
Output Low Voltage	VOL1	IOL=10mA, If Pins 4, 6, 7 and 8 are programmed as SSCLK/REFCLK	-	-	0.5	V

Input High Current	IIH	VIN=VDD, Pins 4 and 8. If outputs are programmed as PD#, OE, SSON# or FS and no pull-up/down resister used	-15	-	15	µA
Input Low Current	IIL	VIN=GND, Pins 4 and 8. If outputs are programmed as PD#, OE, SSON# or FS and no pull-up/down resister used	-15	-	15	µA
Pull-up or Down Resistors	RPU/D	CMOS Level, if Pins 4 and 8 programmed as PD#, OE, SSON# or FS	100	150	250	kΩ
Operating Supply Current	IDD	FIN=30MHz and all 4 clocks are at 66MHz and +/-2.0% Spread and CL=0	-	8.2	9.8	mA
Standby Current	ISBC	PD#=GND	-	80	100	µA
Output Leakage Current	IOL	Pins 4, 6, 7 and 8. If programmed as SSCLK or REFCLK	-10	-	10	µA
Programmable Input Capacitance at Pins 2 and 3	PCin PCout	Minimum setting value	-	7	-	pF
		Maximum setting value	-	38	-	pF
		Resolution (programming steps)	-	0.5	-	pF
Input Capacitance	CIN2	Pins 4 and 8 If programmed as PD#, OE, SSON or FS	-	4	6	pF
Load Capacitance	CL	Pins 4, 6, 7 and 8. If programmed as SSCLK or REFCLK	-	-	15	pF

AC Electrical Characteristics (I-Grade)

Unless otherwise stated VDD= 3.3V+/- 10%, CL=15pF and Ambient Temperature range -40 to +85 Deg C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Frequency Range	FIN1	Crystal or Ceramic Resonator	8	-	48	MHz
Input Frequency Range	FIN2	External Clock	3	-	166	MHz
Output Frequency Range	FOUT1	SSCLK	3	-	200	MHz
Output Frequency Range	FOUT2	REFCLK, crystal or resonator input	0.25	-	48	MHz
Output Frequency Range	FOUT3	REFCLK, clock input	0.25	-	166	MHz
Output Duty Cycle	DC1	SSCLK	45	50	55	%
Output Duty Cycle	DC2	REFCLK, Xtal input	45	50	55	%
Output Duty Cycle	DC3	REFCLK, clock input	40	50	60	%
Input Duty Cycle	DCIN	Clock Input, Pin 3	40	50	60	%
Output Rise/Fall Time	tr/f1	Programmable, VDD=3.3V, CL=15pF, 20 to 80% of VDD	-	4.00	4.80	ns

Output Rise/Fall Time	tr/f2	Programmable, VDD=3.3V, CL=15pF, 20 to 80% of VDD	-	2.00	2.40	ns
Output Rise/Fall Time	tr/f3	Programmable, VDD=3.3V, CL=15pF, 20 to 80% of VDD	-	1.40	1.70	ns
Output Rise/Fall Time	tr/f4	Programmable, VDD=3.3V, CL=15pF, 20 to 80% of VDD	-	1.10	1.35	ns
Output Rise/Fall Time	tr/f5	Programmable, VDD=3.3V, CL=15pF, 20 to 80% of VDD	-	0.85	1.00	ns
Output Rise/Fall Time	tr/f6	Programmable, VDD=3.3V, CL=15pF, 20 to 80% of VDD	-	0.70	0.85	ns
Output Rise/Fall Time	tr/f7	Programmable, VDD=3.3V, CL=15pF, 20 to 80% of VDD	-	0.55	0.67	ns
Cycle-to-Cycle Jitter (SSCLK – Pins 4/6/7/8)	CCJ1	FIN=30MHz, all 4 clocks are at 33MHz, +/-2.0% Spread. CL=15pF	-	TBD	TBD	ps
Cycle-to-Cycle Jitter (SSCLK – Pins4/6/7/8)	CCJ2	FIN=30MHz, all 4 clocks are at 66MHz, +/-2.0% Spread. CL=15pF	-	TBD	TBD	ps
Power-down Time	tPD	Time from PD# falling edge to Hi-Z at outputs (Asynchronous)	-	150	350	ns
Power-up Time (Crystal or Clock)	tPU	Time from PD# rising edge to valid frequency at outputs (Asynchronous)	-	3.5	5.0	ms
Power Supply Ramp Time	tPSR	Time for VDD reaching minimum specified value and monolithic power supply ramp	-	-	12	ms
Output Enable Time	tOE	Time from OE falling edge to Hi-Z at outputs (Asynchronous)	-	180	350	ns
Output Disable Time	tOD	Time from OE falling edge to Hi-Z at outputs (Asynchronous)	-	180	350	ns
Spread Percent Range	SPR-1	Center Spread, SSCLK-1/2/3/4	+/-0.125	-	+/-2.5	%
Spread Percent Range	SPR-2	Down Spread, SSCLK-1/2/3/4	-5.0	-	-0.25	%
Spread Percent Variation	ΔSS%	Variation of programmed Spread %	-20	-	20	%
Modulation Frequency	FMOD	Programmable, 31.5 kHz standard	25	31.5	120	kHz

DC Electrical Characteristics (I-Grade)

Unless otherwise stated VDD= 2.5V+/- 10%, CL=15pF and Ambient Temperature range -40 to +85 Deg C

Description	Symbol	Condition	Min	Typ	Max	Unit
Operating Voltage	VDD	VDD+/-10%	2.25	2.5	2.75	V
Input Low Voltage	VIL	CMOS Level, if Pins 4 and 8 programmed as PD#, OE, SSON# or FS	0	-	0.3VDD	V
Input High Voltage	VIH	CMOS Level, if Pins 4 and 8 programmed as PD#, OE, SSON# or FS.	0.7VDD	-	VDD	V

Output High Voltage	VOH1	IOH=10mA , If Pins 4, 6, 7 and 8 are programmed as SSCLK/REFCLK	VDD-0.4	-	-	V
Output Low Voltage	VOL1	IOL=10mA, If Pins 4, 6, 7 and 8 are programmed as SSCLK/REFCLK	-	-	0.4	V
Input High Current	IIH	VIN=VDD, Pins 4 and 8. If outputs are programmed as PD#, OE, SSON# or FS and no pull-up/down resister used	-15	-	15	µA
Input Low Current	IIL	VIN=GND, Pins 4 and 8. If outputs are programmed as PD#, OE, SSON# or FS and no pull-up/down resister used	-15	-	15	µA
Pull-up or Down Resistors	RPU/D	CMOS Level, if Pins 4 and 8 programmed as PD#, OE, SSON# or FS	100	150	250	kΩ
Operating Supply Current	IDD	FIN=30MHz and all 4 clocks are at 66MHz and +/-2.0% Spread and CL=0	-	7.2	8.6	mA
Standby Current	ISBC	PD#=GND	-	80	100	µA
Output Leakage Current	IOL	Pins 4, 6, 7 and 8. If programmed as SSCLK or REFCLK	-10	-	10	µA
Programmable Input Capacitance at Pins 2 and 3	PCin PCout	Minimum setting value	-	7	-	pF
		Maximum setting value	-	38	-	pF
		Resolution (programming steps)	-	0.5	-	pF
Input Capacitance	CIN2	Pins 4 and 8 If programmed as PD#, OE, SSON or FS	-	4	6	pF
Load Capacitance	CL	Pins 4, 6, 7 and 8. If programmed as SSCLK or REFCLK	-	-	15	pF

AC Electrical Characteristics (I-Grade)

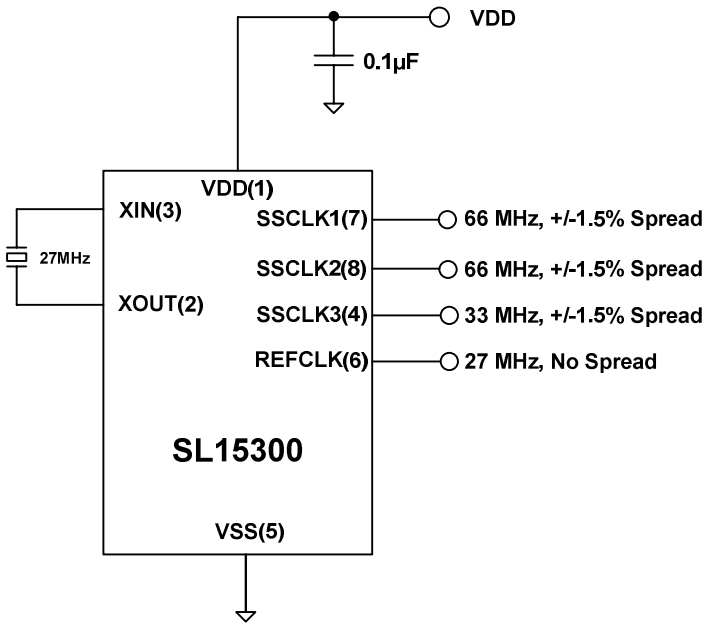
Unless otherwise stated VDD= 2.5V+/- 10%, CL=15pF and Ambient Temperature range -40 to +85 Deg C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Frequency Range	FIN1	Crystal or Ceramic Resonator	8	-	48	MHz
Input Frequency Range	FIN2	External Clock	3	-	166	MHz
Output Frequency Range	FOUT1	SSCLK	3	-	200	MHz
Output Frequency Range	FOUT2	REFCLK, crystal or resonator input	0.25	-	48	MHz
Output Frequency Range	FOUT3	REFCLK, clock input	0.25	-	166	MHz
Output Duty Cycle	DC1	SSCLK	45	50	55	%

Output Duty Cycle	DC2	REFCLK, Xtal input	45	50	55	%
Output Duty Cycle	DC3	REFCLK, clock input	40	50	60	%
Input Duty Cycle	DCIN	Clock Input, Pin 3	40	50	60	%
Output Rise/Fall Time	tr/f1	Programmable, VDD=2.5 CL=15pF, 20 to 80% of VDD	-	4.80	5.80	ns
Output Rise/Fall Time	tr/f2	Programmable, VDD=2.5 CL=15pF, 20 to 80% of VDD	-	2.60	3.10	ns
Output Rise/Fall Time	tr/f3	Programmable, VDD=2.5 CL=15pF, 20 to 80% of VDD	-	1.80	2.20	ns
Output Rise/Fall Time	tr/f4	Programmable, VDD=2.5 CL=15pF, 20 to 80% of VDD	-	1.40	1.70	ns
Output Rise/Fall Time	tr/f5	Programmable, VDD=2.5 CL=15pF, 20 to 80% of VDD	-	1.10	1.35	ns
Output Rise/Fall Time	tr/f6	Programmable, VDD=2.5 CL=15pF, 20 to 80% of VDD	-	0.90	1.10	ns
Output Rise/Fall Time	tr/f7	Programmable, VDD=2.5 CL=15pF, 20 to 80% of VDD	-	0.70	0.85	ns
Cycle-to-Cycle Jitter (SSCLK – Pins 4/6/7/8)	CCJ1	FIN=30MHz, all 4 clocks are at 33MHz, +/-2.0% Spread. CL=15pF	-	TBD	TBD	ps
Cycle-to-Cycle Jitter (SSCLK – Pins 4/6/7/8)	CCJ2	FIN=30MHz, all 4 clocks are at 33MHz, +/-2.0% Spread. CL=15pF	-	TBD	TBD	ps
Power-down Time	tPD	Time from PD# falling edge to Hi-Z at outputs (Asynchronous)	-	180	350	ns
Power-up Time (Crystal or Clock)	tPU	Time from PD# rising edge to valid frequency at outputs (Asynchronous)	-	3.5	5.0	ms
Power Supply Ramp Time	tPSR	Time for VDD reaching minimum specified value and monolithic power supply ramp	-	-	12	ms
Output Enable Time	tOE	Time from OE falling edge to Hi-Z at outputs (Asynchronous)	-	180	350	ns
Output Disable Time	tOD	Time from OE falling edge to Hi-Z at outputs (Asynchronous)	-	180	350	ns
Spread Percent Range	SPR-1	Center Spread, SSCLK-1/2/3/4	+/-0.125	-	+/-2.5	%
Spread Percent Range	SPR-2	Down Spread, SSCLK-1/2/3/4	-5.0	-	-0.25	%
Spread Percent Variation	ΔSS%	Variation of programmed Spread %	-20	-	20	%
Modulation Frequency	FMOD	Programmable, 31.5 kHz standard	25	31.5	120	kHz

External Components & Design Considerations

Typical Application Schematic



Comments and Recommendations

Decoupling Capacitor: A decoupling capacitor of 0.1µF must be used between VDD and VSS on the pins 1 and 5. Place the capacitor on the component side of the PCB as close to the VDD pin as possible. The PCB trace to the VDD pin and to the GND via should be kept as short as possible Do not use vias between the decoupling capacitor and the VDD pin.

Series Termination Resistor: A series termination resistor is recommended if the distance between the outputs (SSCLK or REFCLK pins) and the load is over 1 ½ inch. The nominal impedance of the SSCLK output is about 30 Ω. Use 20 Ω resistor in series with the output to terminate 50Ω trace impedance and place 20 Ω resistor as close to the SSCLK output as possible.

Crystal and Crystal Load: Use only parallel resonant fundamental crystals. DO NOT USE higher overtone crystals. To meet the crystal initial accuracy specification (in ppm); the internal on-chip programmable capacitors PCin and PCout must be programmed to match the crystal load requirement. These values are given by the formula below:

$$PCin(pF) = PCout(pF) = [(CL(pF) - Cp(pF)/2)] \times 2$$

Where CL is crystal load capacitor as given by the crystal datasheet and Cp(pF) is the compensation factor for the total parasitic capacitance at XIN or XOUT pin including PCB related parasitic capacitance.

As an example; if a crystal with CL=18pF is used and Cp=4pF, by using the above formula, PCin=PCout=[(18-(4/2)] x 2 = 32pF. Programming PCin and PCout to 32pF assures that this crystal sees an equivalent load of 18pF and no other external crystal load capacitor is needed. Deviating from the crystal load specification could cause an increase in frequency accuracy in ppm. Refer to the Table 5 for the recommended crystal specifications.

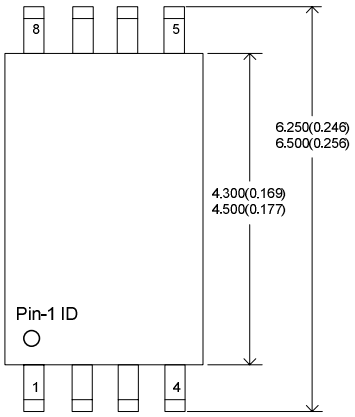
Recommended External Crystal Specifications

Parameter	Description	Min	Typ	Max	Unit	Comments
FNOM	Nominal Crystal Frequency Range	8	-	48	MHz	Fundamental Mode – AT Cut
CL	Nominal Crystal Load	6	12	18	pF	Load for +/-0 ppm Fo resonance value
R1,1	Equivalent Series Resistance	20	40	100	Ohm	F-Range: 8.0 to 12.999 MHz
R1,2	Equivalent Series Resistance	12.5	25	60	Ohm	F-Range: 13.0 to 19.999 MHz
R1,3	Equivalent Series Resistance	10	20	50	Ohm	F-Range: 20.0 to 48.000 MHz
DL1,1	Crystal Drive Level	-	-	200	µW	F-Range: 8.0 to 19.999 MHz
DL1,2	Crystal Drive Level	-	-	150	µW	F-Range: 20.0 to 48.000 MHz
Co1	Shunt Capacitance	-	4	5.4	pF	SMD Xtals
Co2	Shunt Capacitance	-	5	7.2	pF	Through Hole (Leaded) Xtals

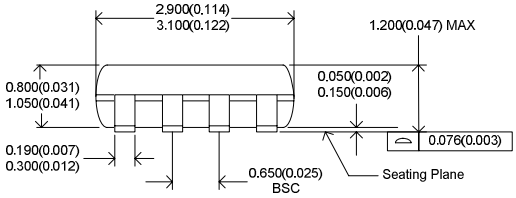
Table 5. Recommended Crystal Specifications

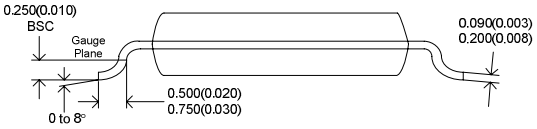
Package Outline and Package Dimensions

8-Pin TSSOP Package (173 Mil)



Dimensions are in milimeters (inches)
Top line: (MIN) and Bottom line: (Max)





Thermal Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Thermal Resistance Junction to Ambient	θ JA	Still air	-	110	-	°C/W
	θ JA	1m/s air flow	-	100	-	°C/W
	θ JA	3m/s air flow	-	80	-	°C/W
Thermal Resistance Junction to Case	θ JC	Independent of air flow	-	35	-	°C/W

Ordering Information [1]

Ordering Number [2]	Marking	Shipping Package	Package	Temperature
SL15300ZC-XXX	SL15300ZC-XXX	Tube	8-pin TSSOP	0 to 70°C
SL15300ZC-XXXT	SL15300ZC-XXX	Tape and Reel	8-pin TSSOP	0 to 70°C
SL15300ZI-XXX	SL15300ZI-XXX	Tube	8-pin TSSOP	-40 to 85°C
SL15300ZI-XXXT	SL15300ZI-XXX	Tape and Reel	8-pin TSSOP	-40 to 85°C

Notes:

1. All SLI products are RoHS compliant.
2. "XXX" is "Dash" number and will be assigned by SLI for final programmed samples or production units based on the each customer programming requirements.