iC-MD RS-422 QUADRATURE ENCODER RECEIVER/COUNTER WITH SPI AND BiSS
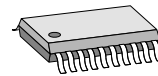
preliminary

iC-Haus

FEATURES

- Configurable quadrature 3-channel binary counter of 16, 24, 32 and 48 bit (TTL, RS422 or LVDS input)
- Fast RS422 12 V receiver for differential A/B/Z encoder signal
- Count frequency to 40 MHz
- Monitoring of A/B phase logic with error message
- Evaluation of distance-coded reference marks
- Pin-triggered touch-probe function with selectable hi/lo edge sensitivity
- Error and warning signal generation
- Operation from 3.3 V to 5 V
- Configuration via bus capable SPI and *BiSS* Interface
- Two actuator output signals
- Default operation mode permits plug & play without programming
- 3 Channel 16 bit counting (TTL: A/B)
- 2 Channel 16, 24 or 16+32 bit counting (TTL: AP/AN/BP, BN/CP/CN)
- 1 Channel 16, 24, 32 or 48 bit counting (TTL: AP/AN/BP or RS422, LVDS: A/B/C differential)
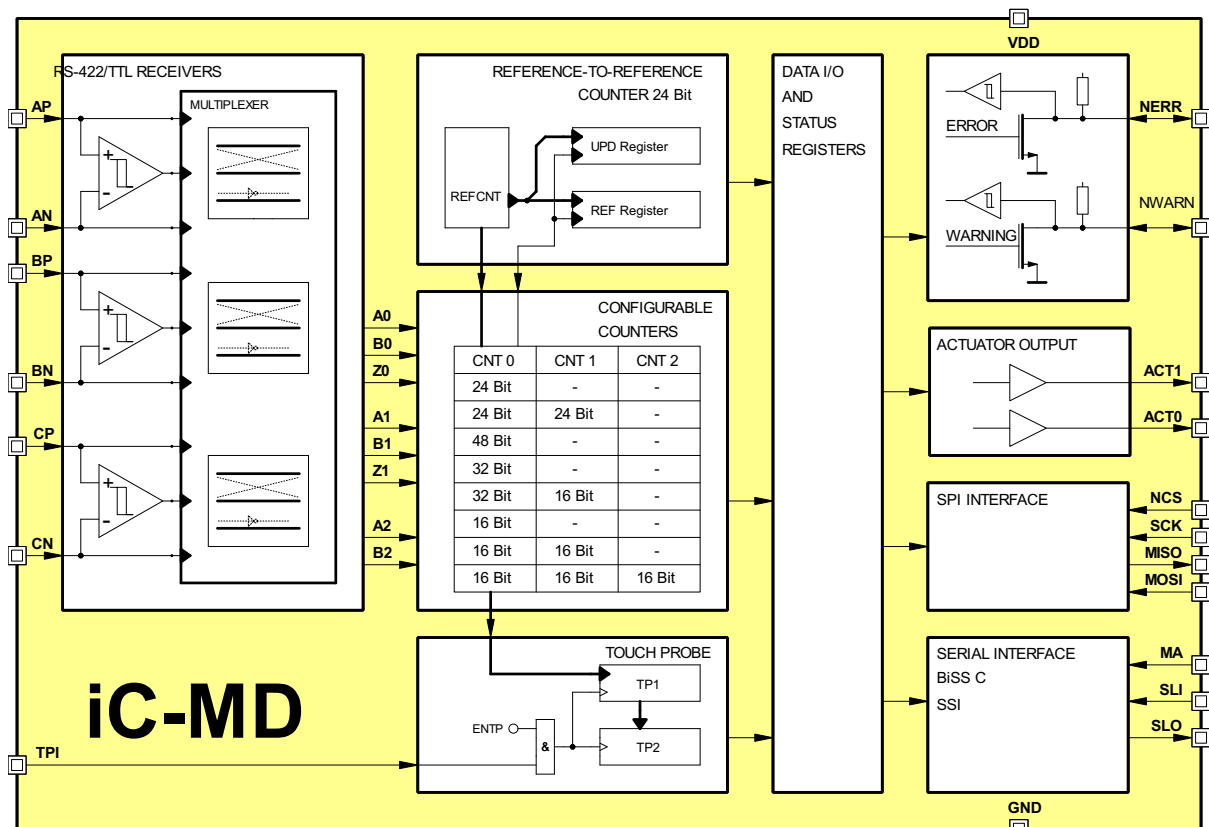
APPLICATIONS

PLC interface to linear scales, rotary encoders, digital gauges
Motion control

PACKAGES

TSSOP 20

BLOCK DIAGRAM

iC-MD RS-422 QUADRATURE ENCODER RECEIVER/COUNTER WITH SPI AND BiSS

preliminary

DESCRIPTION

iC-MD evaluates incremental encoder signals with A, B and index tracks from up to three encoders.

After power-on the iC-MD has all the RAM bits at 0 as default configuration, that means one 24 bit counter configured, and differential inputs. The device can be programmed via the SPI interface or BiSS Interface.

The 48 bit counter can be configured as up to three counters with variable counter depths of 16, 24, 32 or 48 bits, but the sum of bits of all the configured counters can not be higher than 48 bits. Some of the possible configurations are 1x48 bit, 2x24 bit, 3x16 bit, 1x32 + 1x16 bit. Each edge of the synchronized encoder signal counts (fourfold edge evaluation).

An additional 24bit counter REF counter is used to store the distance (number of pulses) between the first two index pulses after power-on and the distance between every last two index pulses in UPD register.

An event at the input pin TPI (configurable as rising, falling or both edges) loads the register TP1 with the actual value of the counter 0, and shift the old value of TP1 in register TP2. This registers can also be loads through the instruction bit TP, via SPI or BiSS (Register communication).

Two bidirectional ports are used as error and warning output (low active) and can be pulled down from outside to signals an external error or external warning. This external error and warning are internally latched in the status registers.
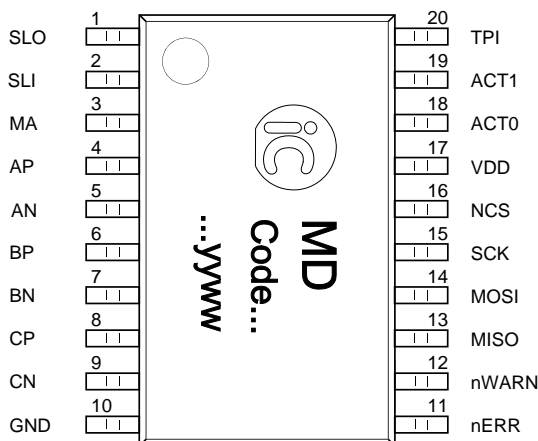
A set of status registers monitor the status of the counter, TP1, TP2, REF, UPD, power on and external error and warning pins.

The BiSS Interface reads out the counter and registers TP1, TP2 and UPD as Sensor data. REF register is read via BiSS register communication.

PACKAGES

PIN CONFIGURATION
TSSOP20 4.4 mm, lead pitch 0.65 mm

PIN FUNCTIONS

No.	Name	Function
1	SLO	BiSS/SSI Interface, data output
2	SLI	BiSS/SSI Interface, data input
3	MA	BiSS/SSI Interface, clock input
4	AP	Signal Input (CNT0 / CNT0)
5	AN	Signal Input (CNT0 / CNT0)
6	BP	Signal Input (CNT0 / CNT1)
7	BN	Signal Input (CNT1 / CNT1)
8	CP	Signal Input (CNT1 / CNT2)
9	CN	Signal Input (CNT1 / CNT2)
10	GND	Ground
11	NERR	Error Message Output (low active) / System Error Message Input
12	NWARN	Warning Message Output (low active) / System Warning Message Input
13	MISO	SPI Interface, data ouput
14	MOSI	SPI Interface, data input
15	SCK	SPI Interface, clock input
16	NCS	SPI Interface, chip select (low active)
17	VDD	3.0 . . . 5.5 VSupply Voltage
18	ACT0	Actuator Output 0
19	ACT1	Actuator Output 1
20	TPI	Touch Probe Input

ABSOLUTE MAXIMUM RATINGS

These ratings do not imply operating conditions; functional operation is not guaranteed. Beyond these ratings device damage may occur.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	V()	Voltage at VDD		-0.3	7	V
G002	V()	Voltage at MA, SLI, NERR, NWARN, NCS, SCK, MOSI, TPI		-0.3	7	V
G003	I()	Current in MA, SLI, NERR, NWARN, NCS, SCK, MOSI, TPI		-4	4	mA
G004	V()	Voltage at AP, AN, BP, BN, CP, CN		-7	7	V
G005	I()	Current in AP, AN, BP, BN, CP, CN		-20	20	mA
G006	Vd()	ESD Susceptibilty at all pins	HBM 100 pF discharged through 1.5 kΩ		2	kV
G007	Tj	Junction Temperature		-40	150	°C
G008	Ts	Storage Temperature Range		-40	150	°C

THERMAL DATA

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range		-40		125	°C

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 3 . . . 5.5 V, Tj = -40 . . . 125 °C, unless otherwise noted.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
General							
001	VDD	Voltage Supply VDD		3		5.5	V
002	I(VDD)	Supply Current in VDD	TTL input configuration, 48 bits counter 10 MHz signal in AP (0° phase) and AN (90° phase), BP, BN, CP and CN to GND			15	mA
003	Vc()hi	Clamp Voltage hi	Vc()hi = V() - VDD, I() = 1 mA	0.4		1.5	V
004	Vc()lo	Clamp Voltage lo	Vc()hi = V() - VDD, I() = 10 mA	-1.5		-0.25	V
Digital Inputs: MA, SLI, SCK, MOSI, NCS, TPI							
101	Vt()hi	Input Threshold Voltage hi				2	V
102	Vt()lo	Input Threshold Voltage lo	VDD = 4.5 . . . 5.5 V VDD = 3 . . . 5.5 V	0.8 0.75			V V
103	Vt()hys	Input Hysteresis		150	250		mV
104	Ipd()	Input Pull-down Current at SCK, MOSI, TPI	V() = 1 V . . . VDD	2	30	75	µA
105	Ipu()	Input Pull-Up Current at NCS, MA	V() = 0 V . . . VDD - 1 V	-75	-30	-2	µA
106	fclk(MA)	Permissible Clock Frequency at MA	NBISS = 1 (SSI protocol) NBISS = 0 (*BiSS* protocol)			4 10	MHz MHz
107	Voc()	Pin Open Voltage at SLI		42	46.5	51	%VDD
108	Ri()	Internal Resistance at SLI	Referenced to VDD Referenced to GND	70 40		170 110	kΩ kΩ
109	fclk(SCK)	Permissible Clock Frequency at SCK				10	MHz
Bidirectional Pins: NWARN, NERR							
201	Ipu()	Pull-Up Current	V() = 0 V . . . VDD - 1 V	-750	-100	-10	µA
202	Vt()hi	Input Threshold Voltage hi				2	V
203	Vt()lo	Input Threshold Voltage lo	VDD = 4.5 . . . 5.5 V VDD = 3 . . . 5.5 V	0.8 0.75			V V
204	Vt()hys	Input Hysteresis		150	250		mV
205	Vs()lo	Saturation Voltage lo	I() = 4 mA			450	mV
206	Isc()lo	Short-Circuit Current lo	V() = 0 V . . . VDD	4		100	mA
ABZ Counter							
301	R()	Counter Resolution				48	bit
302	fcnt()	Permissible Count Frequency				40	MHz
303	PHab2	Permissible A/B Phase Distance	edge A vs. edge B and vice versa TTL=1 TTL=0, LVDS=X	5 13			ns ns
Power-Down Reset and Oscillator							
601	VDDon	Power-On Supply Voltage				2.9	V
602	VDDoff	Power-Down Voltage		2.1			V
603	VDDhys	Power-On Hysteresis	VDDon - VDDoff	35	100		mV
604	Frq(CLK)	Internal Oscillator Frequency		1.4		5.3	MHz
Digital Outputs: SLO, MISO, ACT0, ACT1							
701	Vs()hi	Saturation Voltage hi	Vs()hi = VDD - V(), I() = -4 mA			450	mV
702	Vs()lo	Saturation Voltage lo	I() = 4 mA			450	mV
703	Isc()hi	Short-Circuit Current hi	V() = 0 . . . VDD	-115			mA
704	Isc()lo	Short-Circuit Current lo	V() = 0 . . . VDD			100	mA

iC-MD RS-422 QUADRATURE ENCODER RECEIVER/COUNTER WITH SPI AND BiSS

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 3 . . . 5.5 V, Tj = -40 . . . 125 °C, unless otherwise noted.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
RS-422 Configuration: Differential Inputs AP, AN, BP, BN, CP, CN							
A01	Vcm()	Common Mode Voltage Range	TTL = 0, LVDS = 0 VDD = 4.5 . . . 5.5 V VDD = 3 . . . 5.5 V	0 0		3 1.5	V V
A02	Vd()	Differential Input Threshold Voltage	TTL = 0, LVDS = 0, V() = V(AP) - V(AN) V() = V(BP) - V(BN) V() = V(CP) - V(CN)	-300		300	mV
A03	Vhys()	Differential Input Hysteresis	TTL = 0, LVDS = 0, Vhys() = Vth()hi-Vth()lo (guaranteed by design)	2.5		10	mV
TTL Configuration: Input AP, AN, BP, BN, CP, CN							
B01	Vt()hi	Input Threshold Voltage hi at AP, AN, BP, BN, CP, CN	TTL = 1, LVDS = 0			2	V
B02	Vt()lo	Input Threshold Voltage lo at AP, AN, BP, BN, CP, CN	TTL = 1, LVDS = 0	0.8			V
B03	Vt()hys	Input Hysteresis at AP, AN, BP, BN, CP, CN	TTL = 1, LVDS = 0	150	300		mV
B04	Rpd()	Pull-Down Resistor	TTL = 1, LVDS = 0	35	50	65	kΩ
LVDS Configuration: Differential Inputs AP, AN, BP, BN, CP, CN							
C01	Vin()	Input Voltage Range	TTL = 0, LVDS = 1 VDD = 4.5 . . . 5.5 V VDD = 3 . . . 5.5 V	0.8 0.8		3 1.5	V V
C02	Vd()	Differential Input Threshold Voltage	TTL = 0, LVDS = 1 V() = V(AP)-V(AN) V() = V(BP)-V(BN) V() = V(CP)-V(CN)	-200		200	mV
C03	Vhys()	Differential Input Hysteresis	TTL = 0, LVDS = 1 Vhys() = Vth()hi-Vth()lo (guaranteed by design)	1.2		8	mV

OPERATING REQUIREMENTS: SPI Interface

Operating Conditions: VDD = 3 . . . 5.5 V, Tj = -40 . . . 125 °C, unless otherwise noted.

| Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
SPI Interface						
I001	tsCCL	Setup Time: NCS hi → lo before SCK lo → hi		15		ns
I002	tsDCL	Setup Time: MOSI stable before SCK lo → hi		20		ns
I003	thDCL	Hold Time: MOSI stable after SCK lo → hi		0		ns
I004	tCLh	Signal Duration SCK hi		25		ns
I005	tCLl	Signal Duration SCK lo		25		ns
I006	thCLC	Hold Time: NCS lo after SCK lo → hi		25		ns
I007	tCSh	Signal Duration NCS hi		0		ns
I008	tpCLD	Propagation Delay: MISO stable after SCK hi → lo			40	ns
I009	tpCSD	Propagation Delay: MISO high impedance after NCS lo → hi			25	ns
I010	f(SCK)	Clock Frequency			10	MHz
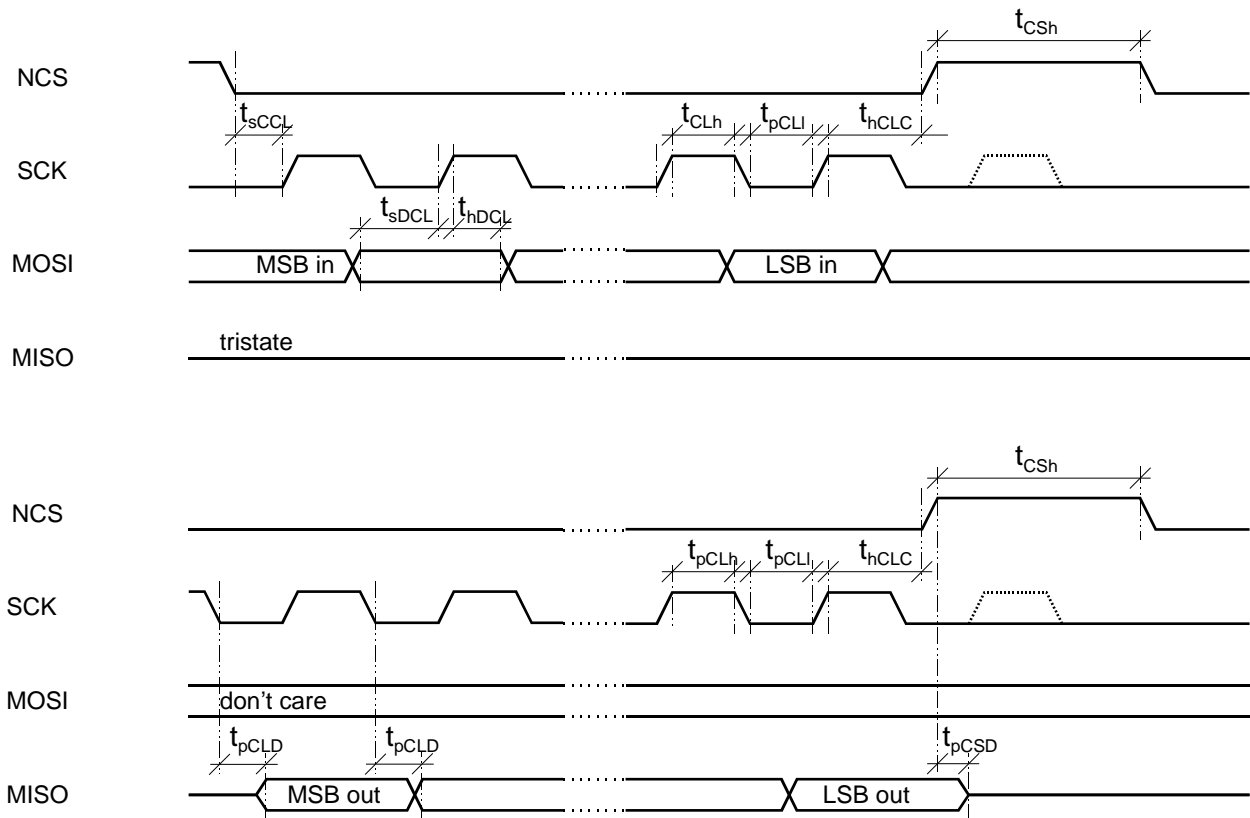
Figure 1: SPI write cycle (top) and read cycle (bottom)

CONFIGURATION PARAMETERS

Read/Write Registers

Configuration

INVZ(1:0)	invert Z signal
EXCH(2:0)	exchange inputs AB
CNTCFG(2:0)	counter configuration
TTL	TTL/differential inputs
CBZ(1:0)	clear counter by zero
CFGZ(1:0)	zero signal configuration
TPCFG(1:0)	TPI configuration
PRIOR	SPI/*BiSS* communication priority
MASK(9:0)	error/warning mask
NMASK(1:0)	error/warning not mask
LVDS	LVDS/RS-422 differential inputs
CH2SEL	*BiSS* channel 2 select
ENCH2	*BiSS* channel 2 enable
CH1SEL	*BiSS* channel 1 select
ENCH1	*BiSS* channel 1 enable
CH0SEL	*BiSS* channel 0 select
NENCH0	*BiSS* channel 0 not enable

Table 5: Register description

Write-Only Registers

Instructions

ACT1	set value of ACT1 pin
ACT0	set value of ACT0 pin
TP	latch TP1 and TP2
ZCEN	enable zero codification
ABRES2	reset AB counter 2
ABRES1	reset AB counter 1
ABRES0	reset AB counter 0

Table 6: Instruction Byte

Read-Only Registers

Status

AB	counter values
NERR	error bit (low active)
NWARN	warning bit (low active)
TP1	touch-probe 1 register
NTPVAL	touch-probe valid (low active)
NABERR	AB counter error (low active)
TP2	touch-probe 2 register
REF	reference register
UPD	update register
NUPDVAL	update register valid (low active)

Table 7: Counter Registers

Error

ABERRx	AB signals error in counter x
EXTERR	external error

Table 8: Error Registers

Warning

OVFx	overflow in counter x
ZEROx	signals zero value in counter x
PDWN	power-down reset
RVAL	REF value valid
UPDVAL	update register up to date
OVFREF	overflow in REF counter
TPVAL	new touch-probe value available
EXTWARN	external warning
COMCOL	communication collision
TPS	actual TPI pin status
ENSSI	SSI enabled

Table 9: Warning Registers

REGISTER MAP

PROGRAMMING								
Adr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Configuration								
0x00	INVZ(1:0)		EXCH(2:0)			CNTCFG(2:0)		
0x01	TTL	CBZ(1:0)		CFGZ(1:0)		TPCFG(1:0)		PRIOR
0x02	MASK(7:0)							
0x03	LVDS				NMASK(1:0)		MASK(9:8)	
0x04	CH2SEL	ENCH2	CH1SEL	ENCH1	CH0SEL	NENCH0		
0x05								
0x06				IDDQ				
0x07	TE	SE				CLK2ACT1	SSIGRAY	IVA
Measurement Data (SPI read only)								
0x08	AB/SPICH(47:0) + NWARN + NERR							
0x09								
0x0A	UPD(23:0) + NUPDVAL + NABERR							
0x0B								
0x0C	TP1(23:0) + NTPVAL + NABERR							
0x0D								
0x0E	TP2(23:0) + NTPVAL + NABERR							
Measurement Data (SPI and *BiSS* read only)								
0x10	REF(23:16)							
0x11	REF(15:8)							
0x12	REF(7:0)							
SPI write only data. (read via AB)								
0x20	SPICH(47:40)							
0x21	SPICH(39:32)							
0x22	SPICH(31:24)							
0x23	SPICH(23:16)							
0x24	SPICH(15:8)							
0x25	SPICH(7:0)							
Instruction Byte (write only)								
0x30		ACT1	ACT0	TP	ZCEN	ABRES2	ABRES1	ABRES0
***BiSS* Profile ROM**								
0x42	*BiSS* Profile ROM - 0x33							
0x43	*BiSS* Profile ROM - 0x18							
Status								
0x48	ABERR0	OVF0	ZERO0	PDWN	RVAL	UPDVAL	OVFREF	TPVAL
0x49	ABERR1	OVF1	ZERO1	PDWN	EXTERR	EXTWARN	COMCOL	TPS
0x4A	ABERR2	OVF2	ZERO2	PDWN	EXTERR	EXTWARN	COMCOL	ENSSI
***BiSS* Device and Manufacturer ID**								
0x78	Device ID - 0x4D ('M')							
0x79	Device ID - 0x44 ('D')							
0x7A	Revision - 0x59 ('Y')							
0x7B	Revision - 0x00 ('0')							
0x7C	Revision - 0x00 ('')							

PROGRAMMING

Adr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x7D	Revision - 0x00 (")							
0x7E	*BiSS* Manufacturer ID (default 0x69)							
0x7F	*BiSS* Manufacturer ID (default 0x43)							

Table 10: Register layout

RS-422, LVDS, TTL RECEIVERS

The input stage for the incremental signals ABZ is configurable as single-ended TTL and differential (RS-422 or LVDS). Differential inputs are possible only for one counter configuration. If two or more counters are configured, it must be used one of the TTL inputs configuration shown in table 11.

Counters	A0	B0	Z0	A1	B1	Z1	A2	B2
1xTTL	AP	AN	BP	-	-	-	-	-
2xTTL	AP	AN	BP	BN	CP	CN	-	-
3xTTL	AP	AN	-	BP	BN	-	CP	CN

Table 11: TTL Input Counters Configuration

Note that the three counters configuration don't implement any Zero signal. It has only A and B input signals. Register bits TTL and LVDS set the configuration of the quadrature input signals.

TTL	Addr. 0x01; bit (7)	0
Code	Function	
0	differential inputs	
1	TTL inputs	

Table 12: TTL Inputs

It is possible to configure the differential input stage of iC-MD in two different modes; differential RS-422 and differential LVDS. See table 13.

LVDS	Addr. 0x03; bit (7)	0
Code	Function	
0	differential RS-422 inputs	
1	differential LVDS inputs	
Notes	condition: TTL=0	

Table 13: LVDS/RS-422 Inputs

The configuration bit EXCH exchanges the input A and the input B of the counters. The default counting direction is positive in clockwise (CW) direction (A edge take place before B edge). But it is also possible to change the counting direction with the register EXCH. See table 14.

EXCH	Addr. 0x00; bit (5:3)	000
Code	Function	
xx1	exchange AB CNT0 (CCW positive)	
x1x	exchange AB CNT1 (CCW positive)	
1xx	exchange AB CNT2 (CCW positive)	

Table 14: Exchange AB Inputs

The index (Z) signal can be inverted as shown in table 15 with the register bits INVZ(1:0).

INVZ	Addr. 0x00; bit (7:6)	00
Code	Function	
x1	invert Z CNT0 (Z=0 active)	
1x	invert Z CNT1 (Z=0 active)	

Table 15: Invert Z Signal

48 BIT COUNTER

iC-MD has a 48 bit counter configurable as from one up to three counters with bit lengths from 16 to 48 bit. Table 16 shows all the possible counters configuration.

The counter configuration is given by the registers CNTCFG as shown in table 16. If it is configured with more than one counter, the input stage must be set to TTL (table 12).

CNTCFG	Addr. 0x00; bit (2:0) 000
Code	Counter Configuration
000	1x24 bit counter
001	2x24 bit counter
010	1x48 bit counter
100	1x32 bit counter
101	1x32 bit + 1x16 bit counter
011	1x16 bit counter
110	2x16 bit counter
111	3x16 bit counter

Table 16: Counter Length

The 48 bit register of the AB counter is also used as "SPI data channel" for data exchanging between SPI and *BiSS* interface, for that purpose the bit CH0SEL (table 45) must be set to 1. When CH0SEL = 1, the counting function for all the counters is deactivated.

Index Signal (Z)
In default operation configuration, the index signal (Z) is active when A = B = 1, as shown in table 17 with EXCH = 0 and INVZ = 0. All other configurations are also possible.

CFGZ	Addr. 0x01; bit (4:3) 00
Code	Function:
00	Z active: when A = 1 B = 1
01	Z active: when A = 1 B = 0
10	Z active: when A = 0 B = 1
11	Z active: when A = 0 B = 0

Table 17: Index Signal Configuration

It can also be deactivated the clearing of counter by the index signal with the configuration bit CBZ (table 18).

The CBZ configuration is only applicable after the second index pulse after power-on or the activation of ZCEN (table 23), because after it, the iC-MD will reset the counter value by the firsts two index pulse, independently of the CBZ configuration, in order to have the AB Counter value referenced to the second index pulse. By default, CBZ is set to 0, also the counters are not reset to 0 by the index signal. But the firsts two Index pulse always reset the counters.

CBZ	Addr. 0x01; bit (6:5) 00
Code	Function
x1	CNT0 cleared by Z0 signal
1x	CNT1 cleared by Z1 signal

Table 18: Clear by Z

24 BIT REFERENCE COUNTER

An aditional 24 bit counter is integrated in order to load the REF and UPD registers. The value of this internal counter can not be read, it can only be read the values of REF and UPD registers. The reference counter is activated by default after power-on and reset with every index signal (it is not affected by the configuration bit CFGZ, table 17).

Since the internal counter for REF and UPD is 24 bit long, the maximum number of edges that can be evaluated (loaded in UPD and REF) between two index signal goes from -2^{23} (negative counting direction) to $2^{23}-1$ (positive counting direction).

REF REGISTER

After the start up (Power on), the iC-MD counts the number of edges between the first two different index signals (Z) in the register REF. This function is always activated by the following situations:

- after power-on.
- by activating the zero codification function via instruction byte (table 23).

The process runs as following: the "reference counter" is set to zero with the first index signal, and the second index signal (must be different of the first one) loads the register REF with the value of "reference counter". It is the distance between the first and the second index signals. The AB counter is then set to 0 with the second index signal. The counter value is then referenced to the position of the second Z signal, and the number of edges between the first two index signals stored in REF.

After the second index signal, the status bit RVAL (table 31) is set and remains at this value until the next power on, the activation of the zero codification function or until the reseting of the counter 0.

The following diagrams show the reference position acquisition process also called as zero codification function.
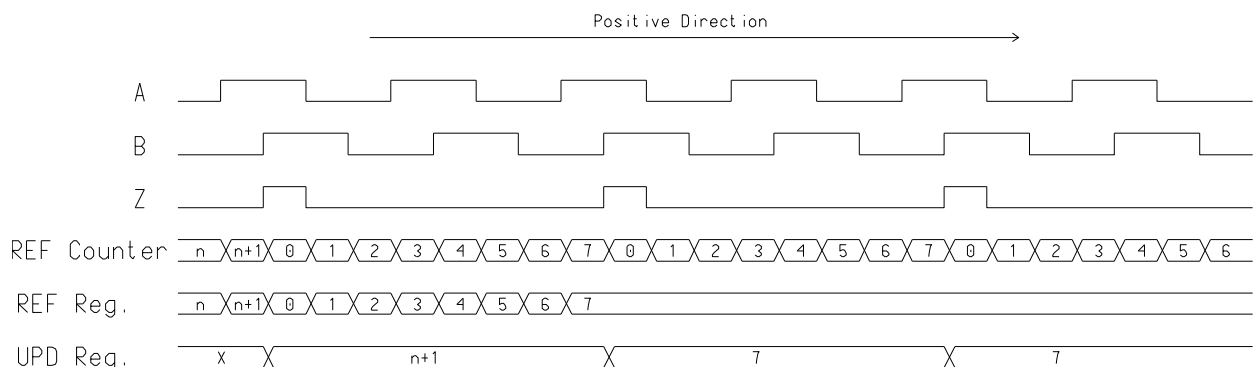
Figure 2: Zero-Codification: REF and UPD registers after activation of Zero Codification function
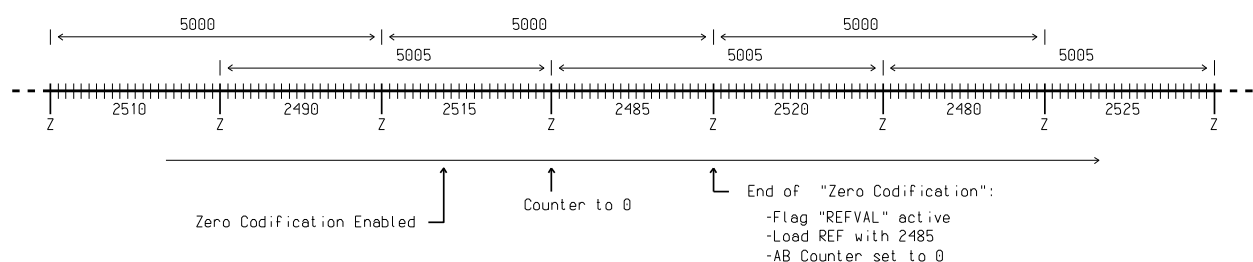
Figure 3: Zero-Codification: reference position acquisition

UPD REGISTER

The register UPD is load at every index pulse with the value of the "reference counter", it is the number of AB edges between the last two index pulses (value of the reference counter). It is used to check that any AB pulse was lost.

The status bit UPDVAL (table 32) signals that a new UPD value is available (UPD register was loaded and still not read).

The following diagram shows the value of REF and UPD after activating the zero codification function when counting in negative direction.

REF	0	-2510	-2510	-2510	-2510	-2510	-2510
UPD	X	-2510	-2490	-2515	-2485	-2520	-2480
CNT	X	0+n	-2490+n	-2515+n	-5000+n	-5520+n	-10000+n
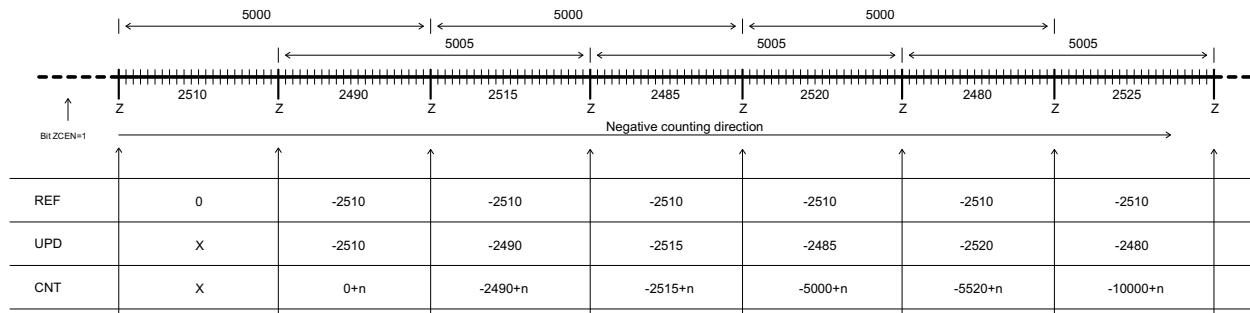
Figure 4: REF and UPD registers in negative direction

TP1, TP2 and AB REGISTERS

TP1, TP2 Registers

The touch probe registers consist of two 24 bit registers which are load with a TPI pin event (see table 19) or writing the instruction bit TP (table 24) via SPI/*BiSS*. At every TPI pin or TP instruction event, the register TP2 is load with the value of TP1 and TP1 is load with the actual value of counter 0.

For using TP registers, AB counter must be configured to 24 bit, but if 2x24 bit counters are configured, only the counter 0 will be latched into TP1/TP2 registers.

The TPI pin events can be configured as falling, rising or both edges, as shown in table 19.

TPCFG	Addr. 0x01; bit (2:1)	00
Code	Function	
00	both edges active	
01	rising edge active	
10	falling edge active	
11	pin TPI disabled	

Table 19: TPI Pin Configuration

The following diagram (figure 5) shows the function of the pin TPI when configured for both rising and falling edge.
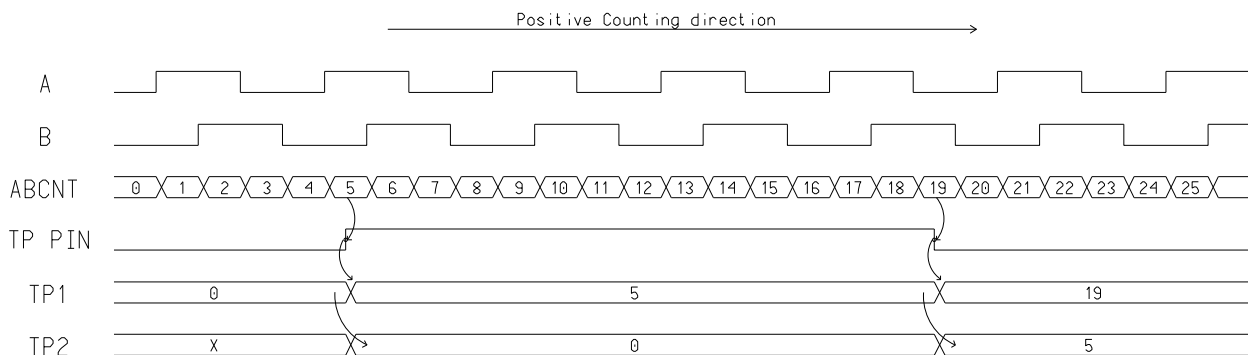
Figure 5: Function of TPI pin when TPCFG=11

AB Register

A 48 bit register (AB) is used to store and shift out the ABCNT Registers (Counters), and also the "SPI Channel Data" (SPICH). The register AB is read via *BiSS* (sensor data, channel 0) or via SPI (Adr 0x08), and the bit length is set by the configuration bits CNTCFG (table 16)

The bit CH0SEL (table 45) selects the data to be load in the AB register when reading the channel 0 via *BiSS* or the address 0x08 via SPI.

COMMUNICATION CONTROL

iC-MD can communicate simultaneously via SPI and *BiSS* in order to exchange data between SPI and *BiSS*. For this purpose, SPI writes the data to be read by *BiSS* in the AB register, and *BiSS* reads the SPICH (BiSS channel 0 configured as SPICH, see table 45).

If both interfaces attempt to read or write at the same time a different RAM address than the SPICH (Adr. 0x20 to 0x25), then the bit error COMCOL (table 37) is set and the communication of the interface without priority (see table 43) is not valid.

Instruction Byte

Register address 0x30 contains the write only instruction byte. When one of these bits is set to 1, then the corresponding operation is executed and then set back to 0, excepts the bits ACT0 and ACT1 which remain to the written value.

ABRES0	Addr. 0x30; bit 0	0
Code	Function	
1	reset of counter 0	

Table 20: Counter 0 Reset

ABRES1	Addr. 0x30; bit 1	0
Code	Function	
1	reset of counter 1	

Table 21: Counter 1 Reset

ABRES2	Addr. 0x30; bit 2	0
Code	Function	
1	reset of counter 2	

Table 22: Counter 2 Reset

ZCEN	Addr. 0x30; bit 3	1
Code	Function	
1	enable zero codification	

Table 23: Enable Zero Codification

TP	Addr. 0x30; bit 4	-
Code	Function	
1	load TP2 with TP1 value, and TP1 with ABCNT value	
Notes	counter must be configured to 24 bit length	

Table 24: Touch Probe Instruction

The instruction bits ACT0 and ACT1 set the actuator pins ACT0 and ACT1 to high or low voltage.

ACT0	Addr. 0x30; bit 5	0
Code	Function	
0	actuator pin 0 set to GND	
1	actuator pin 0 set to VDD	

Table 25: Actuator Pin 0

ACT1	Addr. 0x30; bit 6	0
Code	Function	
0	actuator pin 1 set to GND	
1	actuator pin 1 set to VDD	

Table 26: Actuator Pin 1

STATUS REGISTER and ERROR/WARNING INDICATION

The three bytes status registers (Adr. 0x48 to 0x4A) indicate the state of the iC-MD. All the status bits are latched (except TPS) when an error/warning occurs and are reset when reading the error/warning via SPI or *BiSS* excepts RVAL. The status bits TPVAL and UP-DVAL are also reset by reading the register TP1 and UPD respectively.

The status bit TPS (table 38) is not latched, it signals the actual state of the input pin TPI.

Two of this status bits are error bits; ABERR (AB decodification error, table 27) and EXTERR (external error, table 35), all others status bits signal warnings.

Status bits ABERRx indicate a decodification error of the AB inputs, it ocurrs if the counting frequency is too high or if two incremental edges are too close (PHab2, Spec. Item No.303).

ABERRx	Addr. 0x48, 0x49, 0x4A; bit 7
Code	Description
0	No decodification error in counter x
1	Decodification error in counter x
Notes	x = 0, 1, 2
	Reset by reading Adr. 0x48 (ABERR0), 0x49 (ABERR1) and 0x4A (ABERR2)
	The corresponding counter must be reset (ABRES) after an error

Table 27: AB Decodification Error

The maximum counting range of the counters depends on the counter configuration (see table 16). A counter with the bit length "n" has the maximum counting range will be from -2^{n-1} up to $2^{n-1}-1$. The corresponding bit OVFx is set to 1 if the counter exceeds these values.

OVFx	Addr. 0x48, 0x49, 0x4A; bit 6
Code	Description
0	no overflow in counter x
1	overflow in counter x
Notes	x = 0, 1, 2
	reset by reading Adr. 0x48 (OVF0), 0x49 (OVF1) and 0x4A (OVF2)

Table 28: Counter Overflow Warning

ZEROx bits indicate that the counter value has reached the zero value.

ZEROx	Addr. 0x48, 0x49, 0x4A; bit 5
Code	Description
0	no zero of counter x
1	zero of counter x
Notes	x = 0, 1, 2
	reset by reading Adr. 0x48 (ZERO0), 0x49 (ZERO1) and 0x4A (ZERO2)

Table 29: Zero Value in Counter x

If VDD reaches the power off supply level (VDDoff, Spec. Item No. 602), the iC-MD is reset and the RAM initialized to the default value. Status bit PDWN indicates that this initialization has taken place.

PDWN	Addr. 0x48, 0x49, 0x4A; bit 4
Code	Description
0	No undervoltage
1	Undervoltage
Notes	Reset by reading Adr. 0x48, 0x49 or 0x4A

Table 30: Undervoltage Reset

RVAL status bit indicates that the reference value was load in the REF register, after the "Zero Codification" process. After power-on, this bit remains at 0 until the second different Index pulse.

RVAL	Addr. 0x48; bit 3
Code	Description
0	REF Reg. not valid
1	REF Reg. valid
Notes	Reset by the instruction ZCEN(see table 23)

Table 31: REF Register Valid

Every time that the UPD register is loaded, the status bit UPDVAL (UPD valid) is set to 1 until the status bit UPD or the register UPD is read via SPI or *BiSS*.

UPDVAL	Addr. 0x48; bit 2
Code	Description
0	UPD Reg. not valid
1	UPD Reg. valid
Notes	Reset by reading Adr. 0x48 or the register UPD via SPI (Adr. 0x0A) or *BiSS* (Channel 1)

Table 32: UPD Register Valid

If the number of AB edges between two index signals is greater than $2^{23}-1=8388607$ or lower than $-2^{23}=-8388608$ the status bit OVFREF is set to 1 and indicates that the value of the UPD and REF registers are not valid.

OVFREF	Addr. 0x48; bit 1
Code	Description
0	No Overflow in reference counter
1	Overflow in reference counter
Notes	Reset by reading Adr. 0x48

Table 33: Reference Counter Overflow

After loading TP1/TP2 register, either via pin TPI or instruction TP (see table 24), the bit TPVAL is set to 1 and remains at 1 until the reading of TPVAL, TP1 or TP2 via SPI or *BiSS*.

TPVAL	Addr. 0x48; bit 0
Code	Description
0	TPx registers not loaded
1	New value loaded in TPx
Notes	Reset by reading Adr. 0x48, register TP1 or register TP2 via SPI (Adr. 0x0C and 0x0E) or *BiSS* (channel 1 and channel 2, see table 45)

Table 34: Touch-Probe Valid

The status bit (EXTERR: external error) indicates if the pin NERR was either pulled-down from outside or set to 0 from inside (an internal masked error has ocurred).

EXTERR	Addr. 0x49, 0x4A; bit 3
Code	Description
0	no external error
1	external error
Notes	Reset by reading Adr. 0x49 or 0x4A

Table 35: External Error

The status bit (EXTWARN: external warning) bit indicates if the pin NWARN was either pulled-down from outside or set to 0 from inside (an internal masked warning has ocurred).

EXTWARN	Addr. 0x49, 0x4A; bit 2
Code	Description
0	no external warning
1	external warning
Notes	reset by reading Adr. 0x49 or 0x4A

Table 36: External Warning

If *BiSS*/SSI and SPI try to access at the same time to the internal data bus (*BiSS* register communication and SPI communication) the bit COMCOL will be set indicating that a collision has taken place. If SPICH is activated (table 45), the writing process of AB via SPI and reading of channel 0 via *BiSS* at the same time will generates no COMCOL warning.

If a communication collision take place, only the interface with priority (See table 43) executes the write/read process correctly, but the other interface doesn't write any data or read a false value.

COMCOL	Addr. 0x49, 0x4A; bit 1
Code	Description
0	no communication collision
1	communication collision
Notes	reset by reading Adr. 0x49 or 0x4A

Table 37: Communication Collision

Bit TPS signals the actual state of the input pin TPI. If the pin TPI is high, the bit TPS remains at 1, and if TPI is set to low, TPS status bit is 0.

TPS	Addr. 0x49; bit 0
Code	Description
0	TPI pin at low
1	TPI pin at high

Table 38: Touch-Probe Pin Status

Status bit ENSSI signals if the SSI interface instead of *BiSS* is configured. This is configured by the SLI pin, if the pin is open, the SSI interface is selected. ENSSI has an internal digital filter of 12.5 µs.

ENSSI	Addr. 0x4A; bit 0
Code	Description
0	SSI not enabled
1	SSI enabled (pin SLI open)

Table 39: Enable SSI

Error and warning mask

The masks (MASK) and not masks (NMASK) bits, stipulate whether error and warning events are signaled as an alarm via the open drain I/O pins NERR and NWARN.

MASK	Adr 0x02, bit 7:0; Adr 0x03, bit 1:0
Bit	Error/Warning Event
9	enable SSI (warning)
8	external error (error)
7	zero value of active counter 0, 1 or 2 (warning)
6	touch-probe valid (warning)
5*	power down (RAM was initialized) (warning)
4	overflow of reference counter (warning)
3	overflow of counter 0, 1 or 2 (warning)
2	REF reg. valid (warning)
1	external warning (warning)
0	register comunication collision (warning)
Notes	encoding of bit 9 . . . 0: 0 = message disabled, 1 = message enabled

Table 40: Error/Warning Event Masks

NMASK	Adr 0x03, bit 3:2
Bit	error/warning event
1	AB decodification error. e.g. too high frequency(error)
0	UPD reg. valid (warning)
Notes	encoding of bit 1...0: 0 = message enabled, 1 = message disabled

Table 41: Error/Warning Event Not Masks

SPI INTERFACE

The Serial Peripheral Interface (SPI) of iC-MD consists of a SPI slave interface with polarity 0 and phase 0.

Each transmission starts with a falling edge of NCS and ends with the rising edge. During transmission, commands and data are controlled by SCK and NCS according to the following rules:

- Commands and data are shifted; MSB first, LSB last

- Each output data/status bits are shifted out on the falling edge of SCK (MISO line) and each bit is sampled on the rising edge of SCK (Polarity 0, Phase 0).

- After the device is selected with the falling edge of NCS, an 8-bit command is received. The command defines the operations to be performed (Write/Read) and the address.

- The rising edge of NCS ends all data transfer and resets internal counter and command register

- Data transfer out from MISO starts with the falling edge of SCK immediately after the last bit of the SPI command is sampled in on the rising edge of SCK

- Data transfer to MOSI continues immediately after receiving the command in all cases where data is to be written to iC-MD internal registers

SPI Communication

The first byte to be transmitted to the iC-MD via SPI is the instruction (or command) wich determine the communication direction (read or write), and has the following structure:

SPI Commands							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R/W	ADDRESS(6:0)						

Table 42: SPI command structure

The following diagrams show the SPI write and read processes.
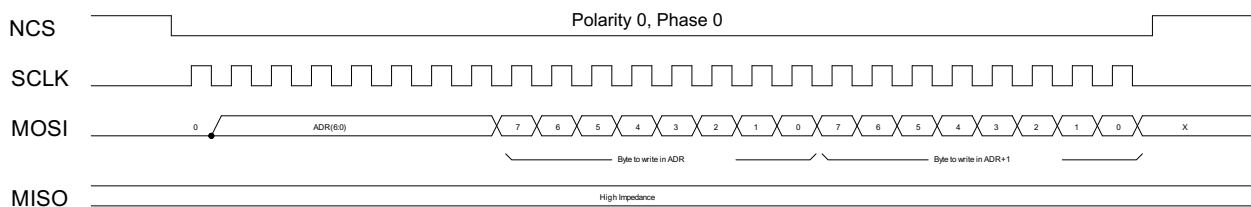
Figure 6: SPI Write Data
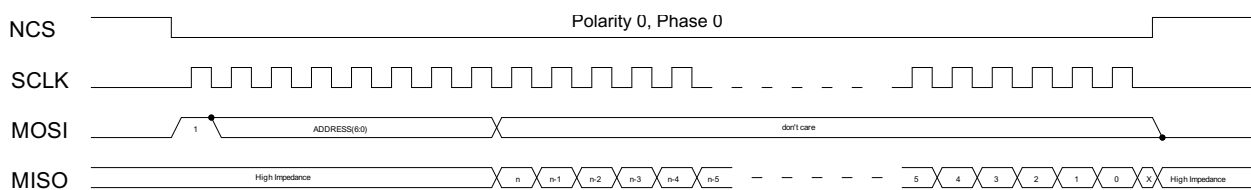
Figure 7: SPI Read Data

The data length to be written is always 8 bit, but it is possible to transmit several bytes of data consecutively

if the NCS signal is not reset and SCLK continues being clocked. The address transmitted is then the start

address which is internally increased by 1 following each transmitted byte.

The data length to be read after the read instruction is variable:

8 bit
For configuration data (Adr.- 0x00 to 0x07), REF and SPICH (Adr.- 0x10 to 0x25), ROM (Adr.- 0x42, 0x43) and Status Bit (Adr.- 0x48 to 0x4A). But it is possible to read several bytes of data consecutively if the NCS signal is not reset and SCLK continues being clocked. The address transmitted is then the start address which is internally increased by 1 following each transmitted byte.

24+2 bit
For TP1, TP2 and UPD registers.

Variable
For counter data, it depends on the counter configuration CNTCFG (Adr. 0x00 bit (2:0)). See the table 16. The total length is CNT length + 2 bit (NERR, NWARN)

Interface Priority
The Configuration bit PRIOR (Adr. 0x03, bit 1), set which interface has priority when taking place a Read-/Write interface collision. It means that if *BiSS* and SPI try to access to the configuration register at the same time, then only the one with the priority will write/read succefully the register. The error in the interface without priority will be signalized by the collision Status bit: SPICOL or BISSCOL, Adr.0x4A, bit(1:0).

PRIOR	Addr. 0x03; bit 1	0
Code	Function	
0	*BiSS* priority	
1	SPI priority	

Table 43: Interface Priority

SPI Channel: SPI to *BiSS* communication
The counter register is also used for the transmission of data from SPI to *BiSS*. The data exchanging take place as following:

1. SPI writes the data to be transmitted in address 0x20 to 0x25, this data is written in the counter registers. The data lenght to be transmitted is selected by CNTCFG (Table 16) and can be configured as 16, 24, 32 or 48-bit

2. After the writing process, the bit SPICHVAL is set to 1 and read via *BiSS* as Warning bit of channel 0.

3. *BiSS* reads out the channel 0, the data written via SPI and two status bits, NERR and NWARN wich indicates if the read data is valid.

BiSS and SSI INTERFACE

The *BiSS* interface is a bidirectional serial interface, which is used to read out the sensor data values and to write and read the internal configuration registers.

For a detailed description of the protocol, see the *BiSS* C specification.

It consist of 3 configurable channels:

channel	eata	error	warning	data length	CRC polynom	CRC mode
CH0	AB counter	NERR	NWARN	16 + 2 bit	1000011	inverted
				24 + 2 bit		
				32 + 2 bit		
				48 + 2 bit		
	SPI Channel	NERR	NSPICHVAL	16 + 2 bit	1000011	inverted
				24 + 2 bit		
				32 + 2 bit		
				48 + 2 bit		
CH1	UPD	NABERR	NUPDVAL	24 + 2 bit	100101	inverted
	TP1	NABERR	NTPVAL	24 + 2 bit	100101	inverted
CH2	TP1	NABERR	NTPVAL	24 + 2 bit	100101	inverted
	TP2	NABERR	NTPVAL	24 + 2 bit	100101	inverted
Notes	channel 0 data length configurable via: CNTCFG (Adr.0x00, bit 3:0)					

Table 44: BiSS Channels

The error (NERR) and warning (NWARN) bit of the channel 0 signal the same data to be output at the pins NERR and NWARN, it's by default:

NERR: ABERR (AB signal error)

NWARN: UPDVAL (UPD Reg. up to date)

This bits can also be configured like the NERR and NWARN outputs, with the registers MASK (table 40) and NMASK(table 41)

Two different data can be selected for each channel, register CHxSEL (table 45) selects the data to be transmitted by the channels.

CHxSEL	Addr. 0x04; bit (7,5,3)	000
Code	Function	
XX0	channel 0: AB counter data	
XX1	channel 0: SPI data channel	
X0X	channel 1: UPD data	
X1X	channel 1: TP1 data	
0XX	channel 2: TP1 data	
1XX	channel 2: TP2 data	

Table 45: *BiSS* Channel Selection

The three channel are enabled by default, but all of them can be disable with the registers NENCH0 (table 46) and ENCHx (table 47)

NENCH0	Addr. 0x04; bit (2)	0
Code	Function	
0	*BiSS* channel 0 enabled	
1	*BiSS* channel 0 disabled	

Table 46: Not Enable *BiSS* Channel 0

ENCHx	Addr. 0x04; bit (6,4)	00
Code	Function	
X0	*BiSS* channel 1 disabled	
0X	*BiSS* channel 2 disabled	

Table 47: Enable *BiSS* Channel 1 and 2

SSI Protocol
An SSI protocol is selected if the input pin SLI is open. This enable signal has an internal digital filter of 5 µs.

A clock pulse train from a controller is used to gate out sensor data. Between each clock pulse train there is a SSI timeout during which fresh data is moved into the register. Data is shifted out when the iC-MD receives a pulse train from the controller. When the least sig-

nificant bit (LSB) goes high after the SSI timeout, new data is available to read.

The AB counter data transmitted is in the form of a binary code (24 bit + NERR + NWARN). If the input MA

continues being clocked without SSI timeout, it will be output a total of 94 bit with the following scheme:

MA ⎍⎍⎍ . . . . ⎍⎍⎍⎍⎍ . . . . ⎍⎍⎍⎍⎍ . . . . ⎍⎍

SLO ═══╳ AB(23:0)&nABERR&nUPDVAL&CRC(5:0) ╳ UPD(23:0)&nABERR&nUPDVAL&CRC(4:0) ╳ TP1(23:0)&nABERR&nTPVAL&CRC(4:0) ╳═══
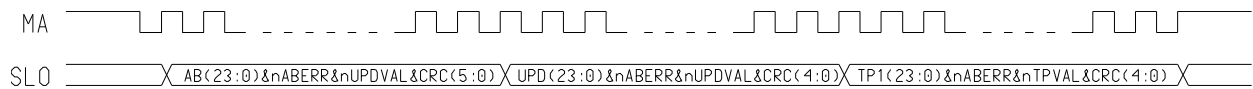
Figure 8: Output data with SSI protocol

ACTUATOR OUTPUTS, ERROR and WARNING I/O PINS

The pins NERR and NWARN are low active bidirectional ports (open collector outputs and digital inputs).

The inputs are used to latch an external error/warning (tables 35 and 36) and makes possible that this

error/warning will be read by the controller via SPI or *BiSS* as status bits.

The instruction bits ACT0 and ACT1 (tables 25 and 26) set the value of the output pins ACT0 and ACT1.

APPLICATIONS NOTES

RS422 12 V capable inputs setup

The following figure shows the resistors configuration
used for a 12 V capable RS422 inputs. (see Fig. 9).
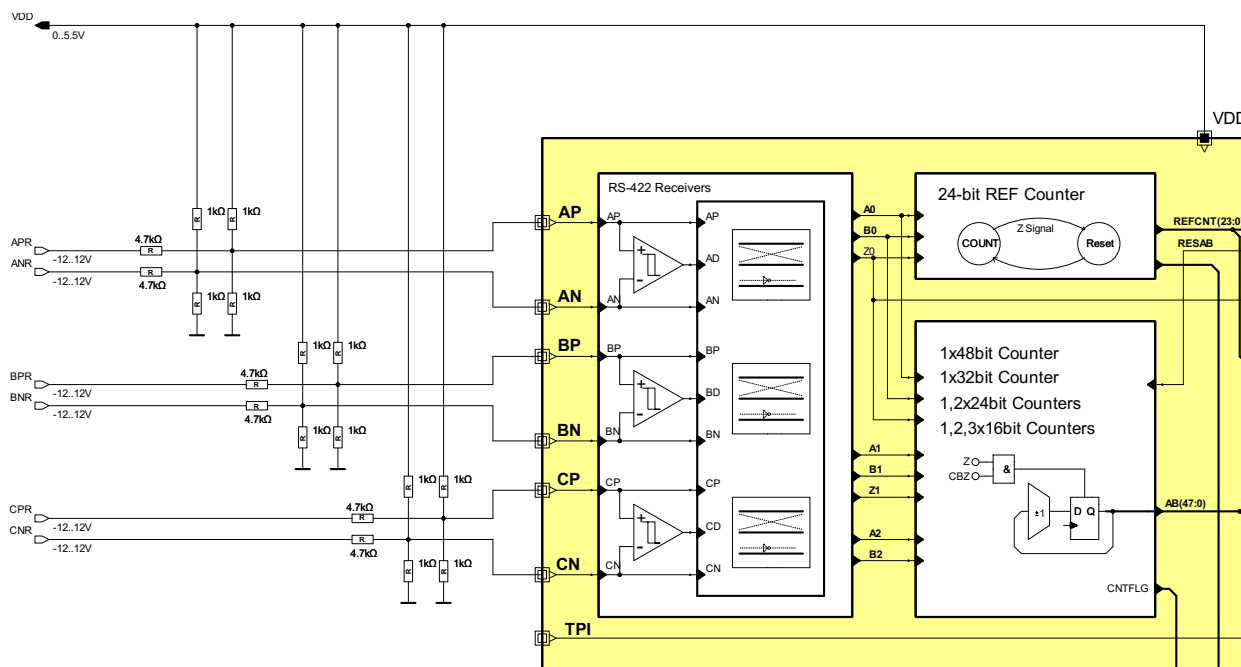
Figure 9: RS422 12 V capable configuration

ORDERING INFORMATION

Type	Package	Order Designation
iC-MD	TSSOP20	iC-MD TSSOP20
Evaluation Board iC-MD	100 mm x 80 mm PCB	iC-MD EVAL MD1D

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