



FLASH-ROM MODULE 8MByte (1M x 64-Bit) ,120PIN SMM,3.3V
Part No. HMF1M64F4V

GENERAL DESCRIPTION

The HMF1M64F4V is a high-speed flash read only memory (FROM) module containing 262,144 words organized in an x64bit configuration. The module consists of four 1M x 16 FROM mounted on a 120-pin, SMM connector FR4-printed circuit board.

Commands are written to the command register using standard microprocessor write timings.

Register contents serve as input to an internal state-machine, which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 12.0V flash or EPROM devices.

Output enable (/OE) and write enable (/WE) can set the memory input and output. The host system can detect a program or erase operation is complete by observing the Ready Pin, or reading the DQ7(Data # Polling) and DQ6(Toggle) status bits.

When FROM module is disable condition the module is becoming power standby mode, system designer can get low -power design. All module components may be powered from a single + 3.0V DC power supply and all inputs and outputs are LVTTTL-compatible

FEATURES

- w Access time : 80, 90, 120ns
- w High-density 8MByte design
- w High-reliability, low-power design
- w Single + 3V \pm 0.3V power supply
- w Easy memory expansion
- w Hardware reset pin(RESET#)
- w FR4-PCB design
- w 120-Pin Designed by 60-Pin Fine Pitch Connector P1,P2
- w Minimum 1,000,000 write cycle guarantee per sector
- w 20-year data retention at 125 °C
- w Flexible sector architecture
- w Embedded algorithms
- w Erase suspend / Erase resume

OPTIONS MARKING

w Timing

80ns access	-80
90ns access	-90
120ns access	-120

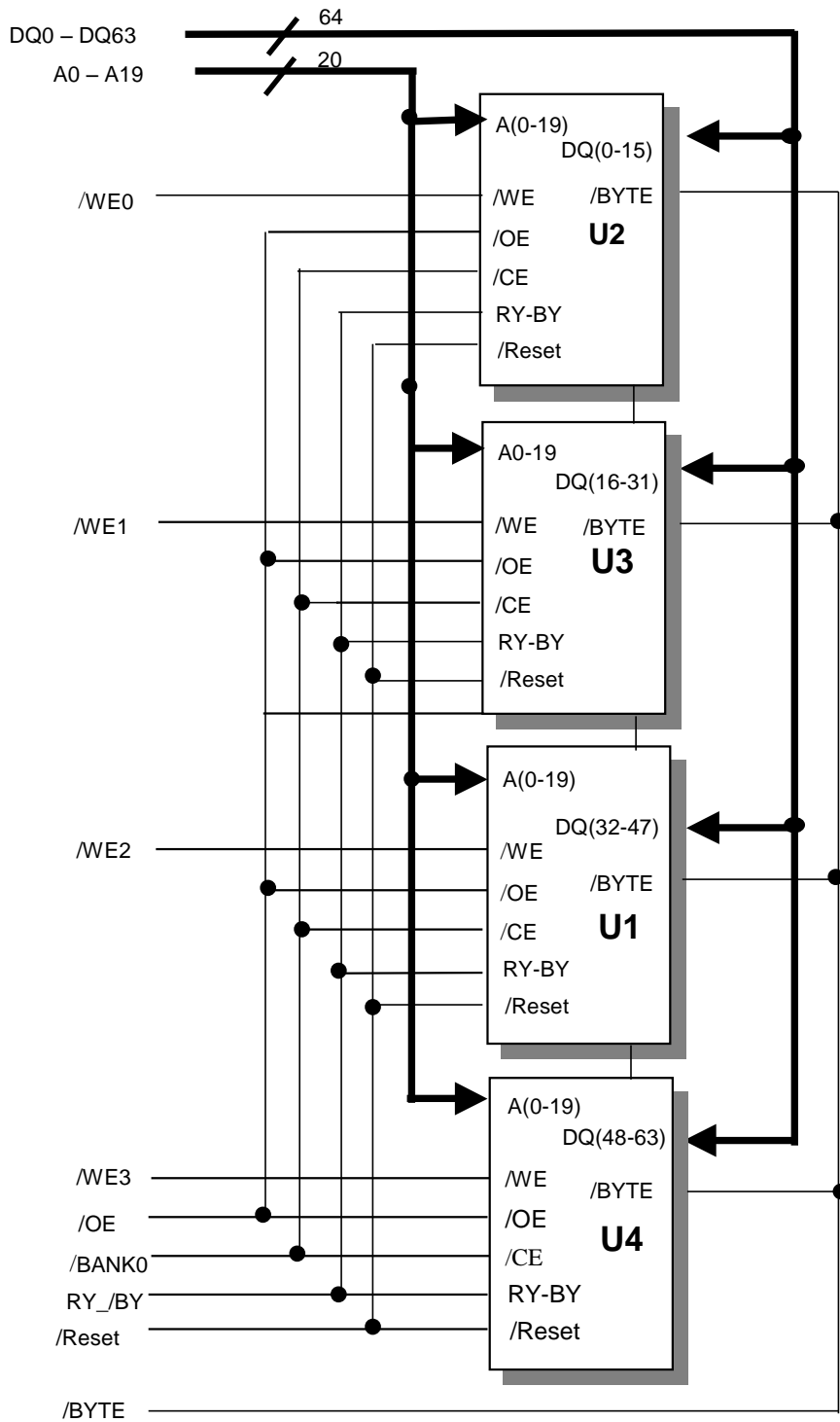
w Packages

120-pin SMM	F
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PIN ASSIGNMENT

P1				P2			
PIN	Symbol	PIN	Symbol	PIN	Symbol	PIN	Symbol
1	VCC	31	VSS	1	VCC	31	VSS
2	DQ32	32	DQ0	2	DQ16	32	DQ48
3	DQ33	33	DQ1	3	DQ17	33	DQ49
4	DQ34	34	DQ2	4	DQ18	34	DQ50
5	DQ35	35	DQ3	5	DQ19	35	DQ51
6	DQ36	36	DQ4	6	DQ20	36	DQ52
7	DQ37	37	DQ5	7	DQ21	37	DQ53
8	DQ38	38	DQ6	8	DQ22	38	DQ54
9	DQ39	39	DQ7	9	DQ23	39	DQ55
10	VCC	40	VSS	10	VCC	40	VSS
11	DQ40	41	DQ8	11	DQ24	41	DQ56
12	DQ41	42	DQ9	12	DQ25	42	DQ57
13	DQ42	43	DQ10	13	DQ26	43	DQ58
14	DQ43	44	DQ11	14	DQ27	44	DQ59
15	DQ44	45	DQ12	15	DQ28	45	DQ60
16	DQ45	46	DQ13	16	DQ29	46	DQ61
17	DQ46	47	DQ14	17	DQ30	47	DQ62
18	DQ47	48	DQ15	18	DQ31	48	DQ63
19	VCC	49	VSS	19	VCC	49	VSS
20	A1	50	A10	20	A20	50	NC[BANK1*]
21	A2	51	A11	21	A0	51	BANK0*
22	A3	52	A12	22	A16	52	VSS
23	A4	53	A13	23	WE1*	53	BYTE*
24	A5	54	A14	24	WE2*	54	WE3*
25	VCC	55	VSS	25	VCC	55	VSS
26	A6	56	A15	26	OE*	56	NC[WE4*]
27	A7	57	A17	27	RESET*	57	NC[WE5*]
28	A8	58	A18	28	WE0*	58	NC[WE6*]
29	A9	59	A19	29	RY_BY*	59	NC[WE7*]
30	VCC	60	VSS	30	VCC	60	VSS

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	/OE	/CE	/WE	/RESET	DQ (/BYTE=L)	POWER
STANDBY	X	H	X	V _{CC} ±0.3V	HIGH-Z	STANDBY
NOT SELECTED	H	L	H	H	HIGH-Z	ACTIVE
READ	L	L	H	H	D _{OUT}	ACTIVE
WRITE or ERASE	X	L	L	H	D _{IN}	ACTIVE

NOTE: X means don't care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING
Voltage with respect to ground all other pins	V _{IN,OUT}	-0.5V to V _{CC} +0.5V
Voltage with respect to ground V _{CC}	V _{CC}	-0.5V to +4.0V
Storage Temperature	T _{STG}	-65°C to +150°C
Operating Temperature	T _A	-40°C to +85°C

w Stresses greater than those listed under " Absolute Maximum Ratings" may cause permanent damage to the device.

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP.	MAX
V _{CC} for ± 10% device Supply Voltages	V _{CC}	2.7V	3.0	3.6V
Ground	V _{SS}	0	0	0

DC AND OPERATING CHARACTERISTICS (0°C ≤ T_A ≤ 70 °C)

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	MAX	UNIT	
Input Leakage Current	V _{CC} =V _{CC} max, V _{IN} = GND to V _{CC}	I _{L1}	-1.0	1.0	μA	
Output Leakage Current	V _{CC} =V _{CC} max, V _{OUT} = GND to V _{CC}	I _{L0}	-1.0	1.0	μA	
Output High Voltage	I _{OH} = -2.0mA, V _{CC} = V _{CC} min	V _{OH}	0.85x V _{CC}	-	V	
Output Low Voltage	I _{OL} = 4.0mA, V _{CC} =V _{CC} min	V _{OL}	-	0.4	V	
V _{CC} Active Read Current (1)	/CE = V _{IL} , /OE = V _{IH} ,	I _{CC1}	5MHZ	-	64	mA
			1MHZ	-	16	
V _{CC} Active Write Current (2)	/CE = V _{IL} , /OE=V _{IH}	I _{CC2}	-	120	mA	
V _{CC} Standby Current (3)	/CE, /RESET=V _{CC} ±0.3V	I _{CC3}	-	20	μA	
Low V _{CC} Lock-Out Voltage		V _{LKO}	2.3	2.5	V	

- Notes:
1. The I_{CC} current listed includes both the DC operating current and the frequent component (at 5MHz).
 2. I_{CC} active while embedded algorithm (program or erase) is in progress
 3. I_{CC} active while Embedded Erase or Embedded Program is in progress.
 4. Not 100% tested

ERASE AND PROGRAMMING PERFORMANCE

PARAMETER	LIMITS			UNIT	COMMENTS
	MIN.	TYP.	MAX.		
Block Erase Time	-	0.7	15	sec	Excludes 00H programming prior to erasure
Chip Erase Time		25		sec	
Word Programming Time	-	11	360	μs	Excludes system-level overhead
Chip Programming Time	-	12	36	sec	

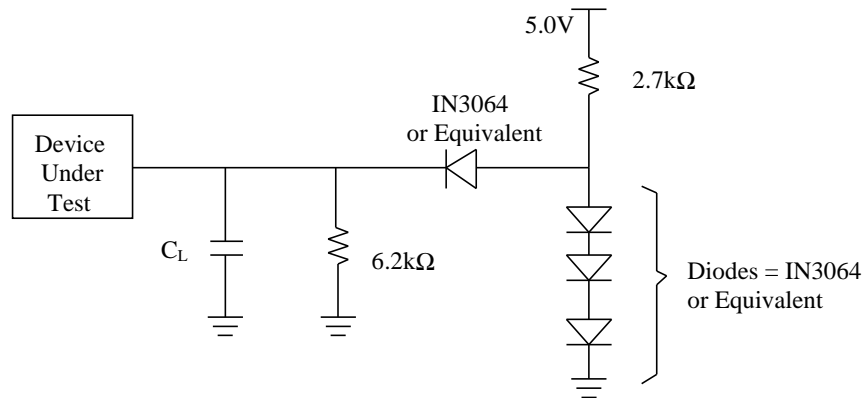
TSOP CAPACITANCE

PARAMETER SYMBOL	PARAMETER DESCRIPTION	TEST SETUP	MIN	MAX	UNIT
C _{IN}	Input Capacitance	V _{IN} = 0	-	7.5	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0	-	12	pF
C _{IN2}	Control Pin Capacitance	V _{IN} = 0	-	9	pF

Notes : Capacitance is periodically sampled and not 100% tested.

TEST SPECIFICATIONS

TEST CONDITION	VALUE	UNIT
Output load	1TTL gate	
Input rise and fall times	5	ns
Input pulse levels	0 to 3	V
Input timing measurement reference levels	1.5	V
Output timing measurement reference levels	1.5	V



Note : C_L = 100pF including jig capacitance

AC CHARACTERISTICS**⌋ Read Only Operations Characteristics**

PARAMETER	DESCRIPTION	SPEED						UNIT
		- 80		-90		-120		
		MIN	MAX	MIN	MAX	MIN	MAX	
t _{RC}	Read Cycle Time	80		90		120		ns
t _{ACC}	Address Access time		80		90		120	ns
t _{CE}	Chip Enable to Access time		80		90		120	ns
t _{OE}	Output Enable time		30		35		50	ns
t _{DF}	Chip Enable to Output High-Z		25		30		30	ns
t _{OEH}	Output Enable Hold Time	0		0		0		ns
t _{QH}	Output Hold Time From Addresses, /CE or /OE	0		0		0		ns

**⌋ Erase/Program Operations
Alternate /WE Controlled Writes**

PARAMETER	DESCRIPTION	-80		-90		-120		
		MIN	MAX	MIN	MAX	MIN	MAX	
t _{WC}	Write Cycle Time (1)	80	-	90	-	120	-	ns
t _{AS}	Address Setup Time	0	-	0	-	0	-	ns
t _{AH}	Address Hold Time	45	-	45	-	50	-	ns
t _{DS}	Data Setup Time	35	-	45	-	50	-	ns
t _{DH}	Data Hold Time	0	-	0	-	0	-	ns
t _{OES}	Output Enable Setup Time	0	-	0	-	0	-	ns
t _{GHWL}	Read Recover Time Before Write	0	-	0	-	0	-	ns
t _{CS}	/CE Setup Time	0	-	0	-	0	-	ns
t _{CH}	/CE Hold Time	0	-	0	-	0	-	ns
t _{WP}	Write Pulse Width	35	-	35	-	50	-	ns
t _{WPH}	Write Pulse Width High	30	-	30	-	30	-	ns
t _{PGM}	Programming Operation	11		11		11		μs
t _{BERS}	Sector Erase Operation (2)	0.7	-	0.7	-	0.7	-	sec
t _{VCS}	Vcc set up time	50	-	50	-	50	-	μs
t _{RB}	Write Recover Time Before RY_/BY	0	-	0	-	0	-	ns
t _{RH}	/RESET High Before Read	50	-	50	-	50	-	ns
t _{RPD}	/RESET Low to Standby Mode	20	-	20	-	20	-	μs
t _{RP}	/RESET Pulse Width	500	-	500	-	500	-	ns

Notes : : 1. Not 100% tested

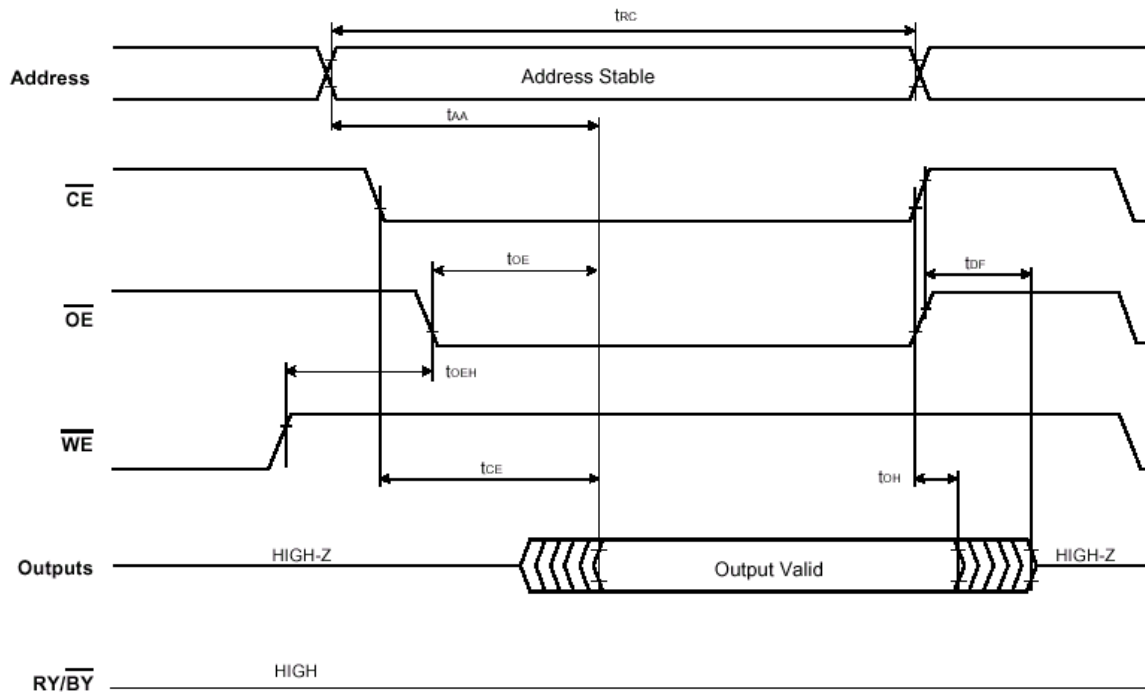
2 . See the "Erase and Programming Performance" section for more information.

U Erase/Program Operations
Alternate /CE Controlled Writes

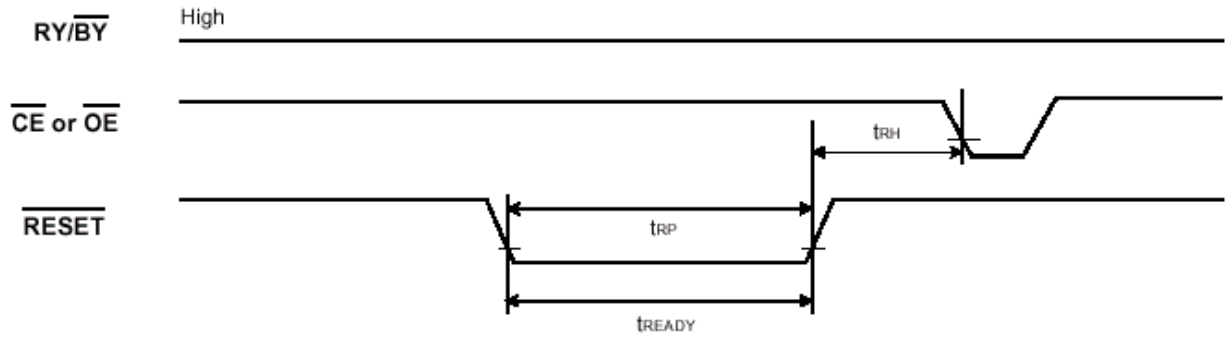
PARAMETER	DESCRIPTION	- 80		-90		-120		
		MIN	MAX	MIN	MAX	MIN	MAX	
t _{WC}	Write Cycle Time(1)	80	-	90	-	120	-	ns
t _{AS}	Address Setup Time	0	-	0	-	0	-	ns
t _{AH}	Address Hold Time	45	-	45	-	50	-	ns
t _{DS}	Data Setup Time	35	-	45	-	50	-	ns
t _{DH}	Data Hold Time	0	-	0	-	0	-	ns
t _{OES}	Output Enable Setup Time	0	-	0	-	0	-	ns
t _{GHWL}	Read Recover Time Before Write	0	-	0	-	0	-	ns
t _{CS}	/CE Setup Time	0	-	0	-	0	-	ns
t _{CH}	/CE Hold Time	0	-	0	-	0	-	ns
t _{WP}	Write Pulse Width	35	-	35	-	50	-	ns
t _{WPH}	Write Pulse Width High	30	-	30	-	30	-	ns
t _{PGM}	Programming Operation	11		11		11		μs
t _{BERS}	Sector Erase Operation (2)	0.7	-	0.7	-	0.7	-	sec

- Notes :** 1. Not 100% tested
 2. This does not include the preprogramming time

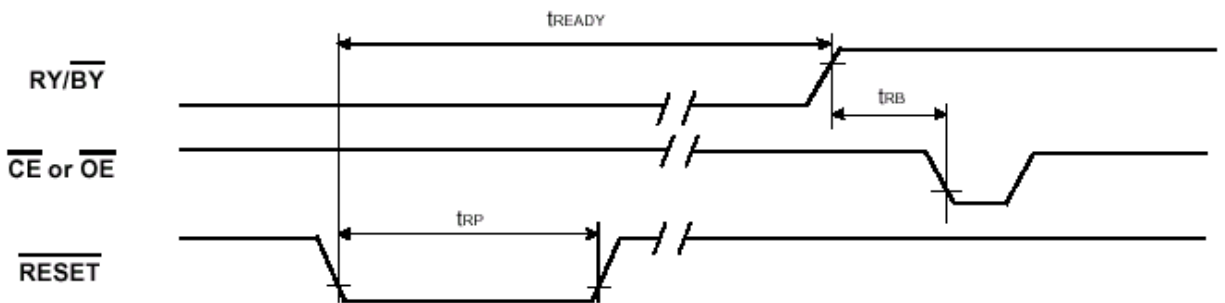
U READ OPERATIONS TIMING



RESET TIMING



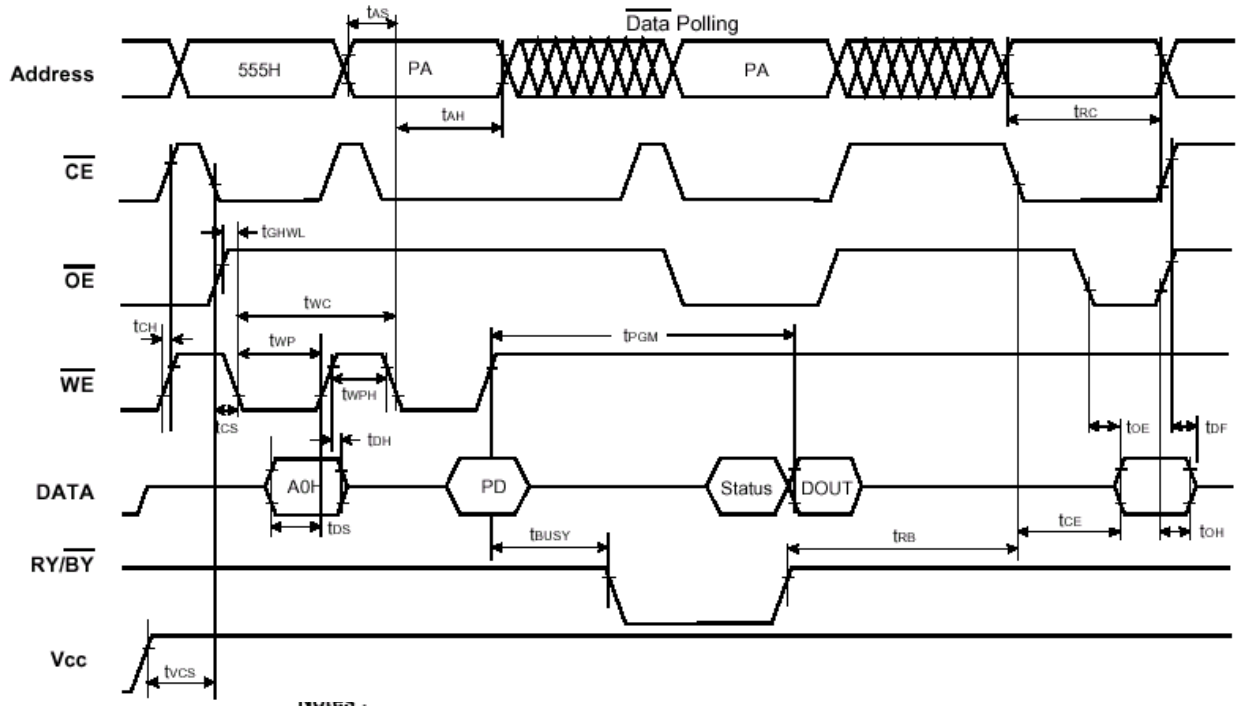
Reset Timings NOT during Internal Routine



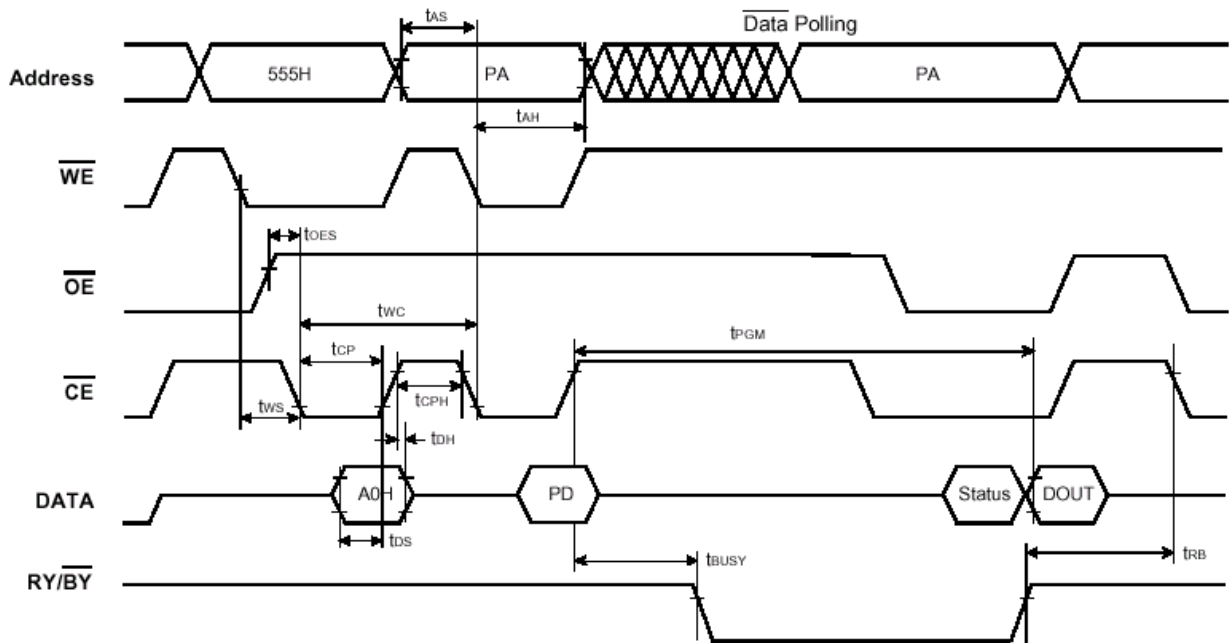
Reset Timings during Internal Routine

PROGRAM OPERATIONS TIMING

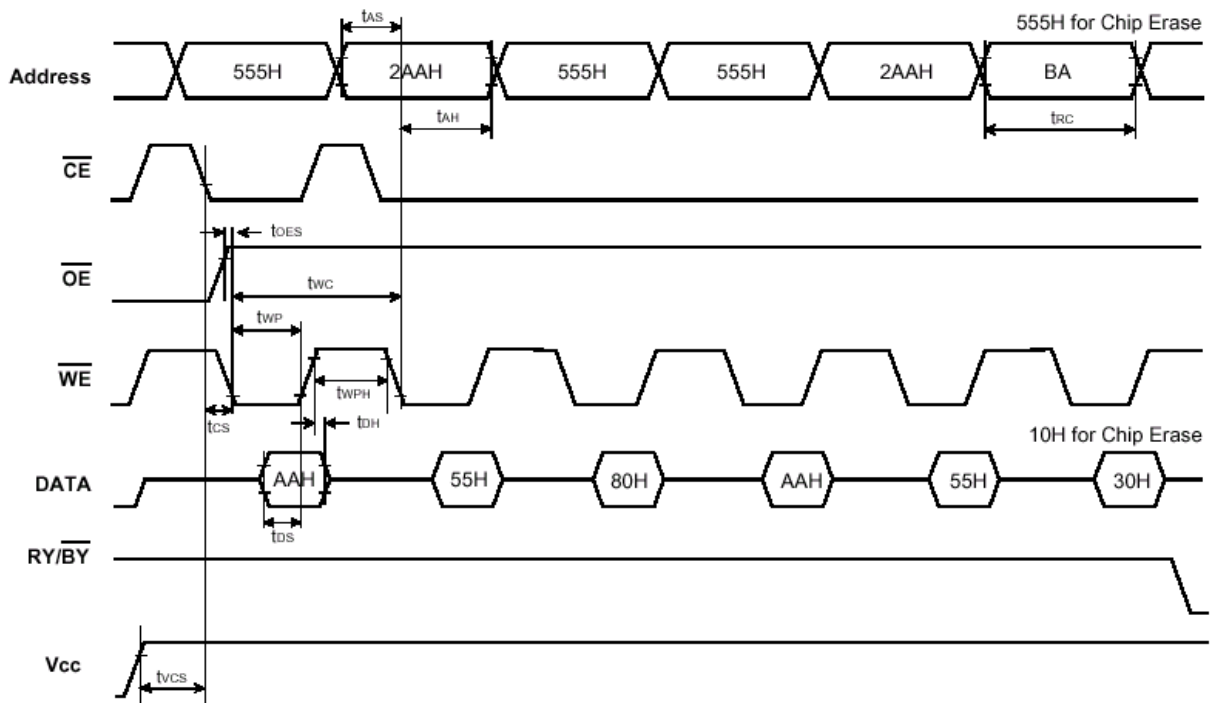
Alternate /WE Controlled Writes



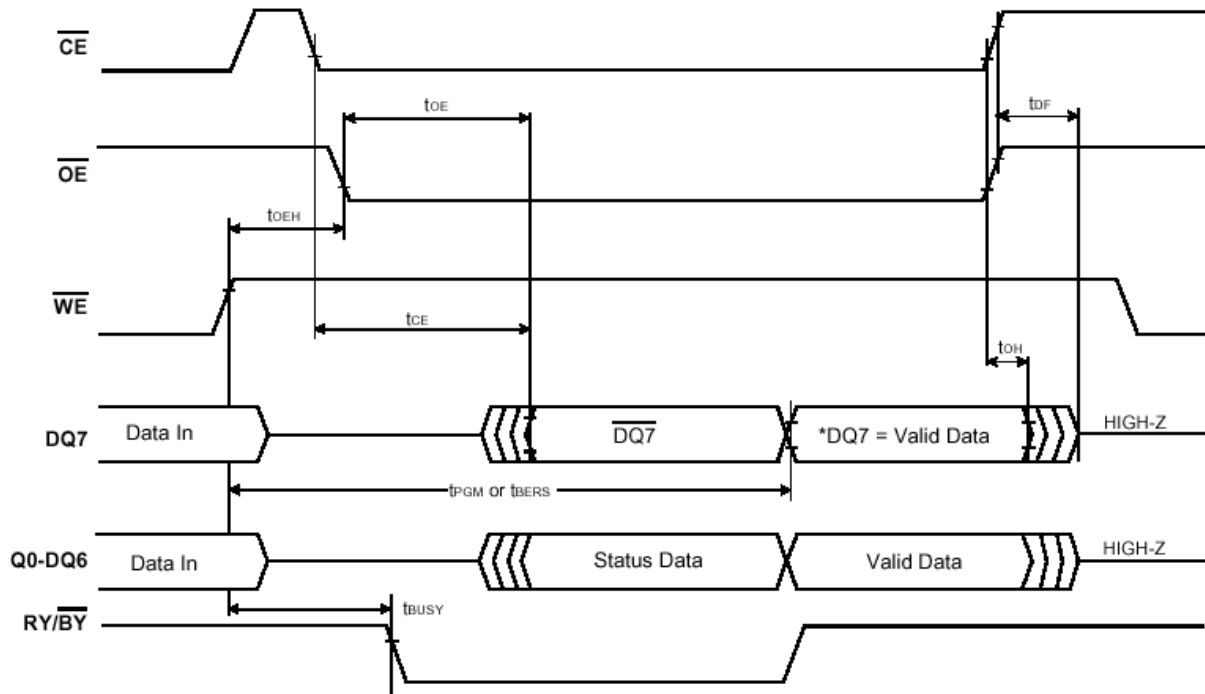
Alternate /CE Controlled Writes



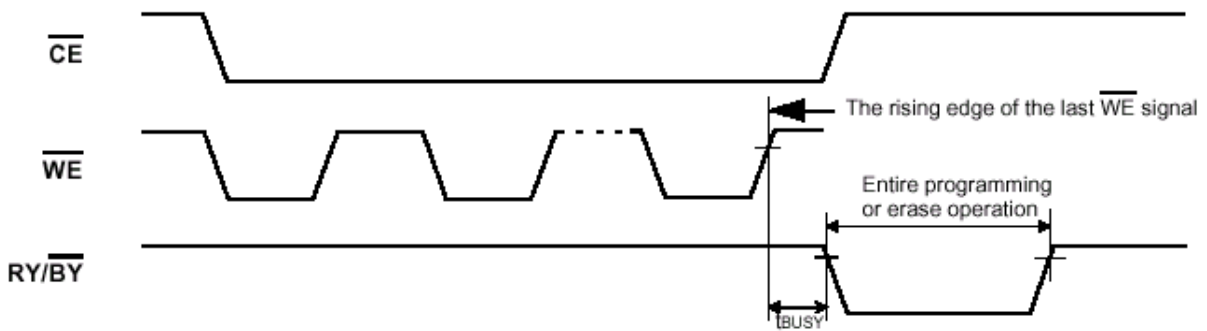
CHIP/BLOCK ERASE OPERATION TIMINGS



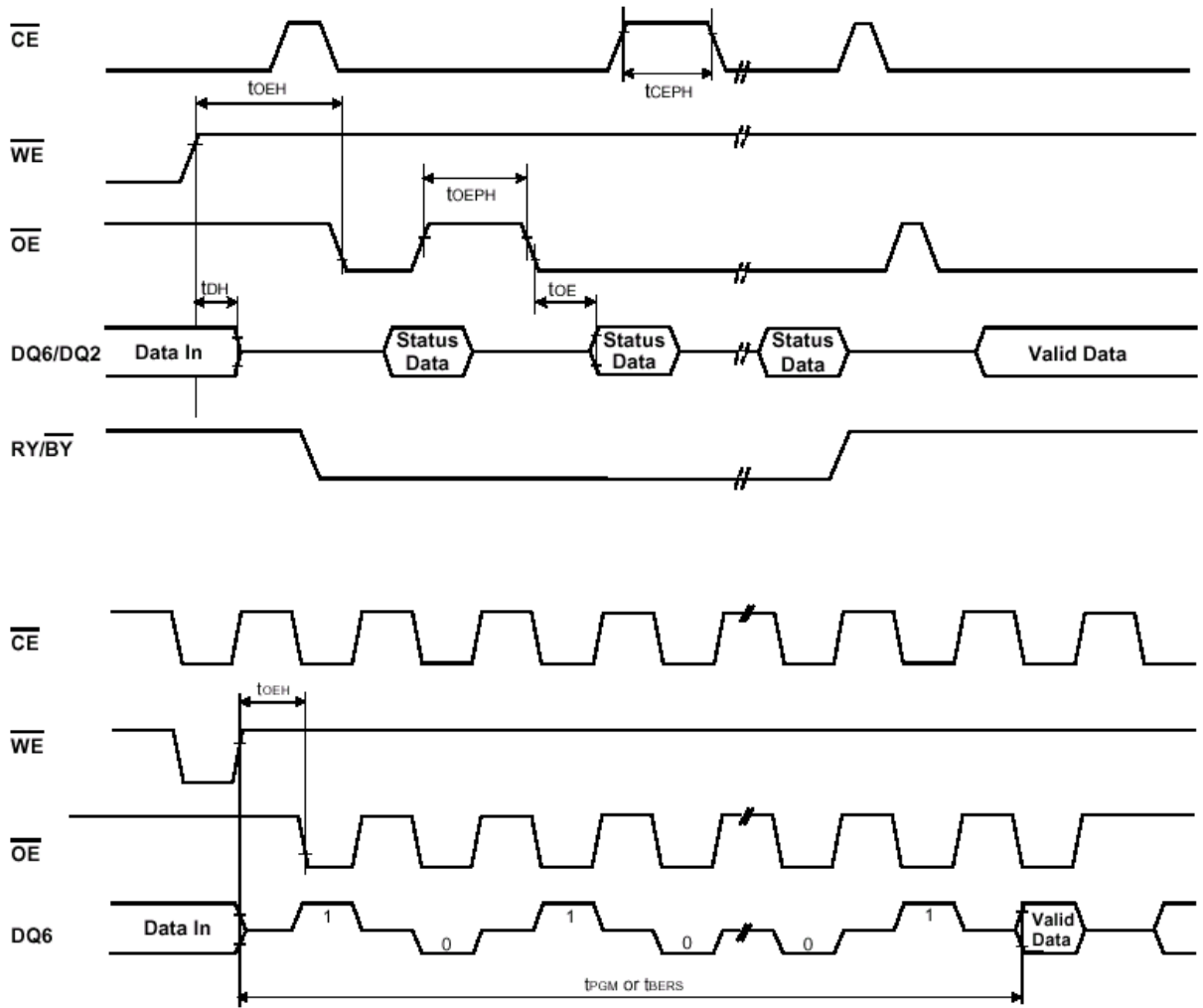
⌒ DATA# POLLING TIMES DURING INTERNAL ROUTINE OPERATION



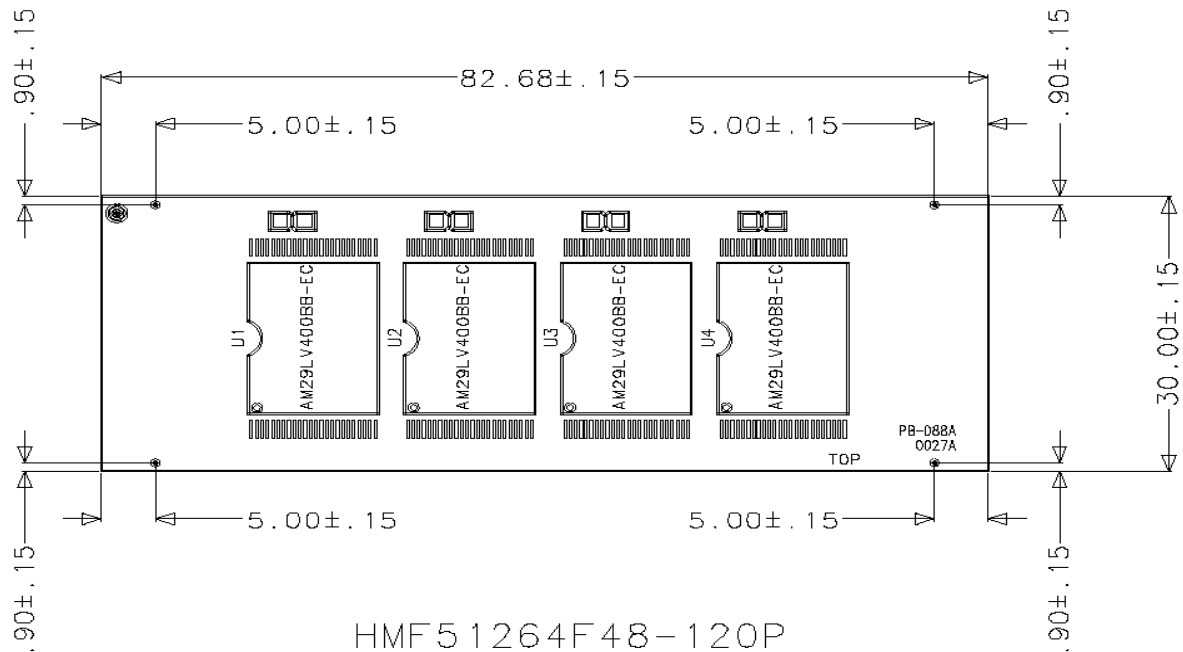
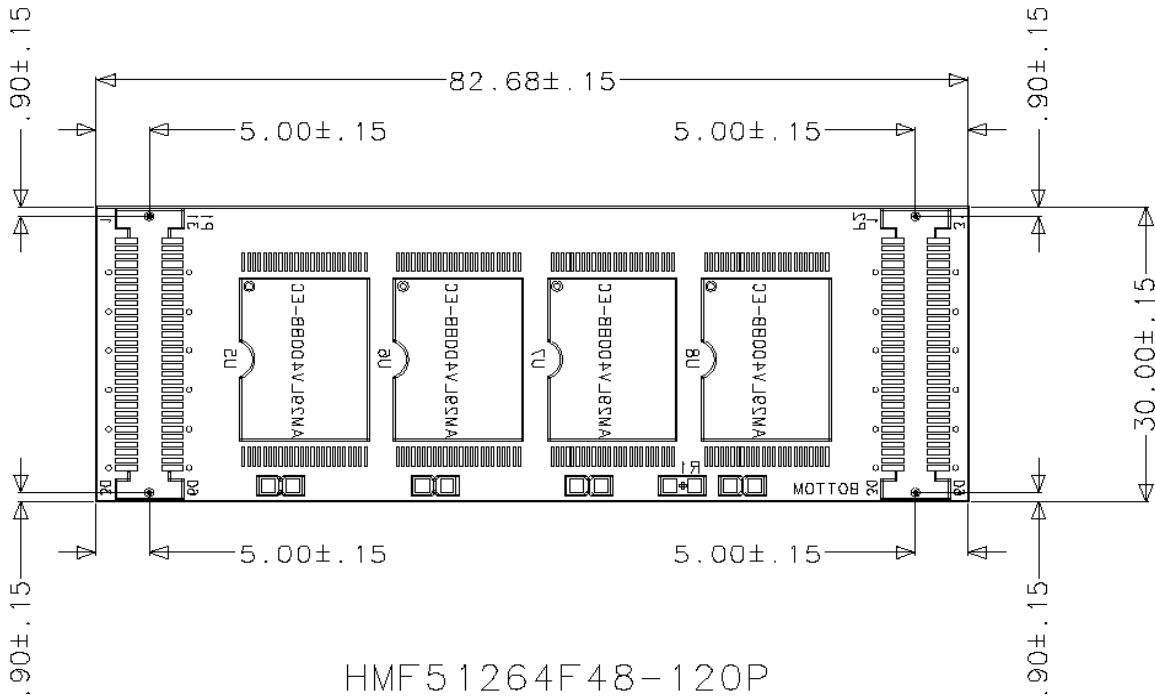
⌒ RY_ /BY TIMEING DURING ERASE / PROGRAM OPERATION



U TOGGLE# BIT DURING INTERNAL ROUTINE OPERATION



PACKAGE DIMENSIONS



ORDERING INFORMATION

Part Number	Density	Org.	Package	Component Number	Vcc	SPEED
HMF1M64F4V-80	8MByte	X 64	120 Pin-SMM	4EA	3.3V	80ns
HMF1M64F4V-90	8MByte	X 64	120 Pin-SMM	4EA	3.3V	90ns
HMF1M64F4V-120	8MByte	X 64	120 Pin-SMM	4EA	3.3V	120ns