Blackfin Embedded Processor

Preliminary Technical Data

ADSP-BF504/F, ADSP-BF506F

FEATURES

- Up to 400 MHz high-performance Blackfin processor
  - Two 16-bit MACs, two 40-bit ALUs, four 8-bit video ALUs, 40-bit shifter
  - RISC-like register and instruction model for ease of programming and compiler-friendly support
  - Advanced debug, trace, and performance monitoring
- Accepts a range of supply voltages for internal and I/O operations. See Processor — Operating Conditions on Page 25
- Internal 32M bit flash (available on ADSP-BF504F and ADSP-BF506F processors)
- Internal ADC (available on ADSP-BF506F processor)
- Off-chip voltage regulator interface
- 88-lead (12 mm × 12 mm) LFCSP package for ADSP-BF504 and ADSP-BF504F processors
- 120-lead (14 mm × 14 mm) LQFP package for ADSP-BF506F processor

MEMORY

- 68K bytes of L1 SRAM (processor core-accessible) memory: (See Table 1 on Page 3 for L1 and L3 memory size details)
- External (interface-accessible) memory controller with glueless support for internal 32M bit flash and boot ROM
- Flexible booting options from internal flash and SPI memory or from host devices including SPI, PPI, and UART
- Memory management unit providing memory protection

PERIPHERALS

- Two 32-bit up/down counters with rotary support
- Eight 32-bit timers/counters with PWM support
- Two three-phase 16-bit center-based PWM units
- Two dual-channel, full-duplex synchronous serial ports (SPORTs), supporting eight stereo I^2S channels
- Two Serial Peripheral Interface (SPI) compatible ports
- Two UARTs with IrDA® support
- Parallel peripheral interface (PPI), supporting ITU-R 656 video data formats
- Removable storage interface (RSI) controller for MMC, SD, SDIO, and CE-ATA
- Internal ADC with 12 channels, 12 bits, and up to 2 MSPS
- ADC controller module (ACM), providing a glue-less interface between Blackfin processor and internal or external ADC
- Controller Area Network (CAN) controller
- Two-wire interface (TWI) controller
- 12 peripheral DMAs
- Two memory-to-memory DMA channels
- Event handler with 52 interrupt inputs
- 35 general-purpose I/Os (GPIOs), with programmable hysteresis
- Debug/JTAG interface
- On-chip PLL capable of frequency multiplication

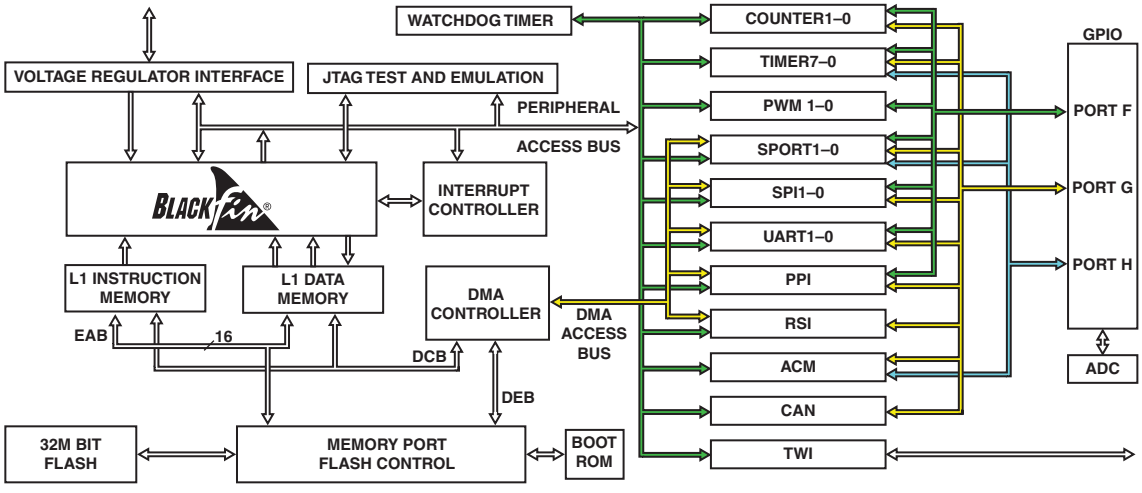

Figure 1. Processor Block Diagram

Rev. PrC

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REVISION HISTORY

1/10—Rev. PrB to Rev. PrC

Numerous small corrections and additions to document.

Major changes/additions include:

Revised all timing diagrams for clarity/consistency in Processor — Timing Specifications 31

Updated specifications (reference PCN 09_0173) in the Clock and Reset Timing section to accurately describe processor cold-startup/reset timing 31

To view product/process change notifications (PCNs) related to this data sheet revision, please visit the processor's product page on the www.analog.com website and use the **View PCN** link.

GENERAL DESCRIPTION

The ADSP-BF50x processors are members of the Blackfin® family of products, incorporating the Analog Devices/Intel Micro Signal Architecture (MSA). Blackfin processors combine a dual-MAC state-of-the-art signal processing engine, the advantages of a clean, orthogonal RISC-like microprocessor instruction set, and single-instruction, multiple-data (SIMD) multimedia capabilities into a single instruction-set architecture.

The ADSP-BF50x processors are completely code compatible with other Blackfin processors. ADSP-BF50x processors offer performance up to 400 MHz and reduced static power consumption. Differences with respect to peripheral combinations are shown in Table 1.

Table 1. Processor Comparison

Feature		ADSP-BF504	ADSP-BF504F	ADSP-BF506F
Up/Down/Rotary Counters		2	2	2
Timer/Counters with PWM		8	8	8
3-Phase PWM Units		2	2	2
SPORTs		2	2	2
SPIs		2	2	2
UARTs		2	2	2
Parallel Peripheral Interface		1	1	1
Removable Storage Interface		1	1	1
CAN		1	1	1
TWI		1	1	1
Internal 32M Bit Flash		–	1	1
ADC Control Module (ACM)		1	1	1
Internal ADC		–	–	1
GPIOs		35	35	35
Memory (bytes)	L1 Instruction SRAM	16K	16K	16K
	L1 Instruction SRAM/Cache	16K	16K	16K
	L1 Data SRAM	16K	16K	16K
	L1 Data SRAM/Cache	16K	16K	16K
	L1 Scratchpad	4K	4K	4K
	L3 Boot ROM	4K	4K	4K
Maximum Speed Grade[1]			400 MHz	
Maximum System Clock Speed			100 MHz	
Package Options		88-Lead LFCSP	88-Lead LFCSP	120-Lead LQFP

[1] Maximum speed grade is not available with every possible SCLK selection.

By integrating a rich set of industry-leading system peripherals and memory, Blackfin processors are the platform of choice for next-generation applications that require RISC-like programmability, multimedia support, and leading-edge signal processing in one integrated package.

PORTABLE LOW-POWER ARCHITECTURE

Blackfin processors provide world-class power management and performance. They are produced with a low-power and low-voltage design methodology and feature on-chip dynamic power management, which provides the ability to vary both the voltage and frequency of operation to significantly lower overall power consumption. This capability can result in a substantial reduction in power consumption, compared with just varying the frequency of operation. This allows longer battery life for portable appliances.

SYSTEM INTEGRATION

The ADSP-BF50x processors are highly integrated system-on-a-chip solutions for the next generation of embedded industrial, instrumentation, and power/motion control applications. By combining industry-standard interfaces with a high-performance signal processing core, cost-effective applications can be developed quickly, without the need for costly external components. The system peripherals include a watchdog timer; two 32-bit up/down counters with rotary support; eight 32-bit timers/counters with PWM support; six pairs of three-phase 16-bit center-based PWM units; two dual-channel, full-duplex synchronous serial ports (SPORTs); two serial peripheral interface (SPI) compatible ports; two UARTs with IrDA support; a parallel peripheral interface (PPI); a removable storage interface (RSI) controller; an internal ADC with 12 channels, 12 bits, up to 2 MSPS, and ACM controller; a controller area network (CAN) controller; a two-wire interface (TWI) controller; and an internal 32M bit flash.

PROCESSOR PERIPHERALS

The ADSP-BF50x processors contain a rich set of peripherals connected to the core via several high-bandwidth buses, providing flexibility in system configuration as well as excellent overall system performance (see the block diagram on Page 1). These Blackfin processors contain high-speed serial and parallel ports, an interrupt controller for flexible management of interrupts from the on-chip peripherals or external sources, and power management control functions to tailor the performance and power characteristics of the processor and system to many application scenarios.

The SPORT, SPI, UART, PPI, and RSI peripherals are supported by a flexible DMA structure. There are also separate memory DMA channels dedicated to data transfers between the processor's various memory spaces, including boot ROM and internal 32M bit synchronous burst flash. Multiple on-chip buses running at up to 100 MHz provide enough bandwidth to keep the processor core running along with activity on all of the on-chip and external peripherals.

The ADSP-BF50x processors include an interface to an off-chip voltage regulator in support of the processor's dynamic power management capability.

BLACKFIN PROCESSOR CORE

As shown in Figure 2, the Blackfin processor core contains two 16-bit multipliers, two 40-bit accumulators, two 40-bit ALUs, four video ALUs, and a 40-bit shifter. The computation units process 8-, 16-, or 32-bit data from the register file.

The compute register file contains eight 32-bit registers. When performing compute operations on 16-bit operand data, the register file operates as 16 independent 16-bit registers. All operands for compute operations come from the multiported register file and instruction constant fields.

Each MAC can perform a 16-bit by 16-bit multiply in each cycle, accumulating the results into the 40-bit accumulators. Signed and unsigned formats, rounding, and saturation are supported.

The ALUs perform a traditional set of arithmetic and logical operations on 16-bit or 32-bit data. In addition, many special instructions are included to accelerate various signal processing tasks. These include bit operations such as field extract and population count, modulo 2^{32} multiply, divide primitives, saturation and rounding, and sign/exponent detection. The set of video instructions include byte alignment and packing operations, 16-bit and 8-bit adds with clipping, 8-bit average operations, and 8-bit subtract/absolute value/accumulate (SAA) operations. Also provided are the compare/select and vector search instructions.

For certain instructions, two 16-bit ALU operations can be performed simultaneously on register pairs (a 16-bit high half and 16-bit low half of a compute register). If the second ALU is used, quad 16-bit operations are possible.

The 40-bit shifter can perform shifts and rotates and is used to support normalization, field extract, and field deposit instructions.

The program sequencer controls the flow of instruction execution, including instruction alignment and decoding. For program flow control, the sequencer supports PC relative and indirect conditional jumps (with static branch prediction), and subroutine calls. Hardware is provided to support zero-overhead looping. The architecture is fully interlocked, meaning that the programmer need not manage the pipeline when executing instructions with data dependencies.

The address arithmetic unit provides two addresses for simultaneous dual fetches from memory. It contains a multiported register file consisting of four sets of 32-bit index, modify, length, and base registers (for circular buffering), and eight additional 32-bit pointer registers (for C-style indexed stack manipulation).

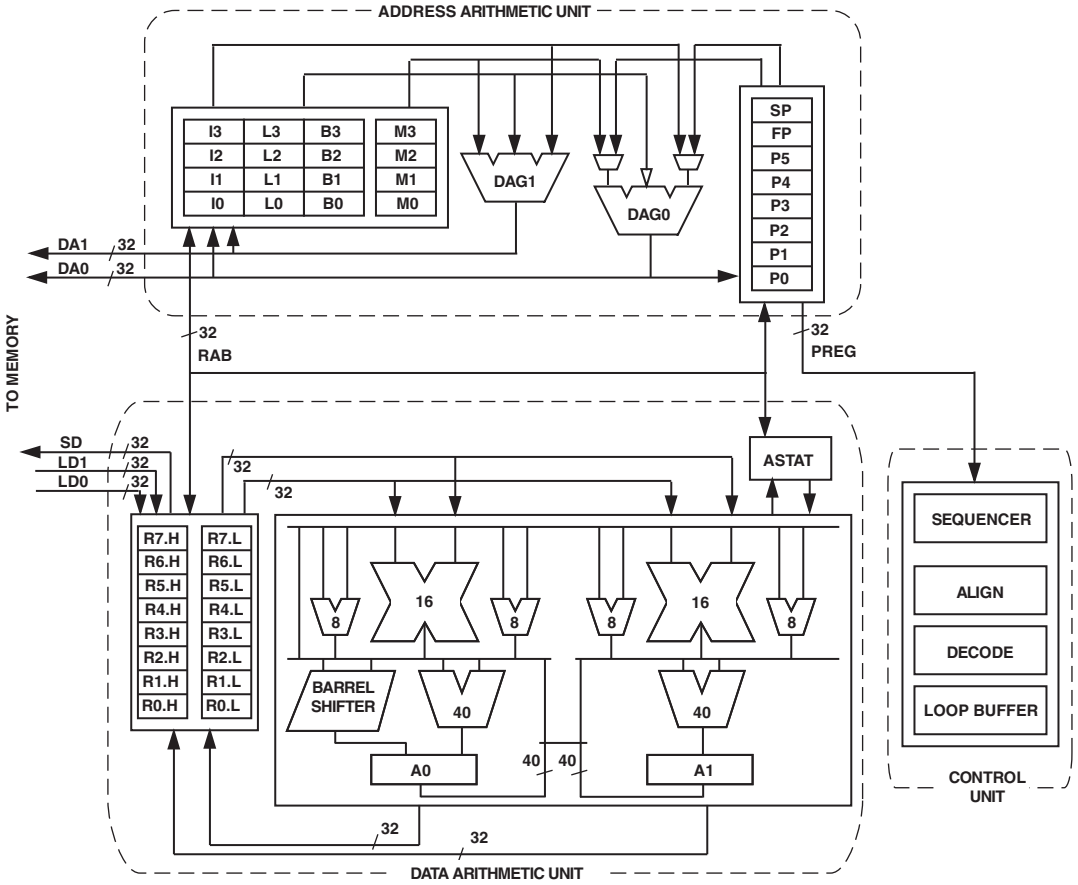


Figure 2. Blackfin Processor Core

Blackfin processors support a modified Harvard architecture in combination with a hierarchical memory structure. Level 1 (L1) memories are those that typically operate at the full processor speed with little or no latency. At the L1 level, the instruction memory holds instructions only. The data memory holds data, and a dedicated scratchpad data memory stores stack and local variable information.

In addition, multiple L1 memory blocks are provided, offering a configurable mix of SRAM and cache. The memory management unit (MMU) provides memory protection for individual tasks that may be operating on the core and can protect system registers from unintended access.

The architecture provides three modes of operation: user mode, supervisor mode, and emulation mode. User mode has restricted access to certain system resources, thus providing a protected software environment, while supervisor mode has unrestricted access to the system and core resources.

The Blackfin processor instruction set has been optimized so that 16-bit opcodes represent the most frequently used instructions, resulting in excellent compiled code density. Complex DSP instructions are encoded into 32-bit opcodes, representing fully featured multifunction instructions. Blackfin processors support a limited multi-issue capability, where a 32-bit instruction can be issued in parallel with two 16-bit instructions, allowing the programmer to use many of the core resources in a single instruction cycle.

The Blackfin processor assembly language uses an algebraic syntax for ease of coding and readability. The architecture has been optimized for use in conjunction with the C/C++ compiler, resulting in fast and efficient software implementations.

MEMORY ARCHITECTURE

The Blackfin processor views memory as a single unified 4G byte address space, using 32-bit addresses. All resources, including internal memory, external memory, and I/O control registers, occupy separate sections of this common address space. The memory portions of this address space are arranged in a hierarchical structure to provide a good cost/performance balance of some very fast, low-latency core-accessible memory as cache or SRAM, and larger, lower-cost and performance interface-accessible memory systems. See Figure 3.

The core-accessible L1 memory system is the highest-performance memory available to the Blackfin processor. The interface-accessible memory system, accessed through the external bus interface unit (EBIU), provides access to the internal flash memory and boot ROM.

The memory DMA controller provides high-bandwidth data-movement capability. It can perform block transfers of code or data between the internal memory and the external memory spaces.

Internal (Core-Accessible) Memory

The processor has three blocks of core-accessible memory, providing high-bandwidth access to the core.

The first block is the L1 instruction memory, consisting of 32K bytes SRAM, of which 16K bytes can be configured as a four-way set-associative cache. This memory is accessed at full processor speed.

The second core-accessible memory block is the L1 data memory, consisting of 32K bytes of SRAM, of which 16K bytes may be configured as cache. This memory block is accessed at full processor speed.

The third memory block is 4K bytes of scratchpad SRAM which runs at the same speed as the L1 memories, but is only accessible as data SRAM and cannot be configured as cache memory.

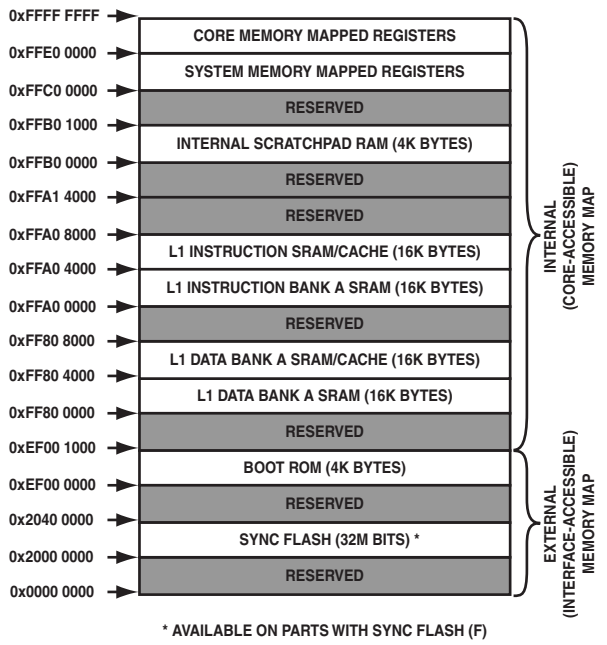


Figure 3. Internal/External Memory Map

External (Interface-Accessible) Memory

External memory is accessed via the EBIU memory port. This 16-bit interface provides a glueless connection to the internal flash memory and boot ROM. Internal flash memory ships from the factory in an erased state except for block 0 of the parameter bank. Block 0 of the Flash memory parameter bank ships from the factory in an unknown state. An erase operation should be performed prior to programming this block.

I/O Memory Space

The processor does not define a separate I/O space. All resources are mapped through the flat 32-bit address space. On-chip I/O devices have their control registers mapped into memory-mapped registers (MMRs) at addresses near the top of the 4G byte address space. These are separated into two smaller blocks, one which contains the control MMRs for all core functions, and the other which contains the registers needed for setup and control of the on-chip peripherals outside of the core. The MMRs are accessible only in supervisor and emulation modes and appear as reserved space to on-chip peripherals.

Booting

The processor contains a small on-chip boot kernel, which configures the appropriate peripheral for booting. If the processor is configured to boot from boot ROM memory space, the processor starts executing from the on-chip boot ROM. For more information, see Booting Modes on Page 16.

Event Handling

The event controller on the processor handles all asynchronous and synchronous events to the processor. The processor provides event handling that supports both nesting and prioritization. Nesting allows multiple event service routines to be active simultaneously. Prioritization ensures that servicing of a higher-priority event takes precedence over servicing of a lower-priority event. The controller provides support for five different types of events:

- Emulation – An emulation event causes the processor to enter emulation mode, allowing command and control of the processor via the JTAG interface.
- Reset – This event resets the processor.
- Nonmaskable Interrupt (NMI) – The NMI event can be generated either by the software watchdog timer, by the NMI input signal to the processor, or by software. The NMI event is frequently used as a power-down indicator to initiate an orderly shutdown of the system.
- Exceptions – Events that occur synchronously to program flow (in other words, the exception is taken before the instruction is allowed to complete). Conditions such as data alignment violations and undefined instructions cause exceptions.
- Interrupts – Events that occur asynchronously to program flow. They are caused by input signals, timers, and other peripherals, as well as by an explicit software instruction.

Each event type has an associated register to hold the return address and an associated return-from-event instruction. When an event is triggered, an interrupt service routine (ISR) must save the state of the processor to the supervisor stack.

The processor event controller consists of two stages: the core event controller (CEC) and the system interrupt controller (SIC). The core event controller works with the system interrupt controller to prioritize and control all system events. Conceptually, interrupts from the peripherals enter into the SIC and are then routed directly into the general-purpose interrupts of the CEC.

Core Event Controller (CEC)

The CEC supports nine general-purpose interrupts (IVG15–7), in addition to the dedicated interrupt and exception events. Of these general-purpose interrupts, the two lowest-priority interrupts (IVG15–14) are recommended to be reserved for software interrupt handlers, leaving seven prioritized interrupt inputs to support the peripherals of the processor. Table 2 describes the inputs to the CEC, identifies their names in the event vector table (EVT), and lists their priorities.

Table 2. Core Event Controller (CEC)

Priority (0 is Highest)	Event Class	EVT Entry
0	Emulation/Test Control	EMU
1	Reset	RST
2	Nonmaskable Interrupt	NMI
3	Exception	EVX
4	Reserved	—
5	Hardware Error	IVHW
6	Core Timer	IVTMR
7	General-Purpose Interrupt 7	IVG7
8	General-Purpose Interrupt 8	IVG8
9	General-Purpose Interrupt 9	IVG9
10	General-Purpose Interrupt 10	IVG10
11	General-Purpose Interrupt 11	IVG11
12	General-Purpose Interrupt 12	IVG12
13	General-Purpose Interrupt 13	IVG13
14	General-Purpose Interrupt 14	IVG14
15	General-Purpose Interrupt 15	IVG15

System Interrupt Controller (SIC)

The system interrupt controller provides the mapping and routing of events from the many peripheral interrupt sources to the prioritized general-purpose interrupt inputs of the CEC. Although the processor provides a default mapping, the user can alter the mappings and priorities of interrupt events by writing the appropriate values into the interrupt assignment registers (SIC_IARx). Table 3 describes the inputs into the SIC and the default mappings into the CEC.

Table 3. System Interrupt Controller (SIC)

Peripheral Interrupt Source	General Purpose Interrupt (at Reset)	Peripheral Interrupt ID	Default Core Interrupt ID	SIC Registers	
PLL Wakeup Interrupt	IVG7	0	0	IAR0	IMASK0, ISR0, IWR0
DMA Error (generic)	IVG7	1	0	IAR0	IMASK0, ISR0, IWR0
PPI Status	IVG7	2	0	IAR0	IMASK0, ISR0, IWR0
SPORT0 Status	IVG7	3	0	IAR0	IMASK0, ISR0, IWR0
SPORT1 Status	IVG7	4	0	IAR0	IMASK0, ISR0, IWR0
UART0 Status	IVG7	5	0	IAR0	IMASK0, ISR0, IWR0
UART1 Status	IVG7	6	0	IAR0	IMASK0, ISR0, IWR0
SPI0 Status	IVG7	7	0	IAR0	IMASK0, ISR0, IWR0
SPI1 Status	IVG7	8	0	IAR1	IMASK0, ISR0, IWR0
CAN Status	IVG7	9	0	IAR1	IMASK0, ISR0, IWR0
RSI Mask 0 Interrupt	IVG7	10	0	IAR1	IMASK0, ISR0, IWR0
Reserved	–	11	–	IAR1	IMASK0, ISR0, IWR0
CNT0 Interrupt	IVG8	12	1	IAR1	IMASK0, ISR0, IWR0
CNT1 Interrupt	IVG8	13	1	IAR1	IMASK0, ISR0, IWR0
DMA Channel 0 (PPI Rx/Tx)	IVG9	14	2	IAR1	IMASK0, ISR0, IWR0
DMA Channel 1 (RSI Rx/Tx)	IVG9	15	2	IAR1	IMASK0, ISR0, IWR0
DMA Channel 2 (SPORT0 Rx)	IVG9	16	2	IAR2	IMASK0, ISR0, IWR0
DMA Channel 3 (SPORT0 Tx)	IVG9	17	2	IAR2	IMASK0, ISR0, IWR0
DMA Channel 4 (SPORT1 Rx)	IVG9	18	2	IAR2	IMASK0, ISR0, IWR0
DMA Channel 5 (SPORT1 Tx)	IVG9	19	2	IAR2	IMASK0, ISR0, IWR0
DMA Channel 6 (SPI0 Rx/Tx)	IVG10	20	3	IAR2	IMASK0, ISR0, IWR0
DMA Channel 7 (SPI1 Rx/Tx)	IVG10	21	3	IAR2	IMASK0, ISR0, IWR0
DMA Channel 8 (UART0 Rx)	IVG10	22	3	IAR2	IMASK0, ISR0, IWR0
DMA Channel 9 (UART0 Tx)	IVG10	23	3	IAR2	IMASK0, ISR0, IWR0
DMA Channel 10 (UART1 Rx)	IVG10	24	3	IAR3	IMASK0, ISR0, IWR0
DMA Channel 11 (UART1 Tx)	IVG10	25	3	IAR3	IMASK0, ISR0, IWR0
CAN Receive	IVG11	26	4	IAR3	IMASK0, ISR0, IWR0
CAN Transmit	IVG11	27	4	IAR3	IMASK0, ISR0, IWR0
TWI	IVG11	28	4	IAR3	IMASK0, ISR0, IWR0
Port F Interrupt A	IVG11	29	4	IAR3	IMASK0, ISR0, IWR0
Port F Interrupt B	IVG11	30	4	IAR3	IMASK0, ISR0, IWR0
Reserved	–	31	–	IAR3	IMASK0, ISR0, IWR0
Timer 0	IVG12	32	5	IAR4	IMASK1, ISR1, IWR1
Timer 1	IVG12	33	5	IAR4	IMASK1, ISR1, IWR1
Timer 2	IVG12	34	5	IAR4	IMASK1, ISR1, IWR1
Timer 3	IVG12	35	5	IAR4	IMASK1, ISR1, IWR1
Timer 4	IVG12	36	5	IAR4	IMASK1, ISR1, IWR1
Timer 5	IVG12	37	5	IAR4	IMASK1, ISR1, IWR1
Timer 6	IVG12	38	5	IAR4	IMASK1, ISR1, IWR1
Timer 7	IVG12	39	5	IAR4	IMASK1, ISR1, IWR1
Port G Interrupt A	IVG12	40	5	IAR5	IMASK1, ISR1, IWR1

Table 3. System Interrupt Controller (SIC) (Continued)

Peripheral Interrupt Source	General Purpose Interrupt (at Reset)	Peripheral Interrupt ID	Default Core Interrupt ID	SIC Registers	
Port G Interrupt B	IVG12	41	5	IAR5	IMASK1, ISR1, IWR1
MDMA Stream 0	IVG13	42	6	IAR5	IMASK1, ISR1, IWR1
MDMA Stream 1	IVG13	43	6	IAR5	IMASK1, ISR1, IWR1
Software Watchdog Timer	IVG13	44	6	IAR5	IMASK1, ISR1, IWR1
Port H Interrupt A	IVG13	45	6	IAR5	IMASK1, ISR1, IWR1
Port H Interrupt B	IVG13	46	6	IAR5	IMASK1, ISR1, IWR1
ACM Status Interrupt	IVG7	47	0	IAR5	IMASK1, ISR1, IWR1
ACM Interrupt	IVG10	48	3	IAR6	IMASK1, ISR1, IWR1
Reserved	–	49	–	IAR6	IMASK1, ISR1, IWR1
Reserved	–	50	–	IAR6	IMASK1, ISR1, IWR1
PWM0 Trip Interrupt	IVG10	51	3	IAR6	IMASK1, ISR1, IWR1
PWM0 Sync Interrupt	IVG10	52	3	IAR6	IMASK1, ISR1, IWR1
PWM1 Trip Interrupt	IVG10	53	3	IAR6	IMASK1, ISR1, IWR1
PWM1 Sync Interrupt	IVG10	54	3	IAR6	IMASK1, ISR1, IWR1
RSI Mask 1 Interrupt	IVG10	55	3	IAR6	IMASK1, ISR1, IWR1
Reserved	–	56 through 63	–	–	IMASK1, ISR1, IWR1

Event Control

The processor provides a very flexible mechanism to control the processing of events. In the CEC, three registers are used to coordinate and control events. Each register is 16 bits wide.

- CEC interrupt latch register (ILAT) – Indicates when events have been latched. The appropriate bit is set when the processor has latched the event and is cleared when the event has been accepted into the system. This register is updated automatically by the controller, but it may be written only when its corresponding IMASK bit is cleared.
- CEC interrupt mask register (IMASK) – Controls the masking and unmasking of individual events. When a bit is set in the IMASK register, that event is unmasked and is processed by the CEC when asserted. A cleared bit in the IMASK register masks the event, preventing the processor from servicing the event even though the event may be latched in the ILAT register. This register may be read or written while in supervisor mode. (Note that general-purpose interrupts can be globally enabled and disabled with the STI and CLI instructions, respectively.)
- CEC interrupt pending register (IPEND) – The IPEND register keeps track of all nested events. A set bit in the IPEND register indicates the event is currently active or nested at some level. This register is updated automatically by the controller but may be read while in supervisor mode.

The SIC allows further control of event processing by providing three pairs of 32-bit interrupt control and status registers. Each register contains a bit, corresponding to each of the peripheral interrupt events shown in Table 3 on Page 7.

- SIC interrupt mask registers (SIC_IMASKx) – Control the masking and unmasking of each peripheral interrupt event. When a bit is set in these registers, the corresponding peripheral event is unmasked and is forwarded to the CEC when asserted. A cleared bit in these registers masks the corresponding peripheral event, preventing the event from propagating to the CEC.
- SIC interrupt status registers (SIC_ISRx) – As multiple peripherals can be mapped to a single event, these registers allow the software to determine which peripheral event source triggered the interrupt. A set bit indicates that the peripheral is asserting the interrupt, and a cleared bit indicates that the peripheral is not asserting the event.
- SIC interrupt wakeup enable registers (SIC_IWRx) – By enabling the corresponding bit in these registers, a peripheral can be configured to wake up the processor, should the core be idled or in sleep mode when the event is generated. For more information, see Dynamic Power Management on Page 13.

Because multiple interrupt sources can map to a single general-purpose interrupt, multiple pulse assertions can occur simultaneously, before or during interrupt processing for an interrupt event already detected on this interrupt input. The IPEND register contents are monitored by the SIC as the interrupt acknowledgement.

The appropriate ILAT register bit is set when an interrupt rising edge is detected (detection requires two core clock cycles). The bit is cleared when the respective IPEND register bit is set. The IPEND bit indicates that the event has entered into the processor pipeline. At this point the CEC recognizes and queues the next rising edge event on the corresponding event input. The minimum latency from the rising edge transition of the

general-purpose interrupt to the IPEND output asserted is three core clock cycles; however, the latency can be much higher, depending on the activity within and the state of the processor.

FLASH MEMORY

The ADSP-BF504F and ADSP-BF506F processors include an on-chip 32M bit (×16, multiple bank, burst) Flash memory. The features of this memory include:

- Synchronous/asynchronous read
  - Synchronous burst read mode: 50 MHz
  - Asynchronous/synchronous read mode
  - Random access times: 70 ns
- Synchronous burst read suspend
- Memory blocks
  - Multiple bank memory array: 4 Mbit banks
  - Parameter blocks (top location)
- Dual operations
  - Program erase in one bank while read in others
  - No delay between read and write operations
- Block locking
  - All blocks locked at power-up
  - Any combination of blocks can be locked or locked down
- Security
  - 128-bit user programmable OTP cells
  - 64-bit unique device number
- Common Flash interface (CFI)
- 100 000 program/erase cycles per block

Flash memory ships from the factory in an erased state *except* for block 0 of the parameter bank. Block 0 of the Flash memory parameter bank ships from the factory in an unknown state. An erase operation should be performed prior to programming this block.

DMA CONTROLLERS

The processor has multiple, independent DMA channels that support automated data transfers with minimal overhead for the processor core. DMA transfers can occur between the processor's internal memories and any of its DMA-capable peripherals. Additionally, DMA transfers can be accomplished between any of the DMA-capable peripherals and external devices connected to the external memory interface. DMA-capable peripherals include the SPORTs, SPI ports, UARTs, RSI, and PPI. Each individual DMA-capable peripheral has at least one dedicated DMA channel.

The processor DMA controller supports both one-dimensional (1-D) and two-dimensional (2-D) DMA transfers. DMA transfer initialization can be implemented from registers or from sets of parameters called descriptor blocks.

The 2-D DMA capability supports arbitrary row and column sizes up to 64K elements by 64K elements, and arbitrary row and column step sizes up to ±32K elements. Furthermore, the column step size can be less than the row step size, allowing implementation of interleaved data streams. This feature is especially useful in video applications where data can be de-interleaved on the fly.

Examples of DMA types supported by the processor DMA controller include:

- A single, linear buffer that stops upon completion
- A circular, auto-refreshing buffer that interrupts on each full or fractionally full buffer
- 1-D or 2-D DMA using a linked list of descriptors
- 2-D DMA using an array of descriptors, specifying only the base DMA address within a common page

In addition to the dedicated peripheral DMA channels, there are two memory DMA channels, which are provided for transfers between the various memories of the processor system with minimal processor intervention. Memory DMA transfers can be controlled by a very flexible descriptor-based methodology or by a standard register-based autobuffer mechanism.

WATCHDOG TIMER

The processor includes a 32-bit timer that can be used to implement a software watchdog function. A software watchdog can improve system availability by forcing the processor to a known state through generation of a core and system reset, nonmaskable interrupt (NMI), or general-purpose interrupt, if the timer expires before being reset by software. The programmer initializes the count value of the timer, enables the appropriate interrupt, then enables the timer. Thereafter, the software must reload the counter before it counts to zero from the programmed value. This protects the system from remaining in an unknown state where software, which would normally reset the timer, has stopped running due to an external noise condition or software error.

If configured to generate a reset, the watchdog timer resets both the core and the processor peripherals. After a reset, software can determine whether the watchdog was the source of the hardware reset by interrogating a status bit in the watchdog timer control register.

The timer is clocked by the system clock (SCLK), at a maximum frequency of f_{SCLK}.

TIMERS

There are nine general-purpose programmable timer units in the processors. Eight timers have an external pin that can be configured either as a pulse width modulator (PWM) or timer output, as an input to clock the timer, or as a mechanism for measuring pulse widths and periods of external events. These timers can be synchronized: to an external clock input to the several other associated PF pins, to an external clock input to the PPI_CLK input pin, or to the internal SCLK.

The timer units can be used in conjunction with the two UARTs to measure the width of the pulses in the data stream to provide a software auto-baud detect function for the respective serial channels.

The timers can generate interrupts to the processor core providing periodic events for synchronization, either to the system clock or to a count of external signals.

In addition to the eight general-purpose programmable timers, a ninth timer is also provided. This extra timer is clocked by the internal processor clock and is typically used as a system tick clock for generation of operating system periodic interrupts.

UP/DOWN COUNTERS AND THUMBWHEEL INTERFACES

Two 32-bit up/down counters are provided that can sense 2-bit quadrature or binary codes as typically emitted by industrial drives or manual thumbwheels. The counters can also operate in general-purpose up/down count modes. Then, count direction is either controlled by a level-sensitive input pin or by two edge detectors.

A third counter input can provide flexible zero marker support and can alternatively be used to input the push-button signal of thumb wheels. All three pins have a programmable debouncing circuit.

Internal signals forwarded to each timer unit enable these timers to measure the intervals between count events. Boundary registers enable auto-zero operation or simple system warning by interrupts when programmable count values are exceeded.

3-PHASE PWM UNITS

The two/dual 3-phase PWM generation units each feature:

- 16-bit center-based PWM generation unit
- Programmable PWM pulse width
- Single/double update modes
- Programmable dead time and switching frequency
- Twos-complement implementation which permits smooth transition to full ON and full OFF states
- Possibility to synchronize the PWM generation to either externally-generated or internally-generated synchronization pulses
- Special provisions for BDCM operation (crossover and output enable functions)
- Wide variety of special switched reluctance (SR) operating modes
- Output polarity and clock gating control
- Dedicated asynchronous PWM shutdown signal

Each PWM block integrates a flexible and programmable 3-phase PWM waveform generator that can be programmed to generate the required switching patterns to drive a 3-phase voltage source inverter for ac induction motor (ACIM) or permanent magnet synchronous motor (PMSM) control. In addition, the PWM block contains special functions that considerably simplify the generation of the required PWM switching patterns for control of the electronically commutated motor (ECM) or brushless dc motor (BDCM). Software can enable a special mode for switched reluctance motors (SRM).

The six PWM output signals (per PWM unit) consist of three high-side drive signals (PWMx_AH, PWMx_BH, and PWMx_CH) and three low-side drive signals (PWMx_AL, PWMx_BL, and PWMx_CL). The polarity of the generated PWM signal can be set with software, so that either active HI or active LO PWM patterns can be produced.

The switching frequency of the generated PWM pattern is programmable using the 16-bit PWM_TM register. The PWM generator can operate in single update mode or double update mode. In single update mode, the duty cycle values are programmable only once per PWM period, so that the resultant PWM patterns are symmetrical about the midpoint of the PWM period. In the double update mode, a second updating of the PWM registers is implemented at the midpoint of the PWM period. In this mode, it is possible to produce asymmetrical PWM patterns that produce lower harmonic distortion in 3-phase PWM inverters.

Pulses synchronous to the switching frequency can be generated internally and output on the PWMx_SYNC pin. The PWM unit can also accept externally generated synchronization pulses through PWMx_SYNC.

Each PWM unit features a dedicated asynchronous shutdown pin, $\overline{\text{PWMx\_TRIP}}$, which (when brought low) instantaneously places all six PWM outputs in the OFF state.

SERIAL PORTS

The processors incorporate two dual-channel synchronous serial ports (SPORT0 and SPORT1) for serial and multiprocessor communications. The SPORTs support the following features:

- I^2S capable operation.
- Bidirectional operation – Each SPORT has two sets of independent transmit and receive pins, enabling eight channels of I^2S stereo audio.
- Buffered (8-deep) transmit and receive ports – Each port has a data register for transferring data words to and from other processor components and shift registers for shifting data in and out of the data registers.
- Clocking – Each transmit and receive port can either use an external serial clock or generate its own, in frequencies ranging from (f_{SCLK}/131,070) Hz to (f_{SCLK}/2) Hz.
- Word length – Each SPORT supports serial data words from 3 to 32 bits in length, transferred most-significant-bit first or least-significant-bit first.
- Framing – Each transmit and receive port can run with or without frame sync signals for each data word. Frame sync signals can be generated internally or externally, active high or low, and with either of two pulse widths and early or late frame sync.

- Companding in hardware – Each SPORT can perform A-law or μ-law companding according to ITU recommendation G.711. Companding can be selected on the transmit and/or receive channel of the SPORT without additional latencies.
- DMA operations with single-cycle overhead – Each SPORT can automatically receive and transmit multiple buffers of memory data. The processor can link or chain sequences of DMA transfers between a SPORT and memory.
- Interrupts – Each transmit and receive port generates an interrupt upon completing the transfer of a data word or after transferring an entire data buffer, or buffers, through DMA.
- Multichannel capability – Each SPORT supports 128 channels out of a 1024-channel window and is compatible with the H.100, H.110, MVIP-90, and HMVIP standards.

SERIAL PERIPHERAL INTERFACE (SPI) PORTS

The ADSP-BF50x processors have two SPI-compatible ports that enable the processor to communicate with multiple SPI-compatible devices.

The SPI interface uses three pins for transferring data: two data pins MOSI (Master Output-Slave Input) and MISO (Master Input-Slave Output) and a clock pin, serial clock (SCK). An SPI chip select input pin ($\overline{\text{SPIx\_SS}}$) lets other SPI devices select the processor, and three SPI chip select output pins ($\overline{\text{SPIx\_SEL3–1}}$) let the processor select other SPI devices. The SPI select pins are reconfigured general-purpose I/O pins. Using these pins, the SPI port provides a full-duplex, synchronous serial interface, which supports both master/slave modes and multimaster environments.

The SPI port's baud rate and clock phase/polarities are programmable, and it has an integrated DMA channel, configurable to support transmit or receive data streams. The SPI's DMA channel can only service unidirectional accesses at any given time.

The SPI port's clock rate is calculated as:

$$SPI\ Clock\ Rate = \frac{f_{SCLK}}{2 \times SPI\_BAUD}$$

Where the 16-bit SPI_BAUD register contains a value of 2 to 65,535.

During transfers, the SPI port simultaneously transmits and receives by serially shifting data in and out on its two serial data lines. The serial clock line synchronizes the shifting and sampling of data on the two serial data lines.

UART PORTS (UARTS)

The ADSP-BF50x Blackfin processors provide two full-duplex universal asynchronous receiver/transmitter (UART) ports. Each UART port provides a simplified UART interface to other peripherals or hosts, enabling full-duplex, DMA-supported, asynchronous transfers of serial data. A UART port includes support for five to eight data bits, one or two stop bits, and none, even, or odd parity. Each UART port supports two modes of operation:

- PIO (programmed I/O). The processor sends or receives data by writing or reading I/O-mapped UART registers. The data is double-buffered on both transmit and receive.
- DMA (direct memory access). The DMA controller transfers both transmit and receive data. This reduces the number and frequency of interrupts required to transfer data to and from memory. Each UART has two dedicated DMA channels, one for transmit and one for receive. These DMA channels have lower default priority than most DMA channels because of their relatively low service rates. Flexible interrupt timing options are available on the transmit side.

Each UART port's baud rate, serial data format, error code generation and status, and interrupts are programmable:

- Supporting bit rates ranging from (f_{SCLK}/1,048,576) to (f_{SCLK}) bits per second.
- Supporting data formats from 7 to 12 bits per frame.
- Both transmit and receive operations can be configured to generate maskable interrupts to the processor.

The UART port's clock rate is calculated as

$$UART\ Clock\ Rate = \frac{f_{SCLK}}{16^{(1-EDBO)} \times UART\_Divisor}$$

Where the 16-bit UART divisor comes from the UARTx_DLH register (most significant 8 bits) and UARTx_DLL register (least significant eight bits), and the EDBO is a bit in the UARTx_GCTL register.

In conjunction with the general-purpose timer functions, autobaud detection is supported.

The UARTs feature a pair of $\overline{\text{UAx\_RTS}}$ (request to send) and $\overline{\text{UAx\_CTS}}$ (clear to send) signals for hardware flow purposes. The transmitter hardware is automatically prevented from sending further data when the $\overline{\text{UAx\_CTS}}$ input is de-asserted. The receiver can automatically de-assert its $\overline{\text{UAx\_RTS}}$ output when the enhanced receive FIFO exceeds a certain high-water level. The capabilities of the UARTs are further extended with support for the Infrared Data Association (IrDA®) Serial Infrared Physical Layer Link Specification (SIR) protocol.

PARALLEL PERIPHERAL INTERFACE (PPI)

The processor provides a parallel peripheral interface (PPI) that can connect directly to parallel A/D and D/A converters, video encoders and decoders, and other general-purpose peripherals. The PPI consists of a dedicated input clock pin, up to three frame synchronization pins, and up to 16 data pins. The input clock supports parallel data rates up to half the system clock rate and the synchronization signals can be configured as either inputs or outputs.

The PPI supports a variety of general-purpose and ITU-R 656 modes of operation. In general-purpose mode, the PPI provides half-duplex, bidirectional data transfer with up to 16 bits of data. Up to three frame synchronization signals are also provided. In ITU-R 656 mode, the PPI provides half-duplex bidirectional transfer of 8- or 10-bit video data. Additionally, on-chip decode of embedded start-of-line (SOL) and start-of-field (SOF) preamble packets is supported.

General-Purpose Mode Descriptions

The general-purpose modes of the PPI are intended to suit a wide variety of data capture and transmission applications. Three distinct submodes are supported:

- Input mode – Frame syncs and data are inputs into the PPI.
- Frame capture mode – Frame syncs are outputs from the PPI, but data are inputs.
- Output mode – Frame syncs and data are outputs from the PPI.

Input Mode

Input mode is intended for ADC applications, as well as video communication with hardware signaling. In its simplest form, PPI_FS1 is an external frame sync input that controls when to read data. The PPI_DELAY MMR allows for a delay (in PPI_CLK cycles) between reception of this frame sync and the initiation of data reads. The number of input data samples is user programmable and defined by the contents of the PPI_COUNT register. The PPI supports 8-bit and 10-bit through 16-bit data, programmable in the PPI_CONTROL register.

Frame Capture Mode

Frame capture mode allows the video source(s) to act as a slave (for frame capture for example). The ADSP-BF50x processors control when to read from the video source(s). PPI_FS1 is an HSYNC output and PPI_FS2 is a VSYNC output.

Output Mode

Output mode is used for transmitting video or other data with up to three output frame syncs. Typically, a single frame sync is appropriate for data converter applications, whereas two or three frame syncs could be used for sending video with hardware signaling.

ITU-R 656 Mode Descriptions

The ITU-R 656 modes of the PPI are intended to suit a wide variety of video capture, processing, and transmission applications. Three distinct submodes are supported:

- Active video only mode
- Vertical blanking only mode
- Entire field mode

Active Video Mode

Active video only mode is used when only the active video portion of a field is of interest and not any of the blanking intervals. The PPI does not read in any data between the end of active video (EAV) and start of active video (SAV) preamble symbols, or any data present during the vertical blanking intervals. In this mode, the control byte sequences are not stored to memory; they are filtered by the PPI. After synchronizing to the start of Field 1, the PPI ignores incoming samples until it sees an SAV code. The user specifies the number of active video lines per frame (in PPI_COUNT register).

Vertical Blanking Interval Mode

In this mode, the PPI only transfers vertical blanking interval (VBI) data.

Entire Field Mode

In this mode, the entire incoming bit stream is read in through the PPI. This includes active video, control preamble sequences, and ancillary data that may be embedded in horizontal and vertical blanking intervals. Data transfer starts immediately after synchronization to Field 1. Data is transferred to or from the synchronous channels through eight DMA engines that work autonomously from the processor core.

RSI INTERFACE

The removable storage interface (RSI) controller acts as the host interface for multimedia cards (MMC), secure digital memory cards (SD), secure digital input/output cards (SDIO), and CE-ATA hard disk drives. The following list describes the main features of the RSI controller.

- Support for a single MMC, SD memory, SDIO card or CE-ATA hard disk drive
- Support for 1-bit and 4-bit SD modes
- Support for 1-bit, 4-bit, and 8-bit MMC modes
- Support for 4-bit and 8-bit CE-ATA hard disk drives
- A ten-signal external interface with clock, command, and up to eight data lines
- Card detection using one of the data signals
- Card interface clock generation from SCLK
- SDIO interrupt and read wait features
- CE-ATA command completion signal recognition and disable

CONTROLLER AREA NETWORK (CAN) INTERFACE

The ADSP-BF50x processors provide a CAN controller that is a communication controller implementing the Controller Area Network (CAN) V2.0B protocol. This protocol is an asynchronous communications protocol used in both industrial and automotive control systems. CAN is well suited for control applications due to its capability to communicate reliably over a network since the protocol incorporates CRC checking, message error tracking, and fault node confinement.

The CAN controller is based on a 32-entry mailbox RAM and supports both the standard and extended identifier (ID) message formats specified in the CAN protocol specification, revision 2.0, part B.

Each mailbox consists of eight 16-bit data words. The data is divided into fields, which includes a message identifier, a time stamp, a byte count, up to 8 bytes of data, and several control bits. Each node monitors the messages being passed on the network. If the identifier in the transmitted message matches an identifier in one of its mailboxes, the module knows that the message was meant for it, passes the data into its appropriate mailbox, and signals the processor of message arrival with an interrupt.

The CAN controller can wake up the processor from sleep mode upon generation of a wake-up event, such that the processor can be maintained in a low-power mode during idle conditions. Additionally, a CAN wake-up event can wake up the on-chip internal voltage regulator from the powered-down hibernate state.

The electrical characteristics of each network connection are very stringent. Therefore, the CAN interface is typically divided into two parts: a controller and a transceiver. This allows a single controller to support different drivers and CAN networks. The ADSP-BF50x CAN module represents the controller part of the interface. This module's network I/O is a single transmit output and a single receive input, which connect to a line transceiver.

The CAN clock is derived from the processor system clock (SCLK) through a programmable divider and therefore does not require an additional crystal.

TWI CONTROLLER INTERFACE

The processors include a two-wire interface (TWI) module for providing a simple exchange method of control data between multiple devices. The TWI is compatible with the widely used $I^2C^®$ bus standard. The TWI module offers the capabilities of simultaneous master and slave operation, support for both 7-bit addressing and multimedia data arbitration. The TWI interface utilizes two pins for transferring clock (SCL) and data (SDA) and supports the protocol at speeds up to 400K bits/sec. The TWI interface pins are compatible with 5 V logic levels.

Additionally, the TWI module is fully compatible with serial camera control bus (SCCB) functionality for easier control of various CMOS camera sensor devices.

PORTS

Because of the rich set of peripherals, the processor groups the many peripheral signals to three ports—Port F, Port G, and Port H. Most of the associated pins are shared by multiple signals. The ports function as multiplexer controls.

General-Purpose I/O (GPIO)

The processor has 35 bidirectional, general-purpose I/O (GPIO) pins allocated across three separate GPIO modules—PORTFIO, PORTGIO, and PORTHIO, associated with Port F, Port G, and Port H, respectively. Each GPIO-capable pin shares functionality with other processor peripherals via a multiplexing scheme; however, the GPIO functionality is the default state of the device upon power-up. Neither GPIO output nor input drivers are active by default. Each general-purpose port pin can be individually controlled by manipulation of the port control, status, and interrupt registers:

- GPIO direction control register – Specifies the direction of each individual GPIO pin as input or output.
- GPIO control and status registers – The processor employs a "write one to modify" mechanism that allows any combination of individual GPIO pins to be modified in a single instruction, without affecting the level of any other GPIO pins. Four control registers are provided. One register is written in order to set pin values, one register is written in order to clear pin values, one register is written in order to toggle pin values, and one register is written in order to specify a pin value. Reading the GPIO status register allows software to interrogate the sense of the pins.
- GPIO interrupt mask registers – The two GPIO interrupt mask registers allow each individual GPIO pin to function as an interrupt to the processor. Similar to the two GPIO control registers that are used to set and clear individual pin values, one GPIO interrupt mask register sets bits to enable interrupt function, and the other GPIO interrupt mask register clears bits to disable interrupt function. GPIO pins defined as inputs can be configured to generate hardware interrupts, while output pins can be triggered by software interrupts.
- GPIO interrupt sensitivity registers – The two GPIO interrupt sensitivity registers specify whether individual pins are level- or edge-sensitive and specify—if edge-sensitive—whether just the rising edge or both the rising and falling edges of the signal are significant. One register selects the type of sensitivity, and one register selects which edges are significant for edge-sensitivity.

DYNAMIC POWER MANAGEMENT

The processor provides five operating modes, each with a different performance/power profile. In addition, dynamic power management provides the control functions to dynamically alter the processor core supply voltage, further reducing power dissipation. When configured for a 0 volt core supply voltage, the processor enters the hibernate state. Control of clocking to each of the processor peripherals also reduces power consumption. See Table 4 for a summary of the power settings for each mode.

Full-On Operating Mode—Maximum Performance

In the full-on mode, the PLL is enabled and is not bypassed, providing capability for maximum operational frequency. This is the power-up default execution state in which maximum performance can be achieved. The processor core and all enabled peripherals run at full speed.

Active Operating Mode—Moderate Dynamic Power Savings

In the active mode, the PLL is enabled but bypassed. Because the PLL is bypassed, the processor's core clock (CCLK) and system clock (SCLK) run at the input clock (CLKIN) frequency. DMA access is available to appropriately configured L1 memories.

In the active mode, it is possible to disable the control input to the PLL by setting the PLL_OFF bit in the PLL control register. This register can be accessed with a user-callable routine in the on-chip ROM called bfrom_SysControl(). If disabled, the PLL control input must be re-enabled before transitioning to the full-on or sleep modes.

Table 4. Power Settings

Mode/State	PLL	PLL Bypassed	Core Clock (CCLK)	System Clock (SCLK)	Core Power
Full On	Enabled	No	Enabled	Enabled	On
Active	Enabled/ Disabled	Yes	Enabled	Enabled	On
Sleep	Enabled	—	Disabled	Enabled	On
Deep Sleep	Disabled	—	Disabled	Disabled	On
Hibernate	Disabled	—	Disabled	Disabled	Off

For more information about PLL controls, see the "Dynamic Power Management" chapter in the *ADSP-BF50x Blackfin Processor Hardware Reference*.

Sleep Operating Mode—High Dynamic Power Savings

The sleep mode reduces dynamic power dissipation by disabling the clock to the processor core (CCLK). The PLL and system clock (SCLK), however, continue to operate in this mode. Typically, an external event wakes up the processor. When in the sleep mode, asserting a wakeup enabled in the SIC_IWRx registers causes the processor to sense the value of the BYPASS bit in the PLL control register (PLL_CTL). If BYPASS is disabled, the processor transitions to the full on mode. If BYPASS is enabled, the processor transitions to the active mode.

DMA accesses to L1 memory are not supported in sleep mode.

Deep Sleep Operating Mode—Maximum Dynamic Power Savings

The deep sleep mode maximizes dynamic power savings by disabling the clocks to the processor core (CCLK) and to all synchronous peripherals (SCLK). Asynchronous peripherals may still be running but cannot access internal resources or external memory. This powered-down mode can only be exited by assertion of the reset pin ($\overline{\text{RESET}}$). Assertion of $\overline{\text{RESET}}$ while in deep sleep mode causes the processor to transition to the full on mode.

Hibernate State—Maximum Static Power Savings

The hibernate state maximizes static power savings by disabling the voltage and clocks to the processor core (CCLK) and to all of the peripherals (SCLK). This setting sets the internal power supply voltage (V_{DDINT}) to 0 V to provide the lowest static power dissipation. Any critical information stored internally (for example, memory contents, register contents, and other information) must be written to a non-volatile storage device prior to removing power if the processor state is to be preserved.

Writing 0 to the HIBERNATE bit causes EXT_WAKE to transition low, which can be used to signal an external voltage regulator to shut down.

Since V_{DDEXT} can still be supplied in this mode, all of the external pins three-state, unless otherwise specified. This allows other devices that may be connected to the processor to still have power applied without drawing unwanted current.

The processor can be woken up by asserting the $\overline{\text{RESET}}$ pin. All hibernate wakeup events initiate the hardware reset sequence. Individual sources are enabled by the VR_CTL register. The EXT_WAKE signal indicates the occurrence of a wakeup event.

As long as V_{DDEXT} is applied, the VR_CTL register maintains its state during hibernation. All other internal registers and memories, however, lose their content in the hibernate state.

Power Savings

As shown in Table 5, the processor supports three different power domains, which maximizes flexibility while maintaining compliance with industry standards and conventions. By isolating the internal logic of the processor into its own power domain, separate from other I/O, the processor can take advantage of dynamic power management without affecting the other I/O devices. There are no sequencing requirements for the various power domains, but all domains must be powered according to the appropriate Processor — Specifications table for processor operating conditions; even if the feature/peripheral is not used.

Table 5. Power Domains

Power Domain	Power Supply
All internal logic, except Memory	V_{DDINT}
Flash Memory	$V_{DDFLASH}$
All other I/O	V_{DDEXT}
ADC digital supply[1] (Logic, I/O)	DV_{DD}, V_{DRIVE}
ADC analog supply[1]	AV_{DD}

[1] On ADSP-BF506F processor only.

The dynamic power management feature of the processor allows both the processor's input voltage (V_{DDINT}) and clock frequency (f_{CCLK}) to be dynamically controlled.

The power dissipated by a processor is largely a function of its clock frequency and the square of the operating voltage. For example, reducing the clock frequency by 25% results in a 25% reduction in dynamic power dissipation, while reducing the voltage by 25% reduces dynamic power dissipation by more than 40%. Further, these power savings are additive, in that if the clock frequency and supply voltage are both reduced, the power savings can be dramatic, as shown in the following equations.

Power Savings Factor

$$= \frac{f_{CCLKRED}}{f_{CCLKNOM}} \times \left(\frac{V_{DDINTRED}}{V_{DDINTNOM}}\right)^2 \times \left(\frac{T_{RED}}{T_{NOM}}\right)$$

$$\% \ Power \ Savings \ = \ (1 - Power \ Savings \ Factor) \times 100\%$$

where the variables in the equations are:

$f_{CCLKNOM}$ is the nominal core clock frequency

$f_{CCLKRED}$ is the reduced core clock frequency

$V_{DDINTNOM}$ is the nominal internal supply voltage

$V_{DDINTRED}$ is the reduced internal supply voltage

T_{NOM} is the duration running at $f_{CCLKNOM}$

T_{RED} is the duration running at $f_{CCLKRED}$

ADSP-BF50X VOLTAGE REGULATION

The ADSP-BF50x processors require an external voltage regulator to power the V_{DDINT} domain. To reduce standby power consumption, the external voltage regulator can be signaled through EXT_WAKE to remove power from the processor core. This signal is high-true for power-up and may be connected directly to the low-true shut-down input of many common regulators.

While in the hibernate state, all external supplies (V_{DDEXT}, $V_{DDFLASH}$) can still be applied, eliminating the need for external buffers. The external voltage regulator can be activated from this power down state by asserting the $\overline{\text{RESET}}$ pin, which then initiates a boot sequence. EXT_WAKE indicates a wakeup to the external voltage regulator.

The power good ($\overline{\text{PG}}$) input signal allows the processor to start only after the internal voltage has reached a chosen level. In this way, the startup time of the external regulator is detected after hibernation. For a complete description of the power good functionality, refer to the *ADSP-BF50x Blackfin Processor Hardware Reference*.

CLOCK SIGNALS

The processor can be clocked by an external crystal, a sine wave input, or a buffered, shaped clock derived from an external clock oscillator.

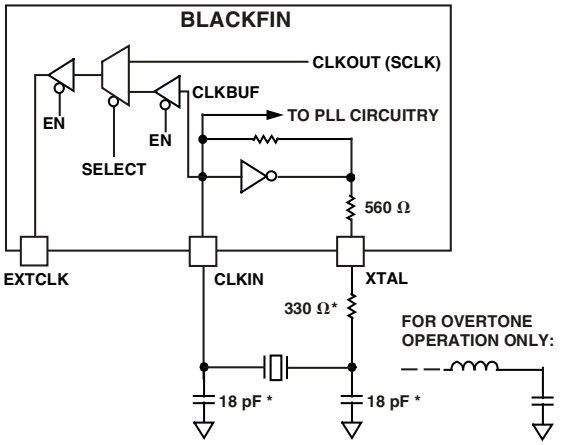
If an external clock is used, it should be a TTL-compatible signal and must not be halted, changed, or operated below the specified frequency during normal operation. This signal is connected to the processor's CLKIN pin. When an external clock is used, the XTAL pin must be left unconnected.

Alternatively, because the processor includes an on-chip oscillator circuit, an external crystal may be used. For fundamental frequency operation, use the circuit shown in Figure 4. A parallel-resonant, fundamental frequency, microprocessor-grade crystal is connected across the CLKIN and XTAL pins. The on-chip resistance between CLKIN and the XTAL pin is in the 500 kΩ range. Further parallel resistors are typically not recommended. The two capacitors and the series resistor shown in Figure 4 fine tune phase and amplitude of the sine frequency.

The capacitor and resistor values shown in Figure 4 are typical values only. The capacitor values are dependent upon the crystal manufacturers' load capacitance recommendations and the PCB physical layout. The resistor value depends on the drive level specified by the crystal manufacturer. The user should verify the customized values based on careful investigations on multiple devices over temperature range.

A third-overtone crystal can be used for frequencies above 25 MHz. The circuit is then modified to ensure crystal operation only at the third overtone, by adding a tuned inductor circuit as shown in Figure 4. A design procedure for third-overtone operation is discussed in detail in application note *(EE-168) Using Third Overtone Crystals with the ADSP-218x DSP* on the Analog Devices website (www.analog.com)—use site search on "EE-168."

The Blackfin core runs at a different clock rate than the on-chip peripherals. As shown in Figure 5, the core clock (CCLK) and system peripheral clock (SCLK) are derived from the input clock (CLKIN) signal. An on-chip PLL is capable of multiplying the CLKIN signal by a programmable multiplication factor (bounded by specified minimum and maximum VCO frequencies). The default multiplier is 6×, but it can be modified by a software instruction sequence.



NOTE: VALUES MARKED WITH * MUST BE CUSTOMIZED, DEPENDING ON THE CRYSTAL AND LAYOUT. PLEASE ANALYZE CAREFULLY. FOR FREQUENCIES ABOVE 33 MHz, THE SUGGESTED CAPACITOR VALUE OF 18 pF SHOULD BE TREATED AS A MAXIMUM, AND THE SUGGESTED RESISTOR VALUE SHOULD BE REDUCED TO 0 Ω.

Figure 4. External Crystal Connections

On-the-fly frequency changes can be effected by simply writing to the PLL_DIV register. The maximum allowed CCLK and SCLK rates depend on the applied voltages V_{DDINT} and V_{DDEXT}; the VCO is always permitted to run up to the CCLK frequency specified by the part's speed grade. The EXTCLK pin can be configured to output either the SCLK frequency or the input buffered CLKIN frequency, called CLKBUF. When configured to output SCLK (CLKOUT), the EXTCLK pin acts as a reference signal in many timing specifications. While active by default, it can be disabled using the EBIU_AMGCTL register.

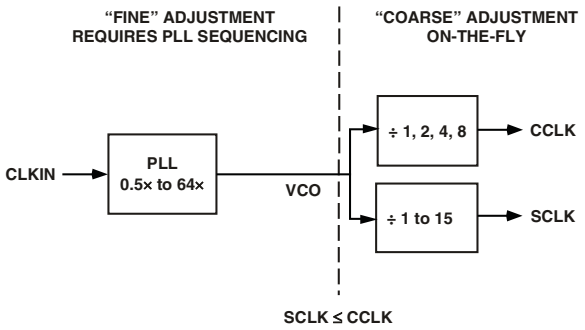


Figure 5. Frequency Modification Methods

All on-chip peripherals are clocked by the system clock (SCLK). The system clock frequency is programmable by means of the SSEL3–0 bits of the PLL_DIV register. The values programmed into the SSEL fields define a divide ratio between the PLL output (VCO) and the system clock. SCLK divider values are 1 through 15. Table 6 illustrates typical system clock ratios.

Note that the divisor ratio must be chosen to limit the system clock frequency to its maximum of f_{SCLK}. The SSEL value can be changed dynamically without any PLL lock latencies by writing the appropriate values to the PLL divisor register (PLL_DIV).

Table 6. Example System Clock Ratios

Signal Name SSEL3–0	Divider Ratio VCO/SCLK	Example Frequency Ratios (MHz)	
		VCO	SCLK
0001	1:1	50	50
0110	6:1	300	50
1010	10:1	400	40

The core clock (CCLK) frequency can also be dynamically changed by means of the CSEL1–0 bits of the PLL_DIV register. Supported CCLK divider ratios are 1, 2, 4, and 8, as shown in Table 7. This programmable core clock capability is useful for fast core frequency modifications.

Table 7. Core Clock Ratios

Signal Name CSEL1–0	Divider Ratio VCO/CCLK	Example Frequency Ratios (MHz)	
		VCO	CCLK
00	1:1	300	300
01	2:1	300	150
10	4:1	400	100
11	8:1	200	25

The maximum CCLK frequency *both* depends on the part's speed grade (see Page 79) *and* depends on the applied V_{DDINT} voltage. See Table 14 for details. The maximal system clock rate (SCLK) depends on the applied V_{DDINT} and V_{DDEXT} voltages (see Table 16).

BOOTING MODES

The processor has several mechanisms (listed in Table 8) for automatically loading internal and external memory after a reset. The boot mode is defined by the BMODE input pins dedicated to this purpose. There are two categories of boot modes. In master boot modes, the processor actively loads data from parallel or serial memories. In slave boot modes, the processor receives data from external host devices.

Table 8. Booting Modes

BMODE2–0	Description
000	Idle/No Boot
001	Boot from internal parallel flash in async mode[1]
010	Boot from internal parallel flash in sync mode[1]
011	Boot through SPI0 master from SPI memory
100	Boot through SPI0 slave from host device
101	Boot through PPI from host
110	Reserved
111	Boot through UART0 slave from host device

[1] This boot mode supported on ADSP-BF504F and ADSP-BF506F processor only.

The boot modes listed in Table 8 provide a number of mechanisms for automatically loading the processor's internal and external memories after a reset. By default, all boot modes use the slowest meaningful configuration settings. Default settings can be altered via the initialization code feature at boot time. Some boot modes require a boot host wait (HWAIT) signal, which is a GPIO output signal that is driven and toggled by the boot kernel at boot time. If pulled high through an external pull-up resistor, the HWAIT signal behaves active high and will be driven low when the processor is ready for data. Conversely, when pulled low, HWAIT is driven high when the processor is ready for data. When the boot sequence completes, the HWAIT pin can be used for other purposes. The BMODE pins of the reset configuration register, sampled during power-on resets and software-initiated resets, implement the modes shown in Table 8.

- IDLE State / No Boot (BMODE = 0x0) — In this mode, the boot kernel transitions the processor into Idle state. The processor can then be controlled through JTAG for recovery, debug, or other functions.
- Boot from stacked parallel flash in 16-bit asynchronous mode (BMODE = 0x1) — In this mode, the boot kernel starts booting from address 0x2000 0000.
- Boot from stacked parallel flash in 16-bit synchronous mode (BMODE = 0x2) — In this mode, the boot kernel loads the first block header from address 0x2000 0000. Boot kernel operation from this point is TBD.
- Boot from serial SPI memory, EEPROM or flash (BMODE = 0x3) — 8-, 16-, 24-, or 32-bit addressable devices are supported. The processor uses the PF13 GPIO pin to select a single SPI EEPROM/flash device (connected to the SPI0 interface) and submits a read command and successive address bytes (0x00) until a valid 8-, 16-, 24-, or

32-bit addressable device is detected. Pull-up resistors are required on the SPI0_SEL1 and MISO pins. By default, a value of 0x85 is written to the SPI_BAUD register.

- Boot from SPI host device (BMODE = 0x4) — The processor operates in SPI slave mode and is configured to receive the bytes of the LDR file from an SPI host (master) agent. The HWAIT signal must be interrogated by the host before every transmitted byte. A pull-up resistor is required on the SPI0_SS input. A pull-down on the serial clock (SCK) may improve signal quality and booting robustness.
- Boot from PPI host device (BMODE = 0x5) — The processor operates in PPI slave mode and is configured to receive the bytes of the LDR file from a PPI host (master) agent.
- Boot from UART0 host on Port G (BMODE = 0x7) — Using an autobaud handshake sequence, a boot-stream formatted program is downloaded by the host. The host selects a bit rate within the UART clocking capabilities.

  When performing the autobaud detection, the UART expects an "@" (0x40) character (eight bits data, one start bit, one stop bit, no parity bit) on the UA0_RX pin to determine the bit rate. The UART then replies with an acknowledgement composed of 4 bytes (0xBF, the value of UART0_DLL, the value of UART0_DLH, then 0x00). The host can then download the boot stream. The processor deasserts the UA0_RTS output to hold off the host; UA0_CTS functionality is not enabled at boot time.

For each of the boot modes, a 16-byte header is first read from an external memory device. The header specifies the number of bytes to be transferred and the memory destination address. Multiple memory blocks may be loaded by any boot sequence. Once all blocks are loaded, program execution commences from the address stored in the EVT1 register.

The boot kernel differentiates between a regular hardware reset and a wakeup-from-hibernate event to speed up booting in the later case. Bits 6-4 in the system reset configuration (SYSCR) register can be used to bypass the pre-boot routine and/or boot kernel in case of a software reset. They can also be used to simulate a wakeup-from-hibernate boot in the software reset case.

The boot process can be further customized by "initialization code." This is a piece of code that is loaded and executed prior to the regular application boot. Typically, this is used to speed up booting by managing the PLL, clock frequencies, wait states, or serial bit rates.

The boot ROM also features C-callable function that can be called by the user application at run time. This enables second-stage boot or boot management schemes to be implemented with ease.

INSTRUCTION SET DESCRIPTION

The Blackfin processor family assembly language instruction set employs an algebraic syntax designed for ease of coding and readability. The instructions have been specifically tuned to provide a flexible, densely encoded instruction set that compiles to a very small final memory size. The instruction set also provides fully featured multifunction instructions that allow the programmer to use many of the processor core resources in a single instruction. Coupled with many features more often seen on microcontrollers, this instruction set is very efficient when compiling C and C++ source code. In addition, the architecture supports both user (algorithm/application code) and supervisor (O/S kernel, device drivers, debuggers, ISRs) modes of operation, allowing multiple levels of access to core processor resources.

The assembly language, which takes advantage of the processor's unique architecture, offers the following advantages:

- Seamlessly integrated DSP/MCU features are optimized for both 8-bit and 16-bit operations.
- A multi-issue load/store modified-Harvard architecture, which supports two 16-bit MAC or four 8-bit ALU + two load/store + two pointer updates per cycle.
- All registers, I/O, and memory are mapped into a unified 4G byte memory space, providing a simplified programming model.
- Microcontroller features, such as arbitrary bit and bit-field manipulation, insertion, and extraction; integer operations on 8-, 16-, and 32-bit data-types; and separate user and supervisor stack pointers.
- Code density enhancements, which include intermixing of 16-bit and 32-bit instructions (no mode switching, no code segregation). Frequently used instructions are encoded in 16 bits.

DEVELOPMENT TOOLS

The processor is supported with a complete set of CROSSCORE® software and hardware development tools, including Analog Devices emulators and VisualDSP++® development environment. The same emulator hardware that supports other Blackfin processors also fully emulates the ADSP-BF50x processors.

EZ-KIT Lite® Evaluation Board

For evaluation of ADSP-BF50x processors, use the EZ-KIT Lite boards *soon to be* available from Analog Devices. *When these evaluation kits are available,* order using part number ADZS-BF506-EZLITE. The boards come with on-chip emulation capabilities and is equipped to enable software development. Multiple daughter cards *will be* available.

DESIGNING AN EMULATOR-COMPATIBLE PROCESSOR BOARD (TARGET)

The Analog Devices family of emulators are tools that every system developer needs in order to test and debug hardware and software systems. Analog Devices has supplied an IEEE 1149.1 JTAG Test Access Port (TAP) on each JTAG processor. The emulator uses the TAP to access the internal features of the processor, allowing the developer to load code, set breakpoints, observe variables, observe memory, and examine registers. The processor must be halted to send data and commands, but once an operation has been completed by the emulator, the processor system is set running at full speed with no impact on system timing.

To use these emulators, the target board must include a header that connects the processor's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, multiprocessor scan chains, signal buffering, signal termination, and emulator pod logic, see *(EE-68) Analog Devices JTAG Emulation Technical Reference* on the Analog Devices website (www.analog.com)—use site search on "EE-68." This document is updated regularly to keep pace with improvements to emulator support.

ADC AND ACM INTERFACE

This section describes the ADC and ACM interface. System designers should also consult the *ADSP-BF50x Blackfin Processor Hardware Reference* for additional information.

The ADC control module (ACM) provides an interface that synchronizes the controls between the processor and the internal analog-to-digital converter (ADC) module. The ACM is available on the ADSP-BF504, ADSP-BF504F, and ADSP-BF506F processors, and the ADC is available on the ADSP-BF506F processor only. The analog-to-digital conversions are initiated by the processor, based on external or internal events.

The ACM allows for flexible scheduling of sampling instants and provides precise sampling signals to the ADC.

The ACM synchronizes the ADC conversion process; generating the ADC controls, the ADC conversion start signal, and other signals. The actual data acquisition from the ADC is done by the SPORT peripherals.

The serial interface on the ADC allows the part to be directly connected to the ADSP-BF504, ADSP-BF504F, and ADSP-BF506F processors using serial interface protocols.

Figure 6 shows how to connect an external ADC to the ACM and one of the two SPORTs on the ADSP-BF504 or ADSP-BF504F processors.

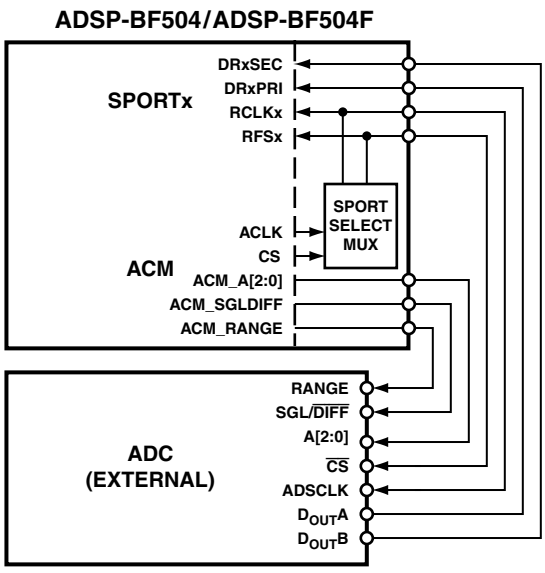


Figure 6. ADC (External), ACM, and SPORT Connections

The ADC is integrated into the ADSP-BF506F product. Figure 7 shows how to connect the internal ADC to the ACM and to one of the two SPORTs on the ADSP-BF506F processor.

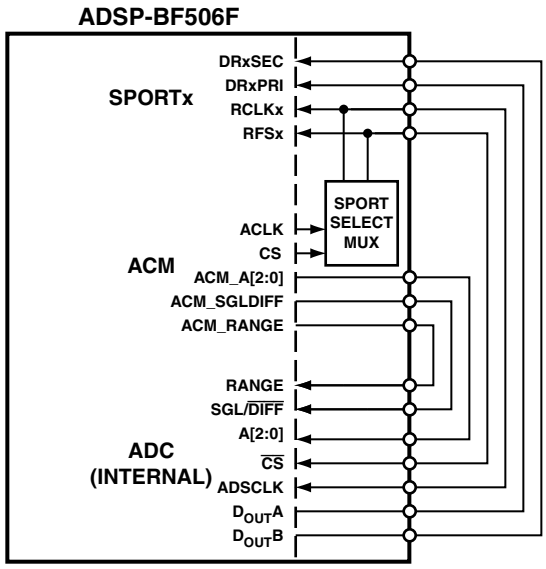


Figure 7. ADC (Internal), ACM, and SPORT Connections

The ADSP-BF504, ADSP-BF504F, and ADSP-BF506F processors interface directly to the ADC without any glue logic required. The availability of secondary receive registers on the serial ports of the Blackfin processors means only one serial port is necessary to read from both D_{OUT} pins simultaneously. Figure 7 (ADC (Internal), ACM, and SPORT Connections) shows both $D_{OUT}A$ and $D_{OUT}B$ of the ADC connected to one of the processor's serial ports. The SPORTx Receive Configuration 1 register and SPORTx Receive Configuration 2 register should be set up as outlined in Table 9 (The SPORTx Receive Configuration 1 Register (SPORTx_RCR1)) and Table 10 (The SPORTx Receive Configuration 2 Register (SPORTx_RCR2)).

Table 9. The SPORTx Receive Configuration 1 Register (SPORTx_RCR1)

Setting	Description
RCKFE = 1	Sample data with rising edge of RSCLK
LRFS = 1	Active low frame signal
RFSR = 1	Frame every word
IRFS = 0	External RFS used
RLSBIT = 0	Receive MSB first
RDTYPE = 00	Zero fill
IRCLK = 0	External receive clock
RSPEN = 1	Receive enabled
TFSR = RFSR = 1	

NOTE: The SPORT must be enabled with the following settings: external clock, external frame sync, and active low frame sync.

Table 10. The SPORTx Receive Configuration 2 Register (SPORTx_RCR2)

Setting	Description
RXSE = 1	Secondary side enabled
SLEN = 1111	16-bit data-word (or may be set to 1101 for 14-bit data-word)

To implement the power-down modes, SLEN should be set to 1001 to issue an 8-bit SCLK burst. A Blackfin driver for the ADC is available to download at www.analog.com.

INTERNAL ADC

An ADC is integrated into the ADSP-BF506F product. All ADC signals are connected out to package pins to enable maximum interconnect flexibility in mixed signal applications.

The internal ADC is a dual, 12-bit, high speed, low power, successive approximation ADC that operates from a single 2.7 V to 5.25 V power supply and features throughput rates up to 2 MSPS. The device contains two ADCs, each preceded by a 3-channel multiplexer, and a low noise, wide bandwidth track-and-hold amplifier that can handle input frequencies in excess of 30 MHz.

Figure 8 shows the functional block diagram of the internal ADC. The ADC features include:

- Dual 12-bit, 3-channel ADC
- Throughput rate: up to 2 MSPS
- Specified for DV_{DD} and AV_{DD} of 2.7 V to 5.25 V
- Pin-configurable analog inputs
  - 12-channel single-ended inputs
    or
  - 6-channel fully differential inputs
    or
  - 6-channel pseudo differential inputs
- Accurate on-chip voltage reference: 2.5 V
- Dual conversion with read 437.5 ns, 32 MHz ADSCLK
- High speed serial interface
  - SPI®-/QSPI™-/MICROWIRE™-/DSP-compatible
- Low power shutdown mode

The conversion process and data acquisition use standard control inputs allowing easy interfacing to microprocessors or DSPs. The input signal is sampled on the falling edge of $\overline{CS}$; conversion is also initiated at this point. The conversion time is determined by the ADSCLK frequency. There are no pipelined delays associated with the part.

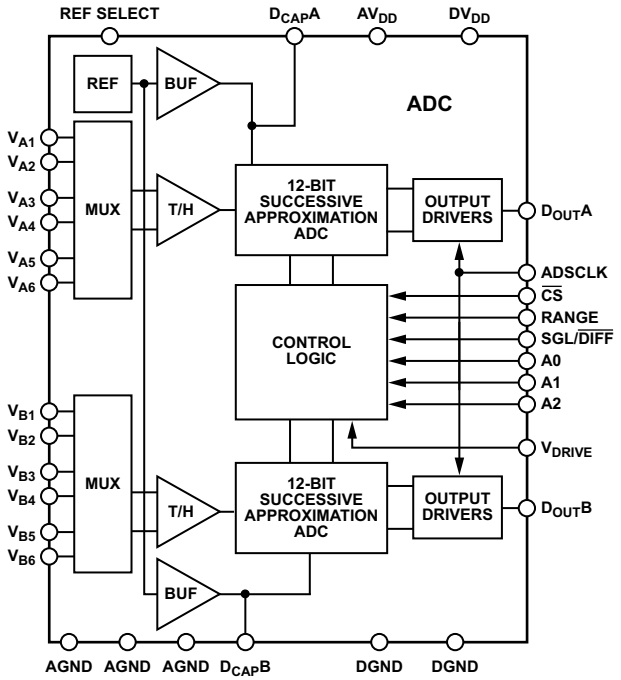


Figure 8. ADC (Internal) Functional Block Diagram

The internal ADC uses advanced design techniques to achieve very low power dissipation at high throughput rates. The part also offers flexible power/ throughput rate management when operating in normal mode as the quiescent current consumption is so low.

The analog input range for the part can be selected to be a 0 V to V_{REF} (or 2 × V_{REF}) range, with either straight binary or twos complement output coding. The internal ADC has an on-chip 2.5 V reference that can be overdriven when an external reference is preferred.

Additional highlights of the internal ADC include:

- Two Complete ADC Functions Allow Simultaneous Sampling and Conversion of Two Channels — Each ADC has three fully/pseudo differential pairs, or six single-ended channels, as programmed. The conversion result of both channels is simultaneously available on separate data lines, or in succession on one data line if only one serial connection is available.
- High Throughput with Low Power Consumption
- The internal ADC offers both a standard 0 V to V_{REF} input range and a 2 × V_{REF} input range.
- No Pipeline Delay — The part features two standard successive approximation ADCs with accurate control of the sampling instant via a $\overline{CS}$ input and once off conversion control.

ADC APPLICATION HINTS

The following sections provide application hints for using the ADC.

Grounding and Layout Considerations

The analog and digital supplies to the ADC are independent and separately pinned out to minimize coupling between the analog and digital sections of the device. The printed circuit board (PCB) that houses the ADC should be designed so that the analog and digital sections are separated and confined to certain areas of the board. This design facilitates the use of ground planes that can be easily separated.

To provide optimum shielding for ground planes, a minimum etch technique is generally best. All AGND pins should be sunk in the AGND plane. Digital and analog ground planes should be joined in only one place. If the ADC is in a system where multiple devices require an AGND to DGND connection, the connection should still be made at one point only, a star ground point that should be established as close as possible to the ground pins on the ADC.

Avoid running digital lines under the device as this couples noise onto the die. Avoid running digital lines in the area of the AGND pad as this couples noise onto the ADC die and into the AGND plane. The power supply lines to the ADC should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line.

To avoid radiating noise to other sections of the board, fast switching signals, such as clocks, should be shielded with digital ground, and clock signals should never run near the analog inputs. Avoid crossover of digital and analog signals. To reduce the effects of feed through within the board, traces on opposite sides of the board should run at right angles to each other.

Good decoupling is also important. All analog supplies should be decoupled with 10 µF tantalum capacitors in parallel with 0.1 µF capacitors to GND. To achieve the best results from these decoupling components, they must be placed as close as possible to the device, ideally right up against the device. The 0.1 µF capacitors should have low effective series resistance (ESR) and effective series inductance (ESI), such as the common ceramic types or surface-mount types. These low ESR and ESI capacitors provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

RELATED DOCUMENTS

The following publications that describe the ADSP-BF50x processors (and related processors) can be ordered from any Analog Devices sales office or accessed electronically on our website:

- *Getting Started With Blackfin Processors*
- *ADSP-BF50x Blackfin Processor Hardware Reference* (volumes 1 and 2)
- *Blackfin Processor Programming Reference*
- *ADSP-BF50x Blackfin Processor Anomaly List*

SIGNAL DESCRIPTIONS

Signal definitions for the ADSP-BF50x processors are listed in Table 11. All pins for the ADC (ADSP-BF506F processor only) are listed in Table 12.

In order to maintain maximum function and reduce package size and pin count, some pins have multiple, multiplexed functions. In cases where pin function is reconfigurable, the default state is shown in plain text, while the alternate functions are shown in italics.

During and immediately after reset, all processor signals (not ADC signals) are three-stated with the following exceptions: EXT_WAKE is driven high and XTAL is driven in conjunction with CLKIN to create a crystal oscillator circuit. During hibernate, all signals are three-stated with the following exceptions: EXT_WAKE is driven low and XTAL is driven to a solid logic level.

During and immediately after reset, all I/O pins have their input buffers disabled until enabled by user software with the exception of the pins that need pull-ups or pull-downs, as noted in Table 11.

Adding a parallel termination to CLKOUT may prove useful in further enhancing signal integrity. Be sure to verify overshoot/undershoot and signal integrity specifications on actual hardware.

Table 11. Processor — Signal Descriptions

Signal Name	Type	Function	Driver Type
Port F: *GPIO and Multiplexed Peripherals*			
PF0/*TSCLK0/UA0_RX/TMR6/CUD0*	I/O	GPIO/*SPORT0 TX Serial CLK/UART0 RX/Timer6/Count Up Dir 0*	TBD
PF1/*RSCLK0/UA0_TX/TMR5/CDG0*	I/O	GPIO/*SPORT0 RX Serial CLK/UART0 TX/Timer5/Count Down Dir 0*	TBD
PF2/*DT0PRI/PWM0_BH/PPI_D8/CZM0*	I/O	GPIO/*SPORT0 TX Pri Data/PWM0 Drive B Hi/PPI Data 8/Counter Zero Marker 0*	TBD
PF3/*TFS0/PWM0_BL/PPI_D9/CDG0*	I/O	GPIO/*SPORT0 TX Frame Sync/PWM0 Drive B Lo/PPI Data 9/Count Down Dir 0*	TBD
PF4/*RFS0/PWM0_CH/PPI_D10/TACLK0*	I/O	GPIO/*SPORT0 RX Frame Sync/PWM0 Drive C Hi/PPI Data 10/Alt Timer CLK 0*	TBD
PF5/*DR0PRI/PWM0_CL/PPI_D11/TACLK1*	I/O	GPIO/*SPORT0 Pri RX Data/PWM0 Drive C Lo/PPI Data 11/Alt Timer CLK 1*	TBD
PF6/*UA1_TX/$\overline{\text{PWM0\_TRIP}}$/PPI_D12*	I/O	GPIO/*UART1 TX/PWM0 TRIP/PPI Data 12*	TBD
PF7/*UA1_RX/PWM0_SYNC/PPI_D13/TACI3*	I/O	GPIO/*UART1 RX/PWM0 SYNC/PPI Data 13/Alt Capture In 3*	TBD
PF8/*$\overline{\text{UA1\_RTS}}$/DT0SEC/PPI_D7*	I/O	GPIO/*UART1 RTS/SPORT0 TX Sec Data/PPI Data 7*	TBD
PF9/*$\overline{\text{UA1\_CTS}}$/DR0SEC/PPI_D6/CZM0*	I/O	GPIO/*UART1 CTS/SPORT0 Sec RX Data/PPI Data 6/Counter Zero Marker 0*	TBD
PF10/*SPI0_SCK/TMR2/PPI_D5*	I/O	GPIO/*SPI0 SCK/Timer2/PPI Data 5*	TBD
PF11/*SPI0_MISO/$\overline{\text{PWM0\_TRIP}}$/PPI_D4/TACLK2*	I/O	GPIO/*SPI0 MISO/PWM0 TRIP/PPI Data 4/Alt Timer CLK 2*	TBD
PF12/*SPI0_MOSI/PWM0_SYNC/PPI_D3*	I/O	GPIO/*SPI0 MOSI/PWM0 SYNC/PPI Data 3*	TBD
PF13/*$\overline{\text{SPI0\_SEL1}}$/TMR3/PPI_D2/$\overline{\text{SPI0\_SS}}$*	I/O	GPIO/*SPI0 Slave Select 1/Timer3/PPI Data 2/SPI0 Slave Select In*	TBD
PF14/*$\overline{\text{SPI0\_SEL2}}$/PWM0_AH/PPI_D1*	I/O	GPIO/*SPI0 Slave Select 2/PWM0 AH/PPI Data 1*	TBD
PF15/*$\overline{\text{SPI0\_SEL3}}$/PWM0_AL/PPI_D0*	I/O	GPIO/*SPI0 Slave Select 3/PWM0 AL/PPI Data 0*	TBD
Port G: *GPIO and Multiplexed Peripherals*			
PG0/*$\overline{\text{SPI1\_SEL3}}$/TMRCLK/PPI_CLK/UA1_RX/TACI4*	I/O	GPIO/*SPI1 Slave Select 3/Timer CLK/PPI Clock/UART1 RX/Alt Capture In 4*	TBD
PG1/*$\overline{\text{SPI1\_SEL2}}$/PPI_FS3/CAN_RX/TACI5*	I/O	GPIO/*SPI1 Slave Select 2/PPI FS3/CAN RX/Alt Capture In 5*	TBD
PG2/*$\overline{\text{SPI1\_SEL1}}$/TMR4/CAN_TX/$\overline{\text{SPI1\_SS}}$*	I/O	GPIO/*SPI1 Slave Select 1/Timer4/CAN TX/SPI1 Slave Select In*	TBD
PG3/*HWAIT/SPI1_SCK/DT1SEC/UA1_TX*	I/O	GPIO/*HWAIT/SPI1 SCK/SPORT1 TX Sec Data/UART1 TX*	TBD
PG4/*SPI1_MOSI/DR1SEC/PWM1_SYNC/TACLK6*	I/O	GPIO/*SPI1 MOSI/SPORT1 Sec RX Data/PWM1 SYNC/Alt Timer CLK 6*	TBD
PG5/*SPI1_MISO/TMR7/$\overline{\text{PWM1\_TRIP}}$*	I/O	GPIO/*SPI1 MISO/Timer7/PWM1 TRIP*	TBD
PG6/*ACM_SGLDIFF/SD_D3/PWM1_AH*	I/O	GPIO/*ADC CM SGL DIFF/SD Data 3/PWM1 Drive A Hi*	TBD
PG7/*ACM_RANGE/SD_D2/PWM1_AL*	I/O	GPIO/*ADC CM RANGE/SD Data 2/PWM1 Drive A Lo*	TBD
PG8/*DR1SEC/SD_D1/PWM1_BH*	I/O	GPIO/*SPORT1 Sec RX Data/SD Data 1/PWM1 Drive B Hi*	TBD
PG9/*DR1PRI/SD_D0/PWM1_BL*	I/O	GPIO/*SPORT1 Pri RX Data/SD Data 0/PWM1 Drive B Lo*	TBD
PG10/*RFS1/SD_CMD/PWM1_CH/TACI6*	I/O	GPIO/*SPORT1 RX Frame Sync/SD CMD/PWM1 Drive C Hi/Alt Capture In 6*	TBD
PG11/*RSCLK1/SD_CLK/PWM1_CL/TACLK7*	I/O	GPIO/*SPORT1 RX Serial CLK/SD CLK/PWM1 Drive C Lo/Alt Timer CLK 7*	TBD
PG12/*UA0_RX/SD_D4/PPI_D15/TACI2*	I/O	GPIO/*UART0 RX/SD Data 4/PPI Data 15/Alt Capture In 2*	TBD
PG13/*UA0_TX/SD_D5/PPI_D14/CZM1*	I/O	GPIO/*UART0 TX/SD Data 5/PPI Data 14/Counter Zero Marker 1*	TBD

Table 11. Processor — Signal Descriptions (Continued)

Signal Name	Type	Function	Driver Type
PG14/*UA0_RTS*/SD_D6/TMR0/PPI_FS1/CUD1	I/O	GPIO/*UART0 RTS*/SD Data 6/Timer0/PPI FS1/Count Up Dir 1	TBD
PG15/*UA0_CTS*/SD_D7/TMR1/PPI_FS2/CDG1	I/O	GPIO/*UART0 CTS*/SD Data 7/Timer1/PPI FS2/Count Down Dir 1	TBD
Port H: *GPIO and Multiplexed Peripherals*			
PH0/*ACM_A2*/DT1PRI/*SPI0_SEL3*/WAKEUP	I/O	GPIO/*ADC CM A2*/SPORT1 TX Pri Data/SPI0 Slave Select 3/Wake-up Input	TBD
PH1/*ACM_A1*/TFS1/*SPI1_SEL3*/TACLK3	I/O	GPIO/*ADC CM A1*/SPORT1 TX Frame Sync/SPI1 Slave Select 3/Alt Timer CLK 3	TBD
PH2/*ACM_A0*/TSCLK1/*SPI1_SEL2*/TACI7	I/O	GPIO/*ADC CM A0*/SPORT1 TX Serial CLK/SPI1 Slave Select 2/Alt Capture In 7	TBD
TWI (Two-Wire Interface) Port			
SCL	I/O 5V	TWI Serial Clock (This signal is an open-drain output and requires a pull-up resistor. Consult version 2.1 of the I^2C specification for the proper resistor value.)	TBD
SDA	I/O 5V	TWI Serial Data (This signal is an open-drain output and requires a pull-up resistor. Consult version 2.1 of the I^2C specification for the proper resistor value.)	TBD
JTAG Port			
TCK	I	JTAG CLK	
TDO	O	JTAG Serial Data Out	C
TDI	I	JTAG Serial Data In	
TMS	I	JTAG Mode Select	
$\overline{\text{TRST}}$	I	JTAG Reset (This signal should be pulled low if the JTAG port is not used.)	
$\overline{\text{EMU}}$	O	Emulation Output	C
Clock			
CLKIN	I	CLK/Crystal In	
XTAL	O	Crystal Output	
EXTCLK	O	Clock Output	B
Mode Controls			
$\overline{\text{RESET}}$	I	Reset	
$\overline{\text{NMI}}$	I	Nonmaskable Interrupt (This signal should be pulled high when not used.)	
BMODE2–0	I	Boot Mode Strap 2-0	
ADSP-BF50x Voltage Regulation I/F			
EXT_WAKE	O	Wake up Indication	C
$\overline{\text{PG}}$	I	Power Good	
Power Supplies		**ALL SUPPLIES MUST BE POWERED** See Processor — Operating Conditions on Page 25.	
V_{DDEXT}	P	I/O Power Supply	
V_{DDINT}	P	Internal Power Supply	
$V_{DDFLASH}$	P	Flash Memory Power Supply	
GND	G	Ground for All Supplies	

Table 12. ADC — Signal Descriptions (ADSP-BF506F Processor Only)

Signal Name	Type	Function
DGND	G	Digital Ground. This is the ground reference point for all digital circuitry on the internal ADC. Both DGND pins should connect to the DGND plane of a system. The DGND and AGND voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
REF SELECT	I	Internal/External Reference Selection. Logic input. If this pin is tied to DGND, the on-chip 2.5 V reference is used as the reference source for both ADC A and ADC B. In addition, Pin $D_{CAP}A$ and Pin $D_{CAP}B$ must be tied to decoupling capacitors. If the REF SELECT pin is tied to a logic high, an external reference can be supplied to the internal ADC through the $D_{CAP}A$ and/or $D_{CAP}B$ pins.
AV_{DD}	P	Analog Supply Voltage, 2.7 V to 5.25 V. This is the only supply voltage for all analog circuitry on the internal ADC. The AV_{DD} and DV_{DD} voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis. This supply should be decoupled to AGND.
$D_{CAP}A$, $D_{CAP}B$ (V_{REF})	I	Decoupling Capacitor Pins. Decoupling capacitors (470 nF recommended) are connected to these pins to decouple the reference buffer for each respective ADC. Provided the output is buffered, the on-chip reference can be taken from these pins and applied externally to the rest of a system. The range of the external reference is dependent on the analog input range selected.
AGND	G	Analog Ground. Ground reference point for all analog circuitry on the internal ADC. All analog input signals and any external reference signal should be referred to this AGND voltage. All three of these AGND pins should connect to the AGND plane of a system. The AGND and DGND voltages ideally should be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
V_{A1} to V_{A6}	I	Analog Inputs of ADC A. These may be programmed as six single-ended channels or three true differential analog input channel pairs. See Table 51 (Analog Input Type and Channel Selection).
V_{B1} to V_{B6}	I	Analog Inputs of ADC B. These may be programmed as six single-ended channels or three true differential analog input channel pairs. See Table 51 (Analog Input Type and Channel Selection).
RANGE	I	Analog Input Range Selection. Logic input. The polarity on this pin determines the input range of the analog input channels. If this pin is tied to a logic low, the analog input range is 0 V to V_{REF}. If this pin is tied to a logic high when $\overline{CS}$ goes low, the analog input range is $2 \times V_{REF}$. For details, see Table 51 (Analog Input Type and Channel Selection).
SGL/$\overline{DIFF}$	I	Logic Input. This pin selects whether the analog inputs are configured as differential pairs or single ended. A logic low selects differential operation while a logic high selects single-ended operation. For details, see Table 51 (Analog Input Type and Channel Selection).
A0 to A2	I	Multiplexer Select. Logic inputs. These inputs are used to select the pair of channels to be simultaneously converted, such as Channel 1 of both ADC A and ADC B, Channel 2 of both ADC A and ADC B, and so on. The pair of channels selected may be two single-ended channels or two differential pairs. The logic states of these pins need to be set up prior to the acquisition time and subsequent falling edge of $\overline{CS}$ to correctly set up the multiplexer for that conversion. For further details, see Table 51 (Analog Input Type and Channel Selection).
$\overline{CS}$	I	Chip Select. Active low logic input. This input provides the dual function of initiating conversions on the internal ADC and framing the serial data transfer. When connecting $\overline{CS}$ to a processor signal that is three-stated during reset and/or hibernate, adding a pull-up resistor may prove useful to avoid random ADC operation.
ADSCLK	I	Serial Clock. Logic input. A serial clock input provides the ADSCLK for accessing the data from the internal ADC. This clock is also used as the clock source for the conversion process.

Table 12. ADC — Signal Descriptions (ADSP-BF506F Processor Only) (Continued)

Signal Name	Type	Function
$D_{OUT}A$, $D_{OUT}B$	O	Serial Data Outputs. The data output is supplied to each pin as a serial data stream. The bits are clocked out on the falling edge of the ADSCLK input and 14 ADSCLKs are required to access the data. The data simultaneously appears on both pins from the simultaneous conversions of both ADCs. The data stream consists of two leading zeros followed by the 12 bits of conversion data. The data is provided MSB first. If $\overline{CS}$ is held low for 16 ADSCLK cycles rather than 14, then two trailing zeros will appear after the 12 bits of data. If $\overline{CS}$ is held low for a further 16 ADSCLK cycles on either $D_{OUT}A$ or $D_{OUT}B$, the data from the other ADC follows on the D_{OUT} pin. This allows data from a simultaneous conversion on both ADCs to be gathered in serial format on either $D_{OUT}A$ or $D_{OUT}B$ using only one serial port. For more information, see the ADC — Serial Interface section.
V_{DRIVE}	P	Logic Power Supply Input. The voltage supplied at this pin determines at what voltage the digital I/O interface operates. This pin should be decoupled to DGND. The voltage at this pin may be different than that at AV_{DD} and DV_{DD} but should never exceed either by more than 0.3 V.
DV_{DD}	P	Digital Supply Voltage, 2.7 V to 5.25 V. This is the supply voltage for all digital circuitry on the internal ADC. The DV_{DD} and AV_{DD} voltages should ideally be at the same potential and must not be more than 0.3 V apart even on a transient basis. This supply should be decoupled to DGND.

PROCESSOR — SPECIFICATIONS

Specifications are subject to change without notice.

PROCESSOR — OPERATING CONDITIONS

Parameter		Conditions	Min	Nominal	Max	Unit
V_{DDINT}[1]	Internal Supply Voltage		TBD	TBD	TBD	V
V_{DDEXT}[2]	External Supply Voltage	ADSP-BF504	1.7	1.8/2.5/3.3	3.6	V
V_{DDEXT}[2]	External Supply Voltage	ADSP-BF504F, ADSP-BF506F	2.7	3.3	3.6	V
$V_{DDFLASH}$[2,3]	Flash Memory Supply Voltage		1.7	1.8	2.0	V
V_{IH}	High Level Input Voltage[4,5]	V_{DDEXT} = 1.90 V	1.1		3.6	V
V_{IH}	High Level Input Voltage[4,5]	V_{DDEXT} = 2.75 V	1.7		3.6	V
V_{IH}	High Level Input Voltage[4,5]	V_{DDEXT} = 3.6 V	2.0		3.6	V
V_{IHTWI}	High Level Input Voltage[6]	V_{DDEXT} = 1.90 V/2.75 V/3.6 V	0.7 × V_{BUSTWI}[7,8]		V_{BUSTWI}[7,8]	V
V_{IL}	Low Level Input Voltage[4,5]	V_{DDEXT} = 1.7 V	–0.3		0.6	V
V_{IL}	Low Level Input Voltage[4,5]	V_{DDEXT} = 2.25 V	–0.3		0.7	V
V_{IL}	Low Level Input Voltage[4,5]	V_{DDEXT} = 3.0 V	–0.3		0.8	V
V_{ILTWI}	Low Level Input Voltage[6]	V_{DDEXT} = minimum	–0.3		0.3 × V_{BUSTWI}[8]	V
T_J	Junction Temperature	88-Lead LFCSP @ $T_{AMBIENT}$ = –40°C to +85°C	–40		+105	°C
T_J	Junction Temperature	120-Lead LQFP @ $T_{AMBIENT}$ = –40°C to +85°C	–40		+105	°C

[1] The expected nominal value is 1.4 V ±5%, and initial customer designs should design with a programmable regulator that can be adjusted from 0.95 V to 1.5 V in 50 mV steps.
[2] Must remain powered (even if the associated function is not used).
[3] For ADSP-BF504, $V_{DDFLASH}$ pins should be connected to GND.
[4] Bidirectional pins (PF15–0, PG15–0, PH2–0) and input pins (TCK, TDI, TMS, $\overline{TRST}$, CLKIN, $\overline{RESET}$, $\overline{NMI}$, and BMODE3–0) of the ADSP-BF50x processors are 3.3 V tolerant (always accept up to 3.6 V maximum V_{IH}). Voltage compliance (on outputs, V_{OH}) is limited by the V_{DDEXT} supply voltage.
[5] Parameter value applies to all input and bidirectional pins, except SDA and SCL.
[6] Parameter applies to SDA and SCL.
[7] The V_{IHTWI} min and max value vary with the selection in the TWI_DT field of the NONGPIO_DRIVE register. See V_{BUSTWI} min and max values in Table 13.
[8] SDA and SCL are pulled up to V_{BUSTWI}. See Table 13.

Table 13 shows settings for TWI_DT in the NONGPIO_DRIVE register. Set this register prior to using the TWI port.

Table 13. TWI_DT Field Selections and V_{DDEXT}/V_{BUSTWI}

TWI_DT	V_{DDEXT} Nominal	V_{BUSTWI} Minimum	V_{BUSTWI} Nominal	V_{BUSTWI} Maximum	Unit
000 (default)	3.3	2.97	3.3	3.63	V
001	1.8	1.7	1.8	1.98	V
010	2.5	2.97	3.3	3.63	V
011	1.8	2.97	3.3	3.63	V
100	3.3	4.5	5	5.5	V
101	1.8	2.25	2.5	2.75	V
110	2.5	2.25	2.5	2.75	V
111 (reserved)	–	–	–	–	–

ADSP-BF50x Clock Related Operating Conditions

Table 14 describes the core clock timing requirements for the ADSP-BF50x processors. Take care in selecting MSEL, SSEL, and CSEL ratios so as not to exceed the maximum core clock and system clock (see Table 16). Table 15 describes phase-locked loop operating conditions.

Table 14. Core Clock (CCLK) Requirements—ADSP-BF50x Processors—All Speed Grades[1]

Parameter		Maximum	Unit
f_{CCLK}	Core Clock Frequency (V_{DDINT} = tbd V Minimum)	400	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = tbd V Minimum)	TBD	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = tbd V Minimum)	TBD	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = tbd V Minimum)	TBD	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = tbd V Minimum)	TBD	MHz

[1] See the Ordering Guide on Page 79.

Table 15. Phase-Locked Loop Operating Conditions

Parameter		Minimum	Maximum	Unit
f_{VCO}	Voltage Controlled Oscillator (VCO) Frequency	72	Speed Grade[1]	MHz

[1] See the Ordering Guide on Page 79.

Table 16. Maximum SCLK Conditions for ADSP-BF50x Processors

Parameter		V_{DDEXT} = 1.8 V/2.5 V/3.3 V Nominal	Unit
f_{SCLK}	CLKOUT/SCLK Frequency ($V_{DDINT} \geq$ tbd V)	100	MHz
f_{SCLK}	CLKOUT/SCLK Frequency ($V_{DDINT} <$ tbd V)	TBD	MHz

PROCESSOR — ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	Min	Typical	Max	Unit
V_{OH}	High Level Output Voltage	V_{DDEXT} = 1.7 V, I_{OH} = –0.5 mA	1.35			V
V_{OH}	High Level Output Voltage	V_{DDEXT} = 2.25 V, I_{OH} = –0.5 mA	2.0			V
V_{OH}	High Level Output Voltage	V_{DDEXT} = 3.0 V, I_{OH} = –0.5 mA	2.4			V
V_{OL}	Low Level Output Voltage	V_{DDEXT} = 1.7 V/2.25 V/3.0 V, I_{OL} = 2.0 mA			0.4	V
V_{OLTWI}	Low Level Output Voltage	V_{DDEXT} = 1.7 V/2.25 V/3.0 V, I_{OL} = 2.0 mA			TBD	V V
I_{IH}	High Level Input Current[1]	V_{DDEXT} = 3.6 V, V_{IN} = 3.6 V			10.0	µA
I_{IL}	Low Level Input Current[1]	V_{DDEXT} = 3.6 V, V_{IN} = 0 V			10.0	µA
I_{IHP}	High Level Input Current JTAG[2]	V_{DDEXT} = 3.6 V, V_{IN} = 3.6 V			75.0	µA
I_{OZH}	Three-State Leakage Current[3]	V_{DDEXT} = 3.6 V, V_{IN} = 3.6 V			10.0	µA
I_{OZHTWI}	Three-State Leakage Current[4]	V_{DDEXT} = 3.0 V, V_{IN} = 5.5 V			10.0	µA
I_{OZL}	Three-State Leakage Current[3]	V_{DDEXT} = 3.6 V, V_{IN} = 0 V			10.0	µA
C_{IN}	Input Capacitance[5]	f_{IN} = 1 MHz, $T_{AMBIENT}$ = 25°C, V_{IN} = 2.5 V		TBD	TBD[6]	pF
$I_{DDDEEPSLEEP}$[7]	V_{DDINT} Current in Deep Sleep Mode	V_{DDINT} = TBD V, f_{CCLK} = 0 MHz, f_{SCLK} = 0 MHz, T_J = 25°C, ASF = 0.00		TBD		mA
$I_{DDSLEEP}$	V_{DDINT} Current in Sleep Mode	V_{DDINT} = TBD V, f_{SCLK} = 25 MHz, T_J = 25°C		TBD		mA
$I_{DD-IDLE}$	V_{DDINT} Current in Idle	V_{DDINT} = TBD V, f_{CCLK} = 50 MHz, T_J = 25°C, ASF = TBD		TBD		mA
I_{DD-TYP}	V_{DDINT} Current	V_{DDINT} = TBD V, f_{CCLK} = 400 MHz, T_J = 25°C, ASF = 1.00		TBD		mA
$I_{DDHIBERNATE}$[8]	Hibernate State Current	V_{DDEXT} = 3.30 V, $V_{DDFLASH}$ = 1.8 V, T_J = 25°C, CLKIN = 0 MHz (V_{DDINT} = 0 V)		TBD		µA
$I_{DDSLEEP}$[9]	V_{DDINIT} Current in Sleep Mode	f_{CCLK} = 0 MHz, f_{SCLK} > 0 MHz			Table 18 + (TBD × V_{DDINT} × f_{SCLK})	mA[10]
$I_{DDDEEPSLEEP}$[9]	V_{DDINT} Current in Deep Sleep Mode	f_{CCLK} = 0 MHz, f_{SCLK} = 0 MHz			Table 18	mA
I_{DDINT}[9]	V_{DDINT} Current	f_{CCLK} > 0 MHz, f_{SCLK} ≥ 0 MHz			Table 18 + (Table 19 × ASF) + (TBD × V_{DDINT} × f_{SCLK})	mA
$I_{DDFLASH1}$	Flash Memory Supply Current 1 — Asynchronous Read (5 MHz NORCLK[11])			10	20	mA
	Flash Memory Supply Current 1 — Synchronous Read (50 MHz NORCLK[11])	4 Word		18	20	mA
		8 Word		20	22	mA
		16 Word		25	27	mA
		Continuous		28	30	mA
$I_{DDFLASH2}$	Flash Memory Supply Current 2 — Reset/Powerdown			15	50	µA
$I_{DDFLASH3}$	Flash Memory Supply Current 3 — Standby			15	50	µA

Parameter		Test Conditions	Min	Typical	Max	Unit
$I_{DDFLASH4}$	Flash Memory Supply Current 4 — Automatic Standby			15	50	µA
$I_{DDFLASH5}$	Flash Memory Supply Current 5 — Program			15	40	mA
	Flash Memory Supply Current 5 — Erase			15	40	mA
$I_{DDFLASH6}$	Flash Memory Supply Current 6 — Dual Operations	Program/Erase in one bank, asynchronous read in another bank		25	60	mA
		Program/Erase in one bank, synchronous read in another bank		43	70	mA
$I_{DDFLASH7}$	Flash Memory Supply Current 7 — Program/Erase Suspended (Standby)			15	50	µA

[1] Applies to input pins.
[2] Applies to JTAG input pins (TCK, TDI, TMS, $\overline{\text{TRST}}$).
[3] Applies to three-statable pins.
[4] Applies to bidirectional pins SCL and SDA.
[5] Applies to all signal pins.
[6] Guaranteed, but not tested.
[7] See the *ADSP-BF50x Blackfin Processor Hardware Reference Manual* for definition of sleep, deep sleep, and hibernate operating modes.
[8] Applies to V_{DDEXT} supply only. Clock inputs are tied high or low.
[9] Guaranteed maximum specifications.
[10] Unit for V_{DDINT} is V (Volts). Unit for f_{SCLK} is MHz. Example: TBD V, TBD MHz would be TBD x TBD x TBD = TBD mA adder.
[11] See the *ADSP-BF50x Blackfin Processor Hardware Reference Manual* for definition of NORCLK.

Total Power Dissipation

Total power dissipation has two components:

1. Static, including leakage current
2. Dynamic, due to transistor switching characteristics

Many operating conditions can also affect power dissipation, including temperature, voltage, operating frequency, and processor activity. Processor — Electrical Characteristics on Page 27 shows the current dissipation for internal circuitry (V_{DDINT}). $I_{DDDEEPSLEEP}$ specifies static power dissipation as a function of voltage (V_{DDINT}) and temperature (see Table 18), and I_{DDINT} specifies the total power specification for the listed test conditions, including the dynamic component as a function of voltage (V_{DDINT}) and frequency (Table 19).

There are two parts to the dynamic component. The first part is due to transistor switching in the core clock (CCLK) domain. This part is subject to an Activity Scaling Factor (ASF) which represents application code running on the processor core and L1 memories (Table 17).

The ASF is combined with the CCLK Frequency and V_{DDINT} dependent data in Table 19 to calculate this part. The second part is due to transistor switching in the system clock (SCLK) domain, which is included in the I_{DDINT} specification equation.

Table 17. Activity Scaling Factors (ASF)[1]

I_{DDINT} Power Vector	Activity Scaling Factor (ASF)
$I_{DD-PEAK}$	TBD
$I_{DD-HIGH}$	TBD
I_{DD-TYP}	TBD
I_{DD-APP}	TBD
I_{DD-NOP}	TBD
$I_{DD-IDLE}$	TBD

[1] See *Estimating Power for ASDP-BF534/BF536/BF537 Blackfin Processors (EE-297)*. The power vector information also applies to the ADSP-BF50x processors.

Table 18. Preliminary ADSP-BF50x Static Current — $I_{DD-DEEPSLEEP}$ (mA)

	Voltage (V_{DDINT})[1]							
T_J (°C)[1]	TBD V	TBD V	TBD V	TBD V	TBD V	TBD V	TBD V	TBD V
–40	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
–20	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
0	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
25	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
40	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
55	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
70	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
85	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
100	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
105	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

[1] Valid temperature and voltage ranges are model-specific. See Processor — Operating Conditions on Page 25.

Table 19. Preliminary ADSP-BF50x Dynamic Current in CCLK Domain (mA, with ASF = 1.0)[1]

f_{CCLK} (MHz)[2]	Voltage (V_{DDINT})[2]							
	TBD V	TBD V	TBD V	TBD V	TBD V	TBD V	TBD V	TBD V
400	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
300	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
200	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
100	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

[1] The values are not guaranteed as standalone maximum specifications. They must be combined with static current per the equations of Processor — Electrical Characteristics on Page 27.

[2] Valid frequency and voltage ranges are model-specific. See Processor — Operating Conditions on Page 25.

PROCESSOR — ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in Table 20 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 20.

Parameter	Rating
Internal Supply Voltage (V_{DDINT})	–0.3 V to +1.5 V
External (I/O) Supply Voltage (V_{DDEXT})	–0.3 V to +3.8 V
Input Voltage[1, 2]	–0.5 V to +3.6 V
Input Voltage[1, 2, 3]	–0.5 V to +5.5 V
Output Voltage Swing	–0.5 V to V_{DDEXT} + 0.5 V
Storage Temperature Range	–65°C to +150°C
Junction Temperature While Biased	+110°C

[1] Applies to 100% transient duty cycle. For other duty cycles see Table 21.
[2] Applies only when V_{DDEXT} is within specifications. When V_{DDEXT} is outside specifications, the range is V_{DDEXT} ± 0.2 Volts.
[3] Applies to pins SCL and SDA.

Table 21. Maximum Duty Cycle for Input Transient Voltage[1]

V_{IN} Min (V)	V_{IN} Max (V)	Maximum Duty Cycle
–0.50	+3.80	100 %
–0.70	+4.00	40%
–0.80	+4.10	25%
–0.90	+4.20	15%
–1.00	+4.30	10%

[1] Applies to all signal pins with the exception of CLKIN, XTAL, EXT_WAKE.

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PACKAGE INFORMATION

The information presented in Figure 9 and Table 22 provides details about the package branding for the ADSP-BF50x processors. For a complete listing of product availability, see Ordering Guide on Page 79.

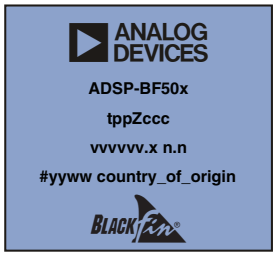


Figure 9. Product Information on Package

Table 22. Package Brand Information

Brand Key	Field Description
ADSP-BF50x	Product Name[1]
t	Temperature Range
pp	Package Type
Z	RoHS Compliant Designation
ccc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
#	RoHS Compliance Designator
yyww	Date Code

[1] See product names in the Ordering Guide on Page 79.

PROCESSOR — TIMING SPECIFICATIONS

Clock and Reset Timing

Table 23 and Figure 10 describe clock and reset operations. Per the CCLK and SCLK timing specifications in Table 14 to Table 16, combinations of CLKIN and clock multipliers must not select core/peripheral clocks in excess of the processor's speed grade.

Table 23. Clock and Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
f_{CKIN}	CLKIN Frequency[1, 2, 3, 4]	12	50	MHz
t_{CKINL}	CLKIN Low Pulse[1]	10		ns
t_{CKINH}	CLKIN High Pulse[1]	10		ns
t_{WRST}	$\overline{\text{RESET}}$ Asserted Pulse Width Low[5]	$11 \times t_{CKIN}$		ns
Switching Characteristic				
$t_{BUFDLAY}$	CLKIN to CLKBUF Delay		10	ns

[1] Applies to PLL bypass mode and PLL non bypass mode.
[2] Combinations of the CLKIN frequency and the PLL clock multiplier must not exceed the allowed f_{VCO}, f_{CCLK}, and f_{SCLK} settings discussed in Table 14 on Page 26 through Table 16 on Page 26.
[3] The t_{CKIN} period (see Figure 10) equals $1/f_{CKIN}$.
[4] If the DF bit in the PLL_CTL register is set, the minimum f_{CKIN} specification is 24 MHz.
[5] Applies after power-up sequence is complete. See Table 24 and Figure 11 for power-up reset timing.

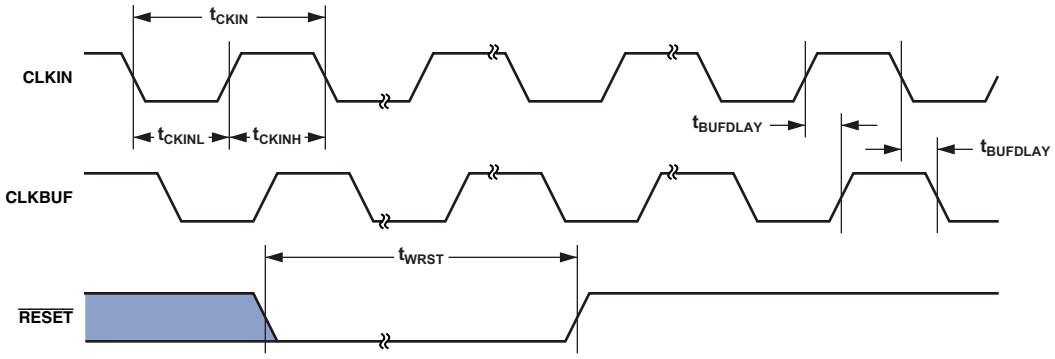


Figure 10. Clock and Reset Timing

Table 24. Power-Up Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
$t_{RST\_IN\_PWR}$	$\overline{\text{RESET}}$ Deasserted after the V_{DDINT}, V_{DDEXT}, $V_{DDFLASH}$, and CLKIN Pins are Stable and Within Specification	$3500 \times t_{CKIN}$		ns

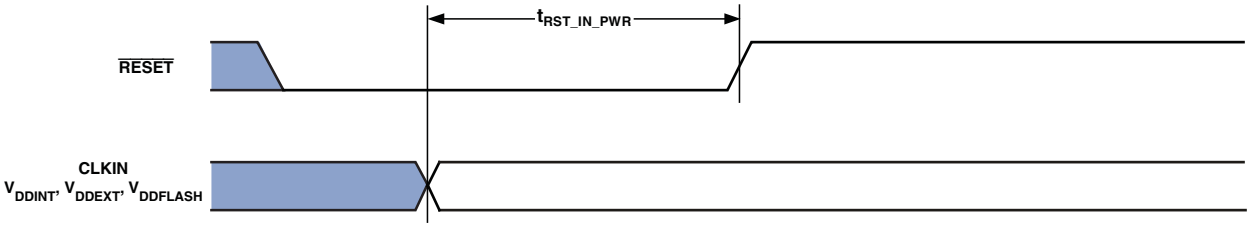


Figure 11. Power-Up Reset Timing

Parallel Peripheral Interface Timing

Table 25 and Figure 12 on Page 33, Figure 18 on Page 39, and Figure 20 on Page 40 describe parallel peripheral interface operations.

Table 25. Parallel Peripheral Interface Timing

Parameter		V_{DDEXT} = 1.8 V		V_{DDEXT} = 2.5/3.3 V		Unit
		Min	Max	Min	Max	
Timing Requirements						
t_{PCLKW}	PPI_CLK Width[1]	6.4		6.4		ns
t_{PCLK}	PPI_CLK Period[1]	20		20		ns
Timing Requirements - GP Input and Frame Capture Modes						
t_{SFSPE}	External Frame Sync Setup Before PPI_CLK (Nonsampling Edge for Rx, Sampling Edge for Tx)	6.7		6.7		ns
t_{HFSPE}	External Frame Sync Hold After PPI_CLK	1.0		1.0		ns
t_{SDRPE}	Receive Data Setup Before PPI_CLK	3.5		3.5		ns
t_{HDRPE}	Receive Data Hold After PPI_CLK	1.5		1.5		ns
Switching Characteristics - GP Output and Frame Capture Modes						
t_{DFSPE}	Internal Frame Sync Delay After PPI_CLK		9.8		8.8	ns
t_{HOFSPE}	Internal Frame Sync Hold After PPI_CLK	1.7		1.7		ns
t_{DDTPE}	Transmit Data Delay After PPI_CLK		9.8		8.8	ns
t_{HDTPE}	Transmit Data Hold After PPI_CLK	1.8		1.8		ns

[1] PPI_CLK frequency cannot exceed $f_{SCLK}/2$

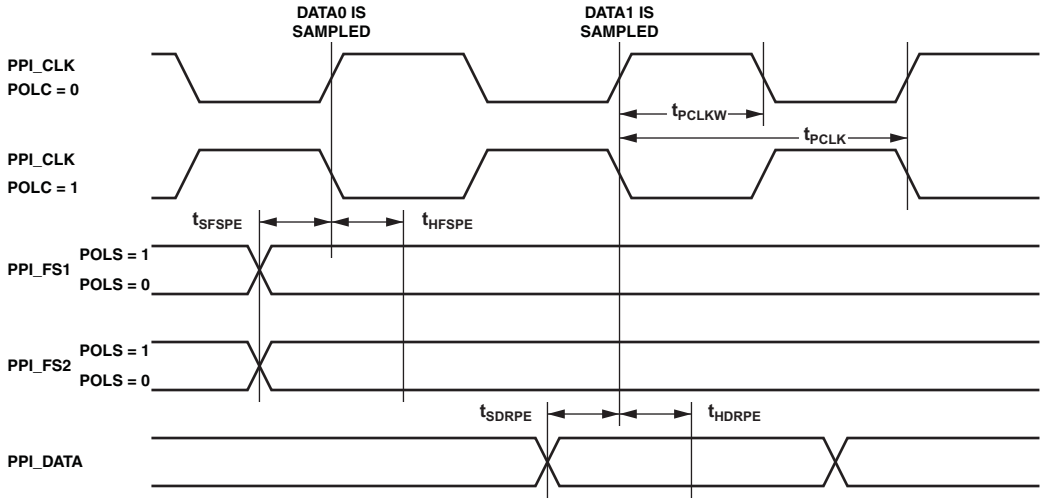


Figure 12. PPI GP Rx Mode with External Frame Sync Timing

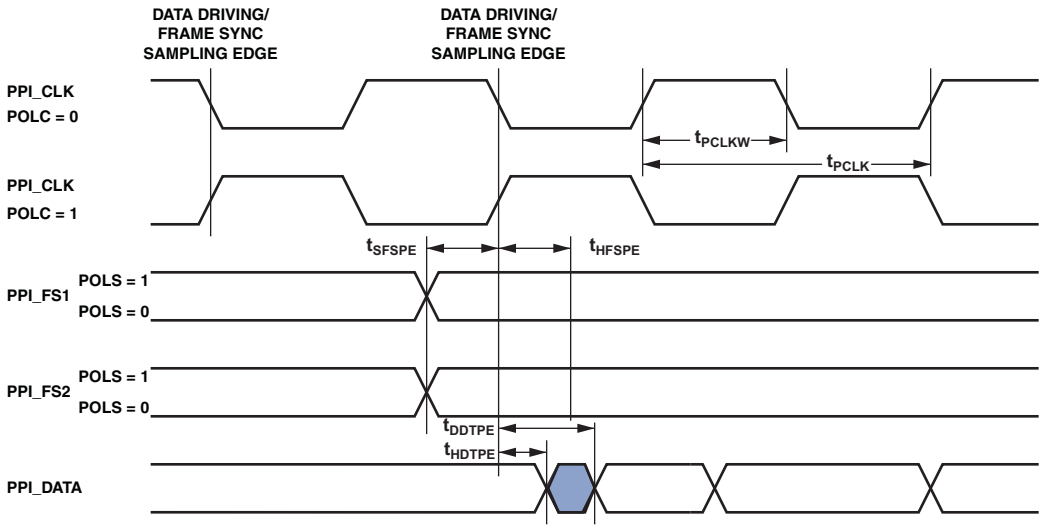


Figure 13. PPI GP Tx Mode with External Frame Sync Timing

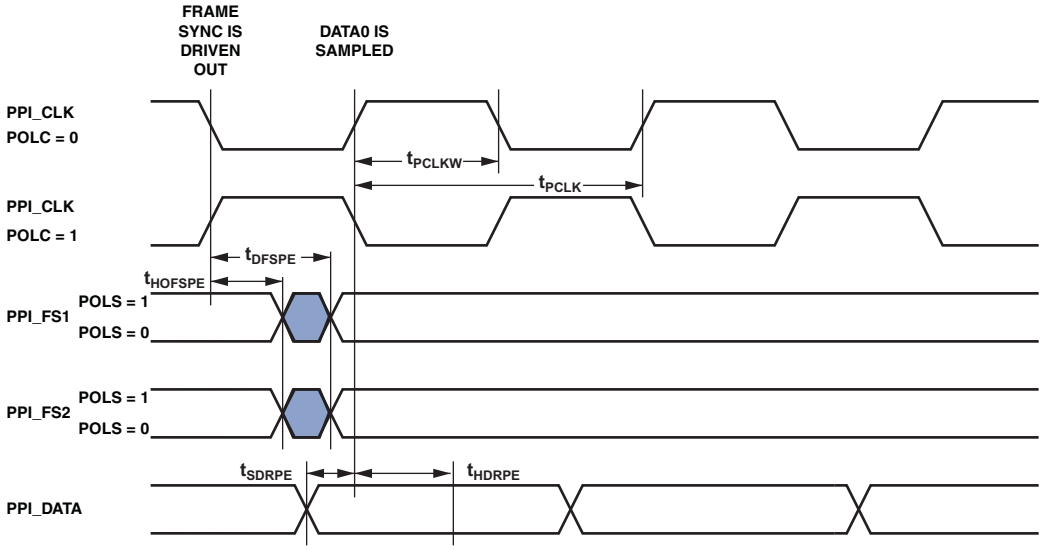


Figure 14. PPI GP Rx Mode with Internal Frame Sync Timing

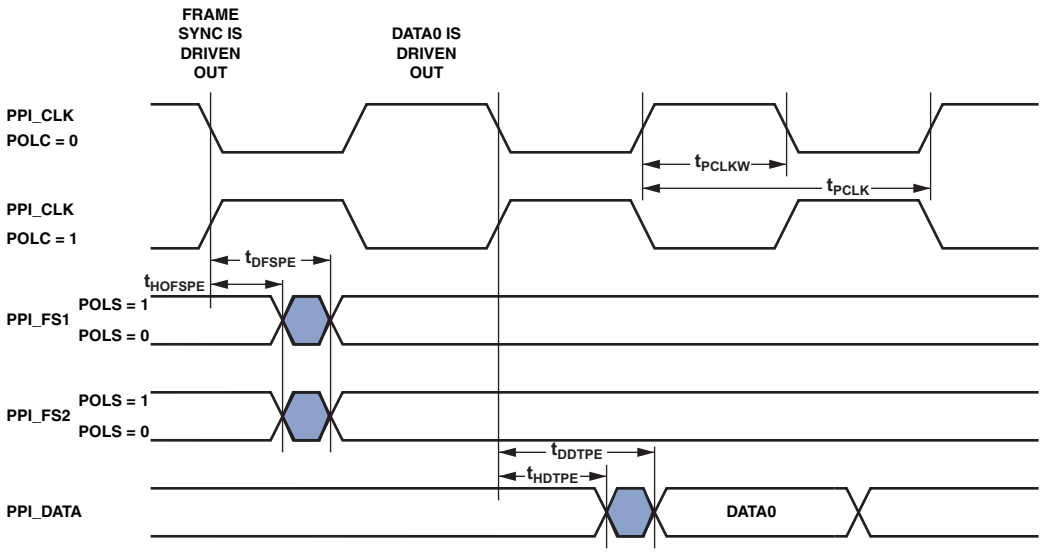


Figure 15. PPI GP Tx Mode with Internal Frame Sync Timing

RSI Controller Timing

Table 26 and Figure 16 describe RSI Controller Timing.
Table 27 and Figure 17 describe RSI controller (high speed) timing.

Table 26. RSI Controller Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{ISU}	Input Setup Time	5.6		ns
t_{IH}	Input Hold Time	2		ns
Switching Characteristics				
f_{PP}[1]	Clock Frequency Data Transfer Mode	0	25	MHz
f_{OD}	Clock Frequency Identification Mode	100[2]	400	kHz
t_{WL}	Clock Low Time	15		ns
t_{WH}	Clock High Time	15		ns
t_{TLH}	Clock Rise Time		10	ns
t_{THL}	Clock Fall Time		10	ns
t_{ODLY}	Output Delay Time During Data Transfer Mode		14	ns
t_{ODLY}	Output Delay Time During Identification Mode		50	ns

[1] $t_{PP} = 1/f_{PP}$
[2] Specification can be 0 kHz, which means to stop the clock. The given minimum frequency range is for cases where a continuous clock is required.

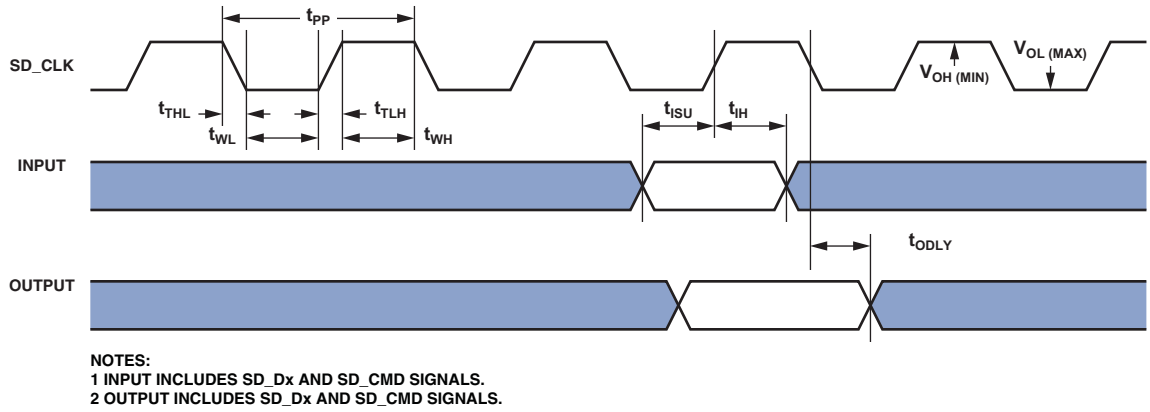


Figure 16. RSI Controller Timing

Table 27. RSI Controller Timing (High Speed Mode)

Parameter		Min	Max	Unit
Timing Requirements				
t_{ISU}	Input Setup Time	5.6		ns
t_{IH}	Input Hold Time	2		ns
Switching Characteristics				
f_{PP}[1]	Clock Frequency Data Transfer Mode	0	50	MHz
t_{WL}	Clock Low Time	9.5		ns
t_{WH}	Clock High Time	9.5		ns
t_{TLH}	Clock Rise Time		3	ns
t_{THL}	Clock Fall Time		3	ns
t_{ODLY}	Output Delay Time During Data Transfer Mode		TBD	ns
t_{OH}	Output Hold Time	2.5		ns

[1] $t_{PP} = 1/f_{PP}$

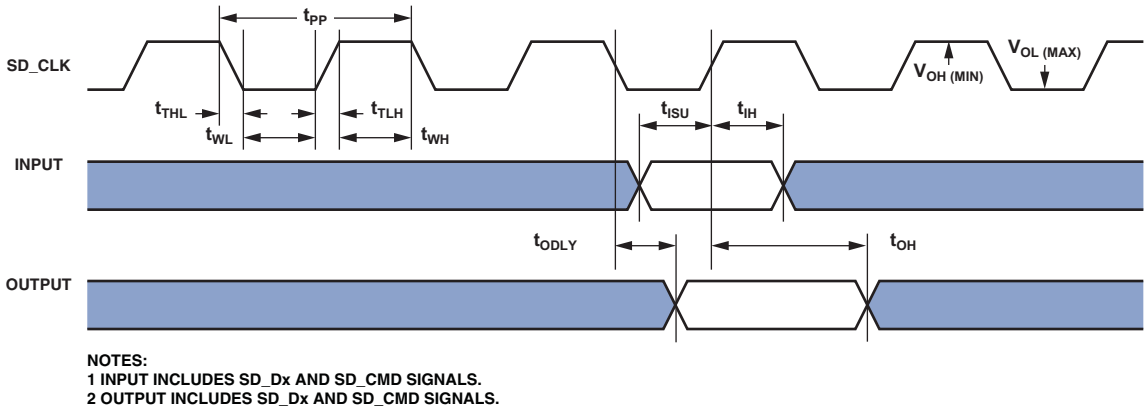


Figure 17. RSI Controller Timing (High-Speed Mode)

Serial Ports

Table 28 through Table 31 on Page 40 and Figure 18 on Page 39 through Figure 20 on Page 40 describe serial port operations.

Table 28. Serial Ports—External Clock

Parameter		V_{DDEXT} = 1.8 V Min	V_{DDEXT} = 1.8 V Max	V_{DDEXT} = 2.5/3.3 V Min	V_{DDEXT} = 2.5/3.3 V Max	Unit
Timing Requirements						
t_{SFSE}	TFSx/RFSx Setup Before TSCLKx/RSCLKx[1]	3.0		3.0		ns
t_{HFSE}	TFSx/RFSx Hold After TSCLKx/RSCLKx[1]	3.0		3.0		ns
t_{SDRE}	Receive Data Setup Before RSCLKx[1,2]	3.0		3.0		ns
t_{HDRE}	Receive Data Hold After RSCLKx[1,2]	3.6		3.6		ns
t_{SCLKEW}	TSCLKx/RSCLKx Width	5.4		5.4		ns
t_{SCLKE}	TSCLKx/RSCLKx Period	18.0		18.0		ns
Switching Characteristics						
t_{DFSE}	TFSx/RFSx Delay After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)[3]		12.5		12.0	ns
t_{HOFSE}	TFSx/RFSx Hold After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)[3]	0.0		0.0		ns
t_{DDTE}	Transmit Data Delay After TSCLKx[3]		12.5		12.0	ns
t_{HDTE}	Transmit Data Hold After TSCLKx[3]	0.0		0.0		ns

[1] Referenced to sample edge.
[2] When SPORT is used in conjunction with the ACM, refer to the timing requirements in Table 39 (ACM Timing).
[3] Referenced to drive edge.

Table 29. Serial Ports—Internal Clock

Parameter		V_{DDEXT} = 1.8 V Min	V_{DDEXT} = 1.8 V Max	V_{DDEXT} = 2.5/3.3 V Min	V_{DDEXT} = 2.5/3.3 V Max	Unit
Timing Requirements						
t_{SFSI}	TFSx/RFSx Setup Before TSCLKx/RSCLKx[1]	12.4		11.3		ns
t_{HFSI}	TFSx/RFSx Hold After TSCLKx/RSCLKx[1]	–1.5		–1.5		ns
t_{SDRI}	Receive Data Setup Before RSCLKx[1,2]	12.4		11.3		ns
t_{HDRI}	Receive Data Hold After RSCLKx[1,2]	–1.5		–1.5		ns
Switching Characteristics						
t_{SCLKIW}	TSCLKx/RSCLKx Width	5.4		5.4		ns
t_{SCLKI}	TSCLKx/RSCLKx Period	18.0		18.0		ns
t_{DFSI}	TFSx/RFSx Delay After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)[3]		3.0		3.0	ns
t_{HOFSI}	TFSx/RFSx Hold After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)[3]	–4.0		–4.0		ns
t_{DDTI}	Transmit Data Delay After TSCLKx[3]		3.0		3.0	ns
t_{HDTI}	Transmit Data Hold After TSCLKx[3]	–1.8		–1.8		ns

[1] Referenced to sample edge.
[2] When SPORT is used in conjunction with the ACM, refer to the timing requirements in Table 39 (ACM Timing).
[3] Referenced to drive edge.

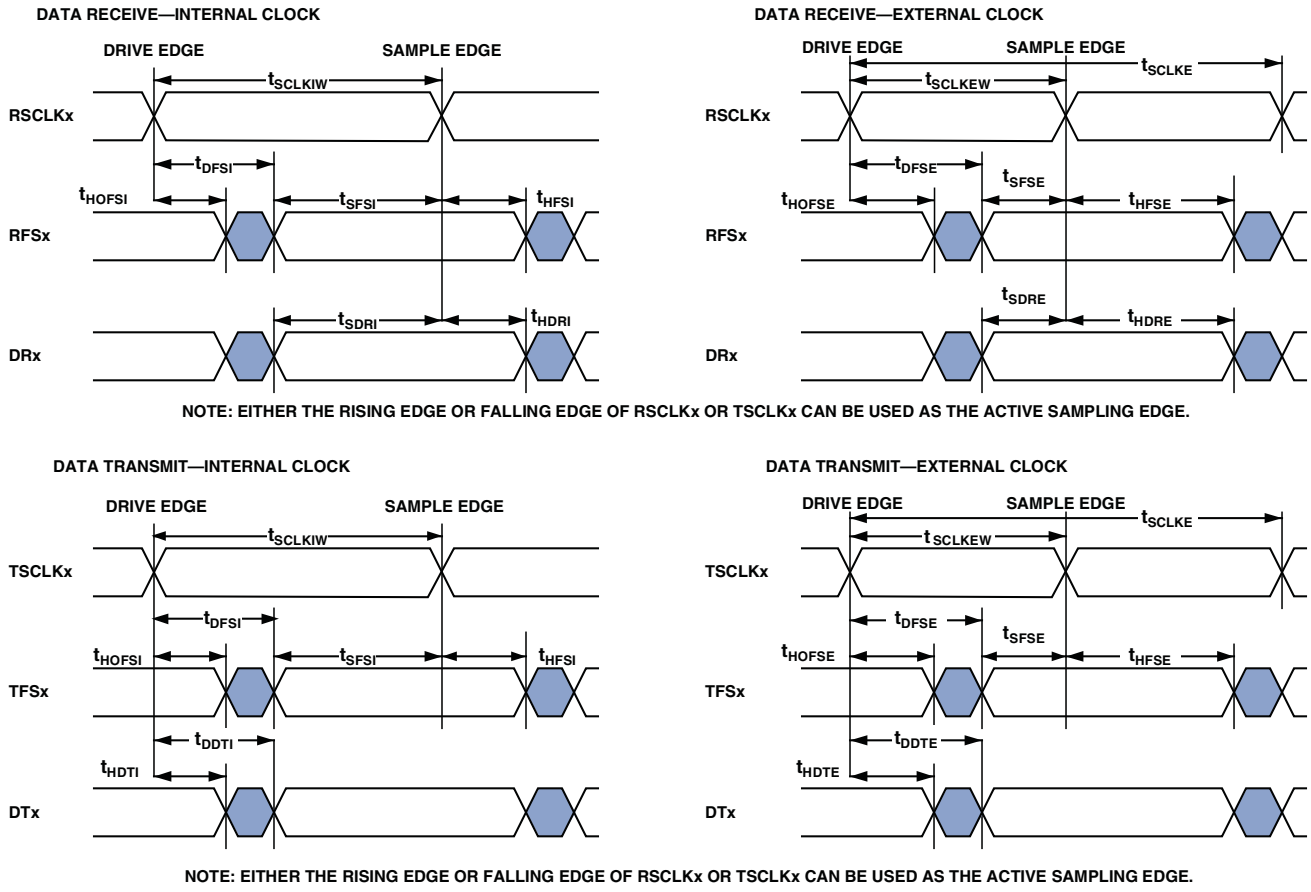


Figure 18. Serial Ports

Table 30. Serial Ports—Enable and Three-State

Parameter		V_{DDEXT}=1.8 V Min	V_{DDEXT}=1.8 V Max	V_{DDEXT}=2.5/3.3 V Min	V_{DDEXT}=2.5/3.3 V Max	Unit
Switching Characteristics						
t_{DTENE}	Data Enable Delay from External TSCLKx[1]	0.0		0.0		ns
t_{DDTTE}	Data Disable Delay from External TSCLKx[1]		10.0		10.0	ns
t_{DTENI}	Data Enable Delay from Internal TSCLKx[1]	–2.0		–2.0		ns
t_{DDTTI}	Data Disable Delay from Internal TSCLKx[1]		3.0		3.0	ns

[1] Referenced to drive edge.

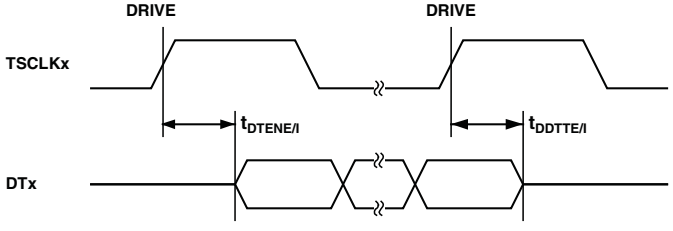


Figure 19. Serial Ports — Enable and Three-State

Table 31. Serial Ports — External Late Frame Sync

Parameter		V_{DDEXT}=1.8 V Min	V_{DDEXT}=1.8 V Max	V_{DDEXT}=2.5/3.3 V Min	V_{DDEXT}=2.5/3.3 V Max	Unit
Switching Characteristics						
$t_{DDTLFSE}$	Data Delay from Late External TFSx or External RFSx in Multi-channel Mode With MFD = 0[1, 2]		11.2		10.0	ns
$t_{DTENLFSE}$	Data Enable from External RFSx in Multi-channel Mode With MFD = 0[1, 2]	0.0		0.0		ns

[1] When in multi-channel mode, TFSx enable and TFSx valid follow $t_{DTENLFSE}$ and $t_{DDTLFSE}$.
[2] If external RFSx/TFSx setup to RSCLKx/TSCLKx > $t_{SCLKE}/2$ then $t_{DDTTE/I}$ and $t_{DTENE/I}$ apply, otherwise $t_{DDTLFSE}$ and $t_{DTENLFSE}$ apply.

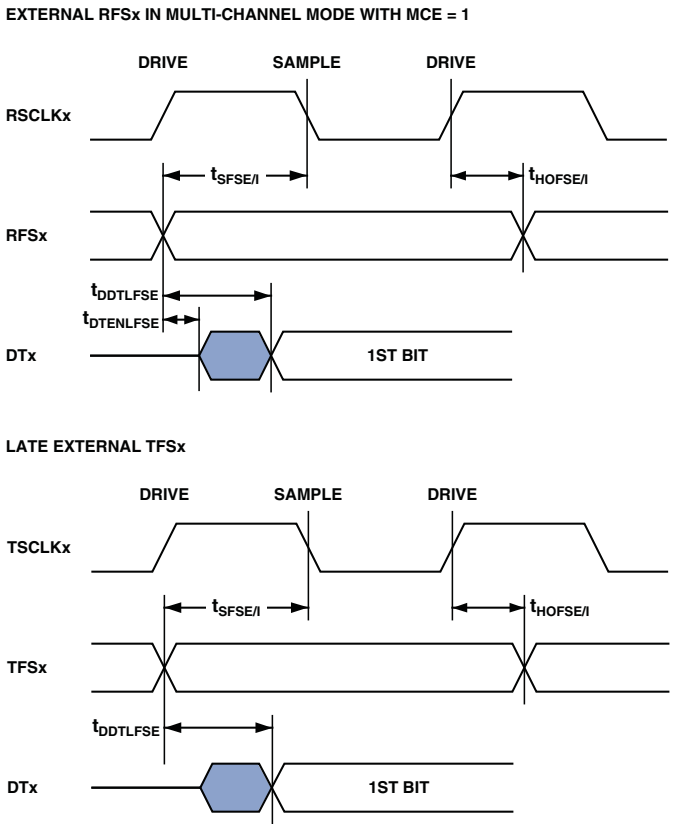


Figure 20. Serial Ports — External Late Frame Sync

Serial Peripheral Interface (SPI) Port—Master Timing

Table 32 and Figure 21 describe SPI port master operations.

Table 32. Serial Peripheral Interface (SPI) Port—Master Timing

Parameter		V_{DDEXT} = 1.8 V Min	V_{DDEXT} = 1.8 V Max	V_{DDEXT} = 2.5/3.3 V Min	V_{DDEXT} = 2.5/3.3 V Max	Unit
Timing Requirements						
t_{SSPIDM}	Data Input Valid to SCK Edge (Data Input Setup)	12.0		11.6		ns
t_{HSPIDM}	SCK Sampling Edge to Data Input Invalid	–1.5		–1.5		ns
Switching Characteristics						
t_{SDSCIM}	$\overline{SPISELx}$ low to First SCK Edge	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICHM}	Serial Clock High Period	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLM}	Serial Clock Low Period	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLK}	Serial Clock Period	$4 \times t_{SCLK} - 1.5$		$4 \times t_{SCLK} - 1.5$		ns
t_{HDSM}	Last SCK Edge to $\overline{SPISELx}$ High	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPITDM}	Sequential Transfer Delay	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
$t_{DDSPIDM}$	SCK Edge to Data Out Valid (Data Out Delay)		6		6	ns
$t_{HDSPIDM}$	SCK Edge to Data Out Invalid (Data Out Hold)	–1.0		–1.0		ns

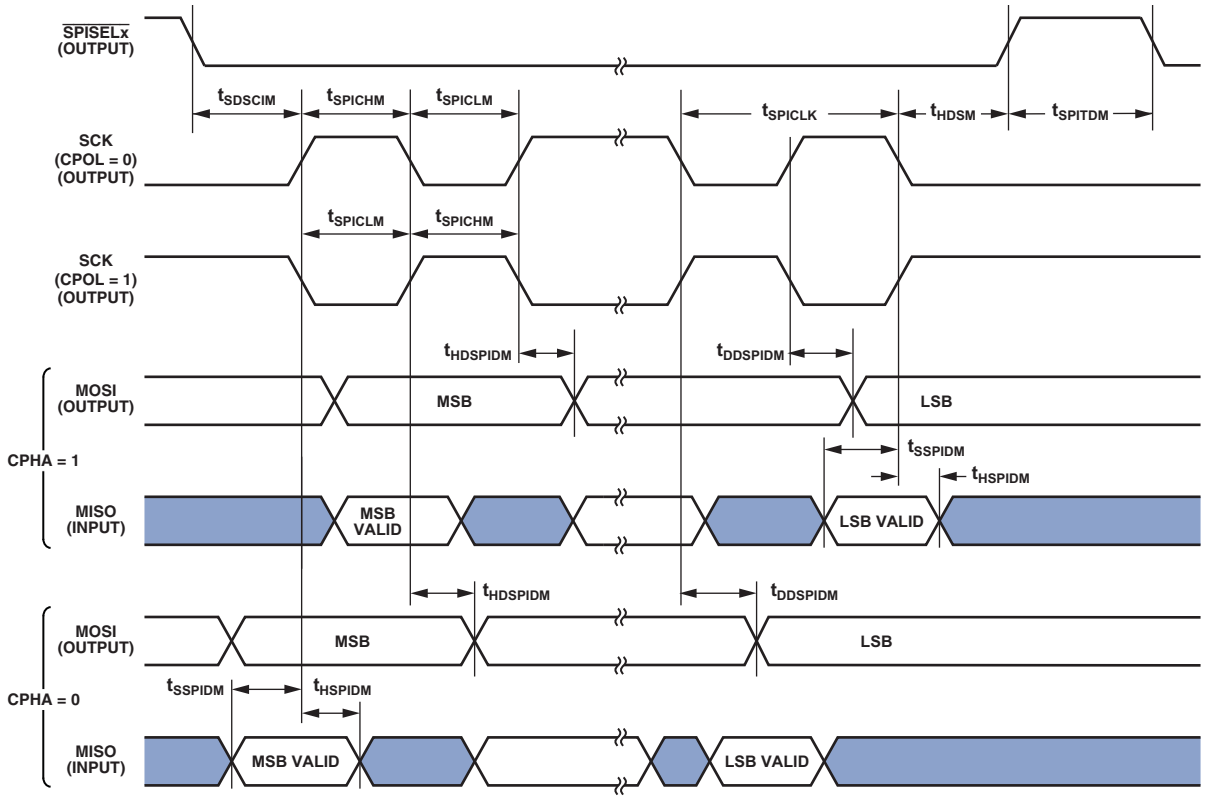


Figure 21. Serial Peripheral Interface (SPI) Port—Master Timing

Serial Peripheral Interface (SPI) Port—Slave Timing

Table 33 and Figure 22 describe SPI port slave operations.

Table 33. Serial Peripheral Interface (SPI) Port—Slave Timing

Parameter		V_{DDEXT} = 1.8 V Min	V_{DDEXT} = 1.8 V Max	V_{DDEXT} = 2.5/3.3 V Min	V_{DDEXT} = 2.5/3.3 V Max	Unit
Timing Requirements						
t_{SPICHS}	Serial Clock High Period	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLS}	Serial Clock Low Period	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLK}	Serial Clock Period	$4 \times t_{SCLK}$		$4 \times t_{SCLK}$		ns
t_{HDS}	Last SCK Edge to $\overline{SPISS}$ Not Asserted	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPITDS}	Sequential Transfer Delay	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SDSCI}	$\overline{SPISS}$ Assertion to First SCK Edge	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SSPID}	Data Input Valid to SCK Edge (Data Input Setup)	1.6		1.6		ns
t_{HSPID}	SCK Sampling Edge to Data Input Invalid	1.6		1.6		ns
Switching Characteristics						
t_{DSOE}	$\overline{SPISS}$ Assertion to Data Out Active	0	12.0	0	12.0	ns
t_{DSDHI}	$\overline{SPISS}$ Deassertion to Data High Impedance	0	8.5	0	8.5	ns
t_{DDSPID}	SCK Edge to Data Out Valid (Data Out Delay)		10		10	ns
t_{HDSPID}	SCK Edge to Data Out Invalid (Data Out Hold)	0		0		ns

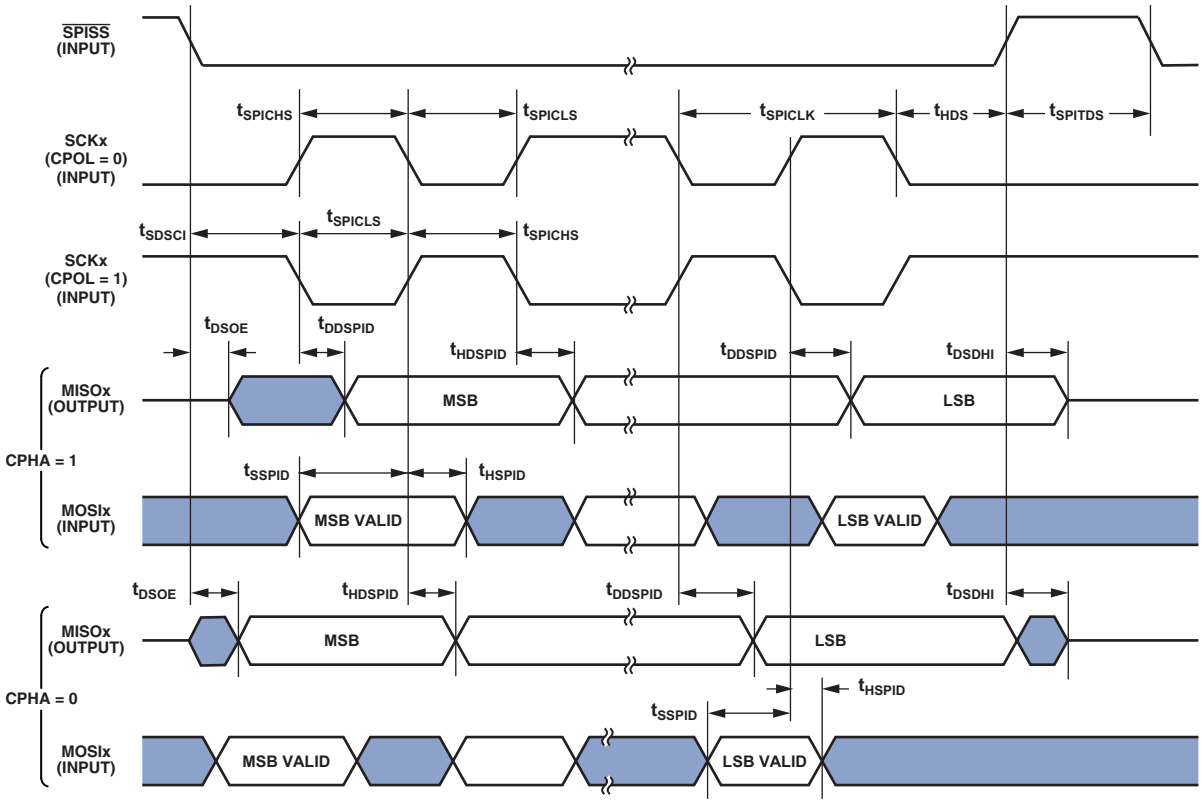


Figure 22. Serial Peripheral Interface (SPI) Port—Slave Timing

Universal Asynchronous Receiver-Transmitter (UART) Ports—Receive and Transmit Timing

The UART ports receive and transmit operations are described in the *ADSP-BF50x Hardware Reference Manual*.

General-Purpose Port Timing

Table 34 and Figure 23 describe general-purpose port operations.

Table 34. General-Purpose Port Timing

Parameter		V_{DDEXT} = 1.8 V Min	V_{DDEXT} = 1.8 V Max	V_{DDEXT} = 2.5/3.3 V Min	V_{DDEXT} = 2.5/3.3 V Max	Unit
Timing Requirement						
t_{WFI}	General-Purpose Port Pin Input Pulse Width	t_{SCLK} + 1		t_{SCLK} + 1		ns
Switching Characteristic						
t_{GPOD}	General-Purpose Port Pin Output Delay from CLKOUT High	0	9.66	0	9.66	ns

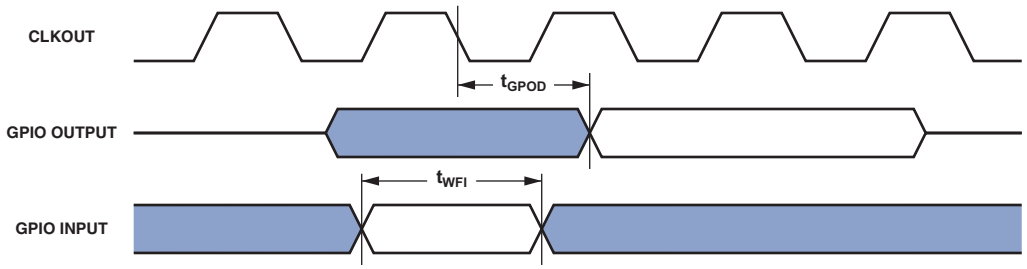


Figure 23. General-Purpose Port Timing

Timer Cycle Timing

Table 35 and Figure 24 describe timer expired operations. The input signal is asynchronous in "width capture mode" and "external clock mode" and has an absolute maximum input frequency of (f_{SCLK}/2) MHz.

Table 35. Timer Cycle Timing

Parameter		V_{DDEXT} = 1.8 V Min	V_{DDEXT} = 1.8 V Max	V_{DDEXT} = 2.5/3.3 V Min	V_{DDEXT} = 2.5/3.3 V Max	Unit
Timing Requirements						
t_{WL}	Timer Pulse Width Input Low (Measured In SCLK Cycles)[1]	$1 \times t_{SCLK}$		$1 \times t_{SCLK}$		ns
t_{WH}	Timer Pulse Width Input High (Measured In SCLK Cycles)[1]	$1 \times t_{SCLK}$		$1 \times t_{SCLK}$		ns
t_{TIS}	Timer Input Setup Time Before CLKOUT Low[2]	5		5		ns
t_{TIH}	Timer Input Hold Time After CLKOUT Low[2]	–2		–2		ns
Switching Characteristics						
t_{HTO}	Timer Pulse Width Output (Measured In SCLK Cycles)	$1 \times t_{SCLK}$	$(2^{32}–1)t_{SCLK}$	$1 \times t_{SCLK}$	$(2^{32}–1)t_{SCLK}$	ns
t_{TOD}	Timer Output Update Delay After CLKOUT High		8.1		8.1	ns

[1] The minimum pulse widths apply for TMRx signals in width capture and external clock modes. They also apply to the PG0 or PPI_CLK signals in PWM output mode.
[2] Either a valid setup and hold time or a valid pulse width is sufficient. There is no need to resynchronize programmable flag inputs.

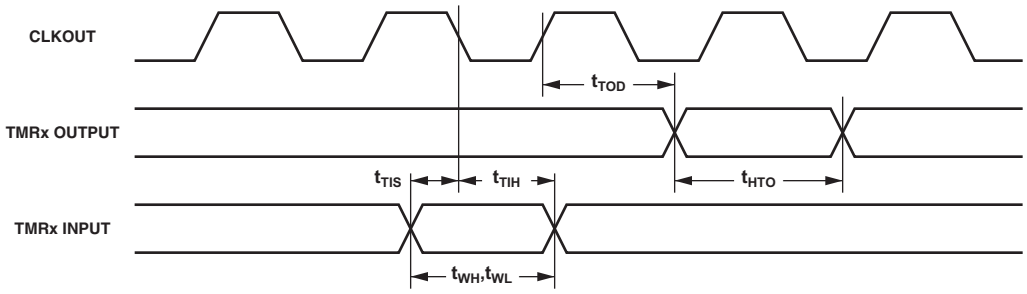


Figure 24. Timer Cycle Timing

Timer Clock Timing

Table 36 and Figure 25 describe timer clock timing.

Table 36. Timer Clock Timing

Parameter		V_{DDEXT} = 1.8 V Min	V_{DDEXT} = 1.8 V Max	V_{DDEXT} = 2.5/3.3 V Min	V_{DDEXT} = 2.5/3.3 V Max	Unit
Switching Characteristic						
t_{TODP}	Timer Output Update Delay After PPI_CLK High		12.0		12.0	ns

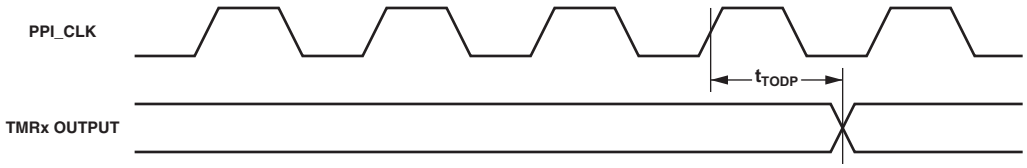


Figure 25. Timer Clock Timing

Up/Down Counter/Rotary Encoder Timing

Table 37. Up/Down Counter/Rotary Encoder Timing

Parameter		V_{DDEXT} = 1.8 V Min	V_{DDEXT} = 1.8 V Max	V_{DDEXT} = 2.5/3.3 V Min	V_{DDEXT} = 2.5/3.3 V Max	Unit
Timing Requirements						
t_{WCOUNT}	Up/Down Counter/Rotary Encoder Input Pulse Width	t_{SCLK} + 1		t_{SCLK} + 1		ns
t_{CIS}	Counter Input Setup Time Before CLKOUT High[1]	5.5		4.0		ns
t_{CIH}	Counter Input Hold Time After CLKOUT High[1]	4.0		4.0		ns

[1] Either a valid setup and hold time or a valid pulse width is sufficient. There is no need to resynchronize counter inputs.

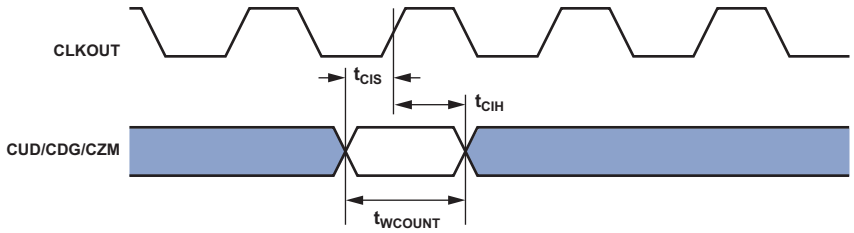


Figure 26. Up/Down Counter/Rotary Encoder Timing

Pulse Width Modulator (PWM) Timing

Table 38 and Figure 27 describe PWM operations.

Table 38. PWM Timing

Parameter		V_{DDEXT} = 1.8 V Min	V_{DDEXT} = 1.8 V Max	V_{DDEXT} = 2.5/3.3 V Min	V_{DDEXT} = 2.5/3.3 V Max	Unit
Timing Requirements						
t_{ES}	External Sync Pulse Width	$2 \times t_{SCLK} + 1$		$2 \times t_{SCLK} + 1$		ns
Switching Characteristics						
t_{DODIS}	Output[1] Inactive (OFF) After Trip Input		TBD		TBD	ns
t_{DOE}	Output[1] Delay After External Sync[2]	$3 \times t_{SCLK} + t_{OD}$	$5 \times t_{SCLK} + t_{OD}$	$3 \times t_{SCLK} + t_{OD}$	$5 \times t_{SCLK} + t_{OD}$	ns
t_{OD}	Output[1] Delay After Falling Edge of CLKOUT		TBD		TBD	ns

[1] PWM outputs are: PWMx_AH, PWMx_AL, PWMx_BH, PWMx_BL, PWMx_CH, and PWMx_CL.

[2] When the external sync signal is synchronous to the peripheral clock, it takes 3 cycles for the output to appear. When the external sync signal is asynchronous to the peripheral clock, it takes 5 cycles for the output to appear.

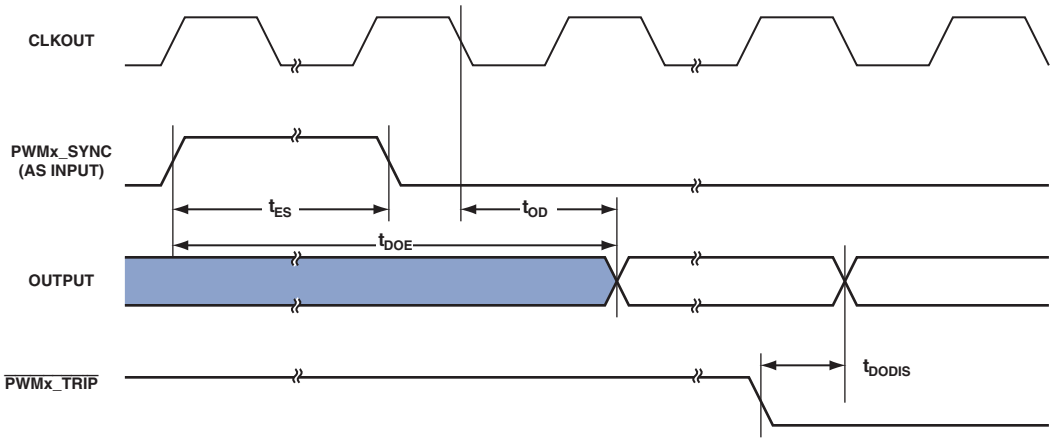


Figure 27. PWM Timing

ADC Controller Module (ACM) Timing

Table 39 and Figure 28 describe ACM operations.

Note that the ACM clock (ACLK) frequency in MHz is set by the following equation (in which ACMCKDIV ranges from 0 to 255).

$$f_{ACLK} = \frac{f_{SCLK}}{(2 \times ACMCKDIV) + 2}$$

$$t_{ACLK} = \frac{1}{f_{ACLK}}$$

Table 39. ACM Timing

Parameter		V_{DDEXT} = 1.8 V Min	V_{DDEXT} = 1.8 V Max	V_{DDEXT} = 2.5/3.3 V Min	V_{DDEXT} = 2.5/3.3 V Max	Units
Timing Requirements						
t_{SDR}	SPORT DRxPRI/DRxSEC Setup Before ACLK	7		7		ns
t_{HDR}	SPORT DRxPRI/DRxSEC Hold After ACLK	0		0		ns
Switching Characteristics						
t_{DO}	ACM Controls (ACM_A[2:0], ACM_RANGE, ACM_SGLDIFF) Delay After Falling Edge of CLKOUT		8.4		8.4	ns
t_{DACLK}	ACLK Delay After Falling Edge of CLKOUT		8.4		8.4	ns
t_{DCS}	$\overline{CS}$ Active Edge Delay After Falling Edge of CLKOUT		5.3		5.3	ns
$t_{DCSACLK}$	The Delay Between the Active Edge of $\overline{CS}$ and the First Edge of ACLK	t_{ACLK}		t_{ACLK}		ns

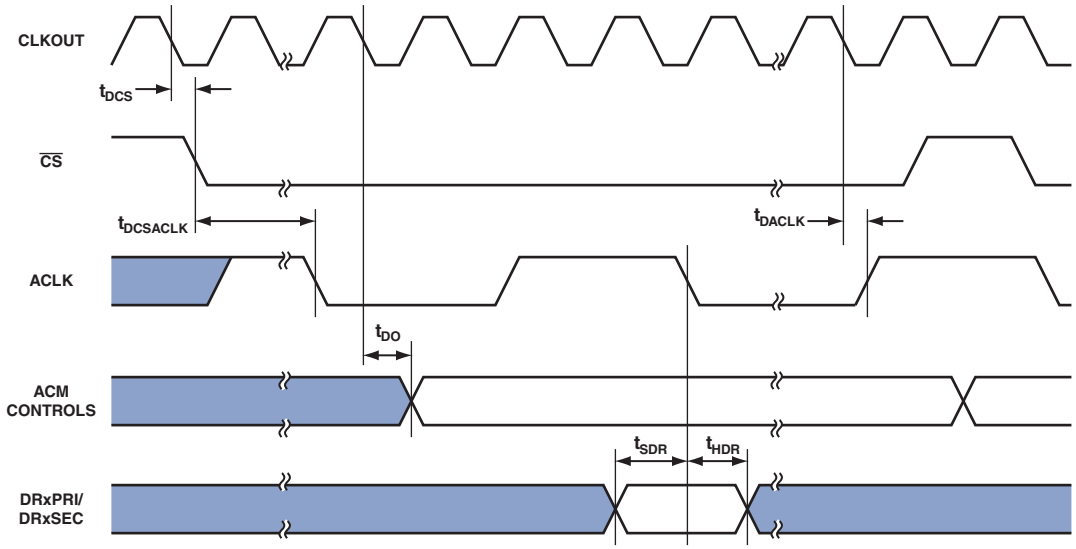


Figure 28. ACM Timing

JTAG Test And Emulation Port Timing

Table 40 and Figure 29 describe JTAG port operations.

Table 40. JTAG Port Timing

Parameter		V_{DDEXT} = 1.8 V Min	V_{DDEXT} = 1.8 V Max	V_{DDEXT} = 2.5/3.3 V Min	V_{DDEXT} = 2.5/3.3 V Max	Unit
Timing Requirements						
t_{TCK}	TCK Period	20		20		ns
t_{STAP}	TDI, TMS Setup Before TCK High	4		4		ns
t_{HTAP}	TDI, TMS Hold After TCK High	4		4		ns
t_{SSYS}	System Inputs Setup Before TCK High[1]	4		4		ns
t_{HSYS}	System Inputs Hold After TCK High[1]	5		5		ns
t_{TRSTW}	$\overline{TRST}$ Pulse Width[2] (measured in TCK cycles)	4		4		TCK
Switching Characteristics						
t_{DTDO}	TDO Delay from TCK Low		10		10	ns
t_{DSYS}	System Outputs Delay After TCK Low[3]		12.6		12	ns

[1] System Inputs = SCL, SDA, PF15–0, PG15–0, PH2–0, $\overline{NMI}$, BMODE3–0, $\overline{RESET}$, $\overline{PG}$.
[2] 50 MHz Maximum
[3] System Outputs = EXTCLK, SCL, SDA, PF15–0, PG15–0, PH2–0.

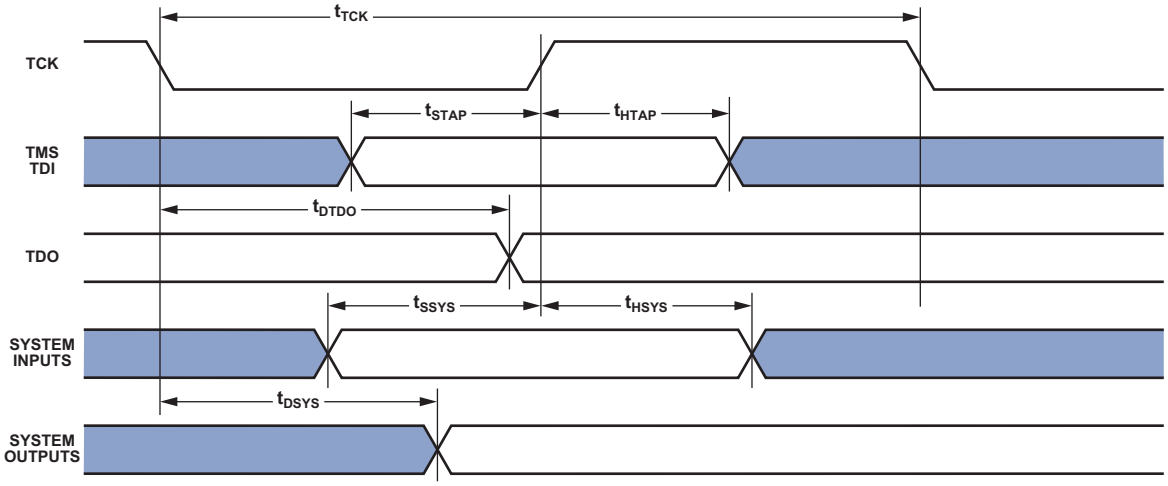


Figure 29. JTAG Port Timing

PROCESSOR — OUTPUT DRIVE CURRENTS

Figure 30 through Figure 44 show typical current-voltage characteristics for the output drivers of the ADSP-BF50x processors.

Figure 30. Driver Type A Current (3.3V V_{DDEXT})

Figure 31. Driver Type A Current (2.5V V_{DDEXT})

Figure 32. Driver Type A Current (1.8V V_{DDEXT})

The curves represent the current drive capability of the output drivers. See Table 11 on Page 21 for information about which driver type corresponds to a particular pin.

Figure 33. Driver Type B Current (3.3V V_{DDEXT})

Figure 34. Driver Type B Current (2.5V V_{DDEXT})

Figure 35. Driver Type B Current (1.8V V_{DDEXT})

Figure 36. Driver Type C Current (3.3V V_{DDEXT})

Figure 37. Drive Type C Current (2.5V V_{DDEXT})

Figure 38. Driver Type C Current (1.8V V_{DDEXT})

Figure 42. Driver Type E Current (3.3V V_{DDEXT})

Figure 39. Driver Type D Current (3.3V V_{DDEXT})

Figure 43. Driver Type E Current (2.5V V_{DDEXT})

Figure 40. Driver Type D Current (2.5V V_{DDEXT})

Figure 44. Driver Type E Current (1.8V V_{DDEXT})

Figure 41. Driver Type D Current (1.8V V_{DDEXT})

PROCESSOR — TEST CONDITIONS

All timing parameters appearing in this data sheet were measured under the conditions described in this section. Figure 45 shows the measurement point for AC measurements (except output enable/disable). The measurement point V_{MEAS} is $V_{DDEXT}/2$ for V_{DDEXT} (nominal) = 1.8 V/2.5 V/3.3 V.

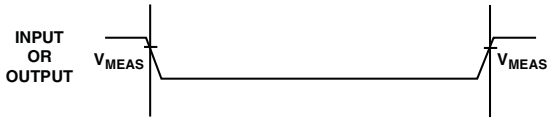


Figure 45. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Enable Time Measurement

Output pins are considered to be enabled when they have made a transition from a high impedance state to the point when they start driving.

The output enable time t_{ENA} is the interval from the point when a reference signal reaches a high or low voltage level to the point when the output starts driving as shown on the right side of Figure 46.

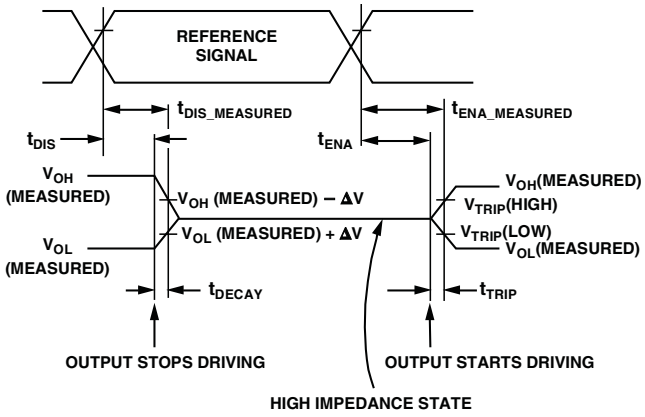


Figure 46. Output Enable/Disable

The time $t_{ENA\_MEASURED}$ is the interval, from when the reference signal switches, to when the output voltage reaches V_{TRIP}(high) or V_{TRIP}(low). For V_{DDEXT} (nominal) = 1.8V, V_{TRIP} (high) is 1.05V, and V_{TRIP} (low) is 0.75V. For V_{DDEXT} (nominal) = 2.5V, V_{TRIP} (high) is 1.5V and V_{TRIP} (low) is 1.0V. For V_{DDEXT} (nominal) = 3.3V, V_{TRIP} (high) is 1.9V, and V_{TRIP} (low) is 1.4V. Time t_{TRIP} is the interval from when the output starts driving to when the output reaches the V_{TRIP}(high) or V_{TRIP}(low) trip voltage.

Time t_{ENA} is calculated as shown in the equation:

$$t_{ENA} = t_{ENA\_MEASURED} - t_{TRIP}$$

If multiple pins are enabled, the measurement value is that of the first pin to start driving.

Output Disable Time Measurement

Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The output disable time t_{DIS} is the difference between $t_{DIS\_MEASURED}$ and t_{DECAY} as shown on the left side of Figure 46.

$$t_{DIS} = t_{DIS\_MEASURED} - t_{DECAY}$$

The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load C_L and the load current I_L. This decay time can be approximated by the equation:

$$t_{DECAY} = (C_L \Delta V)/I_L$$

The time t_{DECAY} is calculated with test loads C_L and I_L, and with ΔV equal to 0.25 V for V_{DDEXT} (nominal) = 2.5 V/3.3 V and 0.15 V for V_{DDEXT} (nominal) = 1.8V.

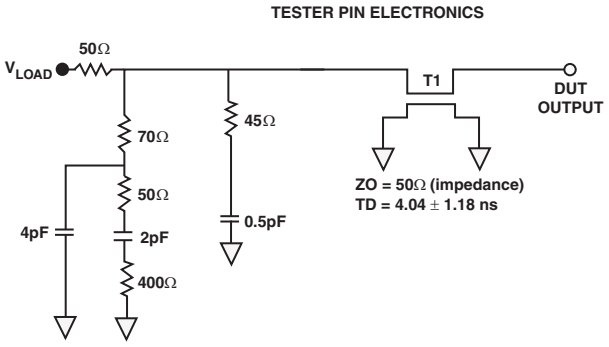
The time $t_{DIS\_MEASURED}$ is the interval from when the reference signal switches, to when the output voltage decays ΔV from the measured output high or output low voltage.

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation given above. Choose ΔV to be the difference between the processor's output voltage and the input threshold for the device requiring the hold time. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three-state current (per data line). The hold time will be t_{DECAY} plus the various output disable times as specified in the Processor — Timing Specifications on Page 31.

Capacitive Loading

Output delays and holds are based on standard capacitive loads of an average of 6 pF on all pins (see Figure 47). V_{LOAD} is equal to (V_{DDEXT}) /2. The graphs of Figure 48 through Figure 55 show how output rise time varies with capacitance. The delay and hold specifications given should be derated by a factor derived from these figures. The graphs in these figures may not be linear outside the ranges shown.



NOTES:
THE WORST CASE TRANSMISSION LINE DELAY IS SHOWN AND CAN BE USED FOR THE OUTPUT TIMING ANALYSIS TO REFELECT THE TRANSMISSION LINE EFFECT AND MUST BE CONSIDERED. THE TRANSMISSION LINE (TD), IS FOR LOAD ONLY AND DOES NOT AFFECT THE DATA SHEET TIMING SPECIFICATIONS.

ANALOG DEVICES RECOMMENDS USING THE IBIS MODEL TIMING FOR A GIVEN SYSTEM REQUIREMENT. IF NECESSARY, A SYSTEM MAY INCORPORATE EXTERNAL DRIVERS TO COMPENSATE FOR ANY TIMING DIFFERENCES.

Figure 47. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

Figure 48. Typical Rise and Fall Times (10%–90%) versus Load Capacitance for Driver A at V_{DDEXT} = Min

Figure 49. Typical Rise and Fall Times (10%–90%) versus Load Capacitance for Driver A at V_{DDEXT} = Max

Figure 50. Typical Rise and Fall Times (10%–90%) versus Load Capacitance for Driver B at V_{DDEXT} = Min

Figure 51. Typical Rise and Fall Times (10%–90%) versus Load Capacitance for Driver B at V_{DDEXT} = Max

Figure 52. Typical Rise and Fall Times (10%–90%) versus Load Capacitance for Driver C at V_{DDEXT} = Min

Figure 53. Typical Rise and Fall Times (10%–90%) versus Load Capacitance for Driver C at V_{DDEXT} = Max

Figure 54. Typical Rise and Fall Times (10%–90%) versus Load Capacitance for Driver D at V_{DDEXT} = Min

Figure 55. Typical Rise and Fall Times (10%–90%) versus Load Capacitance for Driver D at V_{DDEXT} = Max

PROCESSOR — ENVIRONMENTAL CONDITIONS

To determine the junction temperature on the application printed circuit board use:

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:

T_J = Junction temperature (°C).

T_{CASE} = Case temperature (°C) measured by customer at top center of package.

Ψ_{JT} = From Table 41 and Table 42.

P_D = Power dissipation (see Total Power Dissipation on Page 29 for the method to calculate P_D).

Table 41. Thermal Characteristics (88-Lead LFCSP)

Parameter	Condition	Typical	Unit
θ_{JA}	0 linear m/s air flow	26.2	°C/W
θ_{JMA}	1 linear m/s air flow	23.7	°C/W
θ_{JMA}	2 linear m/s air flow	22.9	°C/W
θ_{JB}		16.0	°C/W
θ_{JC}		9.8	°C/W
Ψ_{JT}	0 linear m/s air flow	0.21	°C/W
Ψ_{JT}	1 linear m/s air flow	0.36	°C/W
Ψ_{JT}	2 linear m/s air flow	0.43	°C/W

Table 42. Thermal Characteristics (120-Lead LQFP)

Parameter	Condition	Typical	Unit
θ_{JA}	0 linear m/s air flow	26.9	°C/W
θ_{JMA}	1 linear m/s air flow	24.2	°C/W
θ_{JMA}	2 linear m/s air flow	23.3	°C/W
θ_{JB}		16.4	°C/W
θ_{JC}		12.7	°C/W
Ψ_{JT}	0 linear m/s air flow	0.50	°C/W
Ψ_{JT}	1 linear m/s air flow	0.77	°C/W
Ψ_{JT}	2 linear m/s air flow	1.02	°C/W

Values of θ_{JA} are provided for package comparison and printed circuit board design considerations. θ_{JA} can be used for a first order approximation of T_J by the equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:

T_A = Ambient temperature (°C)

Values of θ_{JC} are provided for package comparison and printed circuit board design considerations when an external heat sink is required.

Values of θ_{JB} are provided for package comparison and printed circuit board design considerations.

In Table 41 and Table 42, airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6, and the junction-to-board measurement complies with JESD51-8. The junction-to-case measurement complies with MIL-STD-883 (Method 1012.1). All measurements use a 2S2P JEDEC test board.

FLASH PROGRAM AND ERASE TIMES AND ENDURANCE CYCLES

The program and erase times and the number of program/ erase cycles per block are shown in Table 43. Exact erase times may change depending on the memory array condition. The best case is when all the bits in the block or bank are at '0' (pre programmed). The worst case is when all the bits in the block or bank are at '1' (not pre programmed). Usually, the system overhead is negligible with respect to the erase time.

Table 43. Program/Erase Times and Endurance Cycles

Parameter	Condition	Typ	Typ after 100 k W/E cycles	Max	Unit
Erase	Parameter Block (4K word)[1]	0.3	1	2.5	s
	Main Block (32K word)				
	Pre Programmed	0.8	3	4	s
	Not Pre Programmed	1		4	s
Program[2]	Word	12	12	100	µs
	Parameter Block (4K word)	40			ms
	Main Block (32K word)	300			ms
Suspend Latency	Program	5		10	µs
	Erase	5		20	µs
Program/Erase Cycles (per Block)	Main Blocks			100,000	Cycles
	Parameter Blocks			100,000	Cycles

[1] The difference between pre programmed and not pre programmed is not significant (< 30 ms).
[2] Values are liable to change with the external system-level overhead (command sequence and Status Register polling execution).

FLASH – ABSOLUTE MAXIMUM RATINGS

Table 44 shows the ADC absolute maximum ratings.

Table 44. Flash Absolute Maximum Ratings

Parameter	Rating
Junction Temperature While Biased	See Table 20 on Page 30
Storage Temperature Range	–65°C to +150°C
Flash Memory Supply Voltage ($V_{DDFLASH}$)	–0.2 V to +2.45 V

ADC — SPECIFICATIONS

ADC — OPERATING CONDITIONS

Parameter	Conditions	Min	Nominal	Max	Unit
V_{DD}[1] (AV_{DD}, DV_{DD}, V_{DRIVE})	f_{ADSCLK} = 24 MHz, f_S up to 1.5 MSPS, internal or external reference = 2.5 V ± 1% unless otherwise noted	2.7		3.6	V
V_{DD} (AV_{DD}, DV_{DD}, V_{DRIVE})	f_{ADSCLK} = 32 MHz, f_S up to 2.0 MSPS, internal or external reference = 2.5 V ± 1% unless otherwise noted	4.75 (AV_{DD}, DV_{DD}) 2.7 (V_{DRIVE})		5.25 (AV_{DD}, DV_{DD}) 5.25 (V_{DRIVE})	V V
T_J Junction Temperature	120-Lead LQFP @ $T_{AMBIENT}$ = –40°C to +85°C	–40		+105	°C

[1] Throughout this datasheet, V_{DD} refers to both AV_{DD} and DV_{DD}.

Table 45. Operating Conditions (Analog, Voltage Reference, and Logic I/O)

Parameter	Specification	Unit	Test Conditions/Comments
ANALOG INPUT[1]			
Single-Ended Input Range	0 V to V_{REF}	V	RANGE= low
	0 V to 2 × V_{REF}	V	RANGE = high
Pseudo Differential Input Range: V_{IN+} – V_{IN-}[2]	0 to V_{REF}	V	RANGE = low
	2 × V_{REF}	V	RANGE = high
Fully Differential Input Range: V_{IN+} and V_{IN-}	V_{CM} ± V_{REF}/2	V	V_{CM} = common-mode voltage[3] = V_{REF}/2, RANGE = low
	V_{CM} ± V_{REF}	V	V_{CM} = V_{REF}, RANGE = high
DC Leakage Current	±1	µA max	V_{A1} to V_{A6}, V_{B1} to V_{B6}
Input Capacitance[4]	45	pF typ	When in track
	10	pF typ	When in hold
INTERNAL VOLTAGE REFERENCE (OUTPUT)[5]			
Reference Output Voltage	2.5 ± 0.2%	V	@ 25°C, AV_{DD} = 2.7 V to 5.25 V
Long-Term Stability	150	ppm typ	For 1000 hours
Output Voltage Hysteresis[6]	50	ppm typ	
D_{CAP}A, D_{CAP}B Output Impedance	10	Ω typ	
Reference Temperature Coefficient	20	ppm/°C max	10ppm/°C typ
V_{REF} Noise	20	µV rms typ	
EXTERNAL VOLTAGE REFERENCE (INPUT)[5]			
Reference Input Voltage Range[7]	0.1/AV_{DD}	V min/V max	See ADC — Typical Performance Characteristics
DC Leakage Current[7]	±2	µA max	External reference applied to Pin D_{CAP}A/Pin D_{CAP}B
Input Capacitance	25	pF typ	
DIGITAL LOGIC INPUTS			
Input High Voltage, V_{INH}	2.8	V min	
Input Low Voltage, V_{INL}	0.4	V max	
Input Current, I_{IN}	±15	nA typ	V_{IN} = 0 V or V_{DRIVE}
Input Capacitance, C_{IN}[4]	5	pF typ	

Table 45. Operating Conditions (Analog, Voltage Reference, and Logic I/O) (Continued)

Parameter	Specification	Unit	Test Conditions/Comments
DIGITAL LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DRIVE} – 0.2	V min	no DC load (I_{OH} = 0 mA)
Output Low Voltage, V_{OL}	0.4	V max	no DC load (I_{OL} = 0 mA)
Floating State Leakage Current	±1	µA max	V_{IN} = 0V or V_{DRIVE}
Floating State Output Capacitance[4]	7	pF typ	
Output Coding[8]	Straight (natural) binary		SGL/$\overline{DIFF}$ = 1
	Twos complement		SGL/$\overline{DIFF}$ = 0; SGL/$\overline{DIFF}$ = 1

[1] V_{IN-} or V_{IN+} must remain within GND/V_{DD}.
[2] V_{IN-} = 0V for specified performance. For full input range on V_{IN-} pin, see Figure 80 and Figure 81.
[3] For full common-mode range, see Figure 76 and Figure 77.
[4] Sample tested during initial release to ensure compliance.
[5] Relates to Pin D_{CAP}A or Pin D_{CAP}B.
[6] See ADC — Terminology on Page 60.
[7] External voltage reference applied to Pins D_{CAP}A, Pin D_{CAP}B (V_{REF})
[8] See Table 50 and Table 51.

Table 46. Operating Conditions (ADC Performance/Accuracy)

Parameter	Specification	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			
Signal-to-Noise Ratio (SNR)	71	dB min	f_{IN} = 50 kHz sine wave; differential mode
	69	dB min	f_{IN} = 50 kHz sine wave; single-ended and pseudo differential modes
Signal-to-(Noise + Distortion) Ratio (SINAD)[1]	70	dB min	f_{IN} = 50 kHz sine wave; differential mode
	68	dB min	f_{IN} = 50 kHz sine wave; single-ended and pseudo differential modes
Total Harmonic Distortion (THD)[1]	–77	dB max	f_{IN} = 50 kHz sine wave; differential mode
	–73	dB max	f_{IN} = 50 kHz sine wave; single-ended and pseudo differential modes
Spurious-Free Dynamic Range (SFDR)[1]	–75	dB max	f_{IN} = 50 kHz sine wave
Intermodulation Distortion (IMD)[1]			fa = 30 kHz, fb = 50 kHz
Second-Order Terms	–88	dB typ	
Third-Order Terms	–88	dB typ	
Channel-to-Channel Isolation	–88	dB typ	
SAMPLE AND HOLD			
Aperture Delay[2]	11	ns max	
Aperture Jitter[2]	50	ps typ	
Aperture Delay Matching[2]	200	ps max	
Full Power Bandwidth	33/26	MHz typ	@ 3 dB, AV_{DD}, DV_{DD} = 5 V/AV_{DD}, DV_{DD} = 3 V
	3.5/3	MHz typ	@ 0.1 dB, AV_{DD}, DV_{DD} = 5 V/AV_{DD}, DV_{DD} = 3 V

Table 46. Operating Conditions (ADC Performance/Accuracy) (Continued)

Parameter	Specification	Unit	Test Conditions/Comments
DC ACCURACY			
Resolution	12	Bits	
Integral Nonlinearity (INL)[1]	±1	LSB max	±0.7 LSB typ; differential mode
	±1.5	LSB max	±0.9 LSB typ; single-ended and pseudo differential modes
Differential Nonlinearity (DNL)[1, 3]	±0.99	LSB max	Differential mode
	–0.99/+1.5	LSB max	Single-ended and pseudo differential modes
Straight Natural Binary Output Coding			
Offset Error[1]	TBD	LSB max	
Offset Error Match[1]	TBD	LSB typ	
Gain Error[1]	TBD	LSB max	
Gain Error Match[1]	TBD	LSB typ	
Twos Complement Output Coding			
Positive Gain Error[1]	TBD	LSB max	
Positive Gain Error Match[1]	TBD	LSB typ	
Zero Code Error[1]	TBD	LSB max	
Zero Code Error Match[1]	TBD	LSB typ	
Negative Gain Error[1]	TBD	LSB max	
Negative Gain Error Match[1]	TBD	LSB typ	
CONVERSION RATE			
Conversion Time	14	ADSCLK cycles	437.5 ns with ADSCLK = 32 MHz
Track-and-Hold Acquisition Time[2]	90	ns max	Full-scale step input; AV_{DD}, DV_{DD} = 5 V
	110	ns max	Full-scale step input; AV_{DD}, DV_{DD} = 3 V
Throughput Rate	2	MSPS max	

[1] See ADC — Terminology on Page 60.
[2] Sample tested during initial release to ensure compliance.
[3] Guaranteed no missed codes to 12 bits.

Table 47. Operating Conditions (Power[1])

Parameter	Specification	Unit	Test Conditions/Comments
POWER SUPPLY REQUIREMENTS			
V_{DD}	2.7/5.25	V min/V max	
V_{DRIVE}	2.7/5.25	V min/V max	
I_{DD}			Digital Logic Inputs = 0 V or V_{DRIVE}
Normal Mode (Static)	2.3	mA max	V_{DD} = 5.25 V
Operational			
f_S = 2 MSPS	6.4	mA max	V_{DD} = 5.25 V; 5.7 mA typ
f_S = 1.5 MSPS	4	mA max	V_{DD} = 3.6 V; 3.4 mA typ
Partial Power-Down Mode	500	µA max	Static
Full Power-Down Mode (V_{DD})	2.8	µA max	
POWER DISSIPATION			
Normal Mode (Operational)	33.6	mW max	V_{DD} = 5.25 V
Partial Power-Down (Static)	2.625	mW max	V_{DD} = 5.25 V
Full Power-Down (Static)	14.7	µW max	V_{DD} = 5.25 V

[1] In this table, V_{DD} refers to both AV_{DD} and DV_{DD}.

ADC — TIMING SPECIFICATIONS

Table 48. Serial Data Interface[1]

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Description/Conditions
f_{ADSCLK}[2]	4/32	MHz min/max	
$t_{CONVERT}$	14 × t_{ADSCLK}	ns max	$t_{ADSCLK} = 1/f_{ADSCLK}$
	437.5	ns max	f_{ADSCLK} = 32 MHz, f_{SAMPLE} = 2 MSPS; AV_{DD}, DV_{DD} = 5 V
	583.3	ns max	f_{ADSCLK} = 24 MHz, f_{SAMPLE} = 1.5 MSPS; AV_{DD}, DV_{DD} = 3 V
t_{QUIET}	30	ns min	Minimum time between end of serial read and next falling edge of $\overline{CS}$
t_2	20/30	ns min	$\overline{CS}$ to ADSCLK setup time; V_{DRIVE} = 5 V/3 V
t_3	15	ns max	Delay from $\overline{CS}$ until $D_{OUT}A$ and $D_{OUT}B$ are three-state disabled
t_4[3]	27/36	ns max	Data access time after ADSCLK falling edge, V_{DRIVE} = 5 V/3 V
t_5	0.45 t_{ADSCLK}	ns min	ADSCLK low pulse width
t_6	0.45 t_{ADSCLK}	ns min	ADSCLK high pulse width
t_7	5/10	ns min	ADSCLK to data valid hold time, V_{DRIVE} = 5 V/3 V
t_8	15	ns max	$\overline{CS}$ rising edge to $D_{OUT}A$, $D_{OUT}B$, high impedance
t_9	30	ns min	$\overline{CS}$ rising edge to falling edge pulse width
t_{10}	5/35	ns min/max	ADSCLK falling edge to $D_{OUT}A$, $D_{OUT}B$, high impedance

[1] See also Figure 93 on Page 71 and Figure 94 on Page 71.
[2] Minimum ADSCLK for specified performance; with slower ADSCLK frequencies, performance specifications apply typically.
[3] The time required for the output to cross 0.4 V or 2.4 V.

ADC — ABSOLUTE MAXIMUM RATINGS

Stresses above those listed in Table 49 may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 49. Absolute Maximum Ratings

Parameter	Rating
AV_{DD}, DV_{DD} to AGND	–0.3 V to +7 V
DV_{DD} to DGND	–0.3 V to +7 V
V_{DRIVE} to DGND	–0.3 V to DV_{DD}
V_{DRIVE} to AGND	–0.3 V to AV_{DD}
AV_{DD} to DV_{DD}	–0.3 V to +0.3 V
AGND to DGND	–0.3 V to +0.3 V
Analog Input Voltage to AGND	–0.3 V to AV_{DD} + 0.3 V
Digital Input Voltage to DGND	–0.3 V to +7 V
Digital Output Voltage to GND	–0.3 V to V_{DRIVE} + 0.3 V
V_{REF} to AGND	–0.3 V to AV_{DD} + 0.3 V
Input Current to Any ADC Pin Except Supplies[1]	±10 mA
Storage Temperature Range	–65°C to +150°C
Junction Temperature Under Bias	+110°C

[1] Transient currents of up to 100 mA will not cause latch up.

ADC — TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

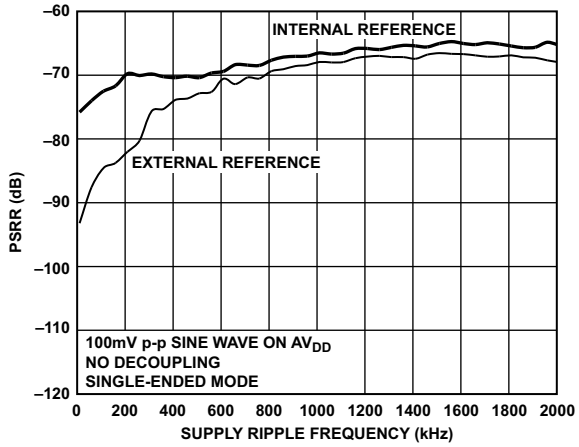


Figure 56. PSRR vs. Supply Ripple Frequency Without Supply Decoupling

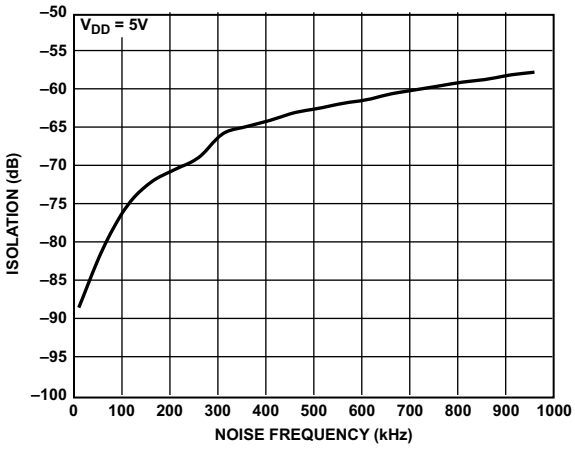


Figure 57. Channel-to-Channel Isolation

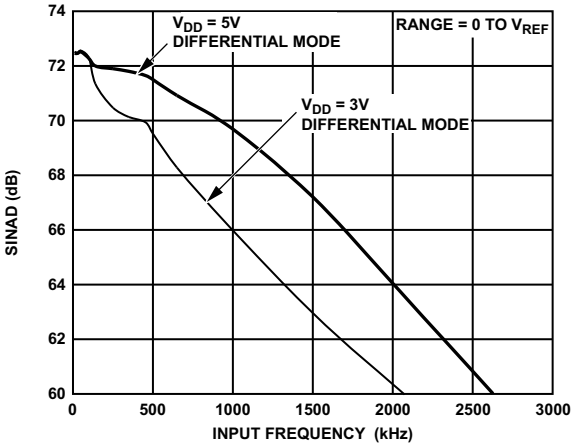


Figure 58. SINAD vs. Analog Input Frequency for Various Supply Voltages

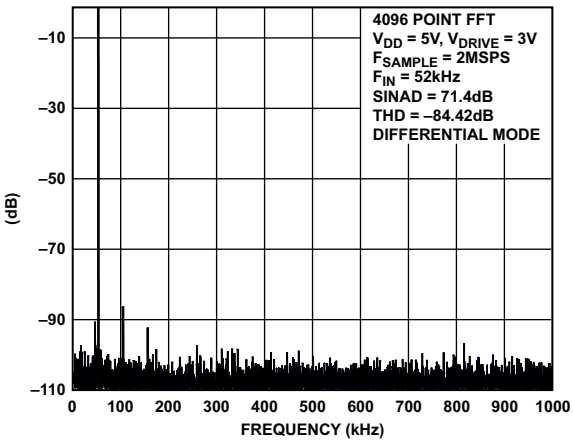


Figure 59. FFT

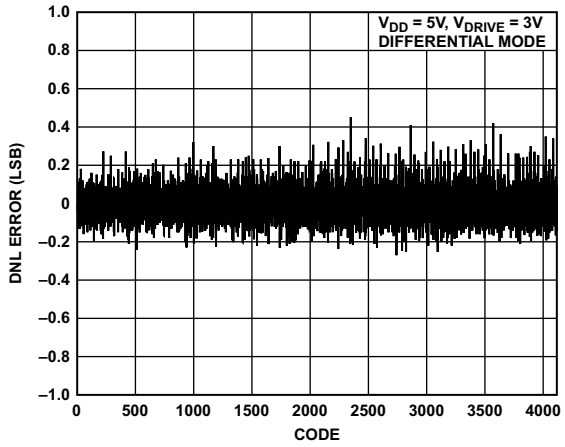


Figure 60. Typical DNL

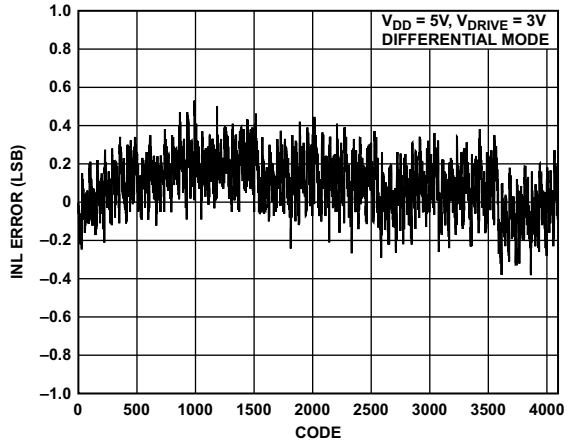


Figure 61. Typical INL

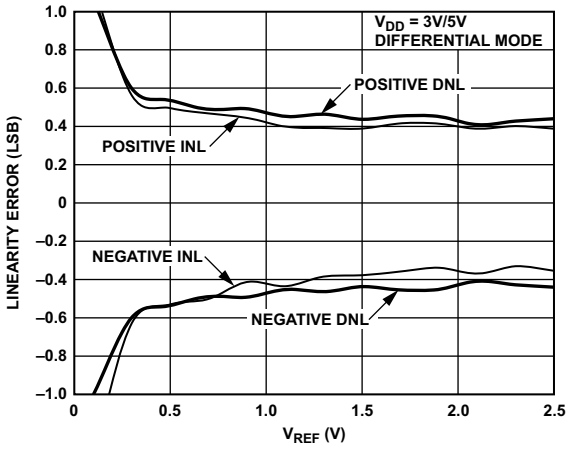


Figure 62. Linearity Error vs. V_{REF}

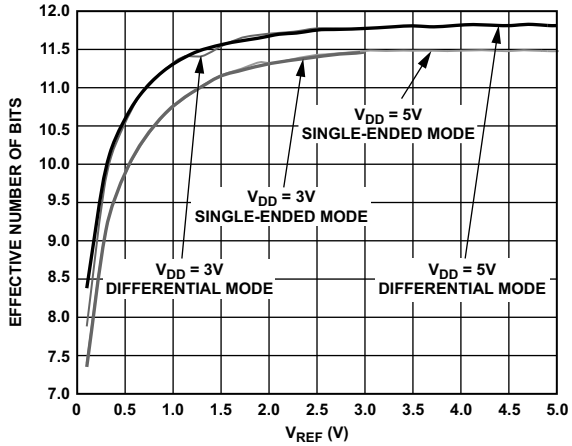


Figure 63. Effective Number of Bits vs. V_{REF}

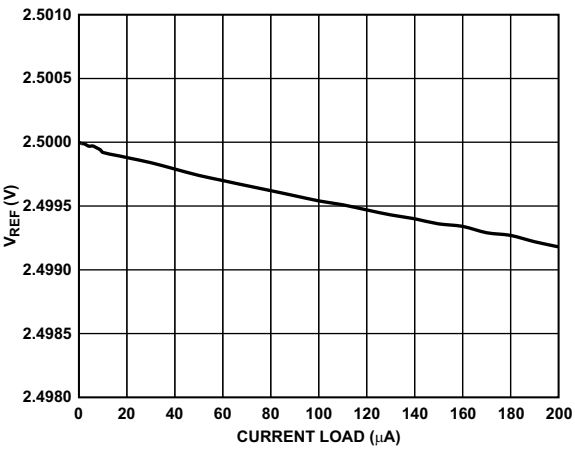


Figure 64. V_{REF} vs. Reference Output Current Drive

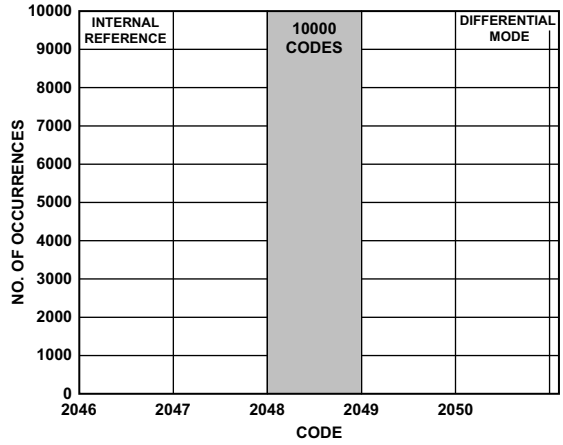


Figure 65. Histogram of Codes for 10k Samples in Differential Mode

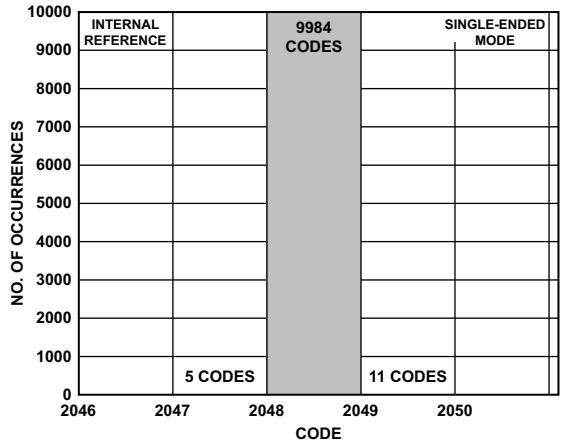


Figure 66. Histogram of Codes for 10k Samples in Single-Ended Mode

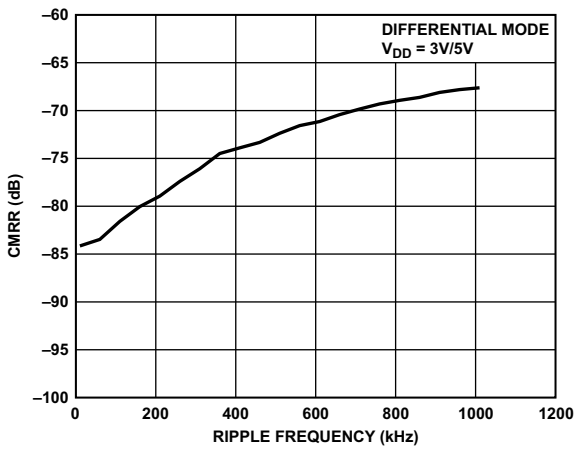


Figure 67. CMRR vs. Common-Mode Ripple Frequency

ADC — TERMINOLOGY

Differential Nonlinearity (DNL)
Differential nonlinearity is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Integral Nonlinearity (INL)
Integral nonlinearity is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale with a single (1) LSB point below the first code transition, and full scale with a 1 LSB point above the last code transition.

Offset Error
Offset error applies to straight binary output coding. It is the deviation of the first code transition (00 . . . 000) to (00 . . . 001) from the ideal (AGND + 1 LSB).

Offset Error Match
Offset error match is the difference in offset error across all 12 channels.

Gain Error
Gain error applies to straight binary output coding. It is the deviation of the last code transition (111 . . . 110) to (111 . . . 111) from the ideal (V_{REF} 1 LSB) after the offset error is adjusted out. Gain error does not include reference error.

Gain Error Match
Gain error match is the difference in gain error across all 12 channels.

Positive Gain Error
This applies when using twos complement output coding with, for example, the 2 × V_{REF} input range as –V_{REF} to +V_{REF} biased about the V_{REF} point. It is the deviation of the last code transition (011…110) to (011…111) from the ideal (+V_{REF} 1 LSB) after the zero code error is adjusted out.

Positive Gain Error Match
This is the difference in positive gain error across all 12 channels.

Zero Code Error
Zero code error applies when using twos complement output coding with, for example, the 2 × V_{REF} input range as –V_{REF} to +V_{REF} biased about the V_{REF} point. It is the deviation of the mid-scale transition (all 0s to all 1s) from the ideal V_{IN} voltage (V_{REF}).

Zero Code Error Match
Zero code error match refers to the difference in zero code error across all 12 channels.

Negative Gain Error
This applies when using twos complement output coding option, in particular the 2 × V_{REF} input range as –V_{REF} to +V_{REF} biased about the V_{REF} point. It is the deviation of the first code transition (100…000) to (100…001) from the ideal (that is, –V_{REF} + 1 LSB) after the zero code error is adjusted out.

Negative Gain Error Match
This is the difference in negative gain error across all 12 channels.

Track-and-Hold Acquisition Time
The track-and-hold amplifier returns to track mode after the end of conversion. Track-and-hold acquisition time is the time required for the output of the track-and-hold amplifier to reach its final value, within ±1/2 LSB, after the end of conversion.

Signal-to-(Noise + Distortion) Ratio (SINAD)
This ratio is the measured ratio of signal-to-(noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitalization process; the more levels, the smaller the quantization noise. The theoretical signal-to-(noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by

Signal-to-(*Noise* + *Distortion*) = (6.02N + 1.76) dB

Therefore, for a 12-bit converter, theoretical SINAD is 74 dB.

Total Harmonic Distortion (THD)
Total harmonic distortion is the ratio of the rms sum of harmonics to the fundamental. For the ADC, it is defined as

$$THD(dB) = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where:

V_1 is the rms amplitude of the fundamental.

V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through the sixth harmonics.

Effective Number of Bits (ENOB)
This is a figure of merit which characterizes the dynamic performance of the ADC at a specified input frequency and sampling rate. ENOB is expressed in bits. For a full scale sinusoidal input, ENOB is defined as:
ENOB = (SINAD – 1.76)/6.02.

Peak Harmonic or Spurious Noise (SFDR)
Peak harmonic, or spurious noise, is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$, excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it is a noise peak.

Channel-to-Channel Isolation
Channel-to-channel isolation is a measure of the level of crosstalk between channels. It is measured by applying a full-scale (2 × V_{REF} when V_{DD} = 5 V, V_{REF} when V_{DD} = 3 V), 10 kHz sine wave signal to all un-selected input channels and

determining how much that signal is attenuated in the selected channel with a 50 kHz signal (0 V to V_{REF}). The result obtained is the worst-case across all 12 channels for the ADC.

Intermodulation Distortion (IMD)

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with non-linearities create distortion products at sum, and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, and so on. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second-order terms include (fa + fb) and (fa fb), while the third-order terms include (2fa + fb), (2fa fb), (fa + 2fb), and (fa 2fb).

The ADC is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second-order terms are usually distanced in frequency from the original sine waves, while the third-order terms are usually at a frequency close to the input frequencies. As a result, the second-order and third-order terms are specified separately. The calculation of the inter-modulation distortion is as per the THD specification, where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dBs.

Common-Mode Rejection Ratio (CMRR)

CMRR is defined as the ratio of the power in the ADC output at full-scale frequency, f, to the power of a 100 mV p-p sine wave applied to the common-mode voltage of V_{IN+} and V_{IN} of frequency f_S as

$$CMRR\ (\text{dB}) = 10\log(Pf/Pf_S)$$

where:

Pf is the power at frequency *f* in the ADC output.

Pf_S is the power at frequency f_S in the ADC output.

Power Supply Rejection Ratio (PSRR)

Variations in power supply affect the full-scale transition but not the converter's linearity. PSRR is the maximum change in the full-scale transition point due to a change in power supply voltage from the nominal value (see Figure 56 (PSRR vs. Supply Ripple Frequency Without Supply Decoupling).

Thermal Hysteresis

Thermal hysteresis is defined as the absolute maximum change of reference output voltage after the device is cycled through temperature from either

$$T\_HYS+ = +25°C \text{ to } T_{MAX} \text{ to } +25°C$$

or

$$T\_HYS = +25°C \text{ to } T_{MIN} \text{ to } +25°C$$

It is expressed in ppm by

$$V_{HYS}(ppm) = \left|\frac{V_{REF}(25°C) - V_{REF}(T\_HYS)}{V_{REF}(25°C)}\right| \times 10^6$$

where:

V_{REF} (25°C) is V_{REF} at 25°C.

V_{REF} *(T_HYS)* is the maximum change of V_{REF} at T_HYS+ or T_HYS.

ADC — THEORY OF OPERATION

The following sections describe the ADC theory of operation.

Circuit Information

The ADC is a fast, micro-power, dual, 12-bit, single-supply, ADC that operates from a 2.7 V to a 5.25 V supply. When operated from a 5 V supply, the ADC is capable of throughput rates of up to 2 MSPS when provided with a 32 MHz clock, and a throughput rate of up to 1.5 MSPS at 3 V.

The ADC contains two on-chip, differential track-and-hold amplifiers, two successive approximation ADCs, and a serial interface with two separate data output pins.

The serial clock input accesses data from the part but also provides the clock source for each successive approximation ADC. The analog input range for the part can be selected to be a 0 V to V_{REF} input or a 2 × V_{REF} input, configured with either single-ended or differential analog inputs. The ADC has an on-chip 2.5 V reference that can be overdriven when an external reference is preferred. If the internal reference is to be used elsewhere in a system, then the output needs to buffered first.

The ADC also features power-down options to allow power saving between conversions. The power-down feature is implemented via the standard serial interface, as described in the ADC — Modes of Operation section.

Converter Operation

The ADC has two successive approximation ADCs, each based around two capacitive DACs. Figure 68 (ADC Acquisition Phase) and Figure 69 (ADC Conversion Phase) show simplified schematics of one of these ADCs in acquisition and conversion phase, respectively. The ADC is comprised of control logic, a SAR, and two capacitive DACs. In Figure 68 (ADC Acquisition Phase) (the acquisition phase), SW3 is closed, SW1 and SW2 are in Position A, the comparator is held in a balanced condition, and the sampling capacitor arrays acquire the differential signal on the input.

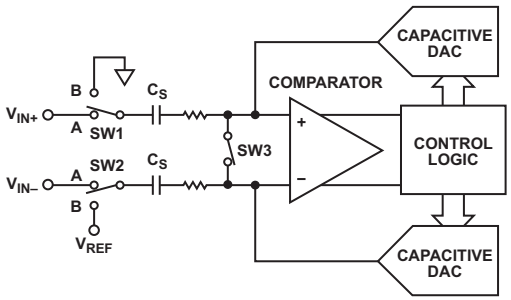


Figure 68. ADC Acquisition Phase

When the ADC starts a conversion (see Figure 69 (ADC Conversion Phase)), SW3 opens and SW1 and SW2 move to Position B, causing the comparator to become unbalanced. Both inputs are disconnected once the conversion begins. The control logic and the charge redistribution DACs are used to add and subtract fixed amounts of charge from the sampling capacitor arrays to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code. The output impedances of the sources driving the V_{IN+} and V_{IN-} pins must be matched; otherwise, the two inputs will have different settling times, resulting in errors.

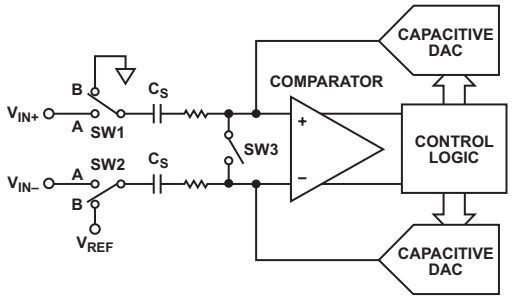


Figure 69. ADC Conversion Phase

Analog Input Structure

Figure 70 (Equivalent Analog Input Circuit, Conversion Phase—Switches Open, Track Phase—Switches Closed) shows the equivalent circuit of the analog input structure of the ADC in differential/pseudo differential mode. In single-ended mode, V_{IN} is internally tied to AGND. The four diodes provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signals never exceed the supply rails by more than 300 mV. This causes these diodes to become forward-biased and starts conducting into the substrate. These diodes can conduct up to 10 mA without causing irreversible damage to the part.

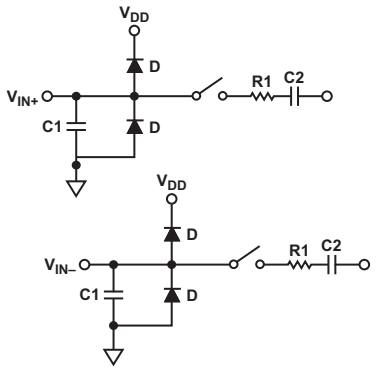


Figure 70. Equivalent Analog Input Circuit, Conversion Phase—Switches Open, Track Phase—Switches Closed

The C1 capacitors in Figure 70 (Equivalent Analog Input Circuit, Conversion Phase—Switches Open, Track Phase—Switches Closed) are typically 4 pF and can primarily be attributed to pin capacitance. The resistors are lumped components made up of the on resistance of the switches. The value of these resistors is typically about 100 Ω. The C2 capacitors are the ADC's sampling capacitors with a capacitance of 45 pF typically.

For ac applications, removing high frequency components from the analog input signal is recommended by the use of an RC low-pass filter on the relevant analog input pins with optimum values of 47 Ω and 10 pF. In applications where harmonic distortion and signal-to-noise ratio are critical, the analog input should be driven from a low impedance source. Large source impedances significantly affect the ac performance of the ADC and may necessitate the use of an input buffer amplifier. The choice of the op amp is a function of the particular application.

When no amplifier is used to drive the analog input, the source impedance should be limited to low values. The maximum source impedance depends on the amount of THD that can be tolerated.

The THD increases as the source impedance increases and performance degrades. Figure 71 (THD vs. Analog Input Frequency for Various Source Impedances, Single-Ended Mode shows a graph of the THD vs. the analog input signal frequency for different source impedances in single-ended mode, while Figure 72 (THD vs. Analog Input Frequency for Various Source Impedances, Differential Mode) shows the THD vs. the analog input signal frequency for different source impedances in differential mode.

Figure 73 (THD vs. Analog Input Frequency for Various Supply Voltages) shows a graph of the THD vs. the analog input frequency for various supplies while sampling at 2 MSPS. In this case, the source impedance is 47 Ω.

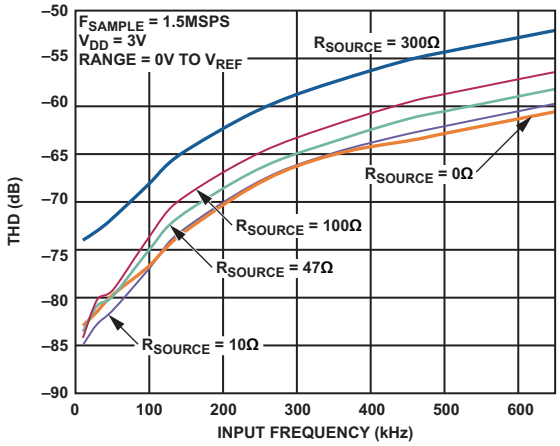


Figure 71. THD vs. Analog Input Frequency for Various Source Impedances, Single-Ended Mode

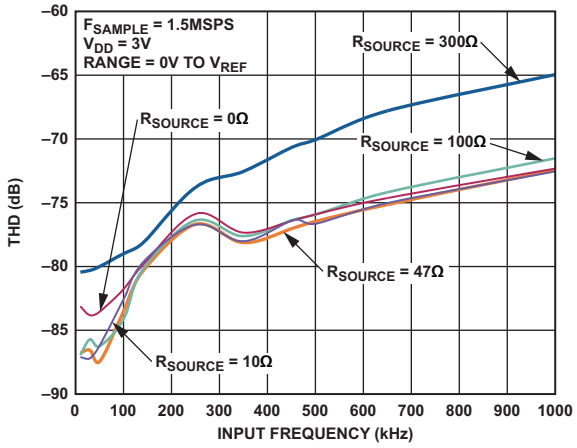


Figure 72. THD vs. Analog Input Frequency for Various Source Impedances, Differential Mode

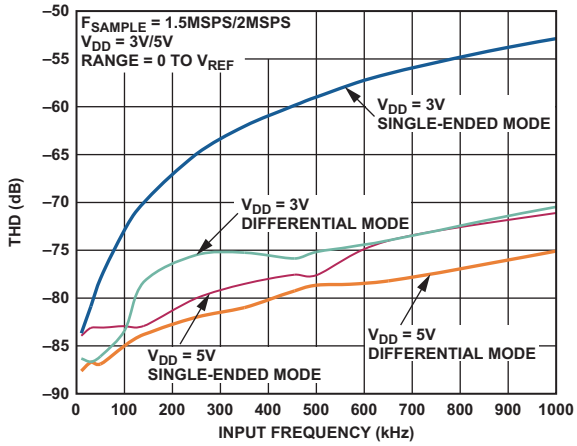


Figure 73. THD vs. Analog Input Frequency for Various Supply Voltages

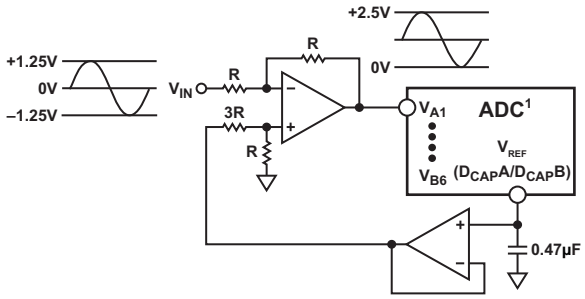
Analog Inputs

The ADC has a total of 12 analog inputs. Each on-board ADC has six analog inputs that can be configured as six single-ended channels, three pseudo differential channels, or three fully differential channels. These may be selected as described in the Analog Input Selection section.

Single-Ended Mode

The ADC can have a total of 12 single-ended analog input channels. In applications where the signal source has high impedance, it is recommended to buffer the analog input before applying it to the ADC. The analog input range can be programmed to be either 0 to V_{REF} or 0 to 2 × V_{REF}.

If the analog input signal to be sampled is bipolar, the internal reference of the ADC can be used to externally bias up this signal to make it correctly formatted for the ADC. Figure 74 shows a typical connection diagram when operating the ADC in single-ended mode.



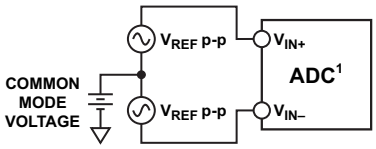
[1]ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 74. Single-Ended Mode Connection Diagram

Differential Mode

The ADC can have a total of six differential analog input pairs.

Differential signals have some benefits over single-ended signals, including noise immunity based on the device's common-mode rejection and improvements in distortion performance. Figure 75 (Differential Input Definition) defines the fully differential analog input of the ADC.



[1]ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 75. Differential Input Definition

The amplitude of the differential signal is the difference between the signals applied to the V_{IN+} and V_{IN-} pins in each differential pair (V_{IN+} V_{IN-}). V_{IN+} and V_{IN-} should be simultaneously driven by two signals each of amplitude V_{REF} (or 2 × V_{REF}, depending on the range chosen) that are 180° out of phase. The amplitude of the differential signal is, therefore (assuming the 0 to V_{REF} range is selected) –V_{REF} to +V_{REF} peak-to-peak (2 × V_{REF}), regardless of the common mode (CM).

The common mode is the average of the two signals

$(V_{IN+} + V_{IN-})/2$

and is, therefore, the voltage on which the two inputs are centered.

This results in the span of each input being CM ± V_{REF}/2. This voltage has to be set up externally and its range varies with the reference value, V_{REF}. As the value of V_{REF} increases, the common-mode range decreases. When driving the inputs with an amplifier, the actual common-mode range is determined by the amplifier's output voltage swing.

Figure 76 (Input Common-Mode Range vs. VREF (0 to VREF Range, VDD = 5 V)) and Figure 77 (Input Common-Mode Range vs. VREF (2 × VREF Range, VDD = 5 V)) show how the common-mode range typically varies with V_{REF} for a 5 V power

supply using the 0 to V_{REF} range or 2 × V_{REF} range, respectively. The common mode must be in this range to guarantee the functionality of the ADC.

When a conversion takes place, the common mode is rejected, resulting in a virtually noise free signal of amplitude –V_{REF} to +V_{REF} corresponding to the digital codes of 0 to 4096. If the 2 × V_{REF} range is used, then the input signal amplitude extends from – 2 V_{REF} to +2 V_{REF} after conversion.

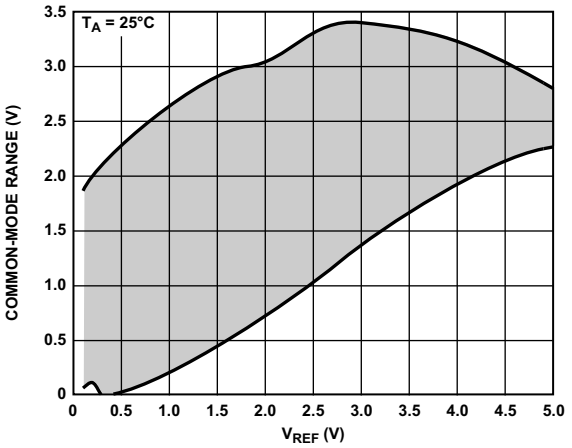


Figure 76. Input Common-Mode Range vs. V_{REF} (0 to V_{REF} Range, V_{DD} = 5 V)

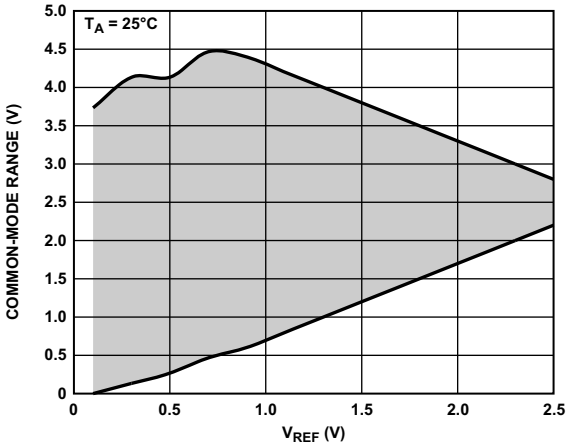


Figure 77. Input Common-Mode Range vs. V_{REF} (2 × V_{REF} Range, V_{DD} = 5 V)

Driving Differential Inputs

Differential operation requires that V_{IN+} and V_{IN-} be simultaneously driven with two equal signals that are 180° out of phase. The common mode must be set up externally. The common-mode range is determined by V_{REF}, the power supply, and the particular amplifier used to drive the analog inputs. Differential modes of operation with either an ac or dc input provide the best THD performance over a wide frequency range. Because not all applications have a signal preconditioned for differential operation, there is often a need to perform single-ended-to-differential conversion.

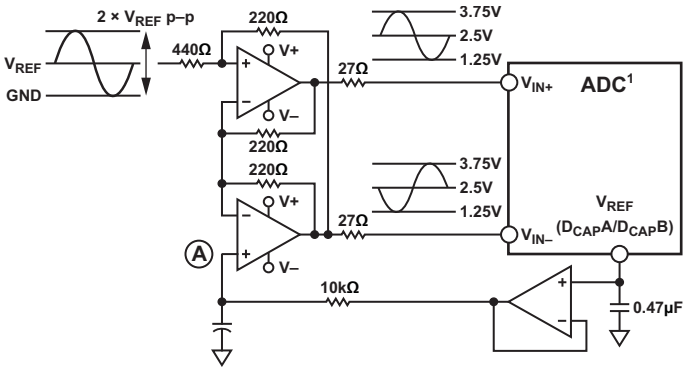
Using an Op Amp Pair

An op amp pair can be used to directly couple a differential signal to one of the analog input pairs of the ADC. The circuit configurations illustrated in Figure 78 (Dual Op Amp Circuit to Convert a Single-Ended Unipolar Signal into a Differential Signal) and Figure 79 (Dual Op Amp Circuit to Convert a Single-Ended Bipolar Signal into a Differential Unipolar Signal) show how a dual op amp can be used to convert a single-ended signal into a differential signal for both a bipolar and unipolar input signal, respectively.

The voltage applied to Point A sets up the common-mode voltage. In both diagrams, it is connected in some way to the reference, but any value in the common-mode range can be input here to set up the common mode. The AD8022 is a suitable dual op amp that can be used in this configuration to provide differential drive to the ADC.

Take care when choosing the op amp; the selection depends on the required power supply and system performance objectives. The driver circuits in Figure 78 (Dual Op Amp Circuit to Convert a Single-Ended Unipolar Signal into a Differential Signal) and Figure 79 (Dual Op Amp Circuit to Convert a Single-Ended Bipolar Signal into a Differential Unipolar Signal) are optimized for dc coupling applications requiring best distortion performance.

The circuit configuration shown in Figure 78 (Dual Op Amp Circuit to Convert a Single-Ended Unipolar Signal into a Differential Signal) converts a unipolar, single-ended signal into a differential signal.



[1]ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 78. Dual Op Amp Circuit to Convert a Single-Ended Unipolar Signal into a Differential Signal

The differential op amp driver circuit shown in Figure 79 (Dual Op Amp Circuit to Convert a Single-Ended Bipolar Signal into a Differential Unipolar Signal) is configured to convert and level shift a single-ended, ground-referenced (bipolar) signal to a differential signal centered at the V_{REF} level of the ADC.

Pseudo Differential Mode

The ADC can have a total of six pseudo differential pairs. In this mode, V_{IN+} is connected to the signal source that must have an amplitude of V_{REF} (or 2 × V_{REF}, depending on the range chosen)

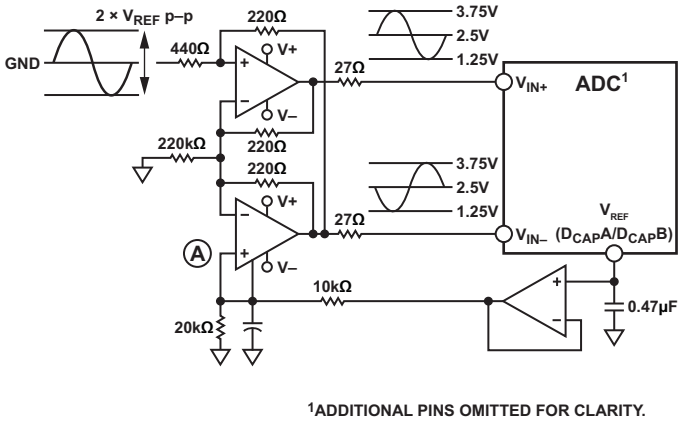


Figure 79. Dual Op Amp Circuit to Convert a Single-Ended Bipolar Signal into a Differential Unipolar Signal

to make use of the full dynamic range of the part. A dc input is applied to the V_{IN-} pin. The voltage applied to this input provides an offset from ground or a pseudo ground for the V_{IN+} input. The benefit of pseudo differential inputs is that they separate the analog input signal ground from the ADC's ground allowing dc common-mode voltages to be cancelled.

The typical voltage range for the V_{IN-} pin, while in pseudo differential mode, is shown in Figure 80 (V_{IN-} Input Voltage Range vs. V_{REF} in Pseudo Differential Mode with V_{DD} = 3 V) and Figure 81 (V_{IN-} Input Voltage Range vs. V_{REF} in Pseudo Differential Mode with V_{DD} = 5 V). Figure 82 (Pseudo Differential Mode Connection Diagram) shows a connection diagram for pseudo differential mode.

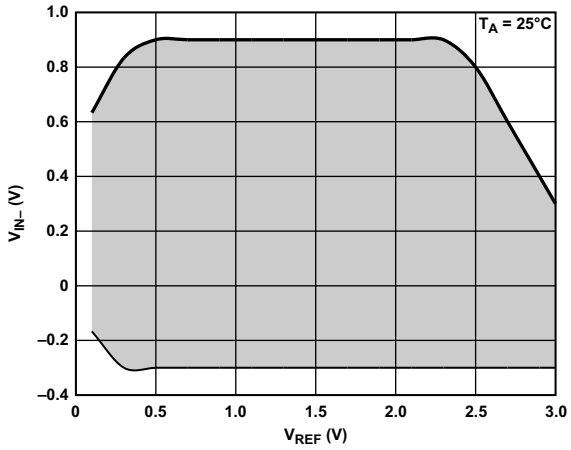


Figure 80. V_{IN-} Input Voltage Range vs. V_{REF} in Pseudo Differential Mode with V_{DD} = 3 V

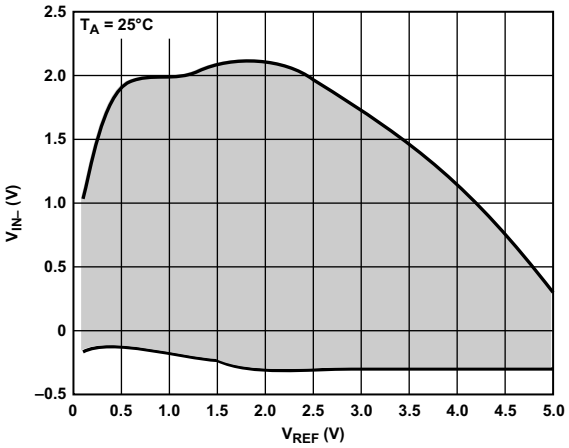


Figure 81. V_{IN-} Input Voltage Range vs. V_{REF} in Pseudo Differential Mode with V_{DD} = 5 V

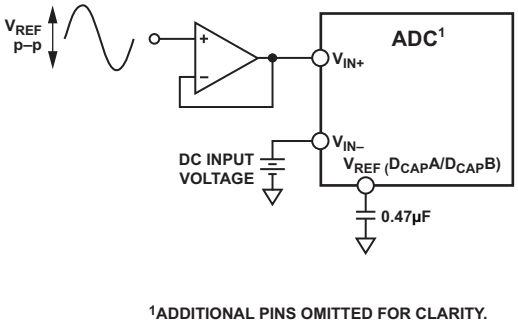


Figure 82. Pseudo Differential Mode Connection Diagram

Analog Input Selection

The analog inputs of the ADC can be configured as single-ended or true differential via the SGL/$\overline{\text{DIFF}}$ logic pin, as shown in Figure 83 (Selecting Differential or Single-Ended Configuration). If this pin is tied to a logic low, the analog input channels to each on-chip ADC are set up as three true differential pairs. If this pin is at logic high, the analog input channels to each on-chip ADC are set up as six single-ended analog inputs. The required logic level on this pin needs to be established prior to the acquisition time and remain unchanged during the conversion time until the track-and-hold has returned to track. The track-and-hold returns to track on the 13th rising edge of ADSCLK after the $\overline{\text{CS}}$ falling edge (see Figure 93 (Serial Interface Timing Diagram)). If the level on this pin is changed, it will be recognized by the ADC; therefore, it is necessary to keep the same logic level during acquisition and conversion to avoid corrupting the conversion in progress.

For example, in Figure 83 (Selecting Differential or Single-Ended Configuration) the SGL/$\overline{\text{DIFF}}$ pin is set at logic high for the duration of both the acquisition and conversion times so the analog inputs are configured as single ended for that conversion (Sampling Point A). The logic level of the SGL/$\overline{\text{DIFF}}$ changed to low after the track-and-hold returned to track and prior to the

required acquisition time for the next sampling instant at Point B; therefore, the analog inputs are configured as differential for that conversion.

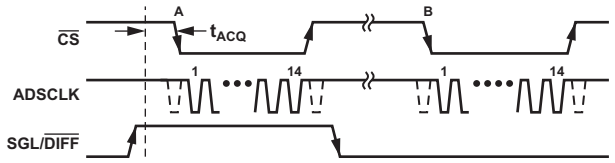


Figure 83. Selecting Differential or Single-Ended Configuration

The channels used for simultaneous conversions are selected via the multiplexer address input pins, A0 to A2. The logic states of these pins also need to be established prior to the acquisition time; however, they may change during the conversion time provided the mode is not changed. If the mode is changed from fully differential to pseudo differential, for example, then the acquisition time would start again from this point. The selected input channels are decoded as shown in Table 51 (Analog Input Type and Channel Selection).

The analog input range of the ADC can be selected as 0 V to V_{REF} or 0 V to 2 × V_{REF} via the RANGE pin. This selection is made in a similar fashion to that of the SGL/$\overline{DIFF}$ pin by setting the logic state of the RANGE pin a time t_{acq} prior to the falling edge of $\overline{CS}$. Subsequent to this, the logic level on this pin can be altered after the third falling edge of ADSCLK. If this pin is tied to a logic low, the analog input range selected is 0 V to V_{REF}. If this pin is tied to a logic high, the analog input range selected is 0 V to 2 × V_{REF}.

Output Coding

The ADC output coding is set to either twos complement or straight binary, depending on which analog input configuration is selected for a conversion. Table 50 (ADC Output Coding) shows which output coding scheme is used for each possible analog input configuration.

Table 50. ADC Output Coding

SGL/$\overline{DIFF}$		RANGE		Output Coding
0	(Differential Input)	0	(0 V to V_{REF})	Twos complement
0	(Differential Input)	1	(0 V to 2 × V_{REF})	Twos complement
1	(Single-Ended Input)	0	(0 V to V_{REF})	Straight binary
1	(Single-Ended Input)	1	(0 V to2 × V_{REF})	Twos complement
0	(Pseudo-Differential Input)	0	(0 V to V_{REF})	Straight binary
0	(Pseudo-Differential Input)	1	(0 V to 2 × V_{REF})	Twos complement

Table 51. Analog Input Type and Channel Selection

				ADC A		ADC B		
SGL/$\overline{DIFF}$	A2	A1	A0	V_{IN+}	V_{IN-}	V_{IN+}	V_{IN-}	Comment
1	0	0	0	V_{A1}	AGND	V_{B1}	AGND	Single ended
1	0	0	1	V_{A2}	AGND	V_{B2}	AGND	Single ended
1	0	1	0	V_{A3}	AGND	V_{B3}	AGND	Single ended
1	0	1	1	V_{A4}	AGND	V_{B4}	AGND	Single ended
1	1	0	0	V_{A5}	AGND	V_{B5}	AGND	Single ended
1	1	0	1	V_{A6}	AGND	V_{B6}	AGND	Single ended
0	0	0	0	V_{A1}	V_{A2}	V_{B1}	V_{B2}	Fully differential
0	0	0	1	V_{A1}	V_{A2}	V_{B1}	V_{B2}	Pseudo differential
0	0	1	0	V_{A3}	V_{A4}	V_{B3}	V_{B4}	Fully differential
0	0	1	1	V_{A3}	V_{A4}	V_{B3}	V_{B4}	Pseudo differential
0	1	0	0	V_{A5}	V_{A6}	V_{B5}	V_{B6}	Fully differential
0	1	0	1	V_{A5}	V_{A6}	V_{B5}	V_{B6}	Pseudo differential

Transfer Functions

The designed code transitions occur at successive integer LSB values (1 LSB, 2 LSB, and so on). In single-ended mode, the LSB size is V_{REF}/4096 when the 0 V to V_{REF} range is used, and the LSB size is 2 × V_{REF}/4096 when the 0 V to 2 × V_{REF} range is used. In differential mode, the LSB size is 2 × V_{REF}/4096 when the 0 V to V_{REF} range is used, and the LSB size is 4 × V_{REF}/4096 when the 0 V to 2 × V_{REF} range is used. The ideal transfer characteristic for the ADC when straight binary coding is output is shown in Figure 84 (Straight Binary Transfer Characteristic), and the ideal transfer characteristic for the ADC when twos complement coding is output is shown in Figure 85 (Twos Complement Transfer Characteristic with VREF ± VREF Input Range) (this is shown with the 2 × V_{REF} range).

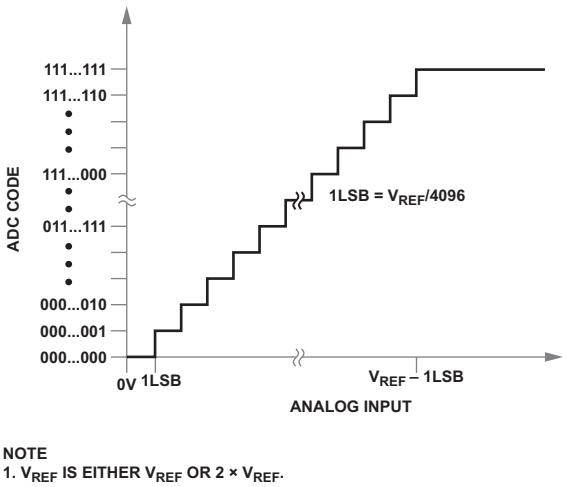


Figure 84. Straight Binary Transfer Characteristic

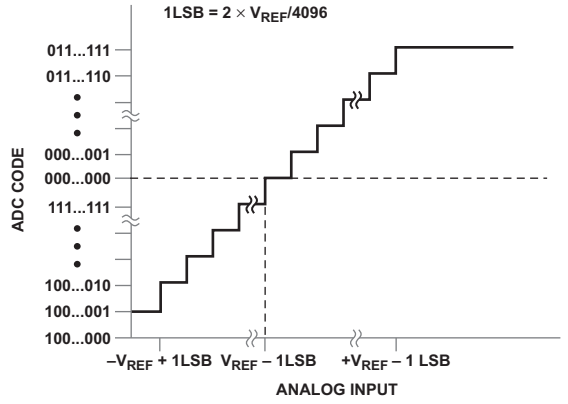


Figure 85. Twos Complement Transfer Characteristic with $V_{REF} \pm V_{REF}$ Input Range

Serial Interface Voltage Drive

The ADC also has a V_{DRIVE} feature to control the voltage at which the serial interface operates. V_{DRIVE} allows the ADC to easily interface to both 3 V and 5 V processors. For example, if the ADC was operated with a AV_{DD}/DV_{DD} of 5 V, the V_{DRIVE} pin could be powered from a 3 V supply, best ADC performance low voltage digital processors. Therefore, the ADC could be used with the 2 × V_{REF} input range, with a AV_{DD}/DV_{DD} of 5 V while still being able to serial interface to 3 V digital I/O parts.

ADC — MODES OF OPERATION

The mode of operation of the ADC is selected by controlling the (logic) state of the $\overline{CS}$ signal during a conversion. There are three possible modes of operation: normal mode, partial power-down mode, and full power-down mode. After a conversion is initiated, the point at which $\overline{CS}$ is pulled high determines which power-down mode, if any, the device enters. Similarly, if already in a power-down mode, $\overline{CS}$ can control whether the device returns to normal operation or remains in power-down. These modes of operation are designed to provide flexible power management options. These options can be chosen to optimize the power dissipation/throughput rate ratio for differing application requirements.

Normal Mode

This mode is intended for applications needing fastest throughput rates because the user does not have to worry about any power-up times with the ADC remaining fully powered at all times. Figure 86 (Normal Mode Operation) shows the general diagram of the operation of the ADC in this mode.

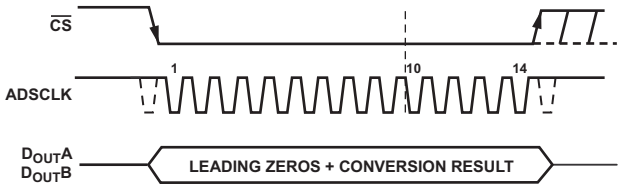


Figure 86. Normal Mode Operation

The conversion is initiated on the falling edge of $\overline{CS}$, as described in the ADC — Serial Interface section. To ensure that the part remains fully powered up at all times, $\overline{CS}$ must remain low until at least 10 ADSCLK falling edges have elapsed after the falling edge of $\overline{CS}$. If $\overline{CS}$ is brought high any time after the 10th ADSCLK falling edge but before the 14th ADSCLK falling edge, the part remains powered up, but the conversion is terminated and $D_{OUT}A$ and $D_{OUT}B$ go back into three-state. Fourteen serial clock cycles are required to complete the conversion and access the conversion result. The D_{OUT} line does not return to three-state after 14 ADSCLK cycles have elapsed, but instead does so when $\overline{CS}$ is brought high again. If $\overline{CS}$ is left low for another 2 ADSCLK cycles (for example, if only a 16 ADSCLK burst is available), two trailing zeros are clocked out after the data. If $\overline{CS}$ is left low for a further 14 (or16) ADSCLK cycles, the result from the other ADC on board is also accessed on the same D_{OUT} line, as shown in Figure 94 (Reading Data from Both ADCs on One DOUT Line with 32 ADSCLKs). See the ADC — Serial Interface section.

Once 32 ADSCLK cycles have elapsed, the D_{OUT} line returns to three-state on the 32nd ADSCLK falling edge. If $\overline{CS}$ is brought high prior to this, the D_{OUT} line returns to three-state at that point. Therefore, $\overline{CS}$ may idle low after 32 ADSCLK cycles until it is brought high again sometime prior to the next conversion (effectively idling $\overline{CS}$ low), if so desired, because the bus still returns to three-state upon completion of the dual result read.

Once a data transfer is complete and $D_{OUT}A$ and $D_{OUT}B$ have returned to three-state, another conversion can be initiated after the quiet time, t_{QUIET}, has elapsed by bringing $\overline{CS}$ low again (assuming the required acquisition time is allowed).

Partial Power-Down Mode

This mode is intended for use in applications where slower throughput rates are required. Either the ADC is powered down between each conversion, or a series of conversions may be performed at a high throughput rate, and the ADC is then powered

down for a relatively long duration between these bursts of several conversions. When the ADC is in partial power-down, all analog circuitry is powered down except for the on-chip reference and reference buffer.

To enter partial power-down mode, the conversion process must be interrupted by bringing $\overline{CS}$ high anywhere after the second falling edge of ADSCLK and before the 10th falling edge of ADSCLK, as shown in Figure 87 (Entering Partial Power-Down Mode). Once $\overline{CS}$ is brought high in this window of ADSCLKs, the part enters partial power-down, the conversion that was initiated by the falling edge of $\overline{CS}$ is terminated, and $D_{OUT}A$ and $D_{OUT}B$ go back into three-state. If $\overline{CS}$ is brought high before the second ADSCLK falling edge, the part remains in normal mode and does not power down. This avoids accidental power-down due to glitches on the $\overline{CS}$ line.

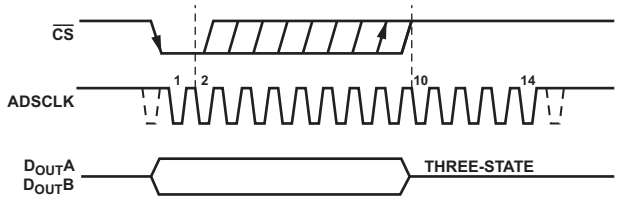


Figure 87. Entering Partial Power-Down Mode

To exit this mode of operation and power up the ADC again, a dummy conversion is performed. On the falling edge of $\overline{CS}$, the device begins to power up and continues to power up as long as $\overline{CS}$ is held low until after the falling edge of the 10th ADSCLK. The device is fully powered up after approximately 1 µs has elapsed, and valid data results from the next conversion, as shown in Figure 88 (Exiting Partial Power-Down Mode). If $\overline{CS}$ is brought high before the second falling edge of ADSCLK, the ADC again goes into partial power-down. This avoids accidental power-up due to glitches on the $\overline{CS}$ line. Although the device may begin to power up on the falling edge of $\overline{CS}$, it powers down again on the rising edge of $\overline{CS}$. If the ADC is already in partial power-down mode and $\overline{CS}$ is brought high between the second and 10th falling edges of ADSCLK, the device enters full power-down mode.

Full Power-Down Mode

This mode is intended for use in applications where throughput rates slower than those in the partial power-down mode are required, as power-up from a full power-down takes substantially longer than that from partial power-down. This mode is more suited to applications where a series of conversions performed at a relatively high throughput rate are followed by a long period of inactivity and thus power-down. When the ADC is in full power-down, all analog circuitry is powered down. Full power-down is entered in a similar way as partial power-down, except the timing sequence shown in Figure 87 (Entering Partial Power-Down Mode) must be executed twice. The conversion process must be interrupted in a similar fashion by bringing $\overline{CS}$ high anywhere after the second falling edge of ADSCLK and before the 10th falling edge of ADSCLK. The device enters partial power-down at this point. To reach full power-down, the next conversion cycle must be interrupted in the same way, as shown in Figure 89 (Entering Full Power-Down Mode). Once $\overline{CS}$ is brought high in this window of ADSCLKs, the part completely powers down.

Note that it is not necessary to complete the 14 ADSCLKs once $\overline{CS}$ is brought high to enter a power-down mode.

To exit full power-down and power up the ADC, a dummy conversion is performed, as when powering up from partial power-down. On the falling edge of $\overline{CS}$, the device begins to power up and continues to power up, as long as $\overline{CS}$ is held low until after the falling edge of the 10th ADSCLK. The required power-up time must elapse before a conversion can be initiated, as shown in Figure 90 (Exiting Full Power-Down Mode). See the Power-Up Times section for the power-up times associated with the ADC.

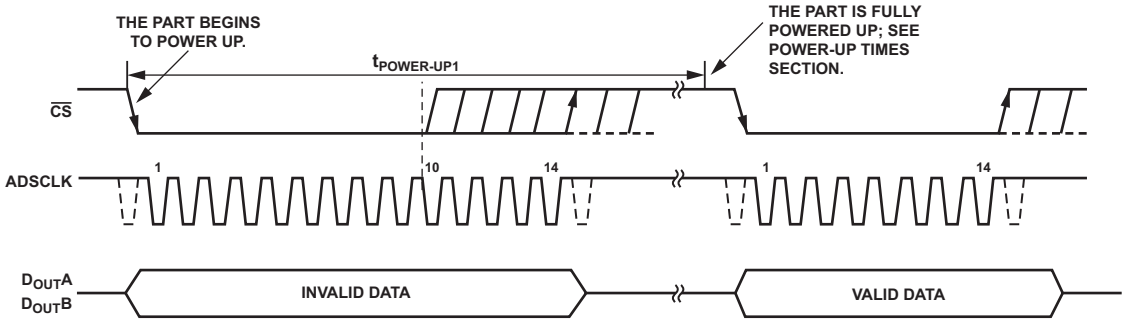


Figure 88. Exiting Partial Power-Down Mode

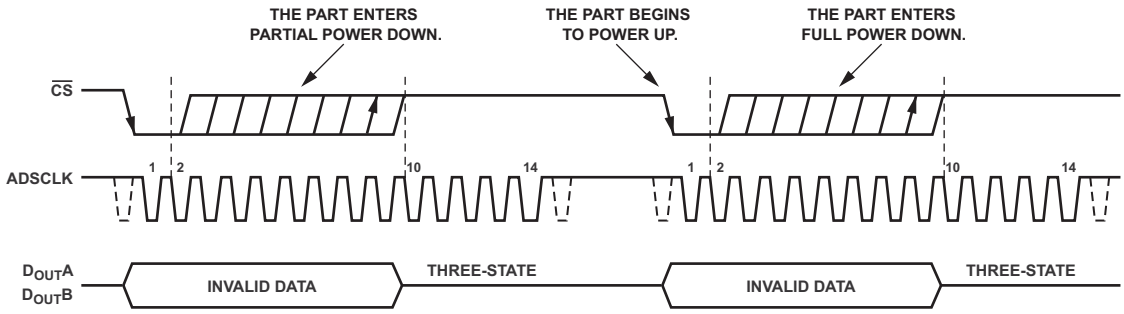


Figure 89. Entering Full Power-Down Mode

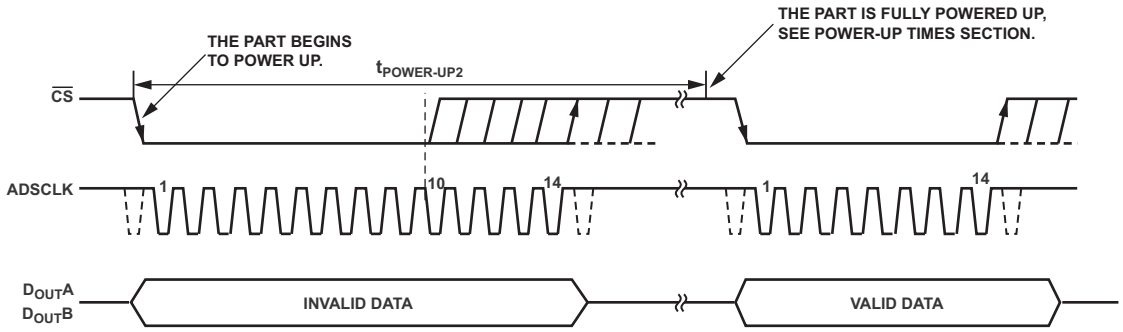


Figure 90. Exiting Full Power-Down Mode

Power-Up Times

As described in detail, the ADC has two power-down modes, partial power-down and full power-down. This section deals with the power-up time required when coming out of either of these modes. It should be noted that the power-up times, as explained in this section, apply with the recommended capacitors in place on the $D_{CAP}A$ and $D_{CAP}B$ pins.

To power up from full power-down, approximately 1.5 ms should be allowed from the falling edge of $\overline{CS}$, shown as $t_{POWER-UP2}$ in Figure 90 (Exiting Full Power-Down Mode). Powering up from partial power-down requires much less time. The power-up time from partial power-down is typically 1 µs; however, if using the internal reference, then the ADC must be in partial power-down for at least 67 µs in order for this power-up time to apply.

When power supplies are first applied to the ADC, the ADC may power up in either of the power-down modes or normal mode. Because of this, it is best to allow a dummy cycle to elapse to ensure the part is fully powered up before attempting a valid conversion. Likewise, if it is intended to keep the part in the partial power-down mode immediately after the supplies are applied, then two dummy cycles must be initiated. The first dummy cycle must hold $\overline{CS}$ low until after the 10th ADSCLK falling edge (see Figure 86 (Normal Mode Operation)); in the second cycle, $\overline{CS}$ must be brought high before the 10th ADSCLK edge but after the second ADSCLK falling edge (see Figure 87 (Entering Partial Power-Down Mode)). Alternatively, if it is intended to place the part in full power-down mode when the supplies are applied, then three dummy cycles must be initiated. The first dummy cycle must hold $\overline{CS}$ low until after the 10th ADSCLK falling edge (see Figure 86 (Normal Mode Operation)); the second and third dummy cycles place the part in full power-down (see Figure 89 (Entering Full Power-Down Mode)).

Once supplies are applied to the ADC, enough time must be allowed for any external reference to power up and charge the various reference buffer decoupling capacitors to their final values.

Power vs. Throughput Rate

The power consumption of the ADC varies with the throughput rate. When using very slow throughput rates and as fast an ADSCLK frequency as possible, the various power-down options can be used to make significant power savings. However, the ADC quiescent current is low enough that even without using the power-down options, there is a noticeable variation in power consumption with sampling rate. This is true whether a fixed ADSCLK value is used or if it is scaled with the sampling rate. Figure 91 (Power vs. Throughput in Normal Mode with VDD = 3 V) and Figure 92 (Power vs. Throughput in Normal Mode with VDD = 5 V) show plots of power vs. the throughput rate when operating in normal mode for a fixed

maximum ADSCLK frequency and an ADSCLK frequency that scales with the sampling rate with V_{DD} = 3 V and V_{DD} = 5 V, respectively. In all cases, the internal reference was used.

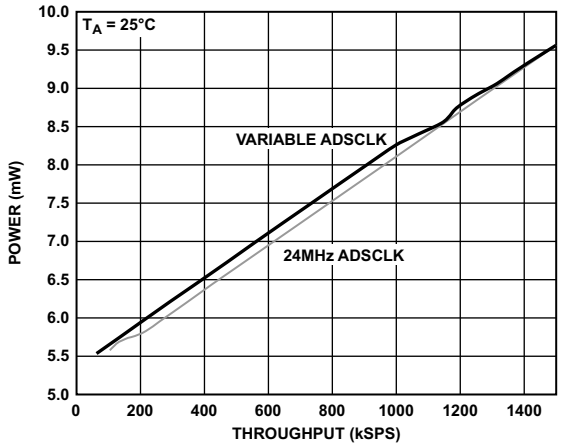


Figure 91. Power vs. Throughput in Normal Mode with V_{DD} = 3 V

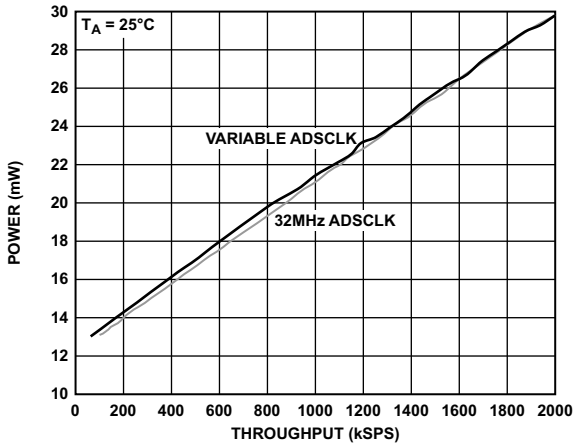


Figure 92. Power vs. Throughput in Normal Mode with V_{DD} = 5 V

ADC — SERIAL INTERFACE

Figure 93 (Serial Interface Timing Diagram) shows the detailed timing diagram for serial interfacing to the ADC. The serial clock provides the conversion clock and controls the transfer of information from the ADC during conversion.

The $\overline{CS}$ signal initiates the data transfer and conversion process. The falling edge of $\overline{CS}$ puts the track-and-hold into hold mode, at which point the analog input is sampled and the bus is taken out of three-state. The conversion is also initiated at this point and requires a minimum of 14 ADSCLKs to complete. Once 13 ADSCLK falling edges have elapsed, the track-and-hold goes back into track on the next ADSCLK rising edge, as shown in Figure 93 (Serial Interface Timing Diagram) at Point B. If a 16 ADSCLK transfer is used, then two trailing zeros appear after the final LSB. On the rising edge of $\overline{CS}$, the conversion is terminated and $D_{OUT}A$ and $D_{OUT}B$ go back into three-state. If $\overline{CS}$ is not brought high but is instead held low for a further 14 (or 16) ADSCLK cycles on $D_{OUT}A$, the data from Conversion B is output on $D_{OUT}A$ (followed by two trailing zeros).

Likewise, if $\overline{CS}$ is held low for a further 14 (or 16) ADSCLK cycles on $D_{OUT}B$, the data from Conversion A is output on $D_{OUT}B$.

This is illustrated in Figure 94 (Reading Data from Both ADCs on One DOUT Line with 32 ADSCLKs) where the case for $D_{OUT}A$ is shown. In this case, the D_{OUT} line in use goes back into three-state on the 32nd ADSCLK falling edge or the rising edge of $\overline{CS}$, whichever occurs first.

A minimum of 14 serial clock cycles are required to perform the conversion process and to access data from one conversion on either data line of the ADC. $\overline{CS}$ going low provides the leading zero to be read in by the microcontroller or DSP. The remaining data is then clocked out by subsequent ADSCLK falling edges, beginning with a second leading zero. Thus, the first falling clock edge on the serial clock has the leading zero provided and also clocks out the second leading zero. The 12-bit result then follows with the final bit in the data transfer valid on the 14th falling edge, having being clocked out on the previous (13th) falling edge. In applications with a slower ADSCLK, it may be possible to read in data on each ADSCLK rising edge depending on the ADSCLK frequency. The first rising edge of ADSCLK after the $\overline{CS}$ falling edge would have the second leading zero provided, and the 13th rising ADSCLK edge would have DB0 provided.

Note that with fast ADSCLK values, and thus short ADSCLK periods, in order to allow adequately for t_2, an ADSCLK rising edge may occur before the first ADSCLK falling edge. This rising edge of ADSCLK may be ignored for the purposes of the timing descriptions in this section. If a falling edge of ADSCLK is coincident with the falling edge of $\overline{CS}$, then this falling edge of ADSCLK is not acknowledged by the ADC, and the next falling edge of ADSCLK will be the first registered after the falling edge of $\overline{CS}$.

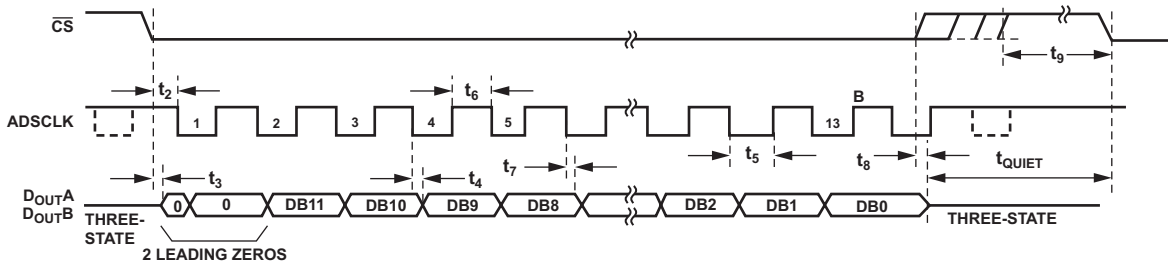


Figure 93. Serial Interface Timing Diagram

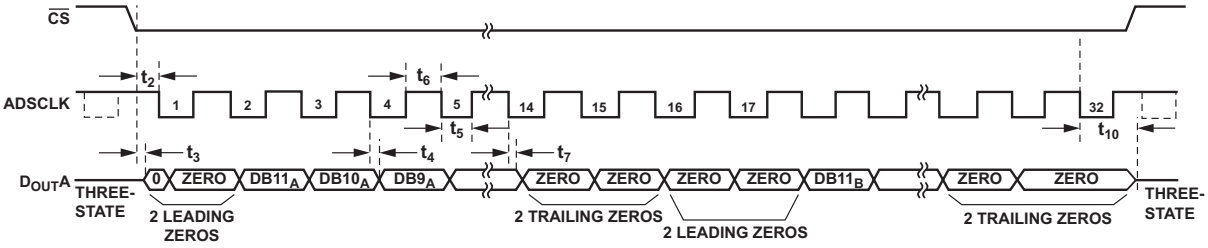


Figure 94. Reading Data from Both ADCs on One D_{OUT} Line with 32 ADSCLKs

120-LEAD LQFP LEAD ASSIGNMENT

Table 52 lists the LQFP leads by signal mnemonic. Table 53 on Page 73 lists the LQFP leads by lead number.

Table 52. 120-Lead LQFP Lead Assignment (Alphabetically by Signal)

Signal	No.	Signal	No.	Signal	No.	Signal	No.
A0	100	NC	72	PG11	46	V_{B5}	88
A1	98	$\overline{NMI}$	11	PG12	47	V_{B6}	87
A2	97	PF0	118	PG13	48	V_{DDEXT}	1
AGND	73	PF1	119	PG14	49	V_{DDEXT}	6
AGND	78	PF2	2	PG15	50	V_{DDEXT}	15
AGND	79	PF3	4	PH0	113	V_{DDEXT}	20
AGND	82	PF4	3	PH1	115	V_{DDEXT}	23
AGND	93	PF5	5	PH2	114	V_{DDEXT}	26
AGND	99	PF6	7	RANGE	95	V_{DDEXT}	30
AV_{DD}	76	PF7	8	REF_SELECT	75	V_{DDEXT}	41
BMODE0	58	PF8	9	$\overline{RESET}$	12	V_{DDEXT}	51
BMODE1	57	PF9	10	SCL	55	V_{DDEXT}	59
BMODE2	56	PF10	14	ADSCLK	102	V_{DDEXT}	62
CLKIN	110	PF11	16	SDA	54	V_{DDEXT}	64
$\overline{CS}$	101	PF12	18	SGL/$\overline{DIFF}$	96	V_{DDEXT}	66
$D_{CAP}A$	77	PF13	19	TCK	34	V_{DDEXT}	67
$D_{CAP}B$	94	PF14	21	TDI	33	V_{DDEXT}	112
DGND	74	PF15	22	TDO	36	V_{DDEXT}	116
DGND	104	$\overline{PG}$	71	TMS	35	$V_{DDFLASH}$	25
$D_{OUT}A$	105	PG0	27	$\overline{TRST}$	37	$V_{DDFLASH}$	63
$D_{OUT}B$	103	PG1	28	V_{A1}	80	$V_{DDFLASH}$	69
DV_{DD}	107	PG2	29	V_{A2}	81	V_{DDINT}	24
$\overline{EMU}$	68	PG3	31	V_{A3}	83	V_{DDINT}	42
EXT_WAKE	70	PG4	32	V_{A4}	84	V_{DDINT}	52
EXTCLK	120	PG5	38	V_{A5}	85	V_{DDINT}	53
GND	13	PG6	39	V_{A6}	86	V_{DDINT}	61
GND	17	PG7	40	V_{B1}	92	V_{DDINT}	65
GND	108	PG8	43	V_{B2}	91	V_{DDINT}	117
GND	109	PG9	44	V_{B3}	90	V_{DRIVE}	106
NC	60	PG10	45	V_{B4}	89	XTAL	111
						GND	121*
						AGND	122**

* Pin no. 121 is the GND supply (see Figure 95 and Figure 96) for the processor (4.6mm × 6.17mm); this pad **must** connect to GND.
** Pin no. 122 is the AGND supply (see Figure 95 and Figure 96) for the ADC (2.81mm × 2.81mm); this pad **must** connect to AGND.

Table 53. 120-Lead LQFP Lead Assignment (Numerically by Lead Number)

No.	Signal	No.	Signal	No.	Signal	No.	Signal
1	V_{DDEXT}	31	PG3	61	V_{DDINT}	91	V_{B2}
2	PF2	32	PG4	62	V_{DDEXT}	92	V_{B1}
3	PF4	33	TDI	63	$V_{DDFLASH}$	93	AGND
4	PF3	34	TCK	64	V_{DDEXT}	94	$D_{CAP}B$
5	PF5	35	TMS	65	V_{DDINT}	95	RANGE
6	V_{DDEXT}	36	TDO	66	V_{DDEXT}	96	SGL/$\overline{DIFF}$
7	PF6	37	$\overline{TRST}$	67	V_{DDEXT}	97	A2
8	PF7	38	PG5	68	$\overline{EMU}$	98	A1
9	PF8	39	PG6	69	$V_{DDFLASH}$	99	AGND
10	PF9	40	PG7	70	EXT_WAKE	100	A0
11	$\overline{NMI}$	41	V_{DDEXT}	71	$\overline{PG}$	101	$\overline{CS}$
12	$\overline{RESET}$	42	V_{DDINT}	72	NC	102	ADSCLK
13	GND	43	PG8	73	AGND	103	$D_{OUT}B$
14	PF10	44	PG9	74	DGND	104	DGND
15	V_{DDEXT}	45	PG10	75	REF_SELECT	105	$D_{OUT}A$
16	PF11	46	PG11	76	AV_{DD}	106	V_{DRIVE}
17	GND	47	PG12	77	$D_{CAP}A$	107	DV_{DD}
18	PF12	48	PG13	78	AGND	108	GND
19	PF13	49	PG14	79	AGND	109	GND
20	V_{DDEXT}	50	PG15	80	V_{A1}	110	CLKIN
21	PF14	51	V_{DDEXT}	81	V_{A2}	111	XTAL
22	PF15	52	V_{DDINT}	82	AGND	112	V_{DDEXT}
23	V_{DDEXT}	53	V_{DDINT}	83	V_{A3}	113	PH0
24	V_{DDINT}	54	SDA	84	V_{A4}	114	PH2
25	$V_{DDFLASH}$	55	SCL	85	V_{A5}	115	PH1
26	V_{DDEXT}	56	BMODE2	86	V_{A6}	116	V_{DDEXT}
27	PG0	57	BMODE1	87	V_{B6}	117	V_{DDINT}
28	PG1	58	BMODE0	88	V_{B5}	118	PF0
29	PG2	59	V_{DDEXT}	89	V_{B4}	119	PF1
30	V_{DDEXT}	60	NC	90	V_{B3}	120	EXTCLK
						121*	GND
						122**	AGND

* Pin no. 121 is the GND supply (see Figure 95 and Figure 96) for the processor (4.6mm × 6.17mm); this pad **must** connect to GND.
** Pin no. 122 is the AGND supply (see Figure 95 and Figure 96) for the ADC (2.81mm × 2.81mm); this pad **must** connect to AGND.

Figure 95 shows the top view of the 120-lead LQFP package lead configuration. Figure 96 shows the bottom view of the 120-lead LQFP package lead configuration.

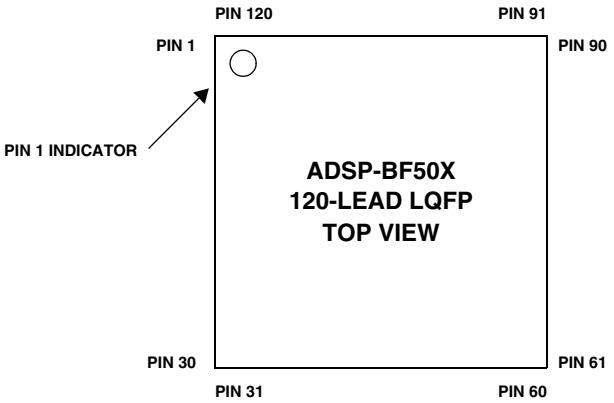


Figure 95. 120-Lead LQFP Package Lead Configuration (Top View)

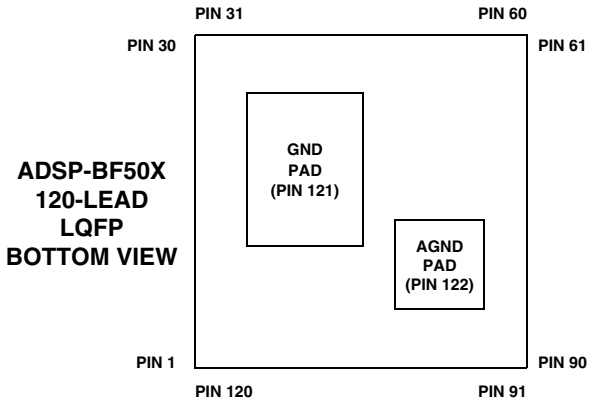


Figure 96. 120-Lead LQFP Package Lead Configuration (Bottom View)

88-LEAD LFCSP LEAD ASSIGNMENT

Table 54 lists the LFCSP leads by signal mnemonic. Table 55 on Page 76 lists the LFCSP by lead number.

Table 54. 88-Lead LFCSP Lead Assignment (Alphabetically by Signal)

Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.
BMODE0	51	PF4	82	PG9	34	V_{DDEXT}	20
BMODE1	50	PF5	83	PG10	35	V_{DDEXT}	31
BMODE2	49	PF6	85	PG11	36	V_{DDEXT}	41
CLKIN	68	PF7	86	PG12	37	V_{DDEXT}	52
$\overline{EMU}$	60	PF8	87	PG13	38	V_{DDEXT}	54
EXT_WAKE	62	PF9	88	PG14	39	V_{DDEXT}	56
EXTCLK	78	PF10	4	PG15	40	V_{DDEXT}	58
GND	3	PF11	6	PH0	71	V_{DDEXT}	59
GND	7	PF12	8	PH1	72	V_{DDEXT}	70
GND	67	PF13	9	PH2	73	V_{DDEXT}	74
NC	45	PF14	11	$\overline{RESET}$	2	V_{DDEXT}	79
NC	46	PF15	12	SCL	44	V_{DDEXT}	84
NC	47	$\overline{PG}$	63	SDA	43	$V_{DDFLASH}$	15
NC	48	PG0	17	TCK	24	$V_{DDFLASH}$	55
NC	64	PG1	18	TDI	23	$V_{DDFLASH}$	61
NC	65	PG2	19	TDO	27	V_{DDINT}	14
NC	66	PG3	21	TMS	25	V_{DDINT}	32
$\overline{NMI}$	1	PG4	22	$\overline{TRST}$	26	V_{DDINT}	42
PF0	76	PG5	28	V_{DDEXT}	5	V_{DDINT}	53
PF1	77	PG6	29	V_{DDEXT}	10	V_{DDINT}	57
PF2	80	PG7	30	V_{DDEXT}	13	V_{DDINT}	75
PF3	81	PG8	33	V_{DDEXT}	16	XTAL	69
						GND	89*

* Pin no. 89 is the GND supply (see Figure 98) for the processor; this pad **must** connect to GND.

Table 55. 88-Lead LFCSP Lead Assignment (Numerically by Lead Number)

Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal
1	$\overline{NMI}$	23	TDI	45	NC	67	GND
2	$\overline{RESET}$	24	TCK	46	NC	68	CLKIN
3	GND	25	TMS	47	NC	69	XTAL
4	PF10	26	$\overline{TRST}$	48	NC	70	V_{DDEXT}
5	V_{DDEXT}	27	TDO	49	BMODE2	71	PH0
6	PF11	28	PG5	50	BMODE1	72	PH1
7	GND	29	PG6	51	BMODE0	73	PH2
8	PF12	30	PG7	52	V_{DDEXT}	74	V_{DDEXT}
9	PF13	31	V_{DDEXT}	53	V_{DDINT}	75	V_{DDINT}
10	V_{DDEXT}	32	V_{DDINT}	54	V_{DDEXT}	76	PF0
11	PF14	33	PG8	55	$V_{DDFLASH}$	77	PF1
12	PF15	34	PG9	56	V_{DDEXT}	78	EXTCLK
13	V_{DDEXT}	35	PG10	57	V_{DDINT}	79	V_{DDEXT}
14	V_{DDINT}	36	PG11	58	V_{DDEXT}	80	PF2
15	$V_{DDFLASH}$	37	PG12	59	V_{DDEXT}	81	PF3
16	V_{DDEXT}	38	PG13	60	$\overline{EMU}$	82	PF4
17	PG0	39	PG14	61	$V_{DDFLASH}$	83	PF5
18	PG1	40	PG15	62	EXT_WAKE	84	V_{DDEXT}
19	PG2	41	V_{DDEXT}	63	$\overline{PG}$	85	PF6
20	V_{DDEXT}	42	V_{DDINT}	64	NC	86	PF7
21	PG3	43	SDA	65	NC	87	PF8
22	PG4	44	SCL	66	NC	88	PF9
						89*	GND

* Pin no. 89 is the GND supply (see Figure 98) for the processor; this pad **must** connect to GND.

Figure 97 shows the top view of the LFCSP pin configuration.
Figure 98 shows the bottom view of the LFCSP lead configuration.

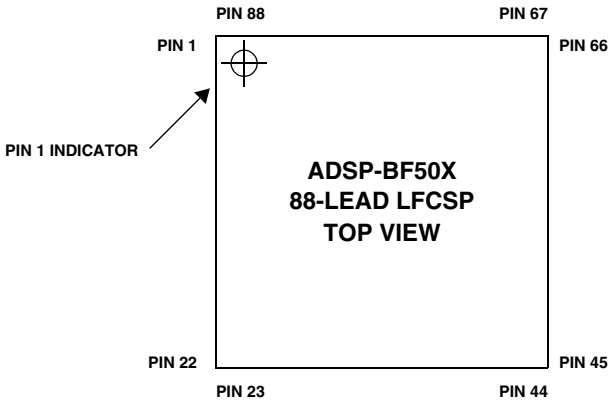


Figure 97. 88-Lead LFCSP Lead Configuration (Top View)

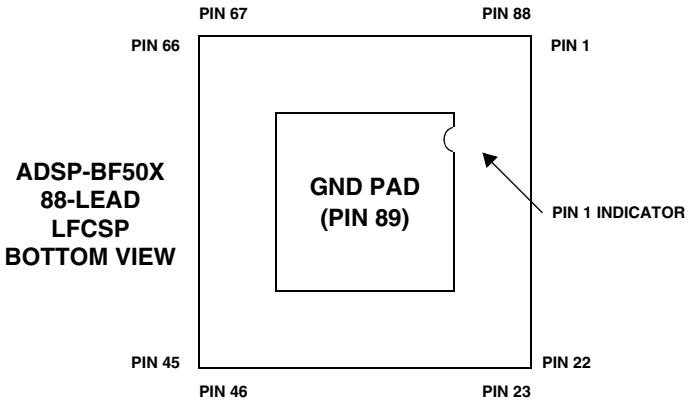


Figure 98. 88-Lead LFCSP Lead Configuration (Bottom View)

OUTLINE DIMENSIONS

Dimensions in Figure 99 (for the 120-lead LQFP) and in Figure 100 (for the 88-lead LFCSP) are shown in millimeters.

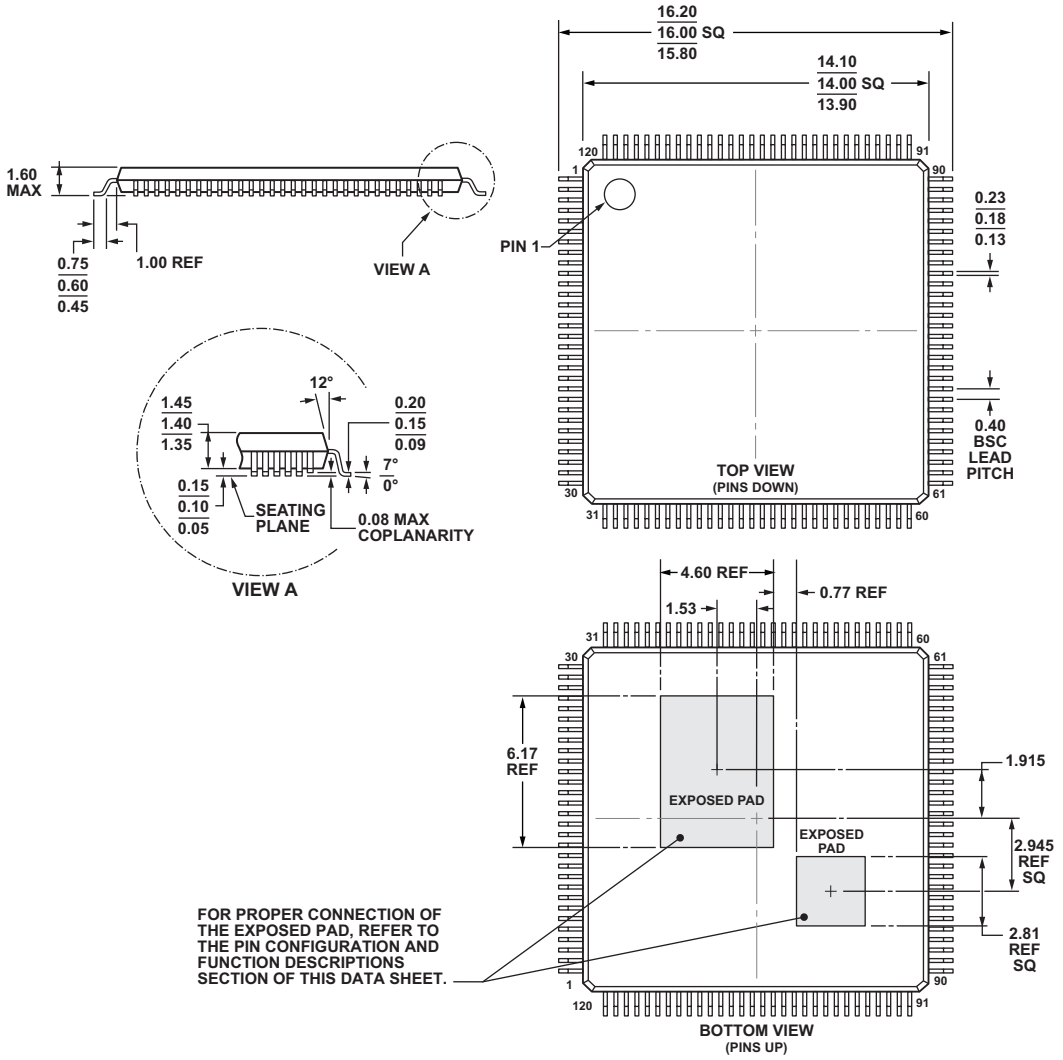


Figure 99. 120-Lead LQFP (SQ-120-2)

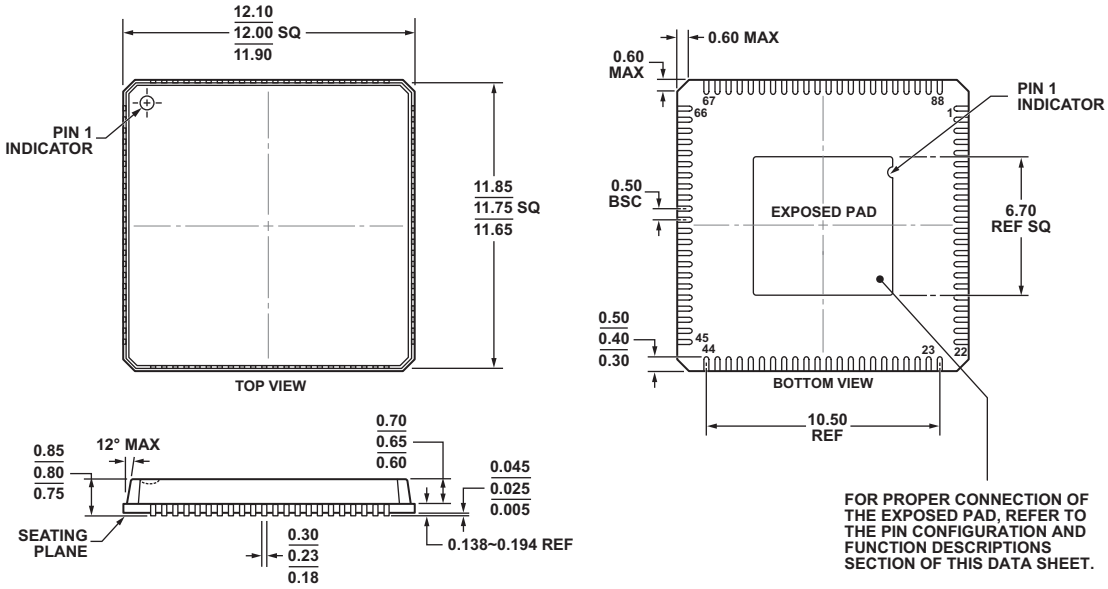


Figure 100. 88-Lead LFCSP (BC-CP-1)

SURFACE MOUNT DESIGN

Table 56 is provided as an aide to PCB design. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface Mount Design and Land Pattern Standard.*

Table 56. Surface Mount Design Supplement

Package	Ball Attach Type	Solder Mask Opening	Lead Pad Size
120-Lead LQFP	Solder Mask Defined	TBD mm diameter	TBD mm diameter
88-Lead LFCSP	Solder Mask Defined	TBD mm diameter	TBD mm diameter

ORDERING GUIDE

Table 57. ADSP-BF50x Processors[1]

Model	Temperature Range[2]	Processor Instruction Rate (Max)	Package Description	Package Option
ADSPBF504BCPZ-ENG	–40°C to +85°C	400 MHz	88-Lead LFCSP	BC-CP-1
ADSPBF504FBCPZ-ENG	–40°C to +85°C	400 MHz	88-Lead LFCSP	BC-CP-1
ADSPBF506FBSWZ-ENG	–40°C to +85°C	400 MHz	120-Lead LQFP	SQ-120-2

[1] For feature comparison between ADSP-BF504, ADSP-BF504F, and ADSP-BF506F processors, see the Processor Comparison in Table 1 on Page 3.
[2] Referenced temperature is ambient temperature.

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