

## Integrated 4A Switch PWM Step-Up Regulator

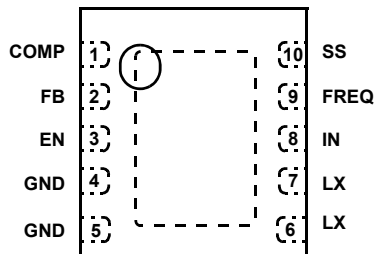
The ISL97656 is a high frequency, high efficiency step-up voltage regulator operated at constant frequency PWM mode. With an internal 4.0A, 120mΩ MOSFET, it can deliver up to 2A output current at over 90% efficiency. The selectable 640kHz and 1.2MHz allows smaller inductors and faster transient response. An external compensation pin gives the user greater flexibility in setting frequency compensation allowing the use of low ESR Ceramic output capacitors.

When shut down, it draws <math><1\mu\text{A}</math> of current and can operate down to 2.3V input supply. These features along with 1.2MHz switching frequency makes it an ideal device for portable equipment and TFT-LCD displays.

The ISL97656 is available in a 10 Ld TDFN package with a maximum height of 1.1mm. The device is specified for operation over the full  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  temperature range.

### Pinout

**ISL97656**  
**(10 LD TDFN)**  
TOP VIEW



### Features

- >90% Efficiency
- 4.0A, 120mΩ Power MOSFET
- 2.3V to 6.0V Input
- Up to 24V Output
- 640kHz/1.2MHz Switching Frequency Selection
- Adjustable Soft-Start
- Internal Thermal Protection
- 0.8mm Max Height 10 Ld TDFN Package
- Pb-Free (RoHS Compliant)
- Halogen Free

### Applications

- TFT-LCD Displays
- DSL Modems
- PCMCIA Cards
- Digital Cameras
- GSM/CDMA Phones
- Portable Equipment
- Handheld Devices

### Ordering Information

PART NUMBER (Note)	PART MARKING	PACKAGE (Pb-Free)	PKG. DWG. #
ISL97656IRTZ	656Z	10 Ld TDFN	L10.3x3B
ISL97656IRTZ-T*	656Z	10 Ld TDFN	L10.3x3B
ISL97656IRTZ-TK*	656Z	10 Ld TDFN	L10.3x3B

\*Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

# ISL97656

## Absolute Maximum Ratings ( $T_A = +25^\circ\text{C}$ )

LX to GND	.....26V
IN to GND	.....6.5V
COMP, FB, EN, SS, FREQ to GND	.....-0.3V to (IN +0.3V)

## Thermal Information

Thermal Resistance (Typical)	$\theta_{JA}$ ( $^\circ\text{C}/\text{W}$ )	$\theta_{JC}$ ( $^\circ\text{C}/\text{W}$ )
10 Ld 3x3 TDFN Package (Notes 1, 2)	53	3
Operating Ambient Temperature	-40 $^\circ\text{C}$ to +85 $^\circ\text{C}$	
Operating Junction Temperature	+135 $^\circ\text{C}$	
Storage Temperature	-65 $^\circ\text{C}$ to +150 $^\circ\text{C}$	
Pb-free reflow profile	see link below	
	<a href="http://www.intersil.com/pbfree/Pb-FreeReflow.asp">http://www.intersil.com/pbfree/Pb-FreeReflow.asp</a>	

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

### NOTES:

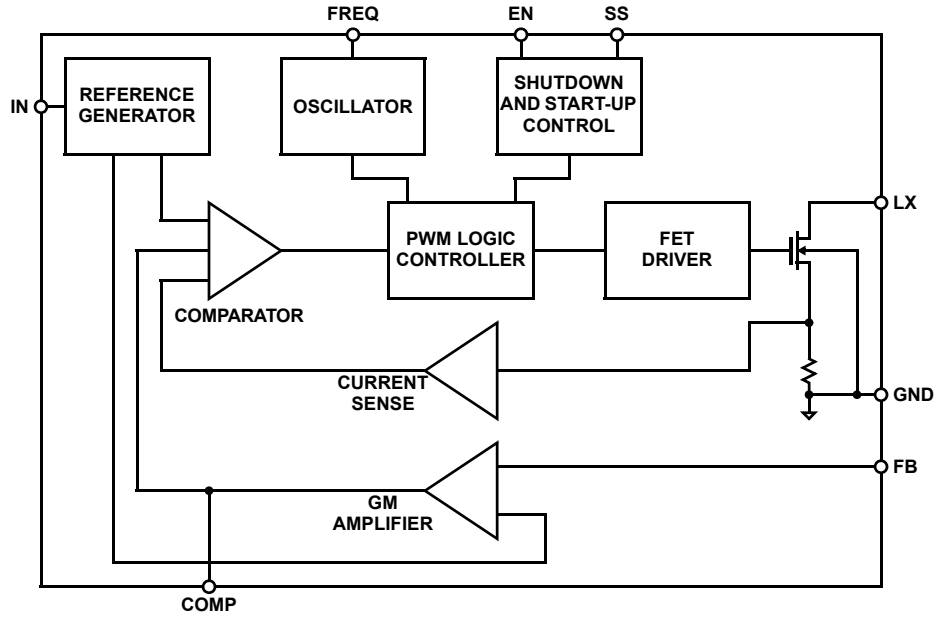
- $\theta_{JA}$  is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
- For  $\theta_{JC}$ , the "case temp" location is the center of the exposed metal pad on the package underside.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore:  $T_J = T_C = T_A$

**Electrical Specifications**  $V_{IN} = 3\text{V}$ ,  $V_{OUT} = 12\text{V}$ ,  $I_{OUT} = 0\text{mA}$ ,  $\text{FREQ} = \text{GND}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ , unless otherwise specified. Parameters with MIN and/or MAX limits are 100% tested at  $+25^\circ\text{C}$ , unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
$I_{Q1}$	Quiescent Current - Shutdown	EN = 0V		0.1	5	$\mu\text{A}$
$I_{Q2}$	Quiescent Current - Not Switching	EN = IN, FB = 1.3V		0.7		mA
$I_{Q3}$	Quiescent Current - Switching	EN = IN, FB = 1.0V		3	5	mA
$V_{FB}$	Feedback Voltage		1.22	1.24	1.26	V
$I_{B-FB}$	Feedback Input Bias Current			0.01	0.5	$\mu\text{A}$
IN	Input Voltage Range		2.3		6.0	V
$D_{MAX} - 640\text{kHz}$	Maximum Duty Cycle	FREQ = 0V	85	92		%
$D_{MAX} - 1.2\text{MHz}$	Maximum Duty Cycle	FREQ = IN	85	90		%
$I_{LIM}$	Current Limit - Max Peak Input Current		3.8	4.0	5.1	A
$I_{EN}$	Shutdown Input Bias Current	EN = 0V		0.01	0.5	$\mu\text{A}$
$r_{DS(ON)}$	Switch ON Resistance	IN = 2.7V, $I_{LX} = 1\text{A}$		0.12		$\Omega$
$I_{LX-LEAK}$	Switch Leakage Current	VSW = 27V		0.01	3	$\mu\text{A}$
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	$2.3\text{V} < V_{IN} < 5.5\text{V}$ , $V_{OUT} = 12\text{V}$		0.2		%
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	$V_{IN} = 3.3\text{V}$ , $V_{OUT} = 12\text{V}$ , $I_O = 30\text{mA}$ to $200\text{mA}$		0.3		%
FOSC1	Switching Frequency Accuracy	FREQ = 0V	500	640	740	kHz
FOSC2	Switching Frequency Accuracy	FREQ = IN	1000	1220	1500	kHz
$V_{IL}$	EN, FREQ Input Low Level				0.5	V
$V_{IH}$	EN, FREQ Input High Level		1.5			V
$G_M$	Error Amp Transconductance	$\Delta I = 5\mu\text{A}$	70	130	250	$1\mu/\Omega$
IN_ON	IN UVLO On Threshold		2.00	2.38	2.57	V
HYS	IN UVLO hysteresis			50		mV
$I_{SS}$	Soft-Start Charge Current		2.5	4.5	7.5	$\mu\text{A}$
OTP	Over-Temperature Protection			150		$^\circ\text{C}$

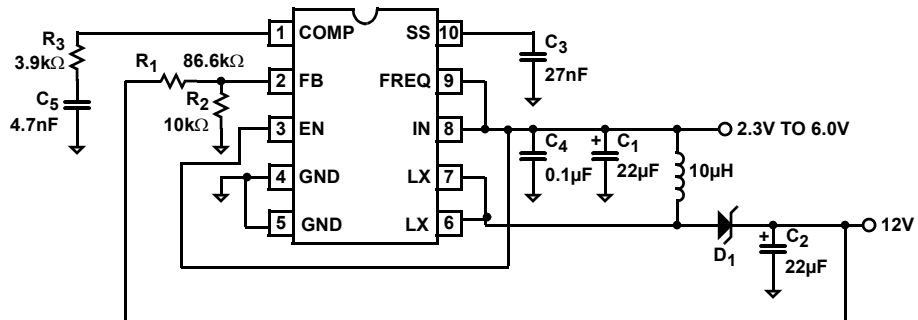
**Block Diagram**



**Pin Descriptions**

PIN NUMBER	PIN NAME	DESCRIPTION
1	COMP	Compensation pin. Output of the internal error amplifier. Capacitor and resistor from COMP pin to ground.
2	FB	Voltage feedback pin. Internal reference is 1.24V nominal. Connect a resistor divider from $V_{OUT}$ . $V_{OUT} = 1.24V (1 + R_1/R_2)$ . See "Typical Application Circuit".
3	EN	Shutdown control pin. Pull EN low to turn off the device.
4, 5	GND	Analog and power ground.
6, 7	LX	Power switch pin. Connected to the drain of the internal power MOSFET.
8	IN	Analog power supply input pin.
9	FREQ	Frequency select pin. When FREQ is set low, switching frequency is set to 620kHz. When connected to high or IN, switching frequency is set to 1.25MHz.
10	SS	Soft-start control pin. Connect a capacitor to control the converter start-up.

**Typical Application Circuit**



Typical Performance Curves

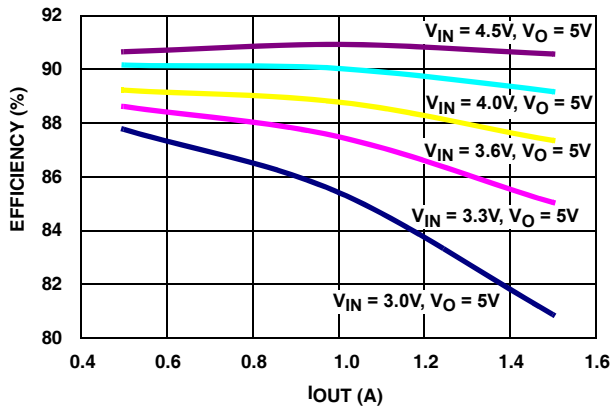


FIGURE 1. 5V BOOST EFFICIENCY vs IOUT

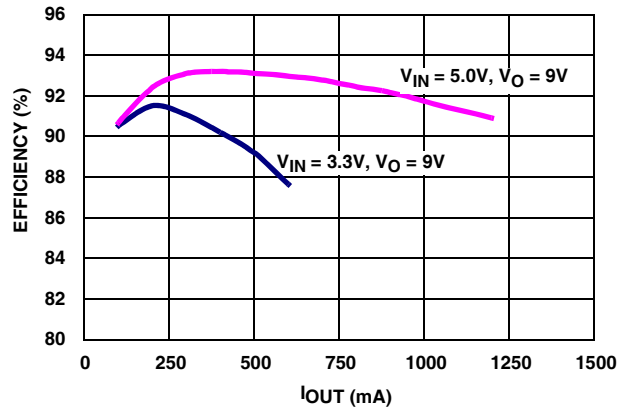


FIGURE 2. 9V BOOST EFFICIENCY vs IOUT

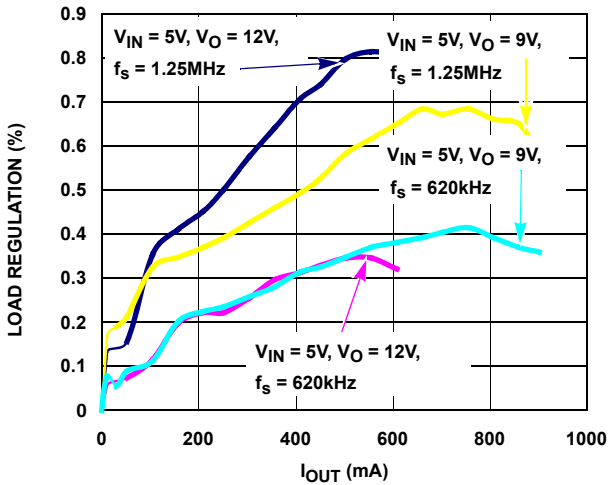


FIGURE 3. LOAD REGULATION vs IOUT

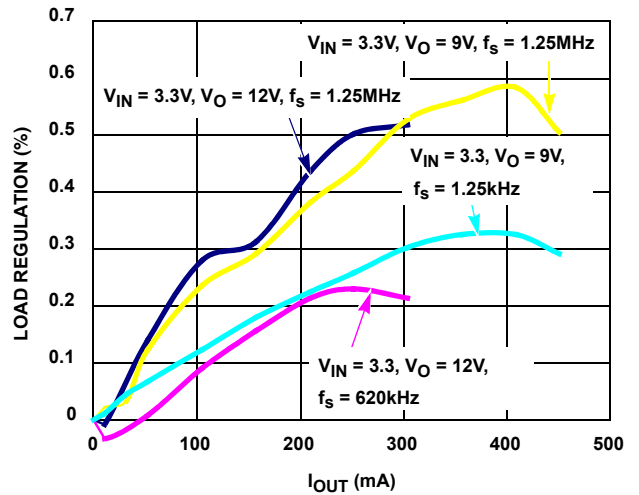


FIGURE 4. LOAD REGULATION vs IOUT

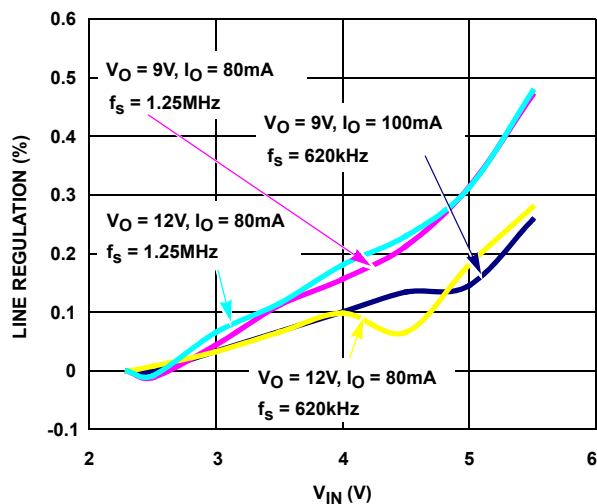


FIGURE 5. LINE REGULATION vs VIN

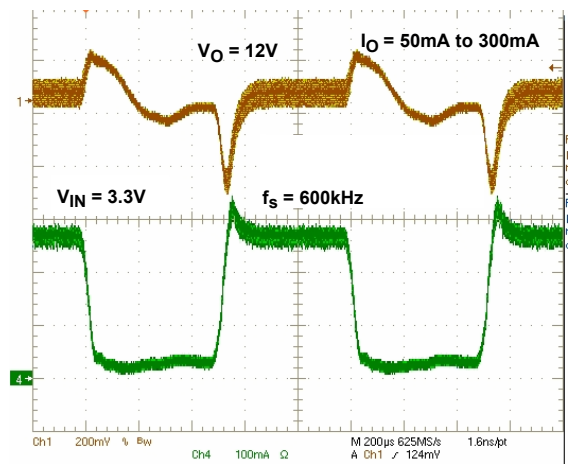


FIGURE 6. TRANSIENT RESPONSE

Typical Performance Curves (Continued)

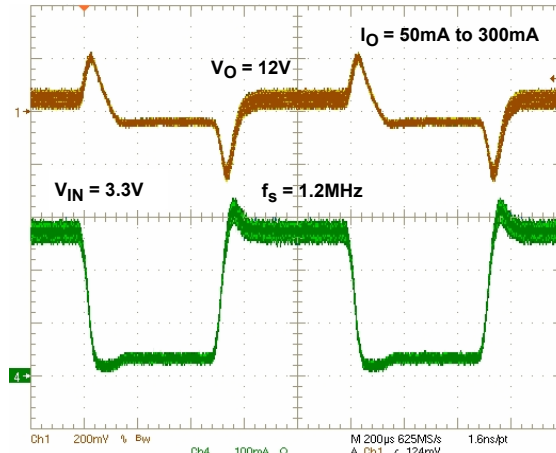


FIGURE 7. TRANSIENT RESPONSE

Applications Information

The ISL97656 is a high frequency, high efficiency boost regulator operated at constant frequency PWM mode. The boost converter stores energy from an input voltage source and deliver it to a higher output voltage. The input voltage range is 2.3V to 6.0V and output voltage range is 5V to 25V. The switching frequency is selectable between 640kHz and 1.2MHz allowing smaller inductors and faster transient response. An external compensation pin gives the user greater flexibility in setting output transient response and tighter load regulation. The converter soft-start characteristic can also be controlled by external C<sub>SS</sub> capacitor. The EN pin allows the user to completely shutdown the device.

Boost Converter Operations

Figure 8 shows a boost converter with all the key components. In steady state operating and continuous conduction mode where the inductor current is continuous, the boost converter operates in two cycles. During the first cycle, as shown in Figure 9, the internal power FET turns on and the Schottky diode is reverse biased and cuts off the current flow to the output. The output current is supplied from the output capacitor. The voltage across the inductor is V<sub>IN</sub> and the inductor current ramps up in a rate of V<sub>IN</sub>/L, L is the inductance. The inductance is magnetized and energy is stored in the inductor. The change in inductor current is shown in Equation 1:

$$\Delta I_{L1} = \Delta T1 \times \frac{V_{IN}}{L}$$

$$\Delta T1 = \frac{D}{f_{SW}}$$

D = Duty Cycle

$$\Delta V_O = \frac{I_{OUT}}{C_{OUT}} \times \Delta T1 \tag{EQ. 1}$$

During the second cycle, the power FET turns off and the Schottky diode is forward biased, (see Figure 10). The energy stored in the inductor is pumped to the output supplying output current and charging the output capacitor.

The Schottky diode side of the inductor is clamp to a Schottky diode above the output voltage. So the voltage drop across the inductor is V<sub>IN</sub> - V<sub>OUT</sub>. The change in inductor current during the second cycle is shown in Equation 2:

$$\Delta I_L = \Delta T2 \times \frac{V_{IN} - V_{OUT}}{L}$$

$$\Delta T2 = \frac{1-D}{f_{SW}} \tag{EQ. 2}$$

For stable operation, the same amount of energy stored in the inductor must be taken out. The change in inductor current during the two cycles must be the same as shown in Equation 3.

$$\Delta I1 + \Delta I2 = 0$$

$$\frac{D}{f_{SW}} \times \frac{V_{IN}}{L} + \frac{1-D}{f_{SW}} \times \frac{V_{IN} - V_{OUT}}{L} = 0$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1-D} \tag{EQ. 3}$$

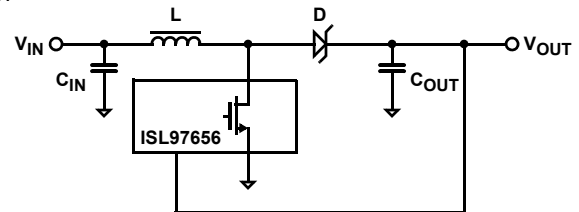


FIGURE 8. BOOST CONVERTER

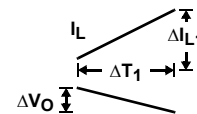
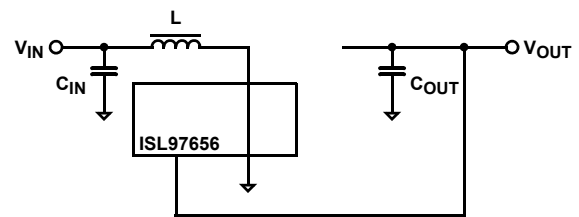


FIGURE 9. BOOST CONVERTER - CYCLE 1, POWER SWITCH CLOSED

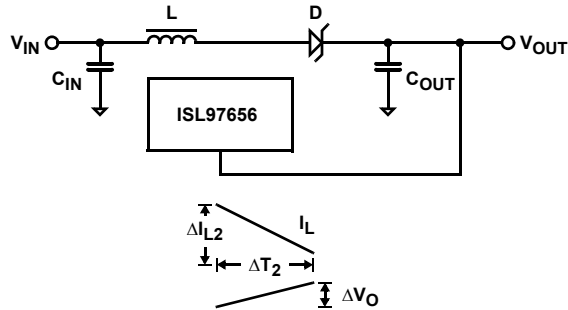


FIGURE 10. BOOST CONVERTER - CYCLE 2, POWER SWITCH OPEN

### Output Voltage

An external feedback resistor divider is required to divide the output voltage down to the nominal 1.24V reference voltage. The current drawn by the resistor network should be limited to maintain the overall converter efficiency. The maximum value of the resistor network is limited by the feedback input bias current and the potential for noise being coupled into the feedback pin. A resistor network less than 100k is recommended. The boost converter output voltage is determined by the relationship as shown in Equation 4. The nominal VFB voltage is 1.24V..

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_1}{R_2}\right) \quad (\text{EQ. 4})$$

### Inductor Selection

The inductor selection determines the output ripple voltage, transient response, output current capability, and efficiency. Its selection depends on the input voltage, output voltage, switching frequency, and maximum output current. For most applications, the inductance should be in the range of 2μH to 33μH. The inductor maximum DC current specification must be greater than the peak inductor current required by the regulator. The peak inductor current can be calculated using Equation 5::

$$I_{L(\text{PEAK})} = \frac{I_{OUT} \times V_{OUT}}{V_{IN}} + 1/2 \times \frac{V_{IN} \times (V_{OUT} - V_{IN})}{L \times V_{OUT} \times \text{FREQ}} \quad (\text{EQ. 5})$$

### Output Capacitor

Low ESR capacitors should be used to minimize the output voltage ripple. Multilayer ceramic capacitors (X5R and X7R) are preferred for the output capacitors because of their lower ESR and small packages. Tantalum capacitors with higher ESR can also be used. The output ripple can be calculated using Equation 6:

$$\Delta V_O = \frac{I_{OUT} \times D}{f_{SW} \times C_O} + I_{OUT} \times \text{ESR} \quad (\text{EQ. 6})$$

For noise sensitive application, a 0.1μF placed in parallel with the larger output capacitor is recommended to reduce the switching noise coupled from the LX switching node.

### Schottky Diode

In selecting the Schottky diode, the reverse break down voltage, forward current and forward voltage drop must be considered for optimum converter performance. The diode must be rated to handle 4.0A, the current limit of the ISL97656. The breakdown voltage must exceed the maximum output voltage. Low forward voltage drop, low leakage current, and fast reverse recovery will help the converter to achieve the maximum efficiency.

### Input Capacitor

The value of the input capacitor depends the input and output voltages, the maximum output current, the inductor value and the noise allowed to put back on the input line. For most applications, a minimum 10μF is required. For applications that run close to the maximum output current limit, input capacitor in the range of 22μF to 47μF is recommended.

The ISL97656 is powered from the VIN. A High frequency 0.1μF bypass capacitor is recommended to be close to the VIN pin to reduce supply line noise and ensure stable operation.

### Loop Compensation

The ISL97656 incorporates a transconductance amplifier in its feedback path to allow the user some adjustment on the transient response and better regulation. The ISL97656 uses current mode control architecture which has a fast current sense loop and a slow voltage feedback loop. The fast current feedback loop does not require any compensation. The slow voltage loop must be compensated for stable operation. The compensation network is a series RC network from COMP pin to ground. The resistor sets the high frequency integrator gain for fast transient response and the capacitor sets the integrator zero to ensure loop stability. For most applications, the compensation resistor in the range of 0k to 2.0k and the compensation capacitor in the range of 3nF to 10nF.

### Soft-Start

The soft-start is provided by an internal 4.5μA current source charges the external CSS, the peak MOSFET current is limited by the voltage on the capacitor. This in turn controls the rising rate of the output voltage. The regulator goes through the start-up sequence as well after the EN pin is pulled to HI.

### Frequency Selection

The ISL97656 switching frequency can be user selected to operate at either constant 640kHz or 1.25MHz. Connecting FREQ pin to ground sets the PWM switching frequency to 640kHz. When connecting FREQ high or IN, the switching frequency is set to 1.2MHz.

### Shutdown Control

When the EN pin is pulled down, the ISL97656 is shutdown reducing the supply current to <1μA.

**Maximum Output Current**

The MOSFET current limit is nominally 4.0A and guaranteed 3.8A. This restricts the maximum output current,  $I_{OMAX}$ , based on Equation 7:

$$I_L = I_{L(AVG)} + (1/2 \times \Delta I_L) \tag{EQ. 7}$$

where:

$I_L$  = MOSFET current limit

$I_{L(AVG)}$  = average inductor current

$\Delta I_L$  = inductor ripple current

$$\Delta I_L = \frac{V_{IN} \times [(V_O + V_{DIODE}) - V_{IN}]}{L \times (V_O + V_{DIODE}) \times f_S} \tag{EQ. 8}$$

$V_{DIODE}$  = Schottky diode forward voltage, typically, 0.6V

$f_S$  = switching frequency, 600kHz or 1.2MHz

$$I_{L-AVG} = \frac{I_{OUT}}{1-D} \tag{EQ. 9}$$

D = MOSFET turn-on ratio:

$$D = 1 - \frac{V_{IN}}{V_{OUT} + V_{DIODE}} \tag{EQ. 10}$$

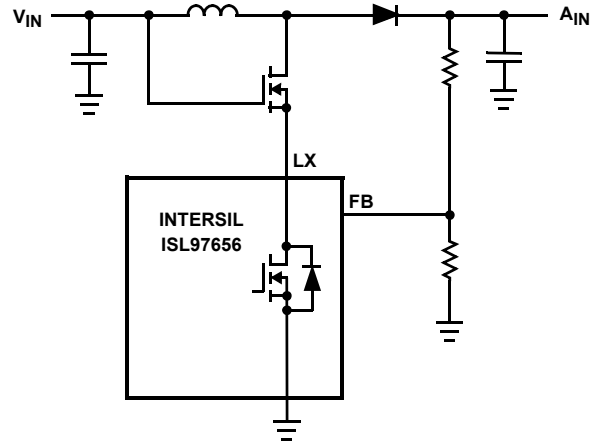
Table 1 gives typical maximum  $I_{OUT}$  values for 1.2MHz switching frequency and 10µH inductor.

**TABLE 1. TYPICAL MAXIMUM  $I_{OUT}$  VALUES**

$V_{IN}$ (V)	$V_{OUT}$ (V)	$I_{OMAX}$ (mA)
2.5	5	1790
2.5	9	990
2.5	12	750
3.3	5	2370
3.3	9	1300
3.3	12	970
5	9	1970
5	12	1470

**Cascaded MOSFET Application**

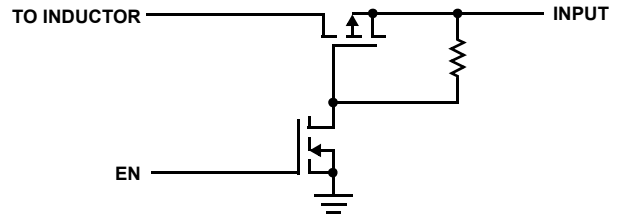
A 24V N-Channel MOSFET is integrated in the boost regulator. For the applications where the output voltage is greater than 24V, an external cascaded MOSFET is needed as shown in Figure 11. The voltage rating of the external MOSFET should be greater than  $A_{IN}$ .



**FIGURE 11. CASCADED MOSFET TOPOLOGY FOR HIGH OUTPUT VOLTAGE APPLICATIONS**

**DC PATH BLOCK APPLICATION**

Note that there is a DC path in the boost converter from the input to the output through the inductor and diode, hence the input voltage will be seen at output with a forward voltage drop of diode before the part is enabled. If this voltage is not desired, the following circuit (see Figure 12) can be inserted between input and inductor to disconnect the DC path when the part is disabled.



**FIGURE 12. CIRCUIT TO DISCONNECT THE DC PATH OF BOOST CONVERTER**

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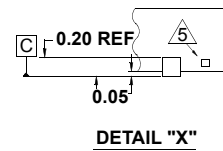
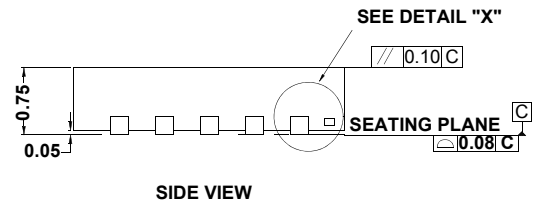
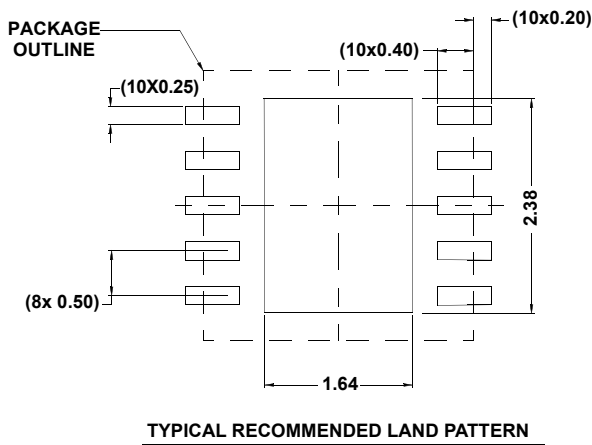
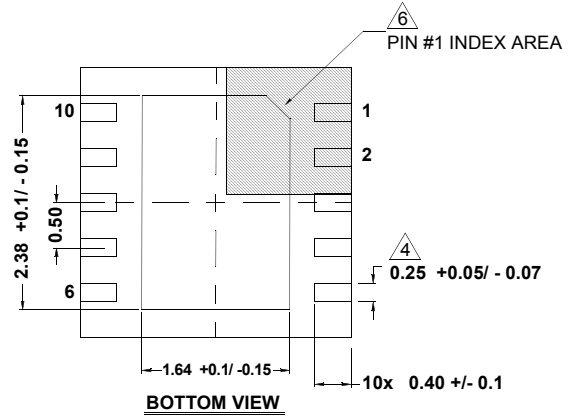
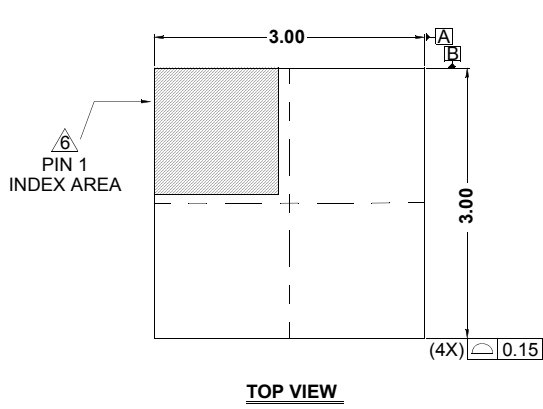
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# Package Outline Drawing

## L10.3x3B

10 LEAD THIN DUAL FLAT PACKAGE (TDFN) WITH E-PAD

Rev 2, 03/10



**NOTES:**

1. Dimensions are in millimeters.  
Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal  $\pm 0.05$
4. Dimension applies to the metallized terminal and is measured between 0.18mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.