

IP4337CX18/LF

7-channel integrated filter network with ESD input protection
to IEC 61000-4-2 level 4

Rev. 02 — 20 August 2009

Product data sheet

1. Product profile

1.1 General description

The IP4337CX18/LF is a 7-channel RC low-pass filter array which is designed to provide filtering of undesired RF signals in the 800 MHz to 3000 MHz frequency band. In addition, the IP4337CX18/LF incorporates diodes to provide protection to downstream components from ElectroStatic Discharge (ESD) voltages as high as ± 15 kV.

The IP4337CX18/LF is fabricated using monolithic silicon technology and integrates 7 resistors and 14 diodes in a single Wafer-Level Chip-Scale Package (WLCSP) measuring 1.96 mm by 1.61 mm (typical). These features make the IP4337CX18/LF ideal for use in applications requiring the utmost in miniaturization.

1.2 Features

- Pb-free, RoHS compliant and free of halogen and antimony (Dark Green compliant)
- Integrated 7-channel π -type RC filter network
- 70 Ω series resistance; 25 pF (typical) capacitance per line
- Integrated ESD protection withstanding ± 15 kV contact discharge, far exceeding IEC 61000-4-2 level 4
- WLCSP with 0.4 mm pitch

1.3 Applications

- Cellular and Personal Communication System (PCS) mobile handsets
- Cordless telephones
- Wireless data (WAN/LAN) systems

2. Pinning information

2.1 Pinning

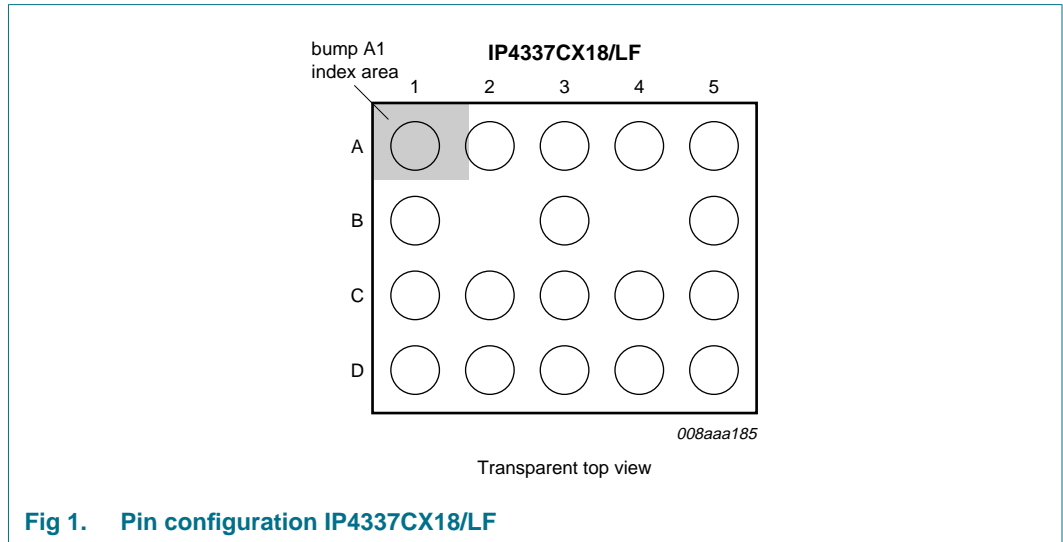


Fig 1. Pin configuration IP4337CX18/LF

2.2 Pin description

Table 1. Pinning

| Pin | Description |
|----------------|------------------|
| A2 and A5 | filter channel 1 |
| A1 and A4 | filter channel 2 |
| B1 and B5 | filter channel 3 |
| C2 and C5 | filter channel 4 |
| C1 and C4 | filter channel 5 |
| D2 and D5 | filter channel 6 |
| D1 and D4 | filter channel 7 |
| A3, B3, C3, D3 | ground |
| B2 and B4 | no balls |

3. Ordering information

Table 2. Ordering information

| Type number | Package | | |
|---------------|----------|--|---------------|
| | Name | Description | Version |
| IP4337CX18/LF | WL CSP18 | wafer level chip-size package; 18 bumps; 1.96 × 1.61 × 0.61 mm | IP4337CX18/LF |

4. Functional diagram

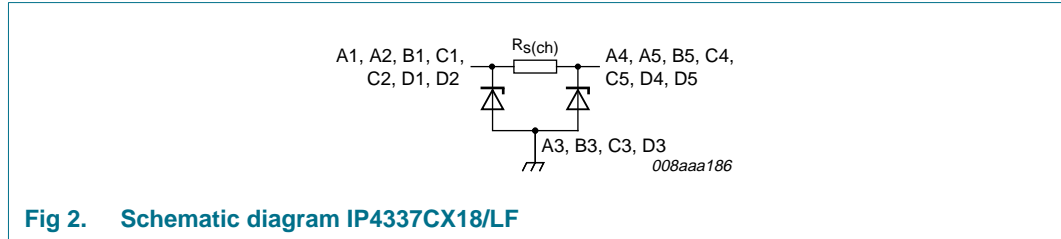


Fig 2. Schematic diagram IP4337CX18/LF

5. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit | |
|--------------------|---------------------------------|---|------|------|------|----|
| V_I | input voltage | | -0.5 | +5.5 | V | |
| V_{ESD} | electrostatic discharge voltage | all pins to ground | | | | |
| | | contact discharge | [1] | -15 | +15 | kV |
| | | air discharge | [1] | -15 | +15 | kV |
| | | IEC 61000-4-2 level 4; all pins to ground | | | | |
| | | contact discharge | | -8 | +8 | kV |
| | | air discharge | | -15 | +15 | kV |
| I_{ch} | channel current (DC) | $T_{amb} = 70\text{ °C}$ | - | 33 | mA | |
| P_{ch} | channel power dissipation | continuous power; $T_{amb} = 70\text{ °C}$ | - | 60 | mW | |
| P_{tot} | total power dissipation | continuous power; $T_{amb} = 70\text{ °C}$ | - | 250 | mW | |
| T_{stg} | storage temperature | | -55 | +150 | °C | |
| $T_{reflow(peak)}$ | peak reflow temperature | 10 s maximum | - | 260 | °C | |
| T_{amb} | ambient temperature | | -30 | +85 | °C | |

[1] Device is qualified with 1000 pulses of ±15 kV contact discharges each, according to the IEC 61000-4-2 model and far exceeds the specified level 4 (8 kV contact discharge).

6. Characteristics

Table 4. Channel characteristics

$T_{amb} = 25\text{ }^{\circ}\text{C}$; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------|---------------------------|--|------|-----|------|----------|
| $R_{s(ch)}$ | channel series resistance | $f = 0\text{ Hz (DC)}$ | 52.5 | 70 | 87.5 | Ω |
| C_{ch} | channel capacitance | $V_{bias(DC)} = 0\text{ V}$; $f = 1\text{ MHz}$ [1] | - | 25 | 30 | pF |
| V_{BR} | breakdown voltage | $I_{test} = 1\text{ mA}$ | 6 | - | 20 | V |
| I_{LR} | reverse leakage current | per channel; $V_I = 3.0\text{ V}$ | - | - | 20 | nA |

[1] Guaranteed by design.

Table 5. Frequency characteristics

$T_{amb} = 25\text{ }^{\circ}\text{C}$; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------|-----------------------|--|-----|-----|-----|------|
| α_{il} | insertion loss | $800\text{ MHz} < f < 3\text{ GHz}$; $R_{gen} = 50\ \Omega$; $R_L = 50\ \Omega$ | - | 20 | - | dB |
| α_{ct} | crosstalk attenuation | $800\text{ MHz} < f < 3\text{ GHz}$; $R_{gen} = 50\ \Omega$; $R_L = 50\ \Omega$ | - | 25 | - | dB |

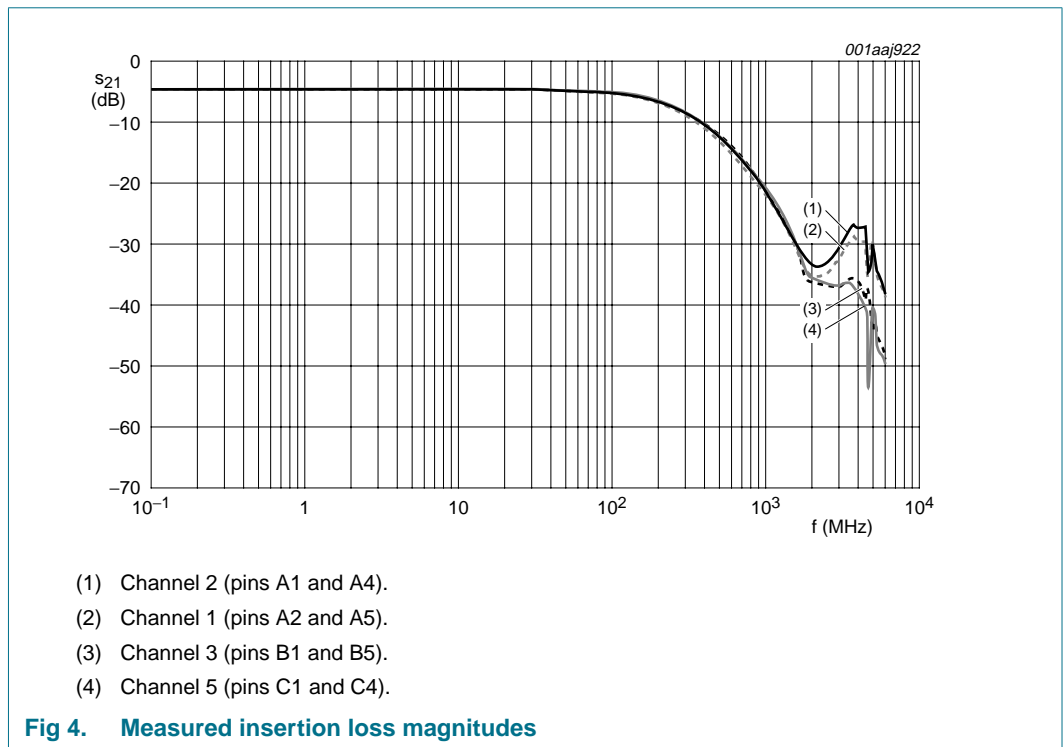
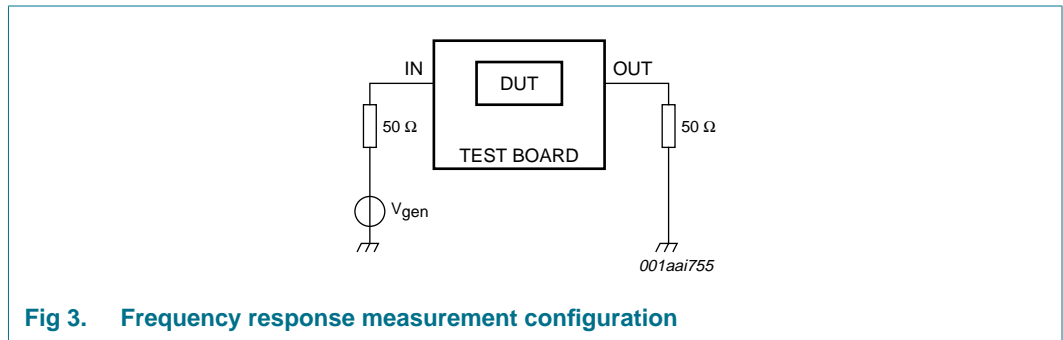
7. Application information

7.1 Insertion loss

The insertion loss measurement configuration of a typical 50 Ω NetWork Analyzer (NWA) system for evaluation of the IP4337CX18/LF is shown in [Figure 3](#).

As an example, the insertion loss of channels between pins A2 and A5, A1 and A4, B1 and B5, C1 and C4 at frequencies up to 6 GHz is displayed in [Figure 4](#).

The insertion loss is measured with a test PCB utilizing laser drilled micro-via holes that connect the PCB ground plane to the IP4337CX18/LF ground pins.



7.2 Crosstalk

The crosstalk measurement configuration of a typical 50 Ω NWA system for evaluation of the IP4337CX18/LF is shown in Figure 5.

The measured crosstalk within the IP4337CX18/LF in a 50 Ω NWA system from one channel to another is shown in Figure 6 for four different pairs of channels. In all cases, unused connections are terminated with 50 Ω to ground.

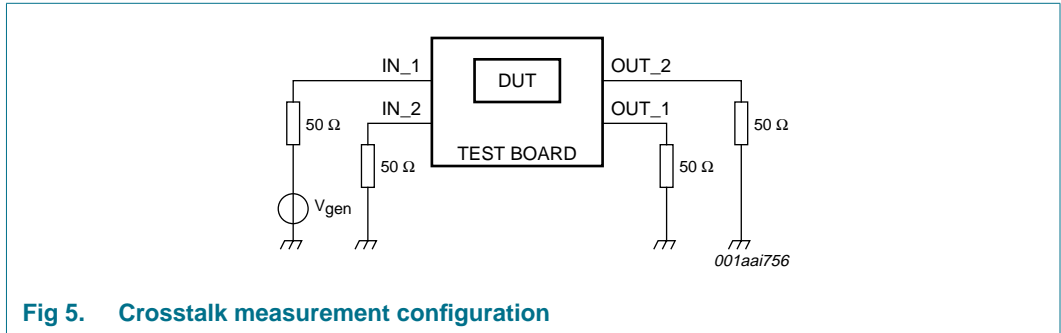


Fig 5. Crosstalk measurement configuration

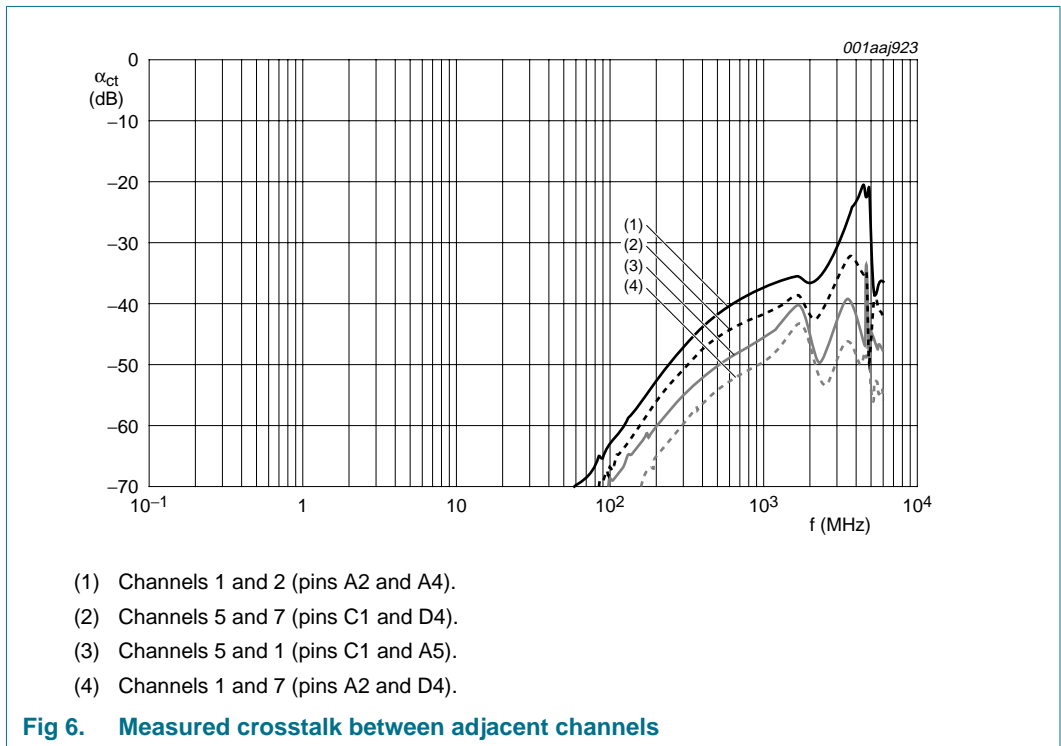


Fig 6. Measured crosstalk between adjacent channels

8. Package outline

WLCSP18: wafer level chip-size package; 18 bumps; 1.96 x 1.61 x 0.61 mm

IP4337CX18/LF

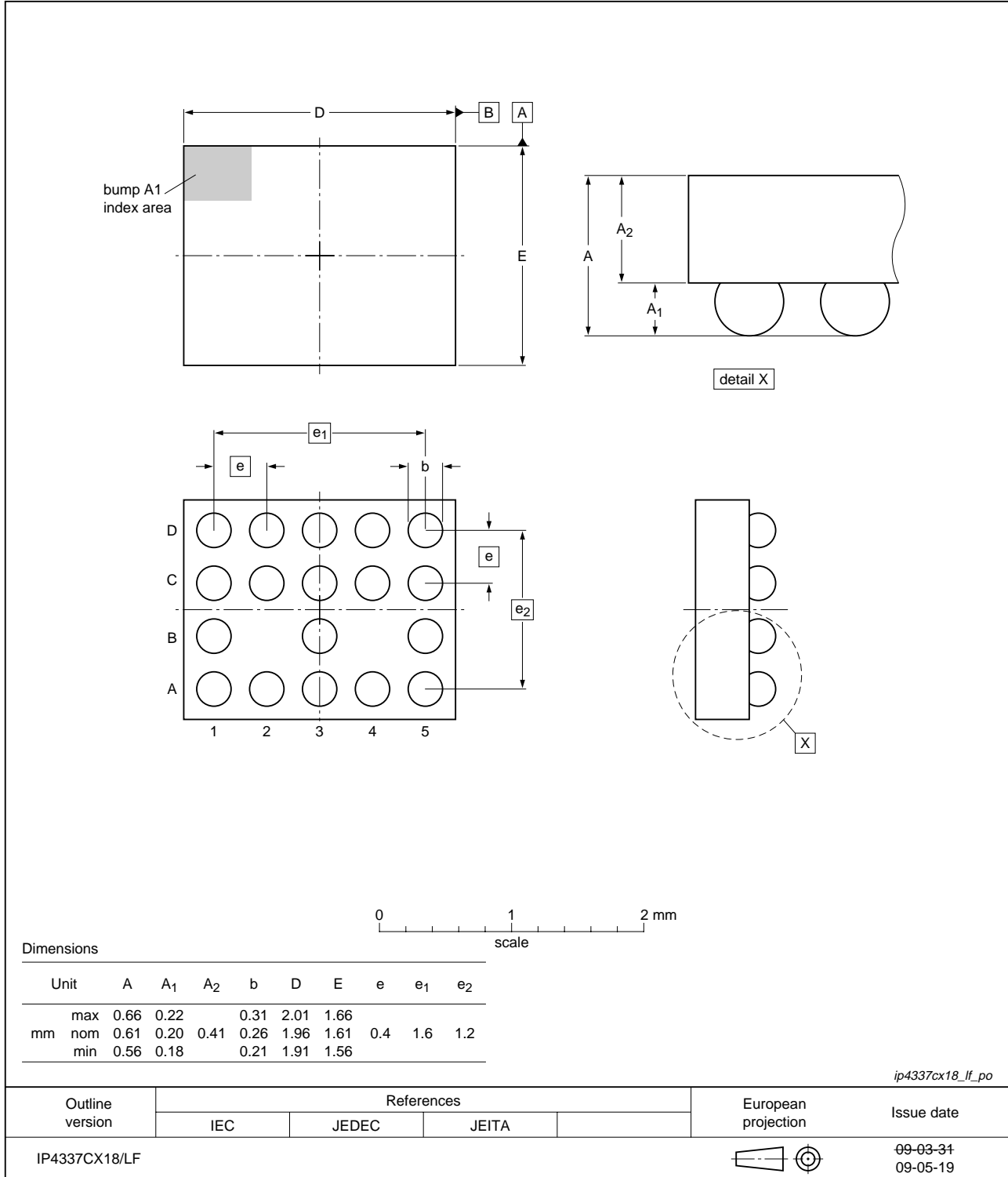


Fig 7. Package outline IP4337CX18/LF (WLCSP18)

9. Soldering of WLCSP packages

9.1 Introduction to soldering WLCSP packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering WLCSP (Wafer Level Chip-Size Packages) can be found in application note AN10439 "Wafer Level Chip Scale Package" and in application note AN10365 "Surface mount reflow soldering description".

Wave soldering is not suitable for this package.

All NXP WLCSP packages are lead-free.

9.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB
2. Component placement with a pick and place machine
3. The reflow soldering itself

9.3 Reflow soldering

Key characteristics in reflow soldering are:

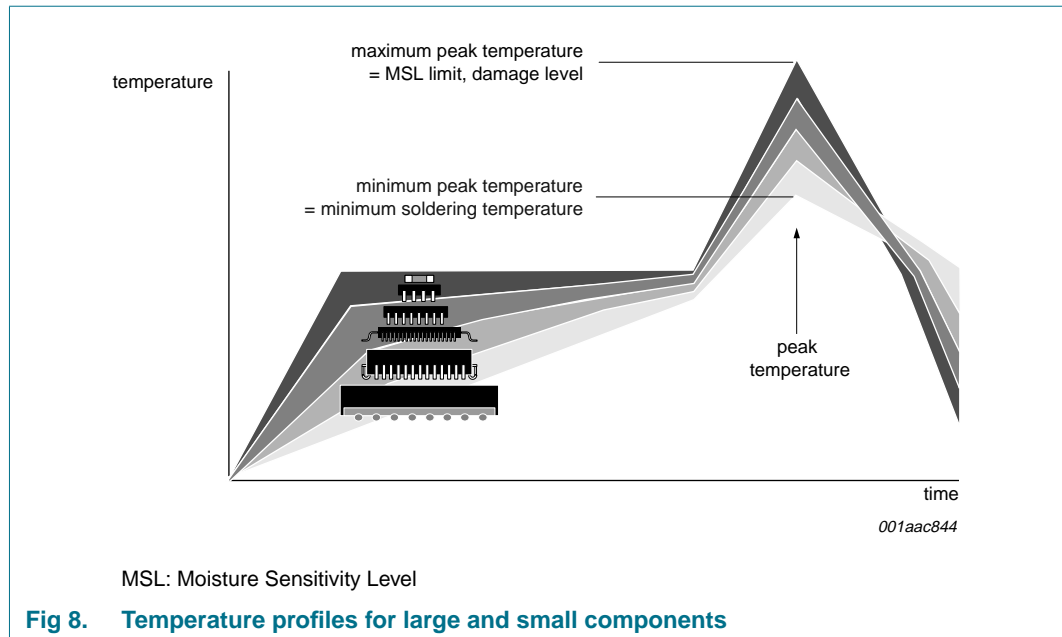
- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 8](#)) than a PbSn process, thus reducing the process window
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic) while being low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 6](#).

Table 6. Lead-free process (from J-STD-020C)

| Package thickness (mm) | Package reflow temperature (°C) | | |
|------------------------|---------------------------------|-------------|--------|
| | Volume (mm ³) | | |
| | < 350 | 350 to 2000 | > 2000 |
| < 1.6 | 260 | 260 | 260 |
| 1.6 to 2.5 | 260 | 250 | 245 |
| > 2.5 | 250 | 245 | 245 |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 8](#).



For further information on temperature profiles, refer to application note *AN10365 "Surface mount reflow soldering description"*.

9.3.1 Stand off

The stand off between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate
- The bump height on the chip

The higher the stand off, the better the stresses are released due to TEC (Thermal Expansion Coefficient) differences between substrate and chip.

9.3.2 Quality of solder joint

A flip-chip joint is considered to be a good joint when the entire solder land has been wetted by the solder from the bump. The surface of the joint should be smooth and the shape symmetrical. The soldered joints on a chip should be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, i.e. low bumps with large diameter. No failures have been found to be related to these voids. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits and voids.

9.3.3 Rework

In general, rework is not recommended. By rework we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip will be damaged. In that case it is recommended not to re-use the chip again.

Device removal can be done when the substrate is heated until it is certain that all solder joints are molten. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. Removing the device must be done using plastic tweezers, because metal tweezers can damage the silicon. The surface of the substrate should be carefully cleaned and all solder and flux residues and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side as well as on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in application note AN10365 "Surface mount reflow soldering description".

9.3.4 Cleaning

Cleaning can be done after reflow soldering.

10. Abbreviations

Table 7. Abbreviations

| Acronym | Description |
|---------|-------------------------------------|
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| LAN | Local Area Network |
| NWA | NetWork Analyzer |
| PCB | Printed-Circuit Board |
| PCS | Personal Communication System |
| RoHS | Restriction of Hazardous Substances |
| WAN | Wide Area Network |
| WLCSP | Wafer-Level Chip-Scale Package |

11. Revision history

Table 8. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|----------------|---|--------------------|---------------|----------------|
| IP4337CX18LF_2 | 20090820 | Product data sheet | - | IP4337CX18LF_1 |
| Modifications: | <ul style="list-style-type: none"> • Figure 4: figure title and symbol changed | | | |
| IP4337CX18LF_1 | 20090618 | Product data sheet | - | - |

12. Legal information

12.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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