

YSS220

(SP3)
Surround Processor 3

■ OUTLINE

YSS220(SP3) is an LSI which has surround capability by digital audio technology.

The LSI has built-in A/D, D/A converters which enable digital sound processing for analog signals.

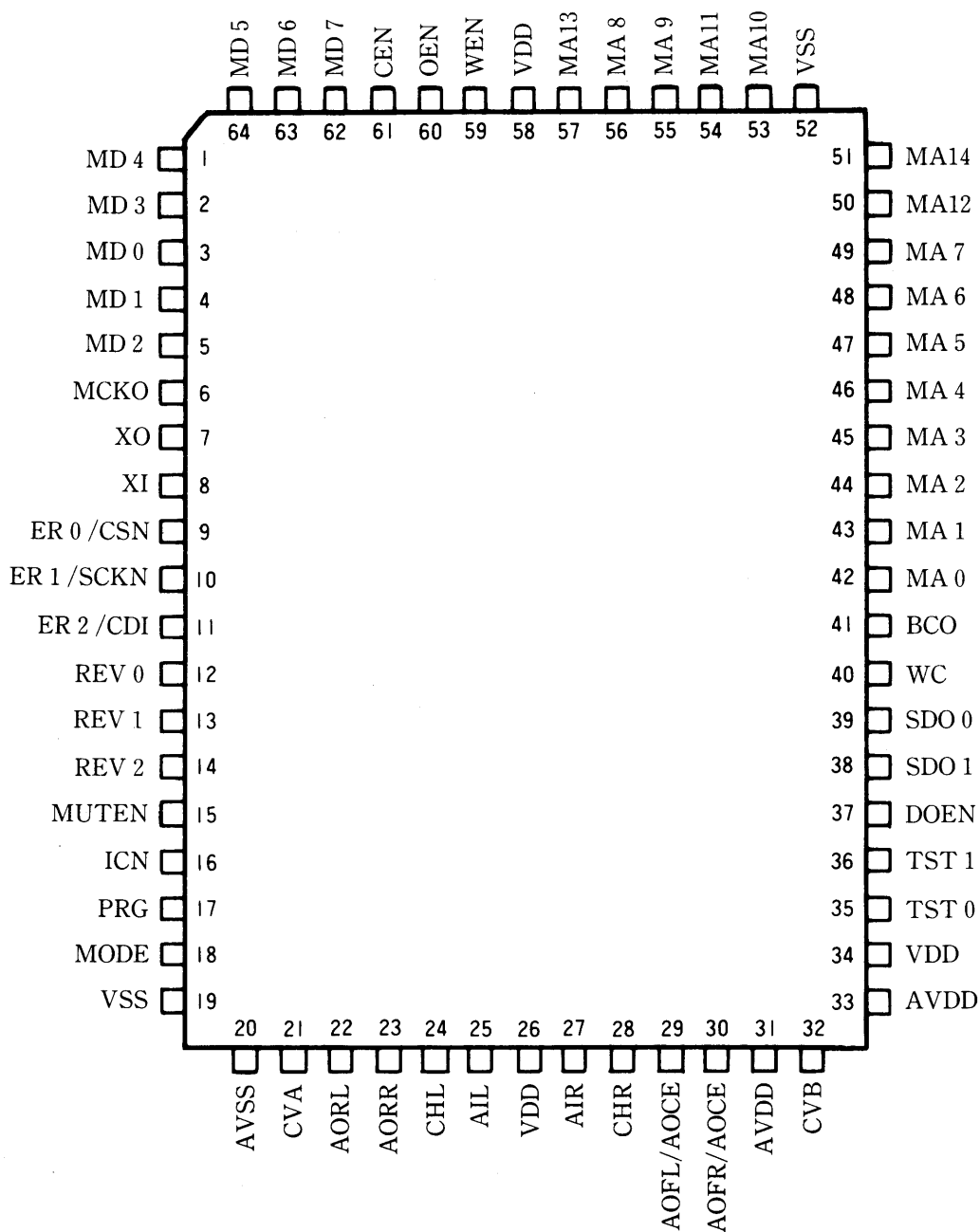
With a 256k pseudo SRAM or SRAM connected, the LSI can process digital delay up to 512ms.

■ FEATURES

- Built-in 15-bit floating ADC (L, R 2 channels) and DAC (FL, FR, RL, RR4 channels) enable digital processing for analog signals with 32kHz internal sampling frequency.
- 4 channels except center output can output digital signals as well. With a DAC connected externally, it will be possible with up to 5 channels (FL, C, FR, RL, RR).
- Hi-performance surround by mixing many echoes with using up to 512ms digital delay.
- Preset mode for easy control by terminal setting.
- Register control mode where it is possible to set various coefficients using microprocessor serial interface for original sound processing.
- Internal DSP is a 24-bit × 13-bit high speed multiplier with 128 steps.
- One 256k (32k × 8) pseudo SRAM or SRAM to be connected.
- 12.288MHz (384fs) master clock.
- 5V single power supply, Si-gate CMOS process.
- 64-pin plastic QFP(YSS220-F)

Note: Due to the nature of the product, the preset data cannot be disclosed although partially.

■ PIN DESCRIPTION



<64pin QFP Top View>

No.	Name	I/O	Description	
1	MD4	I/O	External RAM interface data terminal	
2	MD3	I/O	External RAM interface data terminal	
3	MD0	I/O	External RAM interface data terminal	
4	MD1	I/O	External RAM interface data terminal	
5	MD2	I/O	External RAM interface data terminal	
6	MCKO	O	DOEN='L' : Master clock output (12.288MHz) DOEN='H' : Fixed to 'L'	
7	XO	O	X'tal oscillator terminal	
8	XI	I	X'tal oscillator terminal or external clock input(12.288MHz)	
			MODE='H'	MODE='L'
9	ER0/CSN	I+s	ER0 : E/R preset select 0	CSN : CPU I/F chip select
10	ER1/SCKN	I+s	ER1 : E/R preset select 1	SCKN : CPU I/F serial clock
11	ER2/CDI	I+s	ER2 : E/R preset select 2	CDI : CPU I/F serial data
12	REV0	I+	Reverbration preset select 0	
13	REV1	I+	Reverbration preset select 1	
14	REV2	I+	Reverbration preset select 2	
15	MUTEN	I+	Output muting control (low-active)	
16	ICN	Is	Initial clear input	
17	PRG	I+	DSP program select (available only when MODE='H') 'L' : Mode 0, 'H' : Mode 1	
18	MODE	I+	Operation mode select 'L' : Register control mode, 'H' : Preset mode	
19	VSS	—	Ground (digital block)	
20	AVSS	—A	Ground (analog block)	
21	CVA	—A	L-ch ADC center voltage terminal	
22	AORL	OA	Rear L-ch DAC output	
23	AORR	OA	Rear R-ch DAC output	
24	CHL	—A	AIL input sample/hold capacitor terminal	
25	AIL	IA	L-ch ADC input	
26	VDD	—	+5V power supply (digital block)	
27	AIR	IA	R-ch ADC input	
28	CHR	—A	AIR input sample/hold capacitor terminal	
29	AOFL/AOCE	OA	DOEN='H' : Front L-ch DAC output DOEN='L' : C-ch DAC output	
30	AOFR/AOCE	OA	DOEN='H' : Front R-ch DAC output DOEN='L' : C-ch DAC output	
31	AVDD	—A	+5V power supply (analog block)	
32	CVB	—A	R-ch, C-ch ADC center voltage terminal	

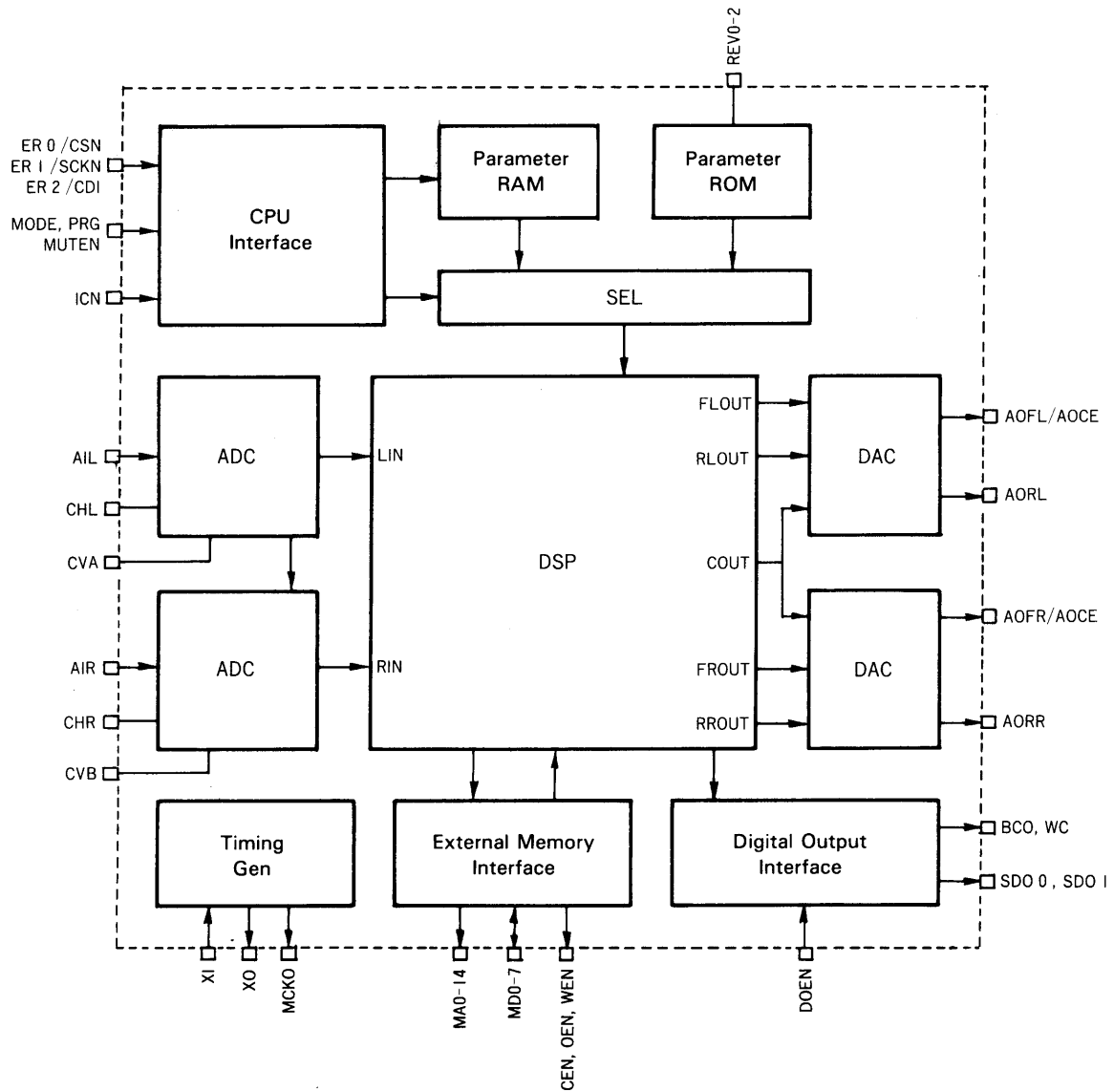
No.	Name	I/O	Description	
33	AVDD	- A	+5V power supply (analog block)	
34	VDD	-	+5V power supply (digital block)	
35	TST0	I+	LSI test terminal (Connect to VDD)	
36	TST1	I+	LSI test terminal (Connect to VDD)	
37	DOEN	I+	Digital signal output/Analog C-ch output enable	
			DOEN= 'L'	DOEN= 'H'
38	SDO1	O	Digital signal output rear channel (RL, RR)	Fixed to 'L'
39	SDO0	O	Digital signal output front channel (FL, FR)	Fixed to 'L'
40	WC	O	Digital signal output word clock fs	Fixed to 'L'
41	BCO	O	Digital signal output bit clock 64fs	Fixed to 'H'
42	MA0	O	External RAM interface address terminal	
43	MA1	O	External RAM interface address terminal	
44	MA2	O	External RAM interface address terminal	
45	MA3	O	External RAM interface address terminal	
46	MA4	O	External RAM interface address terminal	
47	MA5	O	External RAM interface address terminal	
48	MA6	O	External RAM interface address terminal	
49	MA7	O	External RAM interface address terminal	
50	MA12	O	External RAM interface address terminal	
51	MA14	O	External RAM interface address terminal	
52	VSS	-	Ground (digital block)	
53	MA10	O	External RAM interface address terminal	
54	MA11	O	External RAM interface address terminal	
55	MA9	O	External RAM interface address terminal	
56	MA8	O	External RAM interface address terminal	
57	MA13	O	External RAM interface address terminal	
58	VDD	-	+5V power supply (digital block)	
59	WEN	O	External RAM interface write enable terminal	
60	OEN	O	External RAM interface output enable terminal	
61	CEN	O	External RAM interface chip enable terminal	
62	MD7	I/O	External RAM interface data terminal	
63	MD6	I/O	External RAM interface data terminal	
64	MD5	I/O	External RAM interface data terminal	

NOTE) I+: Input terminal with a pull-up resistor

IS : Schmitt input

A : analog terminal

■ BLOCK DIAGRAM



■ FUNCTION DESCRIPTION

1. Clocks XI, XO, MCKO

X'tal oscillation circuit is formed by using XI, XO terminals. The oscillation frequency is 12.288MHz (fs=32KHz).

When DOEN='L', master clock is output through MCKO terminal.

2. ADCs and DACs AIL, AIR, CHL, CHR, AOFL/AOCE, AORL, AOFR/AOCE, AORR, CVA, CVB

L, R audio signals are input to AIL, AIR terminals. External capacitors are required to CHL, CHR terminals for sample/hold. CVA, CVB are center voltage terminals of L and R channels ADCs. Connect capacitors for stability, and bias AIL, AIR terminals with these voltages, respectively. The AIL and AIR signal are DC-cut by internal HPF after A/D conversion.

DAC sigals are output thorough AOFL/AOCE, AORL, AOFR/AOCE, AORR terminals. Connect capacitors for sample/hold, and buffer with a hi-impedance input for output.

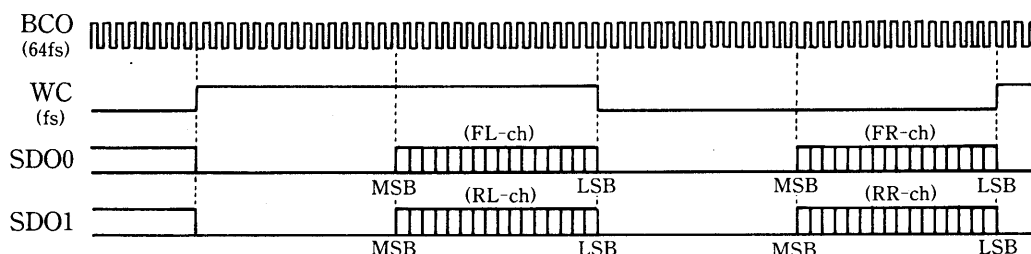
According to setting of DOEN terminal, outputs from the DACs are as follows:

DOEN	MODE	AOFL/ AOCE	AOFR/ AOCE	AORL	AORR	DIGITAL OUT
'H'	4CHANNEL MODE	FLOUT	FROUT	RLOUT	RROUT	OFF
'L'	5CHANNEL MODE	COUT	COUT	RLOUT	RROUT	FL, FR, (RL, RR)

3. Digital output DOEN, BCO, WC, SD00, SD01

Except center channel, each channel can also output digital data.

If digital output is required, set DOEN terminal to 'L'.



4. Microprocessor interface **MODE, PRG, MUTEN** **ER0/CSN, ER1/SCKN, ER2/CDI, REV0, REV1, REV2**

LSI control method varies according to setting for MODE terminal.

(Each of ER0/CSN, ER1/SCKN, ER2/CDI terminals has different functions depending on its MODE setting and terminal names indicate both functions. In this section, however, only the name for the set mode is indicated.)

(1) Preset mode (MODE= 'H')

All control is done by terminal settings.

Use PRG terminal for program setting, ER0, ER1, ER2, REV0, REV1, REV2 terminals for preset selection.

In this mode, when MUTEN terminal is set to 'L', both DAC outputs and digital outputs are muted instantly.

(2) Register control mode (MODE= 'L')

All control is done by writing data to registers using microprocessor serial interface (using CSN, SCKN, CEDI terminals).

In this mode, REV0, REV1, REV2, MUTEN terminals are invalid.

5. External RAM interface **MA0 ~ MA14, MD0 ~ 7, CEN, WEN, OEN**

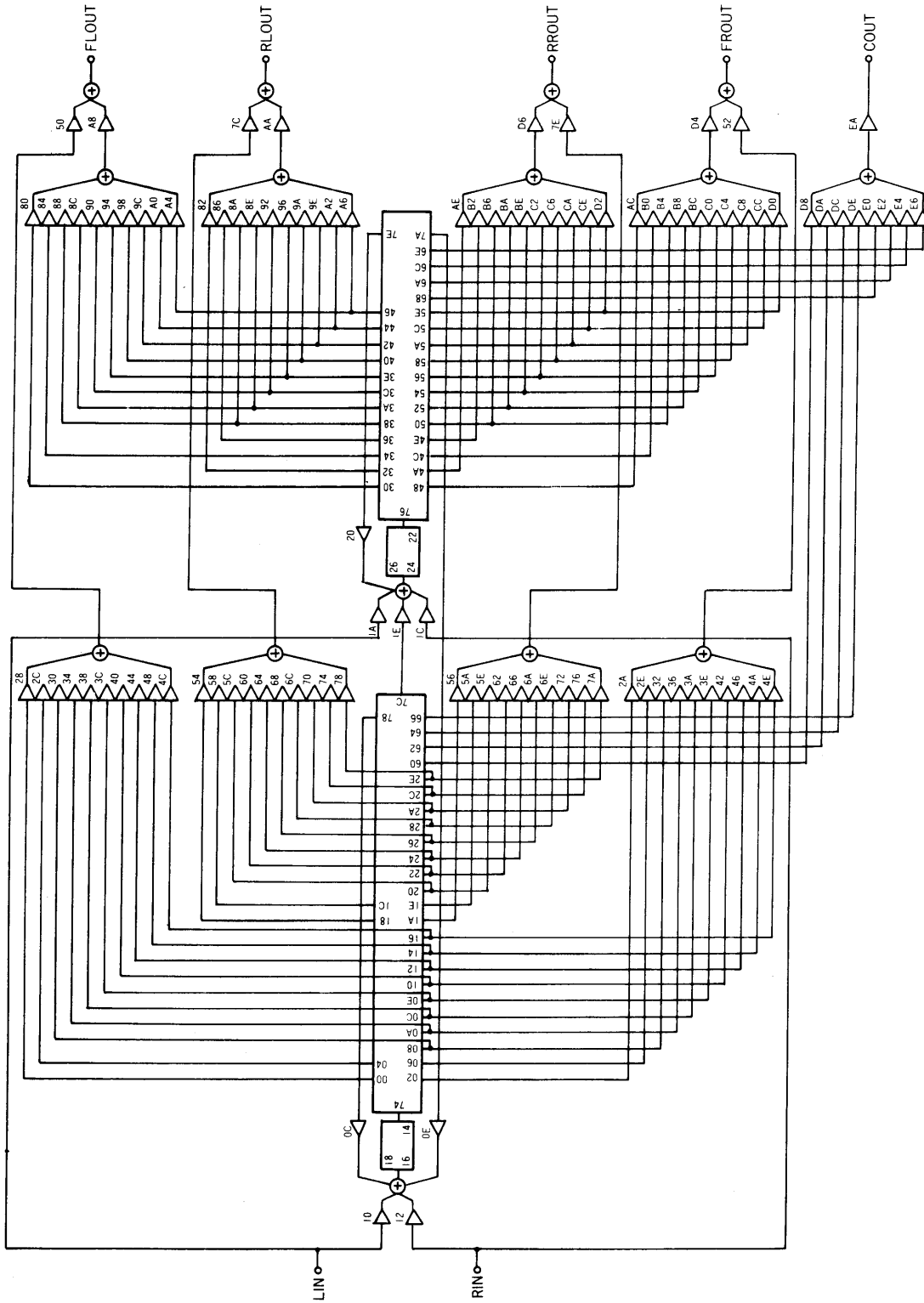
This LSI requires a 256K(32k*8word) pseudo SRAM or SRAM.

6. Initial clear **ICN, TST0, TST1**

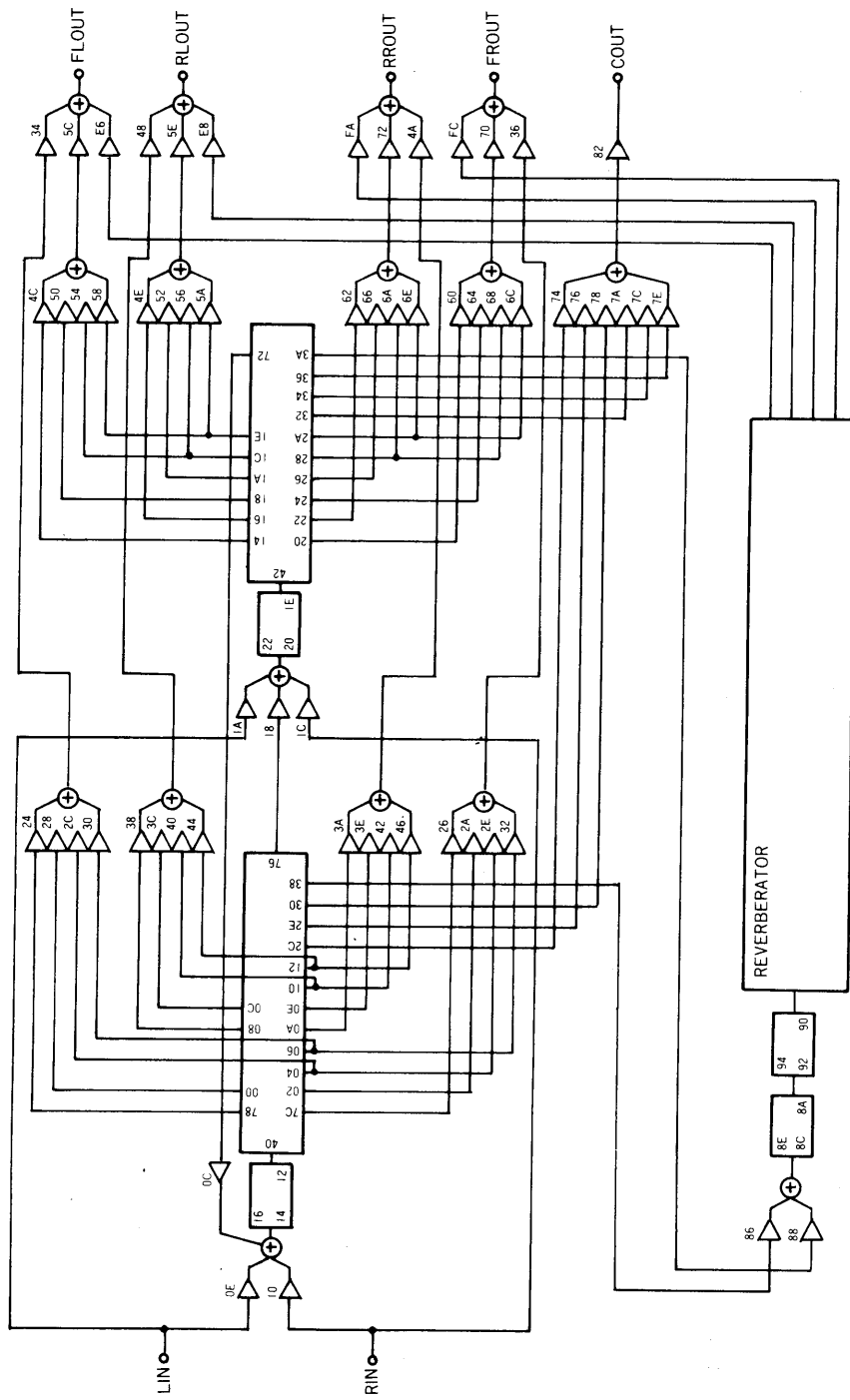
This LSI requires initial clear when the power is turned on. Set ICN terminal to 'L' for one sampling period or more. TST0, TST1 are LSI test terminals. Connect them to VDD.

■ DSP SIGNAL FLOW

1. MODE 0



2. MODE 1



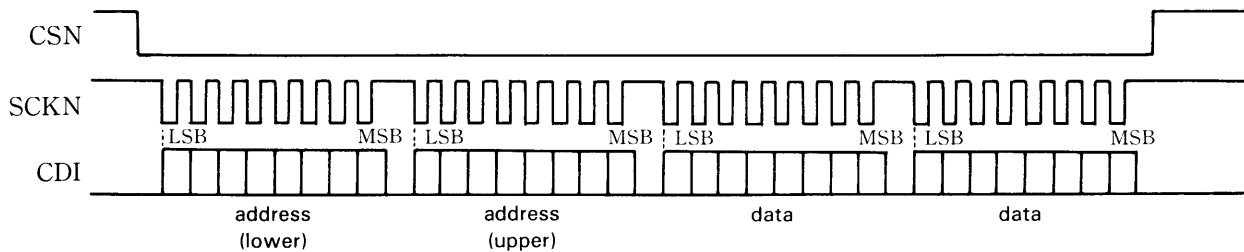
■ CONTROL DESCRIPTION

1. Microprocessor interface

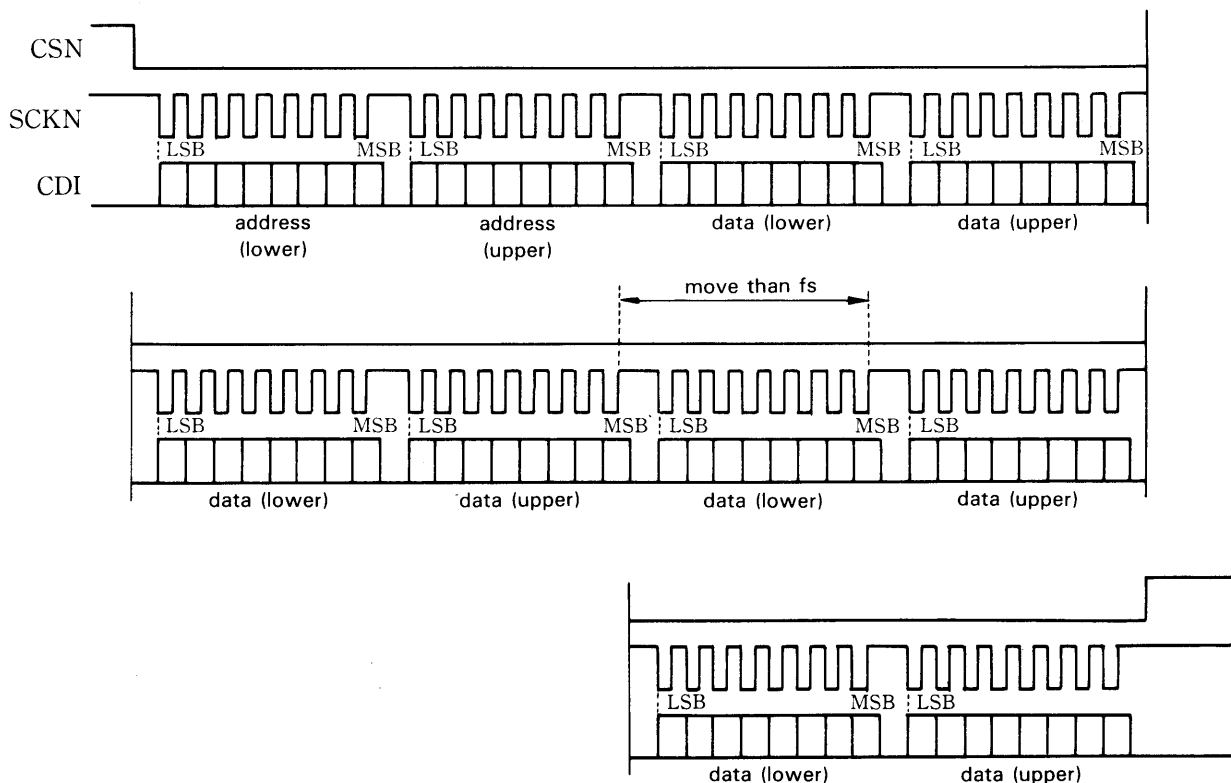
When in the register control mode (MODE='L'), function control and setting of DSP parameter are performed by writing data to the registers.

After setting the CSN terminal to 'L', send 2 bytes of the register addresses and then send the data, using SCKN and CDI terminals. As the register address where the data is written undergoes automatic increment at each sending of 1-byte data, the data is written in continuous addresses one after another only by sending them.

a) When address is 0000H or 0001H.



b) When address is 0100H or more.



2. Register map

Address (HEX)	Name	Description
0000	OPR0	Internal operation setting register
0001	OPR1	Preset data selection register
0100 ↓ 017F	M00 ↓ M7F	Memory pointer register
0200 ↓ 02FF	C00 ↓ CFE	Coefficient register

(Note)

* Do not write data in the other addresses.

* Data is not fixed when initial clear (except OPR0).

3. Data setting

(1)OPR0

- b0 (LSB) : Output muting ('1'=Muted)
- b1 : Program select ('0'=Mode 0, '1'=Mode 1)
- b2 : "VOL block" preset mode selection ('1'=preset)
- b3 : "E/R block" preset mode selection ('1'=preset)
- b4-b7 (MSB) : Set to '0' at all times.

(2)OPR1

- b0 (LSB), b1, b2 : "E/R block" preset pattern selection
(Preset # = $b2*4 + b1*2 + b0$)
- b3 : Don't care.
- b4, b5, b6 : "REV block" preset pattern selection (Mode 1 only)
(Preset # = $b6*4 + b5*2 + b4$)
- b7 (MSB) : don't care.

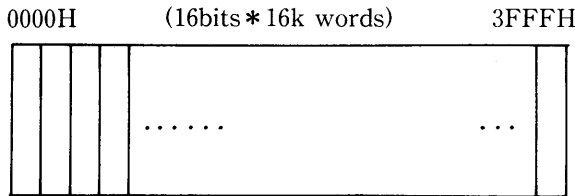
<Preset patterns>

	E/R Preset #	Guide name	REV Preset #	Rev. time
Mode 0	0	Hall 1	Fix to 0	
	1	Hall 2		
	2	Stadium		
	3	Disco 1		
Mode 1	0	Hall 3	0	Hall 1.0S
	1	Hall 4	1	Hall 1.5S
	2	Church 1	2	Hall 2.0s
	3	Church 2	3	Hall 2.5s
	4	Plate	4	Hall 3.0s
	5	Disco 2	5	Hall 3.5s
	6	«Mute»	6	Plate 1.5s
7	(INHIBIT)	7	Plate 2.5s	

(3)M00 ~ M7F

These registers control the delay time by setting read and write addresses of the external RAM. The upper byte of the memory pointer register address is defined by 01H and the data written in that address and the next one becomes the access pointer of the memory map as shown below. The lower byte of the memory pointer register address corresponds to the number marked on the delay tap in the DSP signal flow diagram.

The access pointers are defined by 2-byte and available between 0000H and 3FFFH.



The audio data is written in the memory address indicated by the write pointer and read from the address indicated by the read pointer. The data in the memory shifts to the next address for every sample time.

Therefore, the difference between the write pointer and the read pointer is defined as delay time and obtained by using the following equation where the sampling frequency is 32KHz.

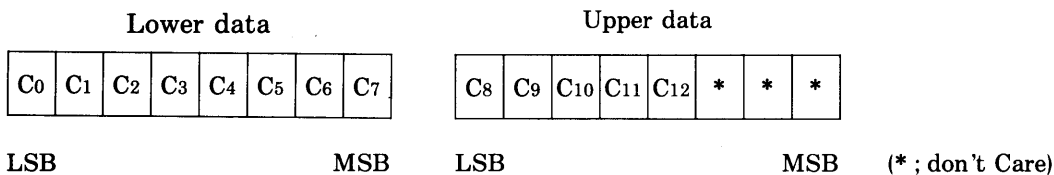
$$\text{Delay time} = [\text{Read pointer} - \text{Write pointer}] \times (1/32000) \text{ [S]}$$

(4)C00 ~ CFF

These registers determine coefficients of the internal multiplier.

The lower byte coefficient register address is defined by 02H and the data written in that address and the next one becomes the coefficient value according to the data assignments as shown below.

The lower byte of the coefficient register address corresponds to the number marked on the multiplier in the DSP signal flow diagram.



The coefficient value of the attenuator is 13-bit, 2's complement :

$$\text{(Coefficient value)} = (-1) \times C_{12} + \sum_{N=0}^{11} C_N \times 2^{N-12}$$

4. Terminal control

When in the preset mode (MODE = 'H'), function control and setting of DSP parameter are performed by setting terminals.

Terminal	Function	Description
PRG	DSP mode selection	'L' : Mode 0 'H' : Mode 1
ER0 ER1 ER2	E/R Preset selection	Preset # = ER2*4 + ER1*2 + ER0 (0 = 'L', 1 = 'H') Refer to <Preset Patterns> table.
REV0 REV1 REV2	REV preset selection (Available only when in Mode 1. Fix all to 'L' when in Mode 0)	Preset # = REV2*4 + REV1*2 + REV0 (0 = 'L', 1 = 'H') Refer to <Preset Patterns> table.
MUTEN	Output Muting	'L' : Muting

■ ELECTRICAL CHARACTERISTICS

1. Absolute maximum ratings

Parameter	Symbol	Rating	Unit
Power supply voltage	VDD	-0.3 ~ 7.0	V
Input voltage	VI	-0.3 ~ VDD+0.5	V
Operating temperature	T _{op}	-40 ~ 85	°C
Storage temperature	T _{stg}	-50 ~ 125	°C

2. Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	VDD	4.5	5.0	5.5	V
Operating temperature	T _{op}	0	25	70	°C

3. DC Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply current	W	VDD=5.0V			225	mW
Input voltage H level (1)	VIH1	*1	2.2			V
Input voltage L level (1)	VIL1	*1			0.8	V
Input voltage H level (2)	VIH2	*2	3.5			V
Input voltage L level (2)	VIL2	*2			1.5	V
Input voltage H level (3)	VIH3	*3	3.5			V
Input voltage L level (3)	VIL3	*3			0.8	V
Input leakage current	VLI				10	μA
Input capacitance	CI				10	pF
Input capacitance	CO				10	pF
Output voltage H level (1)	VOL	IOL=0.4mA, *4	VDD - 1.0			V
Output voltage L level (1)	VOH	IOH= -1.6mA, *4			0.4	V
Output voltage H level (2)	VOL	IOL=0.4mA, *5	VDD - 1.0			V
Output voltage L level (2)	VOH	IOH= -1.6mA, *5			1.0	V

*1) Applicable to MD0 ~ MD7 terminals.

*2) Applicable to input terminals other than XI terminal.

*3) Applicable to XI terminal.

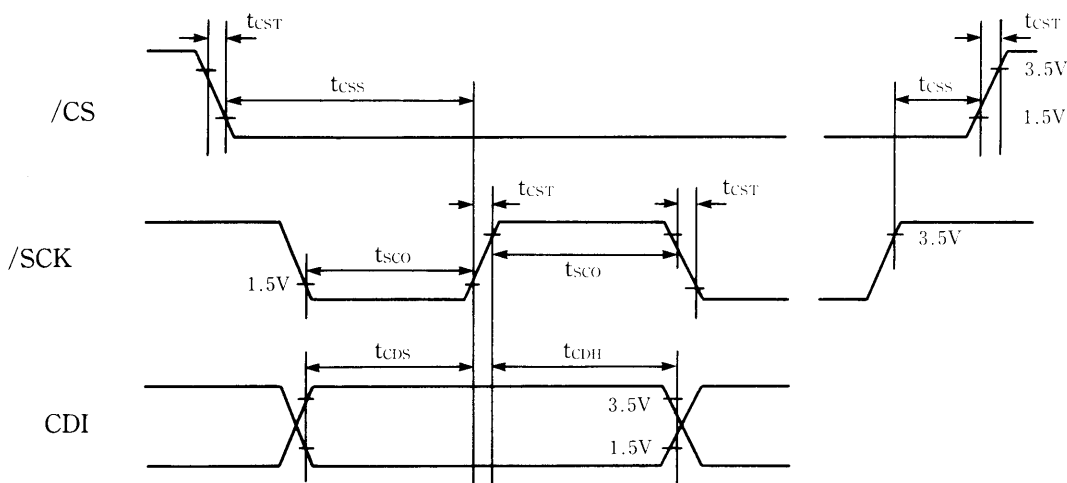
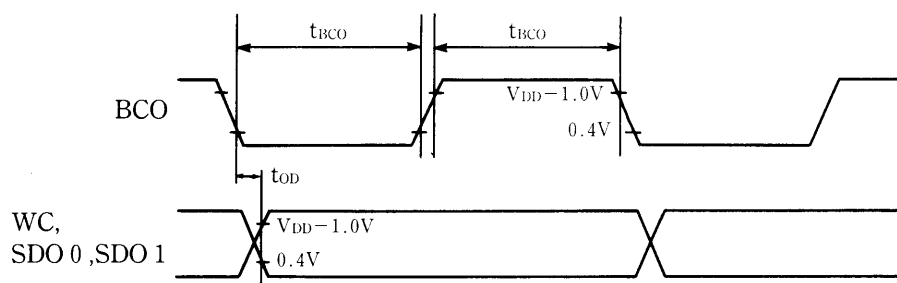
*4) Applicable to output terminals other than XO terminal.

*5) Applicable to XO terminal.

4. AC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
XI frequency	f_{XI}	11.0	12.288	13.0	MHz
XI duty	D_{XI}		50		%
BCO frequency	f_{BC}		$64f_{XI}$		Hz
BCO ON/OFF time	t_{BCO}	180			ns
WC, SDO0, SDO1 output delay	t_{OD}	-40		40	ns
CSN setup time	t_{CSS}	1/50fs			s
SCKN ON/OFF time	t_{SCO}	1/50fs			s
CDI setup time	t_{CDS}	1/100fs			s
CDI hold time	t_{CDH}	1/100fs			s
CSN, SCKN Transition time	t_{CST}			1/150fs	s

(Note) Load capacitance 30pF



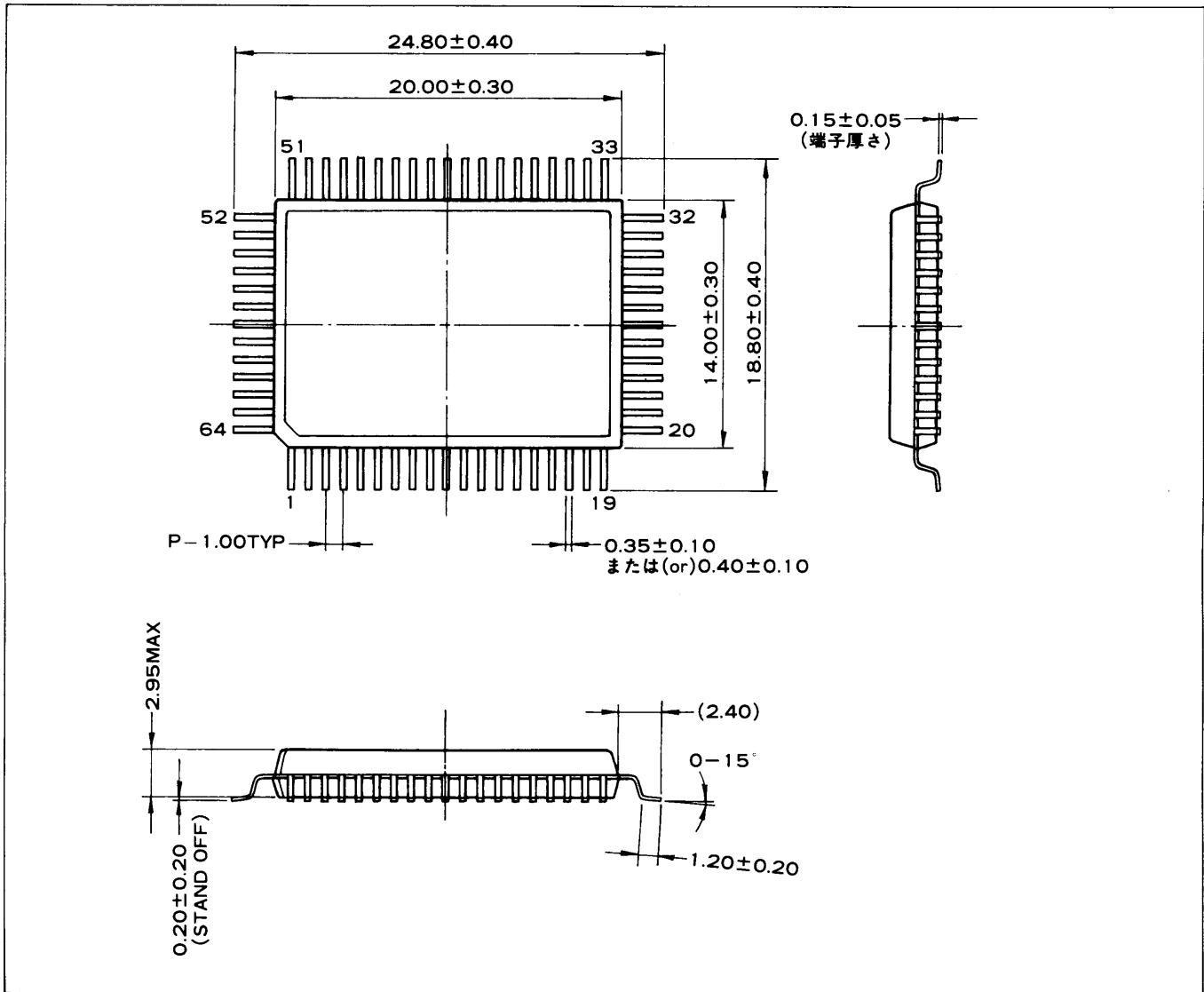
5. Analog Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Analog input voltage	V _{IA}	Amplitude		4.70		V
Analog output voltage	V _{OA}	Amplitude		4.70		V
DC offset voltage	V _C			2.5		V
Total harmonic distortion * 1	THD+N (1)	1kHz, 0dB		0.4	0.8	%
	THD+N (2)	1kHz, -30dB		0.6	1.2	%
Signal to noise ratio	S/N	S=0dB	80	85		dB

*1) LPF with $f_c=10\text{kHz}$, 36dB/oct is used when $OdB=4.70\text{PP}$, A/D→D/A through.

*2) IHF-A is used when $OdB=4.70\text{VPP}$, A/D→D/A through.

■ EXTERNAL DIMENSIONS



Note) The specifications of this product are subject to improvement changes without prior notice.

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YAMAHA LSI

APPLICATION NEWS

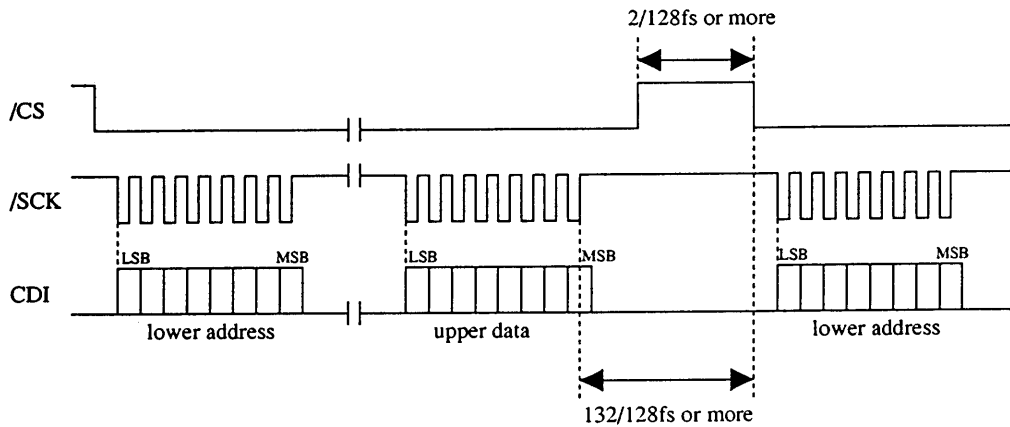
No.	: AN 079
Date of Issue	: 1995. 8. 1
Device Name	: YSS220 (SP3)

YAMAHA CORPORATION
Semi-conductor Sales Department
Sales Engineering Section

YSS220 (SP3) MICROPROCESSOR INTERFACE

■ ADDITIONAL SPECIFICATION

- Data transmission to discontinuous address



When sending the data to the discontinuous address, it is necessary to set the timing as shown above.