FUJITSU MICROELECTRONICS
DATA SHEET

DS07-13733-6E

16-bit Microcontroller

CMOS

F²MC-16LX MB90800 Series

MB90803/803S/F803/F803S/F804-101/ MB90F804-201/F809/F809S/V800

■ DESCRIPTION

The MB90800 series is a general-purpose 16-bit microcontroller that has been developed for high-speed real-time processing required for industrial and office automation equipment and process control, etc. The LCD controller of 48 segment four common is built into.

Instruction set has taken over the same AT architecture as in the F²MC-8L and F²MC-16L, and is further enhanced to support high level languages, extend addressing mode, enhanced divide/multiply instructions with sign and enrichment of bit processing. In addition, long word processing is now available by introducing a 32-bit accumulator.

Note: F²MC is the abbreviation of Fujitsu Flexible Microcontroller.

■ FEATURES

- **Clock**

  Built-in PLL clock frequency multiplication circuit
  Operating clock (PLL clock) : divided-by-2 of oscillation (at oscillation of 6.25 MHz) or
  1 to 4 times the oscillation (at oscillation of 6.25 MHz to 25 MHz).
  Minimum instruction execution time of 40.0 ns (at oscillation of 6.25 MHz, four times the PLL clock, operation at Vcc = 3.3 V)

- **The maximum memory space:16 Mbytes**

  24-bit internal addressing
  Bank addressing

(Continued)

For the information for microcontroller supports, see the following web site.

http://edevice.fujitsu.com/micom/en-support/

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2009.9

(Continued)

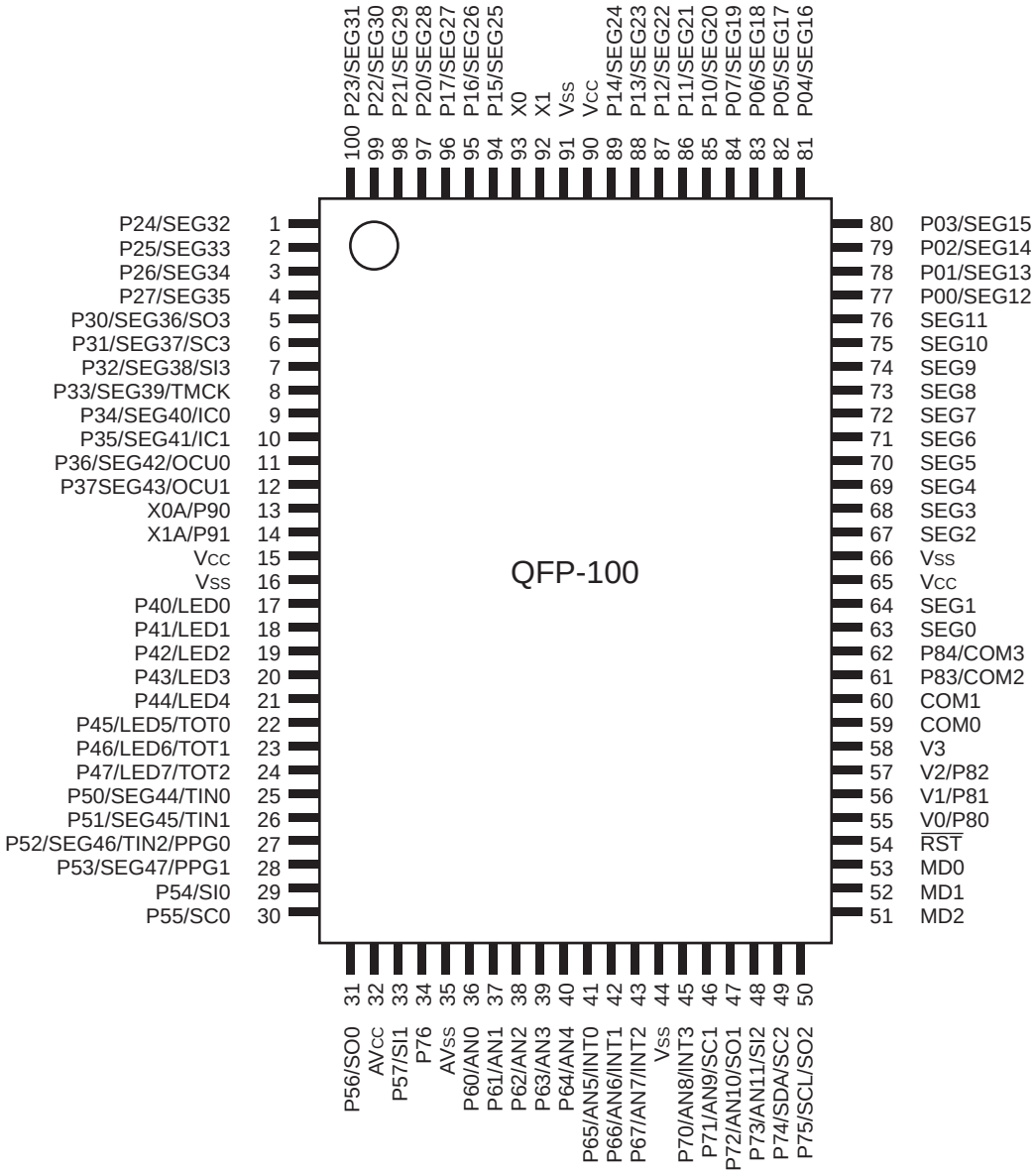
- **Optimized instruction set for controller applications**
  Wide choice of data types (bit, byte, word, and long word)
  Wide choice of addressing modes (23 types)
  High code efficiency
  Enhanced high-precision computing with 32-bit accumulator
  Enhanced Multiply/Divide instructions with sign and the RETI instruction
- **Instruction system compatible with high-level language (C language) and multitask**
  Employing system stack pointer
  Instruction set has symmetry and barrel shift instructions
- **Program Patch Function (2 address pointer)**
- **4-byte instruction queue**
- **Interrupt function**
  The priority level can be set to programmable.
  Interrupt function with 32 factors
- **Data transfer function**
  Expanded intelligent I/O service function (EI^2OS): Maximum of 16 channels
- **Low Power Consumption Mode**
  Sleep mode (a mode that halts CPU operating clock)
  Time-base timer mode (a mode that operates oscillation clock and time-base timer)
  Watch mode (mode in which only the subclock and watch timers operate)
  Stop mode (a mode that stops oscillation clock and sub clock)
  CPU blocking mode (operating CPU at each set cycle)
- **Package**
  QFP-100 (FPT-100P-M06 : 0.65 mm lead pitch)
- **Process : CMOS technology**

(Continued)

Item \ Part number	MB90V800-101/201	MB90F804-101/201	MB90803/MB90803S	MB90F803/MB90F803S	MB90F809/MB90F809S
8/10-bit A/D converter	12 channels (input multiplex) The 8-bit resolution or 10-bit resolution can be set. Conversion time : 5.9 μs (When machine clock 16.8 MHz works).				
UART	Full-duplex double buffer Asynchronous/synchronous transmit (with start/stop bits) are supported. Two channels are built in.				
Extended I/O serial interface	Two channels are built in.				
Interrupt delay interrupt	One channel				
DTP/External interrupt	4 channels Interrupt causes : L → H edge/ H → L edge/ L level/ H level selectable				
Low Power Consumption Mode	Sleep mode/Time-base timer mode/Watch mode/Stop mode/CPU intermittent mode				
Process	CMOS				
Operating voltage	2.7 V to 3.6 V				

■ PIN ASSIGNMENT

(TOP VIEW)



(FPT-100P-M06)

Pin No.	Pin Name	I/O Circuit Type*	Status/function at reset	Function
7	SEG38	E	Port input (High-Z)	A segment output terminal of the LCD controller/ driver.
	P32			General purpose input/output port.
	SI3			Serial data input pin of serial I/O ch.3. This pin may be used during serial I/O ch.3 in input mode, so it cannot use as other pin function.
8	SEG39	E		A segment output terminal of the LCD controller/ driver.
	P33			General purpose input/output port.
	TMCK			Timer clock output pin. It is effective when permitting the power output.
9, 10	SEG40, SEG41	E		A segment output terminal of the LCD controller/ driver.
	P34, P35			General purpose input/output port.
	IC0, IC1			External trigger input pin of input capture ch.0/ch.1.
11, 12	SEG42, SEG43	E		A segment output terminal of the LCD controller/ driver.
	P36, P37			General purpose input/output port.
	OCU0, OCU1			Output terminal for the output compares ch.0/ch.1.
17 to 21	LED0 to LED4	F		It is a output terminal for LED (I_{OL} = 15 mA).
	P40 to P44			General purpose input/output port.
22 to 24	LED5 to LED7	F		It is a output terminal for LED (I_{OL} = 15 mA).
	P45 to P47			General purpose input/output port.
	TOT0 to TOT2			External event output pin of reload timer ch.0 to ch.2. It is effective when permitting the external event output.
25, 26	SEG44, SEG45	E		A segment output terminal of the LCD controller/ driver.
	P50, P51			General purpose input/output port.
	TIN0, TIN1			External clock input pin of reload timer ch.0, ch.1. It is effective when permitting the external clock input.

(Continued)

Pin No.	Pin Name	I/O Circuit Type*	Status/function at reset	Function
27	SEG46	E	Port input (High-Z)	A segment output terminal of the LCD controller/ driver.
	P52			General purpose input/output port.
	TIN2			External clock input pin of reload timer ch.2. It is effective when permitting the external clock input.
	PPG0			PPG timer (ch.0) output pin.
28	SEG47	E		A segment output terminal of the LCD controller/ driver.
	P53			General purpose input/output port.
	PPG1			PPG (ch.1) timer output pin.
29	SIO	G		Serial data input pin of UART ch.0. This pin may be used during UART ch.0 in receiving mode, so it cannot use as other pin function.
	P54			General purpose input/output port.
30	SC0	G		Serial clock input/output pin of UART ch.0. It is effective when permitting the serial clock output of UART ch.0.
	P55			General purpose input/output port.
31	SO0	G		Serial data output pin of UART ch.0. It is effective when permitting the serial clock output of UART ch.0.
	P56			General purpose input/output port.
33	SI1	G		Serial data input pin of UART ch.1. This pin may be used during UART ch.1 in receiving mode, so it cannot use as other pin function.
	P57			General purpose input/output port.
34	P76	G		General purpose input/output port.
36 to 40	AN0 to AN4	I		Analog input pin ch.0 to ch.4 of A/D converter. Enabled when analog input setting is enabled (set by ADER).
	P60 to P64			General purpose input/output port.

(Continued)

Pin No.	Pin Name	I/O Circuit Type*	Status/function at reset	Function
41 to 43	AN5 to AN7	I	Analog input (High-Z)	Analog input pin ch.5 to ch.7 of A/D converter. Enabled when analog input setting is enabled .
	P65 to P67			General purpose input/output port.
	INT0 to INT2			Functions as an external interrupt ch.0 to ch.2 input pin.
45	AN8	I		Analog input pin ch.8 of A/D converter. Enabled when analog input setting is enabled .
	P70			General purpose input/output port.
	INT3			Functions as an external interrupt ch.3 input pin.
46	AN9	I	Port input (High-Z)	Analog input pin ch.9 of A/D converter. Enabled when analog input setting is enabled .
	P71			General purpose input/output port.
	SC1			Serial clock input/output pin of UART ch.1. It is effective when permitting the serial clock output of UART ch.1.
47	AN10	I		Analog input pin ch.10 of A/D converter. Enabled when analog input setting is enabled .
	P72			General purpose input/output port.
	SO1			Serial data output pin of serial I/O ch.1. Valid when serial data output of serial I/O ch.1 is enabled.
48	AN11	I		Analog input pin ch.11 of A/D converter. Enabled when analog input setting is enabled .
	P73			General purpose input/output port.
	SI2			Serial data input pin of serial I/O ch.2. This pin may be used during serial I/O ch.2 in input mode, so it cannot use as other pin function.

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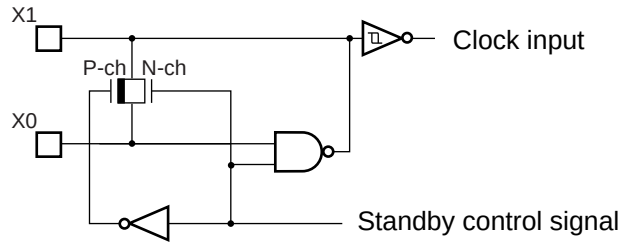
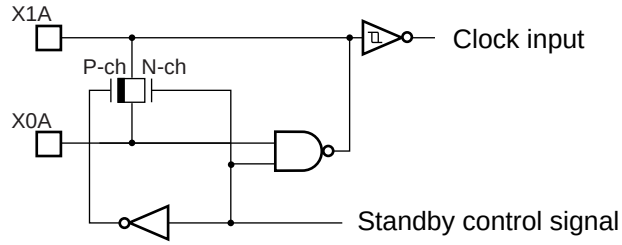
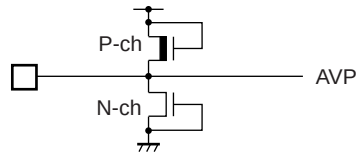
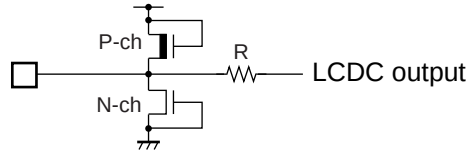
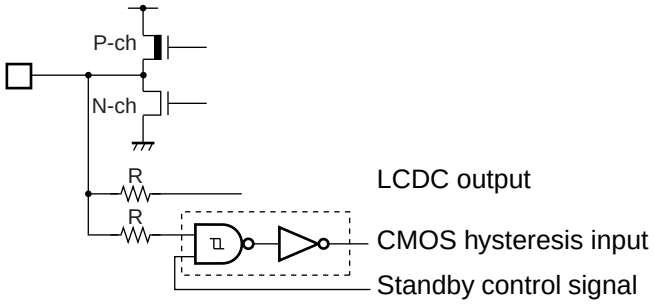
Pin No.	Pin Name	I/O Circuit Type*	Status/function at reset	Function
49	SDA	H	Port input (High-Z)	Data input/output pin of I²C Interface. This pin is enabled when the I²C interface is operated. While the I²C interface is running, the port must be set for input use.
	P74			General purpose input/output port. (N-ch open-drain, withstand voltage of 5 V.)
	SC2			Serial clock input pin of serial I/O ch.2. Valid when serial clock output of serial I/O ch.2 is enabled.
50	SCL	H		Clock input/output pin of I²C Interface. This pin is enabled when the I²C interface is operated. While the I²C interface is running, the port must be set for input use.
	P75			General purpose input/output port. (N-ch open-drain, withstand voltage of 5 V.)
	SO2			Serial data output pin of serial I/O ch.2. Valid when serial data output of serial I/O ch.2 is enabled.
55 to 57	V0 to V2	J	LCD drive power supply input	LCD controller/driver. Reference power terminals of LCD controller/driver.
	P80 to P82			General purpose input/output port.
59, 60	COM0, COM1	D	LCD COM output	A common output terminal of the LCD controller/ driver.
61, 62	P83, P84	E	Port input (High-Z)	General purpose input/output port.
	COM2, COM3			A common output terminal of the LCD controller/ driver.
32	AV_{CC}	C	Power supply	A/D converter exclusive power supply input pin.
35	AV_{SS}	C		A/D converter-exclusive GND power supply pin.
58	V3	J		LCD controller/driver Reference power terminals of LCD controller/driver.
15, 65, 90	V_{CC}	—		These are power supply input pins.
16, 44, 66, 91	V_{SS}	—		GND power supply pin.

* : Refer to ■ I/O CIRCUIT TYPE for details on the I/O circuit types.

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		Oscillation feedback resistance : 1 MΩ approx.
B		Low-rate oscillation feedback resistor, approx.10 MΩ
C		Analog power supply input protection circuit
D		LCDC output
E		CMOS output LCDC output CMOS hysteresis input (With input interception function at standby)

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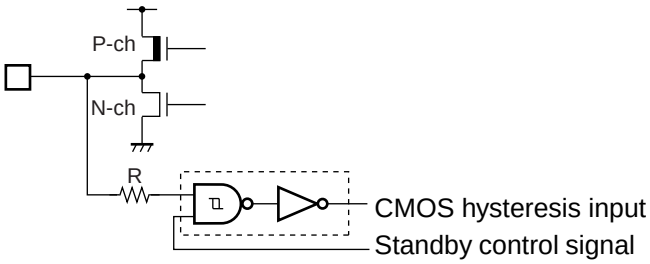
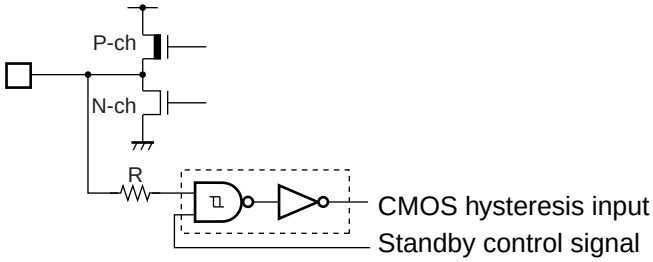
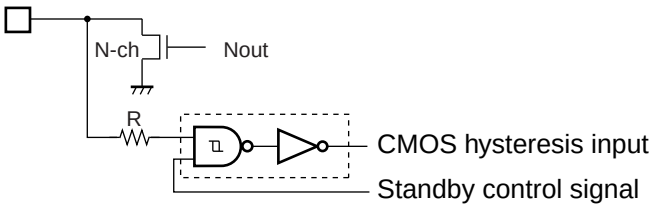
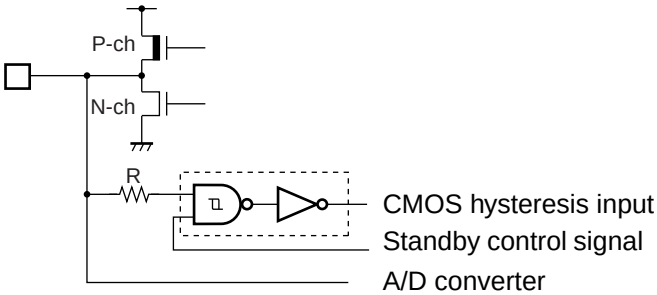
Type	Circuit	Remarks
F		CMOS output (Heavy-current I_{OL} =15 mA for LED drive) CMOS hysteresis input (With input interception function at standby)
G		CMOS output CMOS hysteresis input (With input interception function at standby) Notes : • The I/O port and internal resources share one output buffer for their outputs. • The I/O port and internal resources share one input buffer for their input.
H		CMOS hysteresis input (With input interception function at standby) N-ch open drain output
I		CMOS output CMOS hysteresis input (With input interception function at standby) Analog input (If the bit of analog input enable register = 1, the analog input of A/D converter is enabled.) Notes : • The I/O port and internal resources share one output buffer for their outputs. • The I/O port and internal resources share one input buffer for their inputs.

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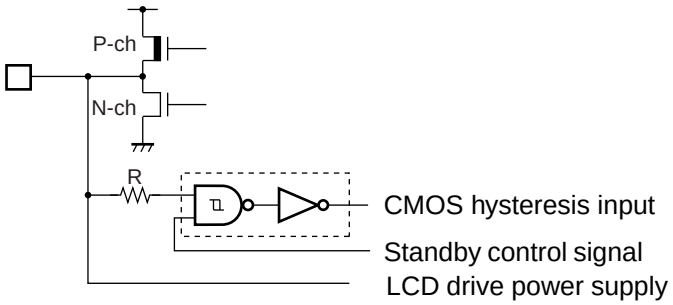
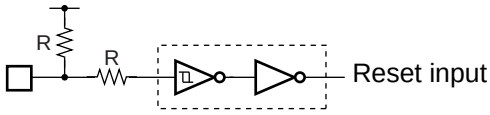
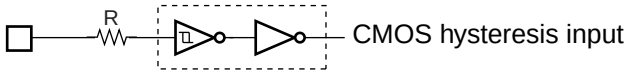
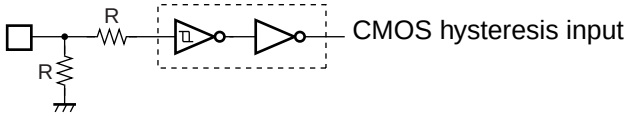
Type	Circuit	Remarks
J		CMOS output CMOS hysteresis input (With input interception function at standby) LCD drive power supply input
K		CMOS hysteresis input with pull-up resistor.
L		CMOS hysteresis input
M		CMOS hysteresis input with pull-down resistor

■ HANDLING DEVICES

1. Preventing Latch-up, Turning on Power Supply

Latch-up may occur on CMOS IC under the following conditions:

- If a voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins,
- A voltage higher than the rated voltage is applied between V_{CC} pin and V_{SS} pin.
- If the AV_{CC} power supply is turned on before the V_{CC} voltage.

Ensure that you apply a voltage to the analog power supply at the same time as V_{CC} or after you turn on the digital power supply (when you perform power-off, turn off the analog power supply first or at the same time as V_{CC} and the digital power supply).

When latch-up occurs, power supply current increases rapidly and might thermally damage elements. When using CMOS IC, take great care to prevent the occurrence of latch-up.

2. Treatment of unused pins

If unused input pins are left open, they may cause abnormal operation or latch-up which may lead to permanent damage to the semiconductor. Any such pins should be pulled up or pulled down through resistance of at least 2 kΩ.

Any unused input/output pins should be left open in output status, or if found set to input status, they should be treated in the same way as input pins.

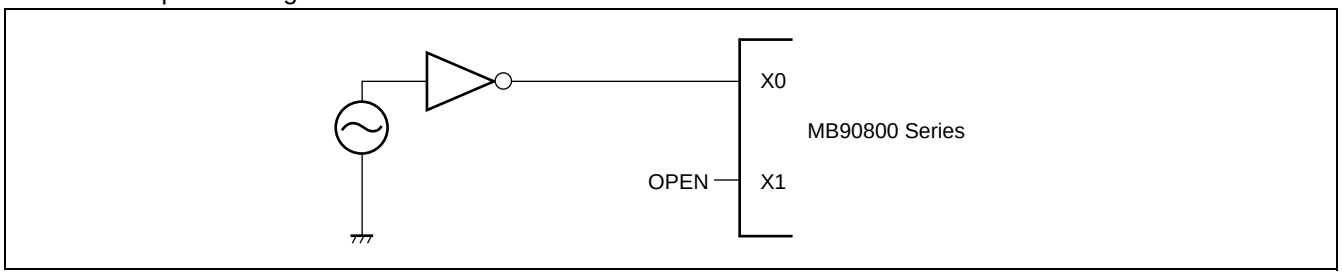
Any unused output pins should be left open.

3. Treatment of A/D converter power supply pins

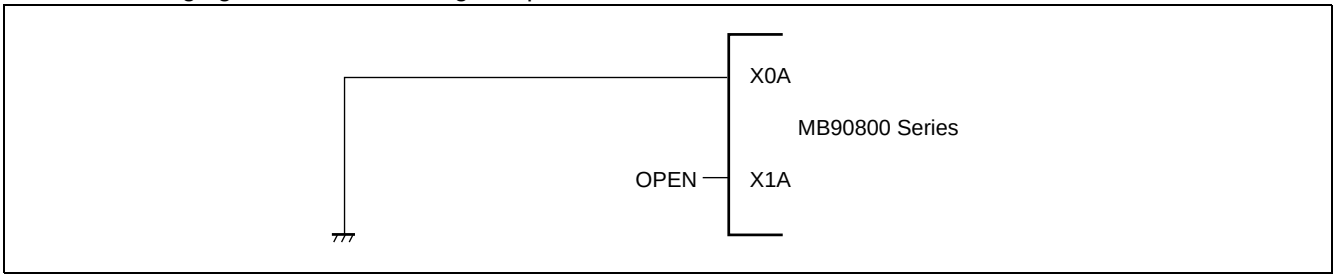
Even if the A/D converter is not used, pins should be connected so that $AV_{CC} = V_{CC}$, and $AV_{SS} = V_{SS}$.

4. About the attention when the external clock is used

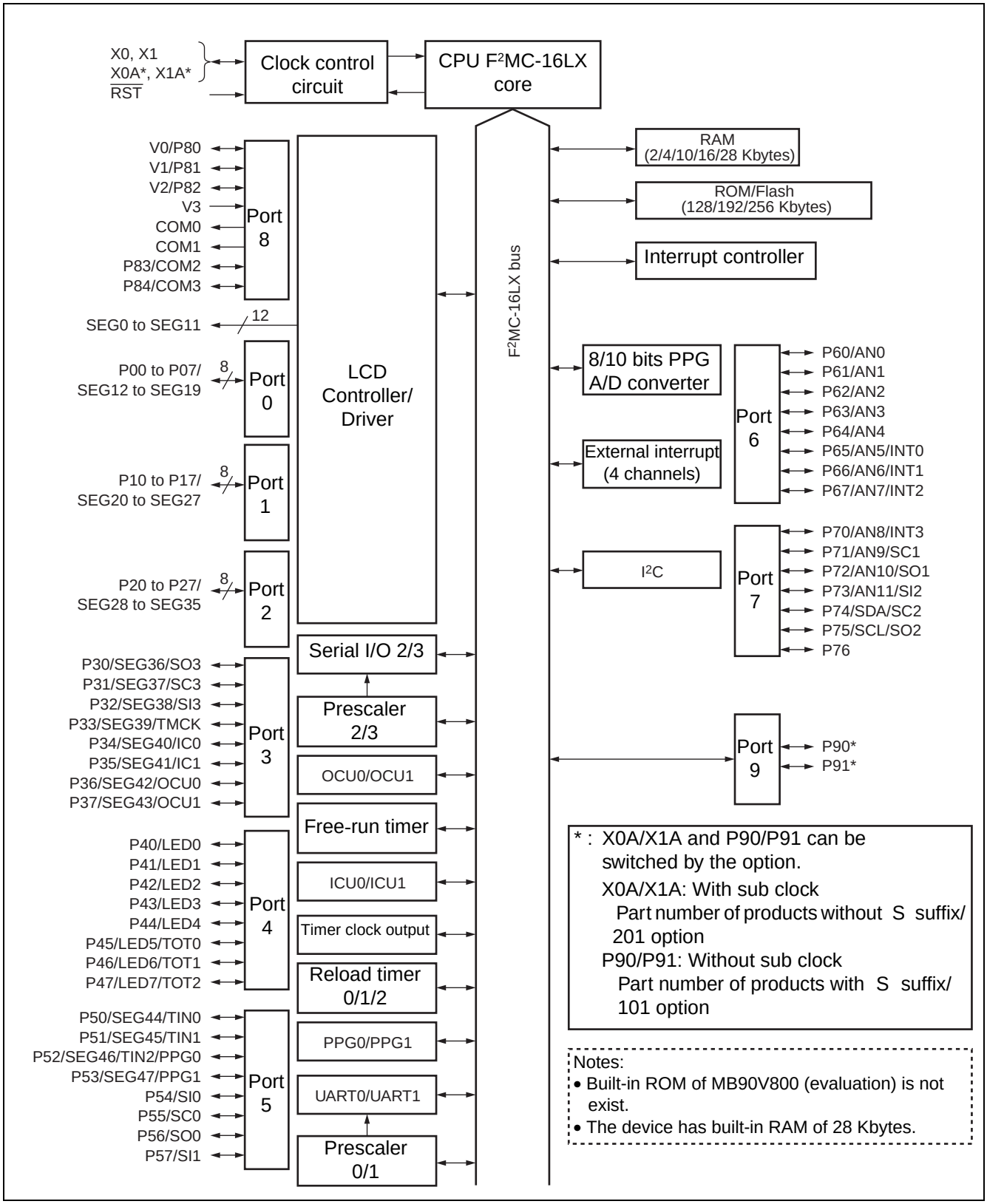
In using an external clock, drive pin X0 only and leave pin X1 open.
The example of using an external clock is shown below.



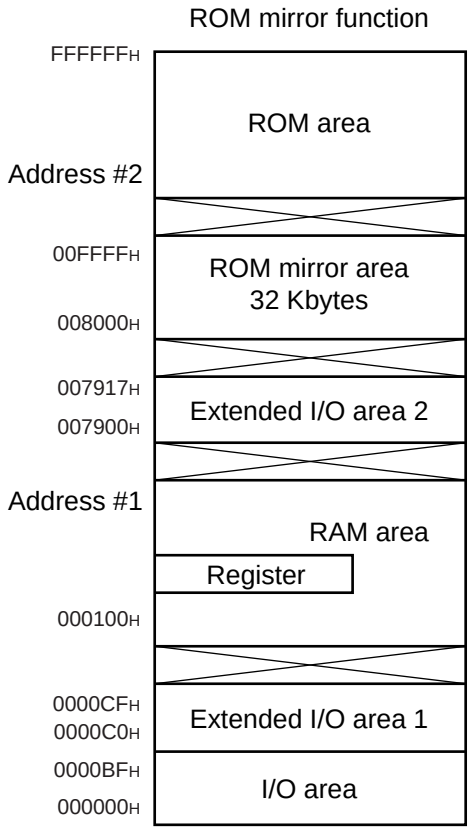
Please set X0A = GND and X1A = open without subclock mode.
The following figure shows the using sample.



■ BLOCK DIAGRAM



■ MEMORY MAP



Part number	Address #1	Address #2
MB90803/S, MB90F803/S	0010FFH	FE0000H
MB90F809/S	0028FFH	FD0000H
MB90F804-101/201	0040FFH	FC0000H
MB90V800-101/201	0070FFH	F80000H*

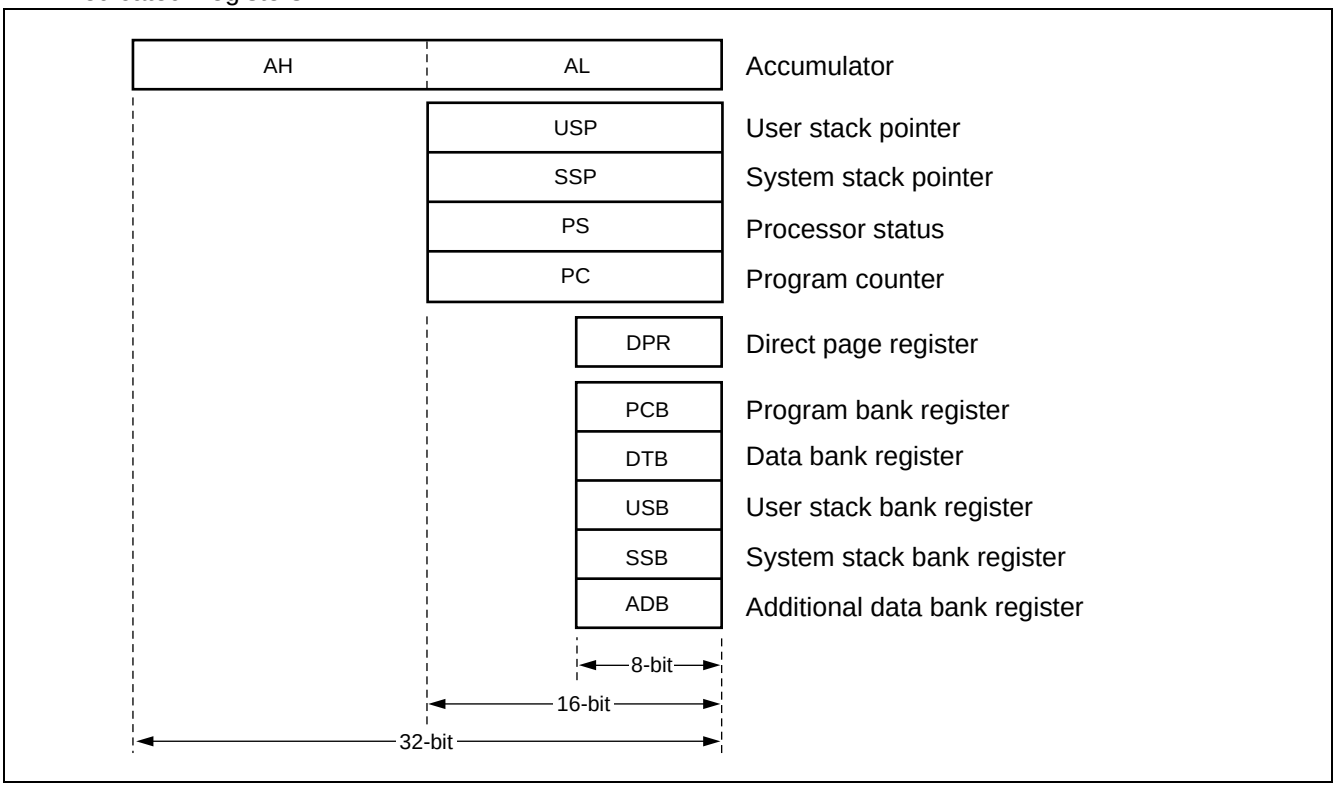
* : ROM is not built into MB90V800.
F80000H is ROM decipherment region on the tool side.

Memory Map of MB90800 Series

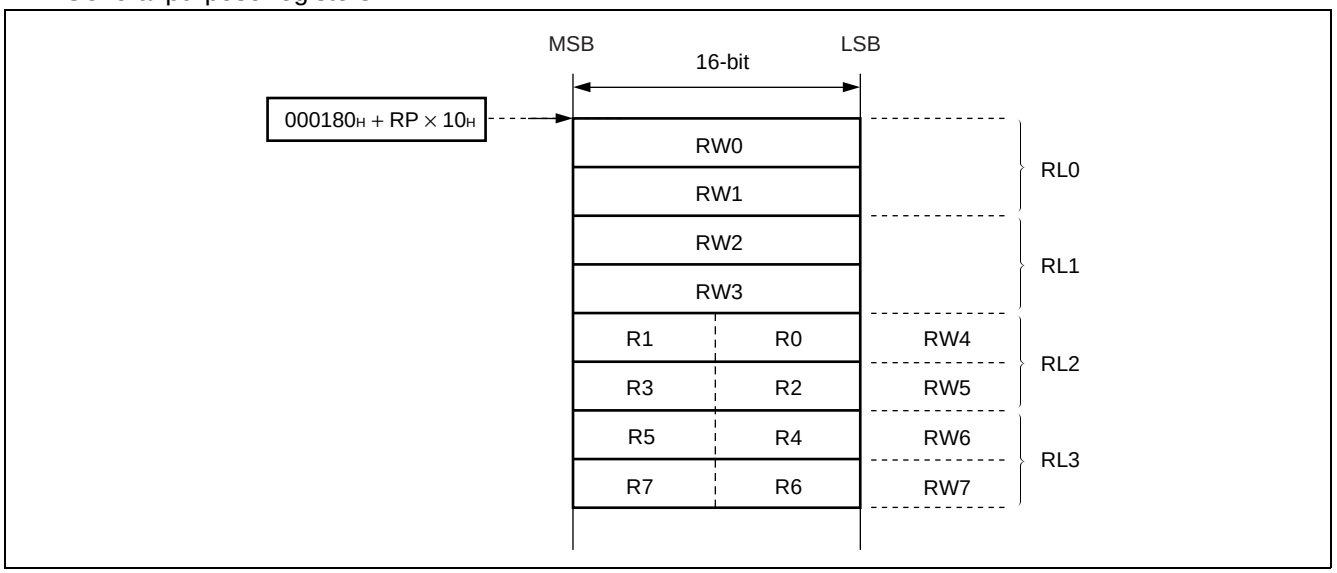
Notes :
- When the ROM mirror function register has been set, the mirror image data at higher addresses (FF4000H to FFFFFFH) of bank FF is visible from the higher addresses (008000H to 00FFFFH) of bank 00.
- The ROM mirror function is for using the C compiler small model.
- The lower 16-bit addresses of bank FF are equivalent to those of bank 00. Note that because the ROM area of bank FF exceeds.
  32 Kbytes, all data in the ROM area cannot be shown in mirror image in bank 00.
- When the C compiler small model is used, the data table can be shown as mirror image at 008000H to 00FFFFH by storing the data table at FF8000H to FFFFFFH . Therefore, data tables in the ROM area can be referenced without declaring the far addressing with the pointer.

■ F²MC-16L CPU Programming model

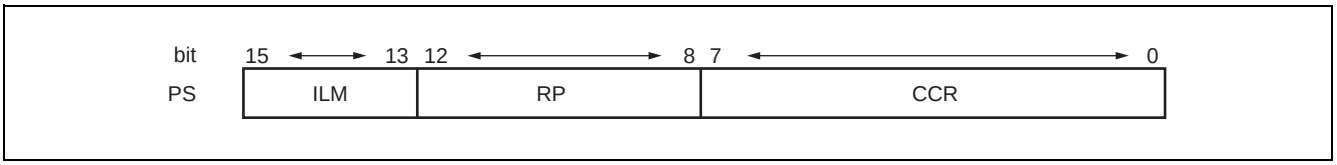
Dedicated Registers



General purpose registers



Processor status



Address	Register abbreviation	Register	Read/ Write	Resource name	Initial Value
000028H	SMR1	Serial mode register	R/W	UART1	0 0 0 0 0 - 0 0B
000029H	SCR1	Serial control register	R/W, W		0 0 0 0 0 1 0 0B
00002AH	SIDR1/ SODR1	Serial input/output register	R/W		XXXXXXXXB
00002BH	SSR1	Serial data register	R/W, R		0 0 0 0 1 0 0 0B
00002CH	Prohibited				
00002DH	CDCR1	Communication prescaler control register	R/W	Prescaler 1	0 0 - - 0 0 0 0B
00002EH	Prohibited				
00002FH					
000030H	ENIR	Interrupt/DTP enable	R/W	External interrupt	- - - - 0 0 0 0B
000031H	EIRR	Interrupt/DTP source	R/W		- - - - XXXXB
000032H	ELVR	Request level set register	R/W		0 0 0 0 0 0 0 0B
000033H	Prohibited				
000034H	ADCS0	Control status register (lower)	R/W	A/D converter	0 0 - - - - - - B
000035H	ADCS1	Control status register (upper)	W, R/W		0 0 0 0 0 0 0 0B
000036H	ADCR0	Data register (lower)	R		XXXXXXXXB
000037H	ADCR1	Data register (upper)	R, W		0 0 1 0 1 - XXB
000038H	Prohibited				
000039H	ADMR	A/D conversion channel set register	R/W	A/D converter	0 0 0 0 0 0 0 0B
00003AH	CPCLR	Compare clear register	R/W	16-bit free-run timer	XXXXXXXXB
00003BH					XXXXXXXXB
00003CH	TCDT	Timer counter data register	R/W		0 0 0 0 0 0 0 0B
00003DH					0 0 0 0 0 0 0 0B
00003EH	TCCSL	Timer counter control/status register (lower)	R/W		0 0 0 0 0 0 0 0B
00003FH	TCCSH	Timer counter control/status register (upper)	R/W		0 - - 0 0 0 0 0B
000040H to 000043H	Prohibited				
000044H	IPCP0	Input capture data register 0	R	Input Capture 0/1	XXXXXXXXB
000045H					XXXXXXXXB
000046H	IPCP1	Input capture data register 1			XXXXXXXXB
000047H					XXXXXXXXB
000048H	ICS01	Control status register	R/W		0 0 0 0 0 0 0 0B
000049H	Prohibited				
00004AH	OCCP0	Compare register 0	R/W	Output compare 0	0 0 0 0 0 0 0 0B
00004BH					0 0 0 0 0 0 0 0B
00004CH	OCCP1	Compare register 1	R/W	Output compare 1	0 0 0 0 0 0 0 0B
00004DH					0 0 0 0 0 0 0 0B

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■ INTERRUPT SOURCES, INTERRUPT VECTORS AND INTERRUPT CONTROL REGISTERS

Interrupt source	EI²OS readiness	Interrupt vector			Interrupt control register		Priority
		Number*		Address	ICR	Address	
Reset	×	#08	08H	FFFFDCH	—	—	High
INT 9 instruction	×	#09	09H	FFFFD8H	—	—	
Exceptional treatment	×	#10	0AH	FFFFD4H	—	—	
DTP/External interrupt ch.0	○	#11	0BH	FFFFD0H	ICR00	0000B0H	
DTP/External interrupt ch.1	○	#13	0DH	FFFFC8H	ICR01	0000B1H	
Serial I/O ch.2	×	#15	0FH	FFFFC0H	ICR02	0000B2H	
DTP/External interrupt ch.2/ch.3	○	#16	10H	FFFFBCH			
Serial I/O ch.3	×	#17	11H	FFFFB8H	ICR03	0000B3H	
16-bit free-run timer	○	#18	12H	FFFFB4H			
Watch timer	×	#19	13H	FFFFB0H	ICR04	0000B4H	
16-bit Reload Timer ch.2	○	#21	15H	FFFFA8H	ICR05	0000B5H	
16-bit Reload Timer ch.0	△	#23	17H	FFFFA0H	ICR06	0000B6H	
16-bit Reload Timer ch.1	△	#24	18H	FFFF9CH			
Input capture ch.0	△	#25	19H	FFFF98H	ICR07	0000B7H	
Input capture ch.1	△	#26	1AH	FFFF94H			
PPG timer ch.0 counter-borrow	○	#27	1BH	FFFF90H	ICR08	0000B8H	
Output compare match	○	#29	1DH	FFFF88H	ICR09	0000B9H	
PPG timer ch.1 counter-borrow	○	#31	1FH	FFFF80H	ICR10	0000BAH	
Time-base timer	×	#33	21H	FFFF78H	ICR11	0000BBH	
UART0 reception end	◎	#35	23H	FFFF70H	ICR12	0000BCH	
UART0 transmission end	△	#36	24H	FFFF6CH			
A/D converter conversion termination	○	#37	25H	FFFF68H	ICR13	0000BDH	
I²C Interface	×	#38	26H	FFFF64H			
UART1 : Reception	◎	#39	27H	FFFF60H	ICR14	0000BEH	
UART1 : Transmission	△	#40	28H	FFFF5CH			
Flash memory status	×	#41	29H	FFFF58H	ICR15	0000BFH	
Delayed interrupt output module	×	#42	2AH	FFFF54H			Low

○ : Available
× : Unavailable
◎ : Available EI²OS function is provided.
△ : Available when a cause of interrupt sharing a same ICR is not used.

* : When interrupts of the same level are output at the same time, the interrupt with the smallest interrupt vector number has the priority.
- For a resource that has two interrupt causes in the same interrupt control register (ICR), use of EI²OS is enabled, EI²OS is started upon detection of one of the interrupt causes. As interrupts other than the start cause are masked during EI²OS start, masking one of the interrupt causes is recommended when using EI²OS.
- For a resource that has two interrupt causes in the same interrupt control register (ICR), the interrupt flag is cleared by an EI²OS interrupt clear signal.

■ PERIPHERAL RESOURCES

1. I/O port

The I/O ports function to output data from the CPU to I/O pins by setting their port data register (PDR) and send signals input to I/O pins to the CPU. In addition, the port can randomly set the direction of the input/output of the port in bit by the port direction register (DDR).

The MB90800 series has 68 (70 ports when the subclock is not used) input/output pins. Port0 to port8 (port0 to port9 when product without the subclock is used) are input/output port.

(1) Port data register

	bit	7	6	5	4	3	2	1	0	Initial Value	Access
PDR0		P07	P06	P05	P04	P03	P02	P01	P00	Indeterminate	R/W*
Address : 000000H											
PDR1	bit	15	14	13	12	11	10	9	8		
Address : 000001H		P17	P16	P15	P14	P13	P12	P11	P10	Indeterminate	R/W*
PDR2	bit	7	6	5	4	3	2	1	0		
Address : 000002H		P27	P26	P25	P24	P23	P22	P21	P20	Indeterminate	R/W*
PDR3	bit	15	14	13	12	11	10	9	8		
Address : 000003H		P37	P36	P35	P34	P33	P32	P31	P30	Indeterminate	R/W*
PDR4	bit	7	6	5	4	3	2	1	0		
Address : 000004H		P47	P46	P45	P44	P43	P42	P41	P40	Indeterminate	R/W*
PDR5	bit	15	14	13	12	11	10	9	8		
Address : 000005H		P57	P56	P55	P54	P53	P52	P51	P50	Indeterminate	R/W*
PDR6	bit	7	6	5	4	3	2	1	0		
Address : 000006H		P67	P66	P65	P64	P63	P62	P61	P60	Indeterminate	R/W*
PDR7	bit	15	14	13	12	11	10	9	8		
Address : 000007H		—	P76	P75	P74	P73	P72	P71	P70	Indeterminate	R/W*
PDR8	bit	7	6	5	4	3	2	1	0		
Address : 000008H		—	—	—	P84	P83	P82	P81	P80	Indeterminate	R/W*
PDR9	bit	15	14	13	12	11	10	9	8		
Address : 000009H		—	—	—	—	—	—	P91	P90	Indeterminate	R/W*

- : Unused

* : R/W access to I/O ports is a bit different in behavior from R/W access to memory as follows

- Input mode
  - When reading : Read the corresponding pin level.
  - When writing : Write into the latch for the output.
- Output mode
  - When reading : Read the value of the data register latch.
  - When writing : Write into the corresponding pin.

(2) Port direction register

	bit	7	6	5	4	3	2	1	0	Initial Value	Access
DDR0 Address : 000010H		D07	D06	D05	D04	D03	D02	D01	D00	00000000B	R/W
DDR1 Address : 000011H	bit	15	14	13	12	11	10	9	8		
		D17	D16	D15	D14	D13	D12	D11	D10	00000000B	R/W
DDR2 Address : 000012H	bit	7	6	5	4	3	2	1	0		
		D27	D26	D25	D24	D23	D22	D21	D20	00000000B	R/W
DDR3 Address : 000013H	bit	15	14	13	12	11	10	9	8		
		D37	D36	D35	D34	D33	D32	D31	D30	00000000B	R/W
DDR4 Address : 000014H	bit	7	6	5	4	3	2	1	0		
		D47	D46	D45	D44	D43	D42	D41	D40	00000000B	R/W
DDR5 Address : 000015H	bit	15	14	13	12	11	10	9	8		
		D57	D56	D55	D54	D53	D52	D51	D50	00000000B	R/W
DDR6 Address : 000016H	bit	7	6	5	4	3	2	1	0		
		D67	D66	D65	D64	D63	D62	D61	D60	00000000B	R/W
DDR7 Address : 000017H	bit	15	14	13	12	11	10	9	8		
		—	D76	D75	D74	D73	D72	D71	D70	- 0000000B	R/W
DDR8 Address : 000018H	bit	7	6	5	4	3	2	1	0		
		—	—	—	D84	D83	D82	D81	D80	- - - 00000B	R/W
DDR9 Address : 000019H	bit	15	14	13	12	11	10	9	8		
		—	—	—	—	—	—	D91	D90	- - - - - - 00B	R/W

- : Unused

When each terminal functions as a port, each correspondent pin are controlled by the port direction register to following;
0 : Input mode
1 : Output mode This bit becomes 0 after a reset.

Note : When accessing this register by using the instruction of the read modify write system (instructions such as bit set) is mode, the bit targeted by an instruction becomes the defined value. However, the content of the output register set to input with the other changes to input value of the pin at that time. Therefore, be sure to write an expected value into PDR firstly, and then set DDR and finally change to the output when changing the input pin to the output pin is made.

(3) Analog Input Enable register

	bit	7	6	5	4	3	2	1	0	Initial Value	Access
ADER0 Address : 00001E$_H$		ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0	11111111$_B$	R/W
ADER1 Address : 00001F$_H$	bit	15	14	13	12	11	10	9	8		
		—	—	—	—	ADE11	ADE10	ADE9	ADE8	- - - -1111$_B$	R/W

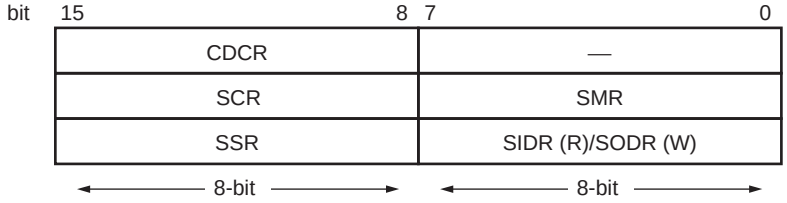
- : Unused

Each pin of port 6 is controlled by the analog input enable register as follow.

0 : Port input/output mode.

1 : Analog input mode.This bit becomes 1 after a reset.

(1) Register list



Serial mode register (SMR0, SMR1)

bit	7	6	5	4	3	2	1	0	Initial Value
Address : 000020H 000028H	MD1	MD0	CS2	CS1	CS0	—	SCKE	SOE	00000 - 00B
	R/W	R/W	R/W	R/W	R/W	—	R/W	R/W	Read/Write

Serial control register(SCR0, SCR1)

bit	15	14	13	12	11	10	9	8	Initial Value
Address : 000021H 000029H	PEN	P	SBL	CL	A/D	REC	RXE	TXE	00000100B
	R/W	R/W	R/W	R/W	R/W	W	R/W	R/W	Read/Write

Serial input/output register (SIDR0, SIDR1/SODR0, SODR1)

bit	7	6	5	4	3	2	1	0	Initial Value
Address : 000022H 00002AH	D7	D6	D5	D4	D3	D2	D1	D0	XXXXXXXXB
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Read/Write

Serial Data Register (SSR0, SSR1)

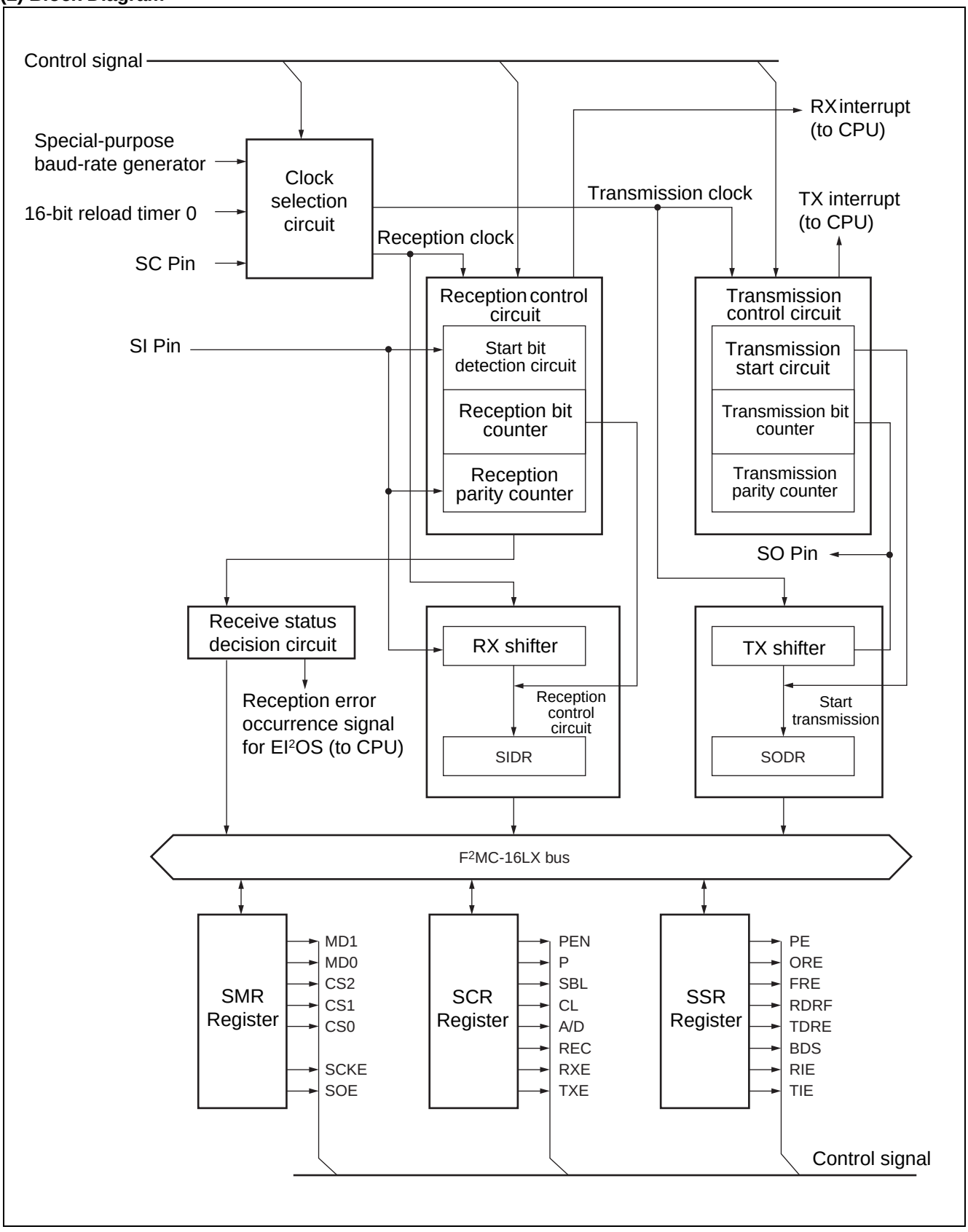
bit	15	14	13	12	11	10	9	8	Initial Value
Address : 000023H 00002BH	PE	ORE	FRE	RDRF	TDRE	BDS	RIE	TIE	00001000B
	R	R	R	R	R	R/W	R/W	R/W	Read/Write

Communication prescaler control register (CDCR0, CDCR1)

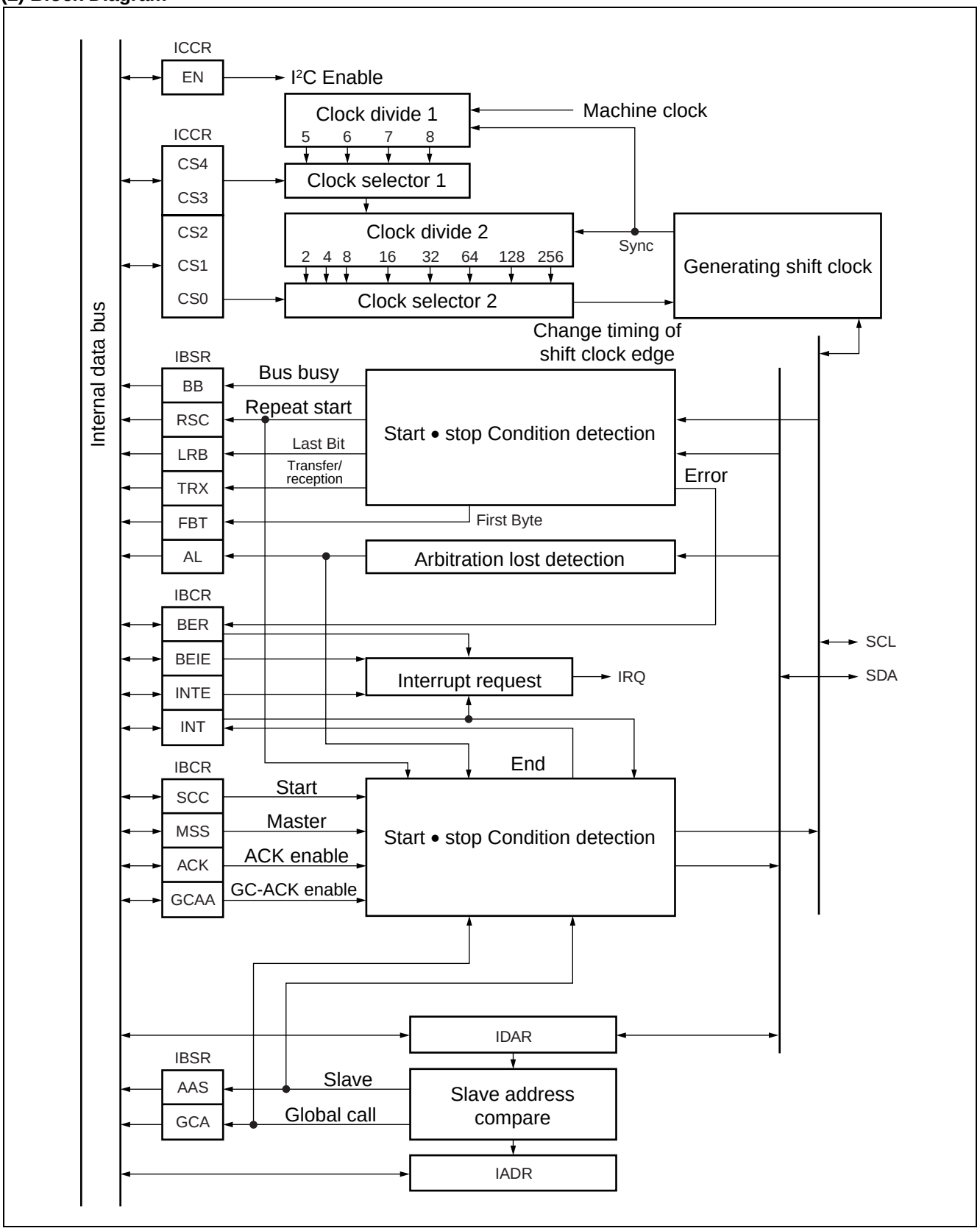
bit	15	14	13	12	11	10	9	8	Initial Value
Address : 000025H 00002DH	MD	URST	—	—	Reserved	DIV2	DIV1	DIV0	00 - - 0000B
	R/W	R/W	—	—	R/W	R/W	R/W	R/W	Read/Write

- : Unused

(2) Block Diagram



(2) Block Diagram



4. Extended I/O serial interface

The extended I/O serial interface is a serial I/O interface that can transfer data through the adoption of 8-bit × 2 channels configured clock synchronization scheme. The extended I/O serial interface also has two alternatives in data transfer called LSB first and MSB first.

The serial I/O interface operates in two modes:

Internal shift clock mode : Transfer data in sync with the internal clock.

External shift clock mode : Transfers data in sync with the clock input through an external pin (SC) . In this mode, transfer operation performed by the CPU instruction is also available by operating the general-use port sharing an external pin (SC) .

(1) Register list

Serial mode control status register (SMCS0, SMCS1)

bit	15	14	13	12	11	10	9	8	Initial Value
Address : 000060H / 000064H	SMD2	SMD1	SMD0	SIE	SIR	BUSY	STOP	STRT	00000010B
	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	Read/Write

bit	7	6	5	4	3	2	1	0	
Address : 000061H / 000065H	—	—	—	—	MODE	BDS	SOE	SCOE	----0000B
	—	—	—	—	R/W	R/W	R/W	R/W	Read/Write

Serial Data Register (SDR0, SDR1)

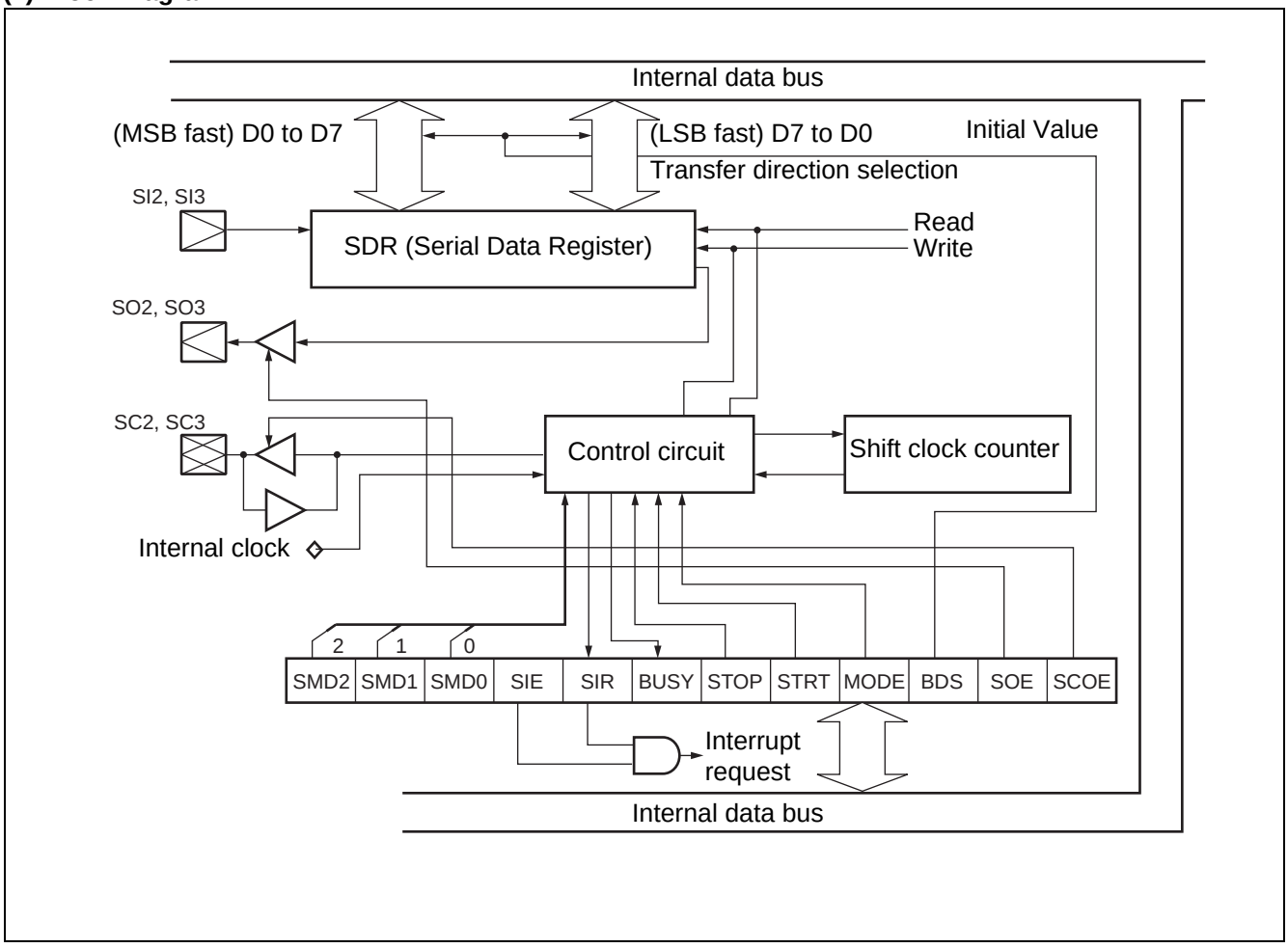
bit	7	6	5	4	3	2	1	0	
Address : 000062H / 000066H	D7	D6	D5	D4	D3	D2	D1	D0	XXXXXXXXB
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Read/Write

Communication Prescaler control register (SDCR0, SDCR1)

bit	15	14	13	12	11	10	9	8	
Address : 000063H / 000067H	MD	—	—	—	Reserved	DIV2	DIV1	DIV0	0---0000B
	R/W	—	—	—	R/W	R/W	R/W	R/W	Read/Write

- : Unused

(2) Block Diagram



5. 8/10-bit A/D converter

The feature of 8/10-bit A/D converter is shown as follows.
conversion time : 3.1 µs minimum per 1 channel

(78 machine cycle/at machine clock 25 MHz/including the sampling time)
Sampling time : 2.0 µs minimum per 1channel

(50 machine cycle/at machine clock 25 MHz)
Uses RC-type successive approximation conversion method with a sample & hold circuit
8-bit resolution or 10-bit resolution can be select.
12 channel program-selectable analog inputs.
Single conversion mode : Convert specified 1 channel
Scan conversion mode : Continuous plural channels (maximum 12 channels can be programmed) are converted.
Continuous conversion mode : Selected channel converted continuously.
Stop conversion time : Perform conversion for one channel, then pause it to wait for the next activation trigger (synchronizes the conversion start timing)
EI^{2}OS can be activated by outputting the interrupt request when the A/D conversion completes.
If the A/D conversion is performed under the condition of the interrupt enable, the converting data will be protected.
Selectable conversion activation trigger : Software, or reload timer (rising edge)

(1) Register list

ADCS1, ADCS0 (Control status register)

ADCS0	bit	7	6	5	4	3	2	1	0	Initial Value
Address : 000034$_H$		MD1	MD0	—	—	—	—	—	—	00 - - - - - - $_B$
		R/W	R/W	—	—	—	—	—	—	Read/Write

ADCS1	bit	15	14	13	12	11	10	9	8	Initial Value
Address : 000035$_H$		BUSY	INT	INTE	PAUS	STS1	STS0	STRT	Reserved	00000000$_B$
		R/W	R/W	R/W	R/W	R/W	R/W	W	R/W	Read/Write

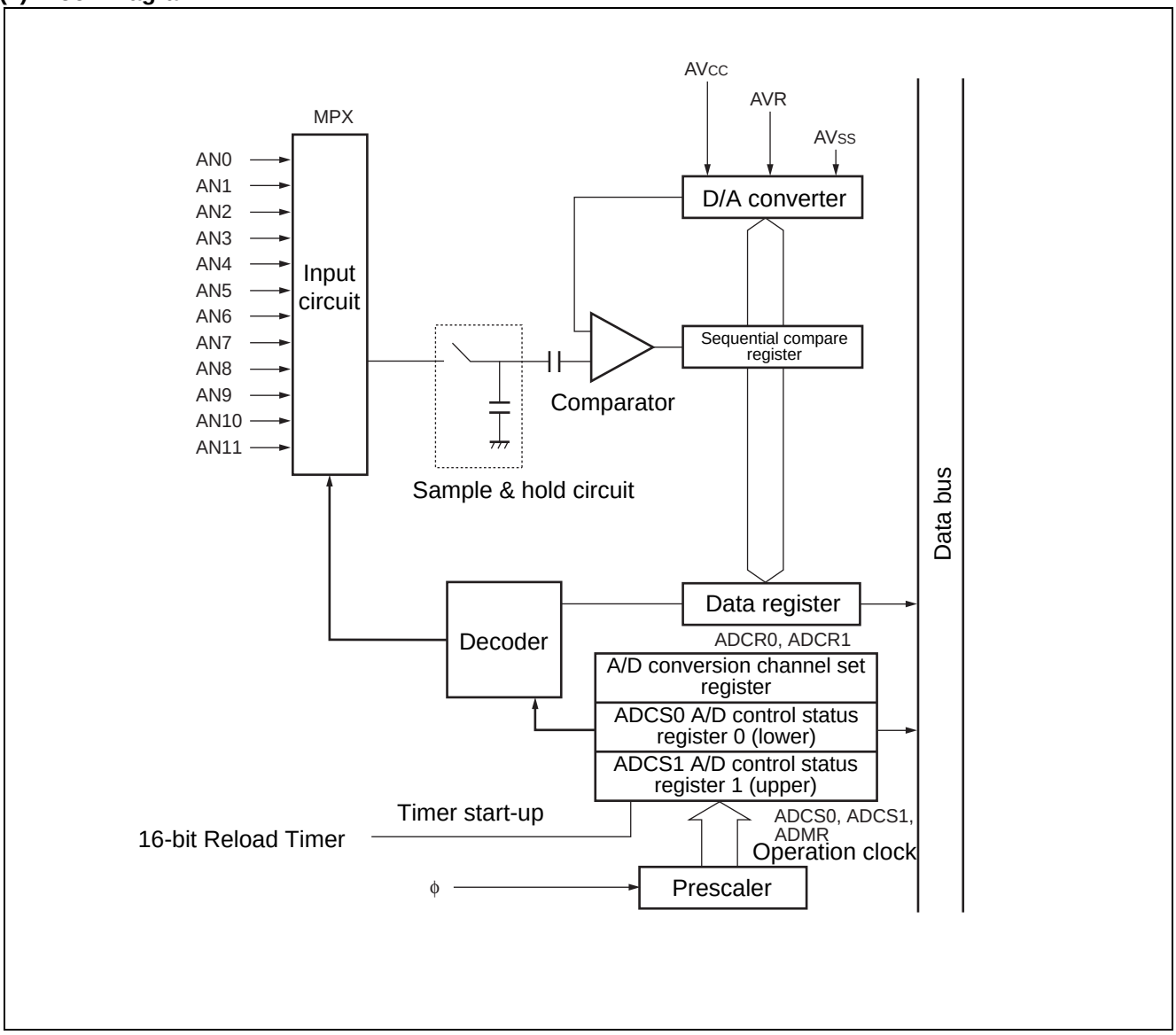
ADCR1, ADCR0 (Data register)

ADCR0	bit	7	6	5	4	3	2	1	0	Initial Value
Address : 000036$_H$		D7	D6	D5	D4	D3	D2	D1	D0	XXXXXXXX$_B$
		R	R	R	R	R	R	R	R	Read/Write

ADCR1	bit	15	14	13	12	11	10	9	8	Initial Value
Address : 000037$_H$		S10	ST1	ST0	CT1	CT0	—	D9	D8	00101 - XX$_B$
		W	W	W	W	W	—	R	R	Read/Write

- : Unused

(2) Block Diagram



6. 16 bits PPG

The PPG timer consists of the following:

- Prescaler
- 16-bit down-counter: 1
- 16-bit data register with a cycle setting buffer
- 16-bit compare register with a duty setting buffer
- Pin control unit

The PPG timer can output pulses synchronized to the software trigger.

The output pulse can be changed to any cycle and duty freely by updating the PCSRL, PCSRH/PDUTL, PDUTH registers.

PWM function

The PPG timer can output pulses programmably by updating the PCSR and PDUT registers described above in synchronization to the trigger.

Can also be used as a D/A converter by an external circuit.

Single shot function

By detecting an edge of the trigger input, a single pulse can be output.

16-bit down counter

The counter operation clock comes from eight kinds optional. There are eight kinds of internal clocks.

(ϕ, ϕ2, ϕ4, ϕ8, ϕ16, ϕ32, ϕ64, ϕ128) ϕ : machine clock

The counter can be initialized to $FFFF_H$ at a reset or counter borrow.

Interrupt request

The PPG timer generates an interrupt request when :

- Timer start-up
- Counter borrow occurrence (cycle match)
- Duty match occurrence

(1) Register list

PCNTH (PCNTH0/PCNTH1 PPG Control Status register)

	bit	15	14	13	12	11	10	9	8	Initial Value
000077H 00007FH		CNTE	STGR	MDSE	RTRG	CKS2	CKS1	CKS0	PGMS	0000000-B
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Read/Write

PCNTL (PCNTL0/PCNTL1 PPG Control Status register)

	bit	7	6	5	4	3	2	1	0	Initial Value
000076H 00007EH		—	—	IREN	IRQF	IRS1	IRS0	POEN	OSEL	- - 000000B
		—	—	R/W	R/W	R/W	R/W	R/W	R/W	Read/Write

PDCRH (PDCRH0/PDCRH1 PPG Down Counter Register)

	bit	15	14	13	12	11	10	9	8	Initial Value
000071H 000079H		DC15	DC14	DC13	DC12	DC11	DC10	DC09	DC08	11111111B
		R	R	R	R	R	R	R	R	Read/Write

PDCRL (PDCRL0/PDCRL1 PPG Down Counter Register)

	bit	7	6	5	4	3	2	1	0	Initial Value
000070H 000078H		DC07	DC06	DC05	DC04	DC03	DC02	DC01	DC00	11111111B
		R	R	R	R	R	R	R	R	Read/Write

PCSRH (PCSRH0/PCSRH1 PPG cycle set register)

	bit	15	14	13	12	11	10	9	8	Initial Value
000073H 00007BH		CS15	CS14	CS13	CS12	CS11	CS10	CS09	CS08	XXXXXXXXB
		W	W	W	W	W	W	W	W	Read/Write

PCSRL (PCSRL0/PCSRL1 PPG cycle set register)

	bit	7	6	5	4	3	2	1	0	Initial Value
000072H 00007AH		CS07	CS06	CS05	CS04	CS03	CS02	CS01	CS00	XXXXXXXXB
		W	W	W	W	W	W	W	W	Read/Write

PDUTH (PDUTH0/PDUTH1 PPG duty set register)

	bit	15	14	13	12	11	10	9	8	Initial Value
000075H 00007DH		DU15	DU14	DU13	DU12	DU11	DU10	DU09	DU08	XXXXXXXXB
		W	W	W	W	W	W	W	W	Read/Write

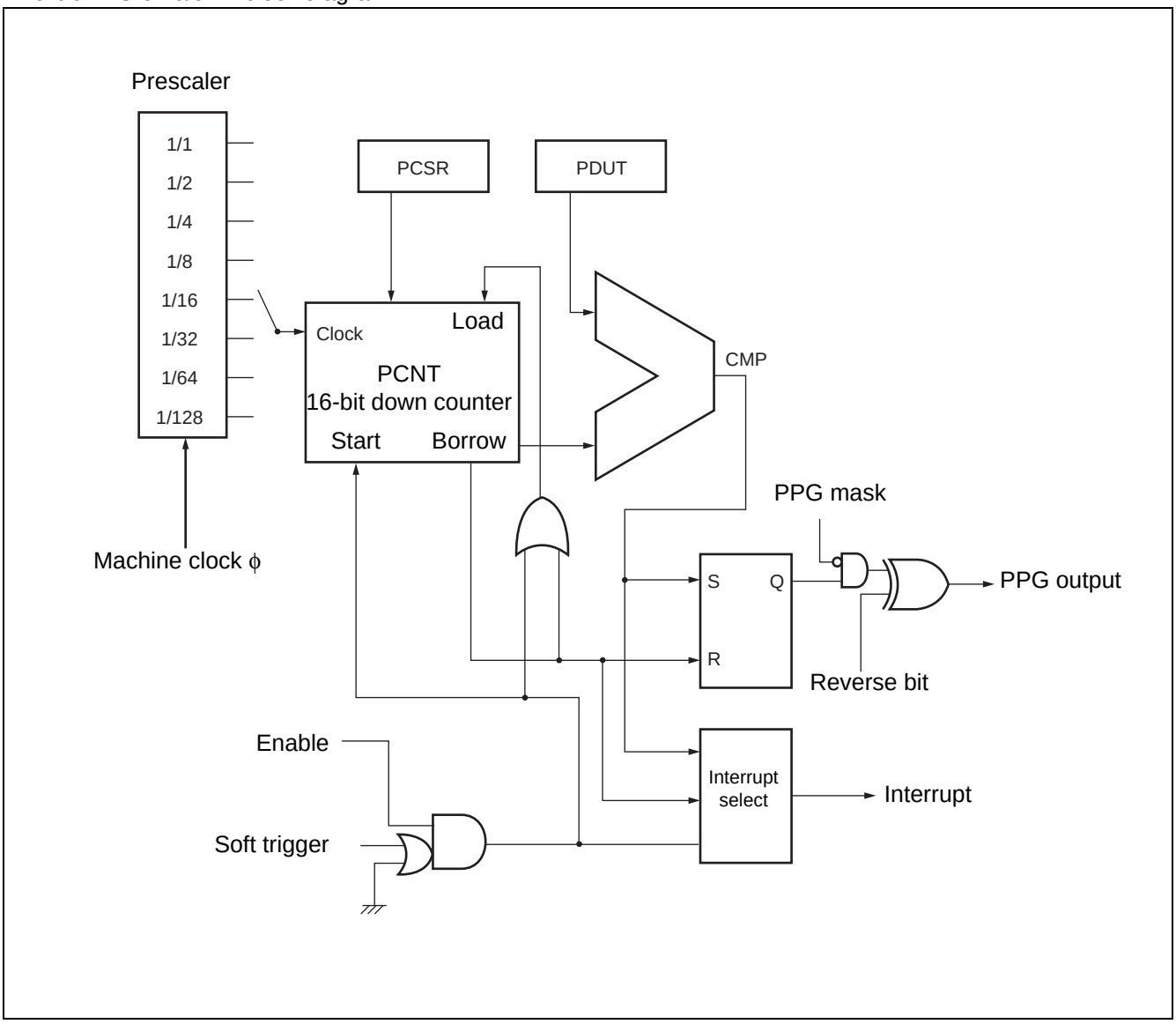
PDUTL (PDUTL0/PDUTL1 PPG duty set register)

	bit	7	6	5	4	3	2	1	0	Initial Value
000074H 00007CH		DU07	DU06	DU05	DU04	DU03	DU02	DU01	DU00	XXXXXXXXB
		W	W	W	W	W	W	W	W	Read/Write

- : Unused

(2) Block Diagram

• 16-bit PPG ch.0/ch.1 block diagram



7. Delay interrupt generator module

The delayed interrupt generation module outputs an interrupt request for task switching. The hardware interrupt request can be generated by software.

(1) Register list

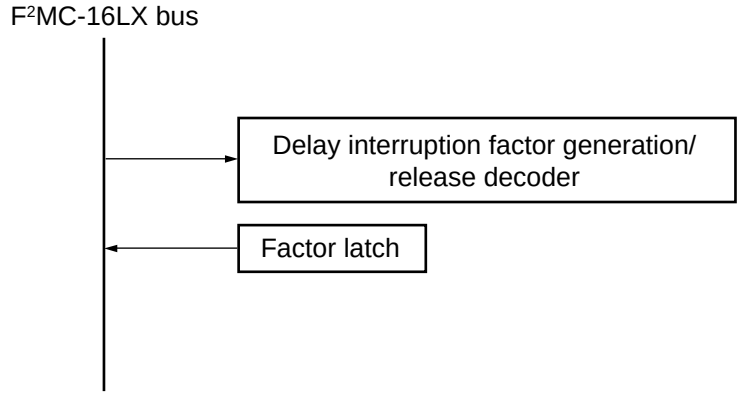
Delayed Interrupt/release register(DIRR)

DIRR Address : 00009F$_H$

bit	15	14	13	12	11	10	9	8	Initial Value
	—	—	—	—	—	—	—	R0	- - - - - - - 0$_B$
	—	—	—	—	—	—	—	R/W	Read/Write

- : Unused

(2) Block diagram



8. DTP/External interrupt

DTP (Data Transfer Peripheral)/External interrupt circuit detects the interrupt request input from the external interrupt input terminal, and outputs the interrupt request.

(1) Register list

Interrupt/DTP enable register (ENIR)

ENIR bit

Address : 000030H

bit	7	6	5	4	3	2	1	0
	—	—	—	—	EN3	EN2	EN1	EN0
	—	—	—	—	R/W	R/W	R/W	R/W

Initial Value: - - - - 0000B

Read/Write

Interrupt/DTP source register (EIRR)

EIRR bit

Address : 000031H

bit	15	14	13	12	11	10	9	8
	—	—	—	—	ER3	ER2	ER1	ER0
	—	—	—	—	R/W	R/W	R/W	R/W

Initial Value: - - - - XXXXB

Read/Write

Request level setting register (ELVR)

ELVR bit

Address : 000032H

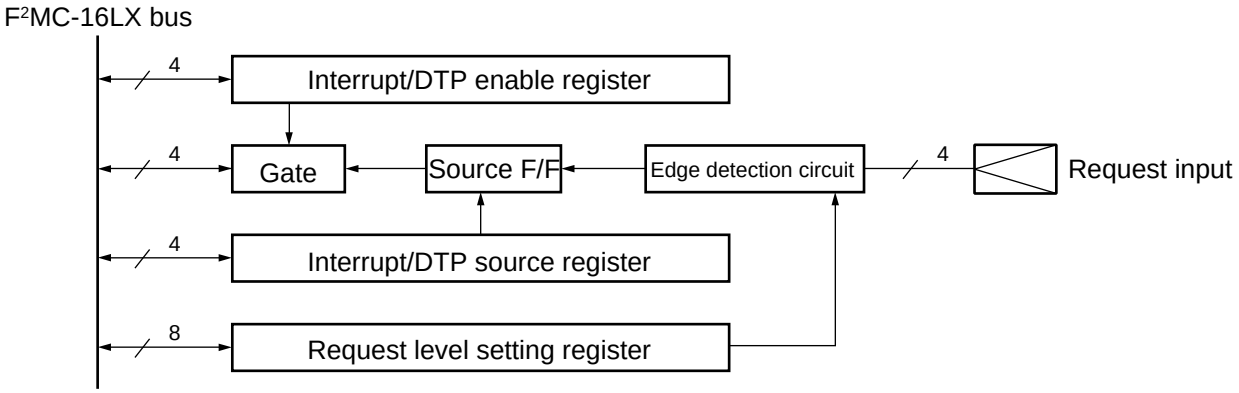
bit	7	6	5	4	3	2	1	0
	LB3	LA3	LB2	LA2	LB1	LA1	LB0	LA0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial Value: 00000000B

Read/Write

- : Unused

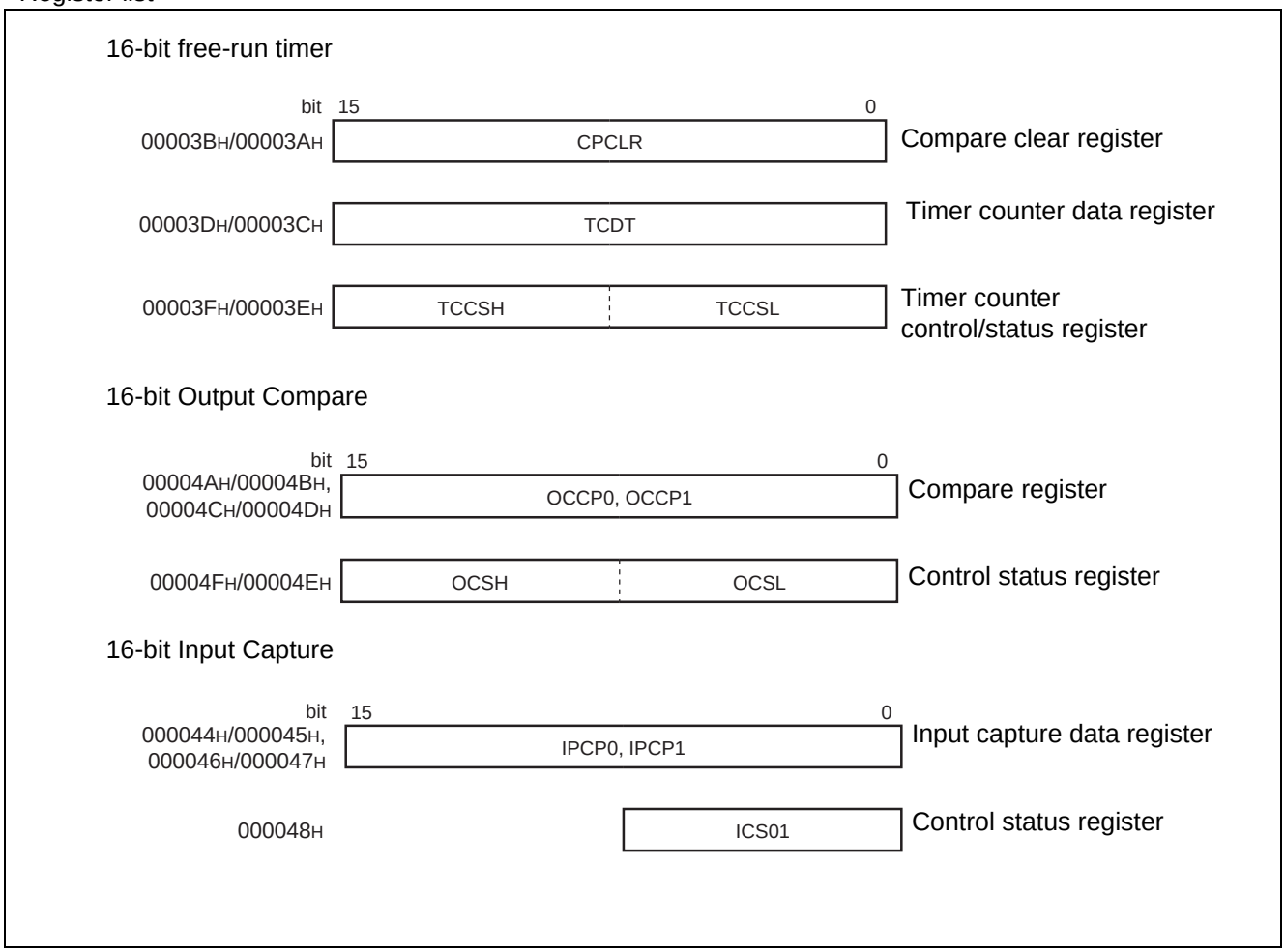
(2) Block diagram



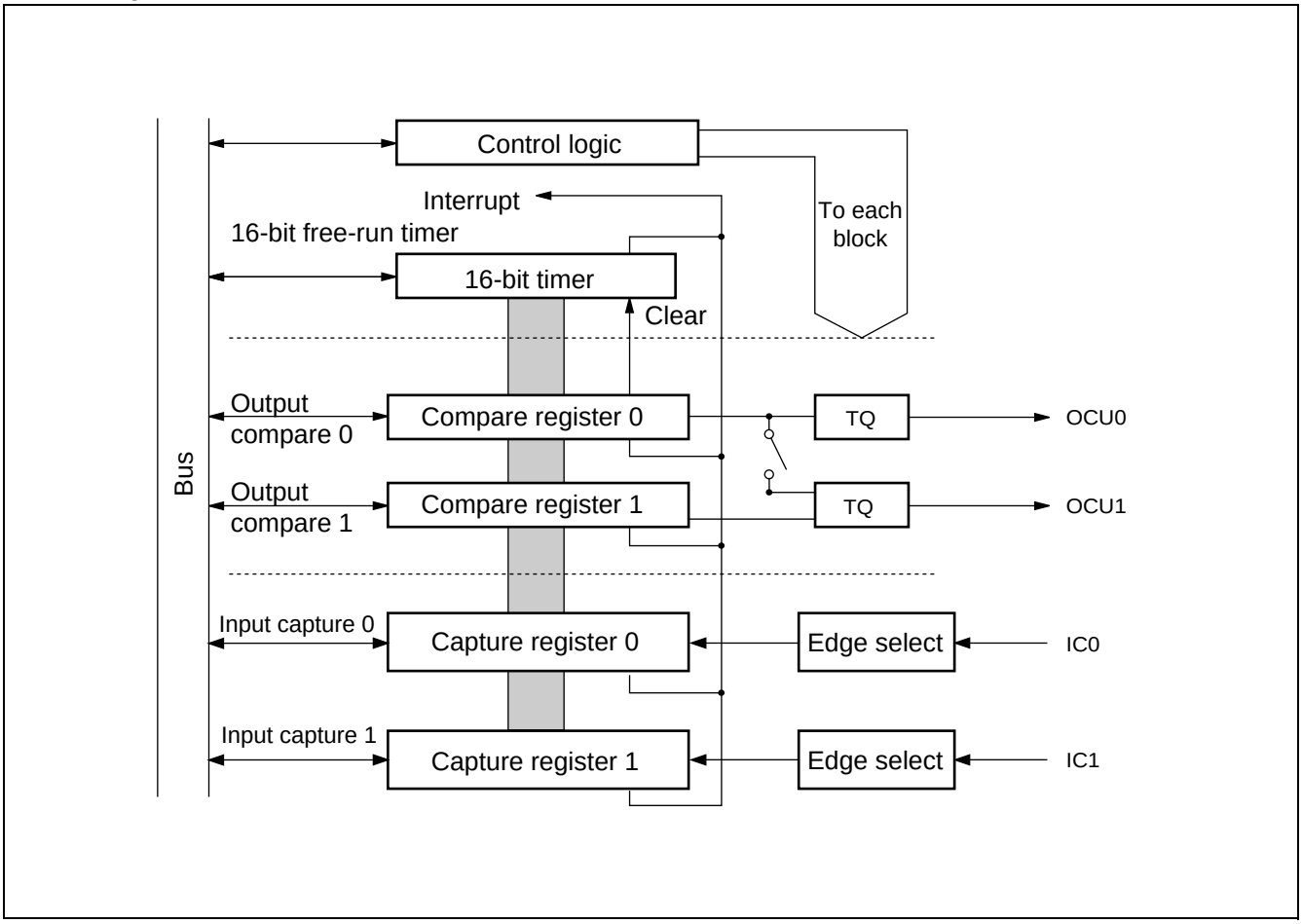
9. 16-bit input/output timer

The 16-bit I/O timer consists of one 16-bit free-run timer, two output compare and two input capture. This function enables six independent waveforms to be output based on the 16-bit free-run timer, and input pulse widths and external clock frequencies to be measured.

• Register list



• Block diagram



(1) 16-bit free-run timer

The 16-bit free-run timer consists of a 16-bit up-down counter and control status register.

Counter value of 16-bit free-run timer is available as base timer for input capture and output compare.
Clock for the counter operation can be selected from eight types.
The counter overflow interruption can be generated.
Setting the mode enables initialization of the counter through compare-match operation with the value of the compare clear register in the output compare and that of the free-run timer counter.

• Register list

Compare clear register (CPCLR)

bit	15	14	13	12	11	10	9	8	Initial Value
00003B$_H$	CL15	CL14	CL13	CL12	CL11	CL10	CL09	CL08	XXXXXXXX$_B$
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Read/Write

bit	7	6	5	4	3	2	1	0	Initial Value
00003A$_H$	CL07	CL06	CL05	CL04	CL03	CL02	CL01	CL00	XXXXXXXX$_B$
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Read/Write

Timer counter data register (TCDT)

bit	15	14	13	12	11	10	9	8	Initial Value
00003D$_H$	T15	T14	T13	T12	T11	T10	T09	T08	00000000$_B$
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Read/Write

bit	7	6	5	4	3	2	1	0	Initial Value
00003C$_H$	T07	T06	T05	T04	T03	T02	T01	T00	00000000$_B$
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Read/Write

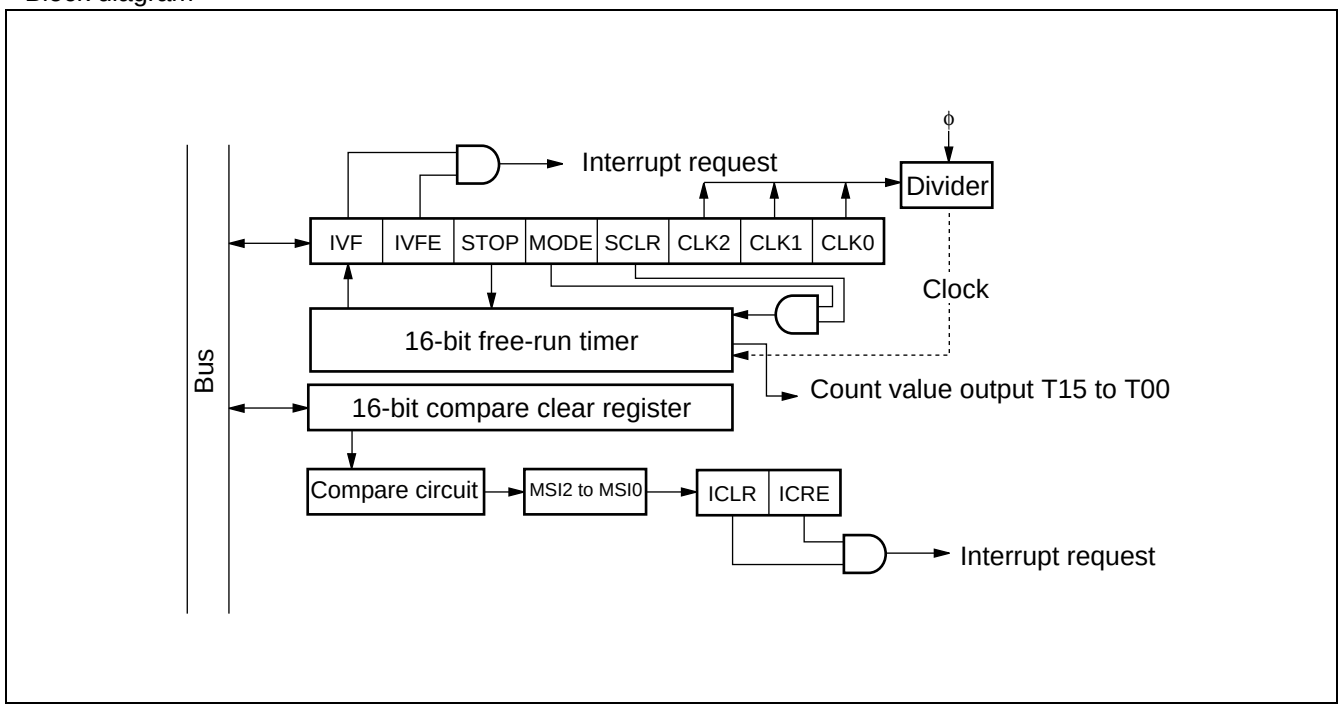
Timer counter control/status register (TCCS)

bit	15	14	13	12	11	10	9	8	Initial Value
00003F$_H$	ECKE	—	—	MSI2	MSI1	MSI0	ICLR	ICRE	0--00000$_B$
	R/W	—	—	R/W	R/W	R/W	R/W	R/W	Read/Write

bit	7	6	5	4	3	2	1	0	Initial Value
00003E$_H$	IVF	IVFE	STOP	MODE	SCLR	CLK2	CLK1	CLK0	00000000$_B$
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Read/Write

- : Unused

• Block diagram



(2) Output compare

The output compare consists of 16-bit compare registers, compare output pin part and a control register. It can reverse the output level for the pin and at the same time, generate an interrupt when the 16-bit free-run timer value matches a value set in one of the 16-bit compare registers of this module.

It has a total of six compare registers that can operate independently. In addition, the output can be set to be controlled by using two compare registers.

An interrupt can be set by a comparing match.

• Register list

Compare register (OCCP0, OCCP1)

bit	15	14	13	12	11	10	9	8	Initial Value
00004B$_H$ 00004D$_H$	OP15	OP14	OP13	OP12	OP11	OP10	OP09	OP08	00000000$_B$
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Read/Write

bit	7	6	5	4	3	2	1	0	Initial Value
00004A$_H$ 00004C$_H$	OP07	OP06	OP05	OP04	OP03	OP02	OP01	C00	00000000$_B$
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Read/Write

Control register (OCSH)

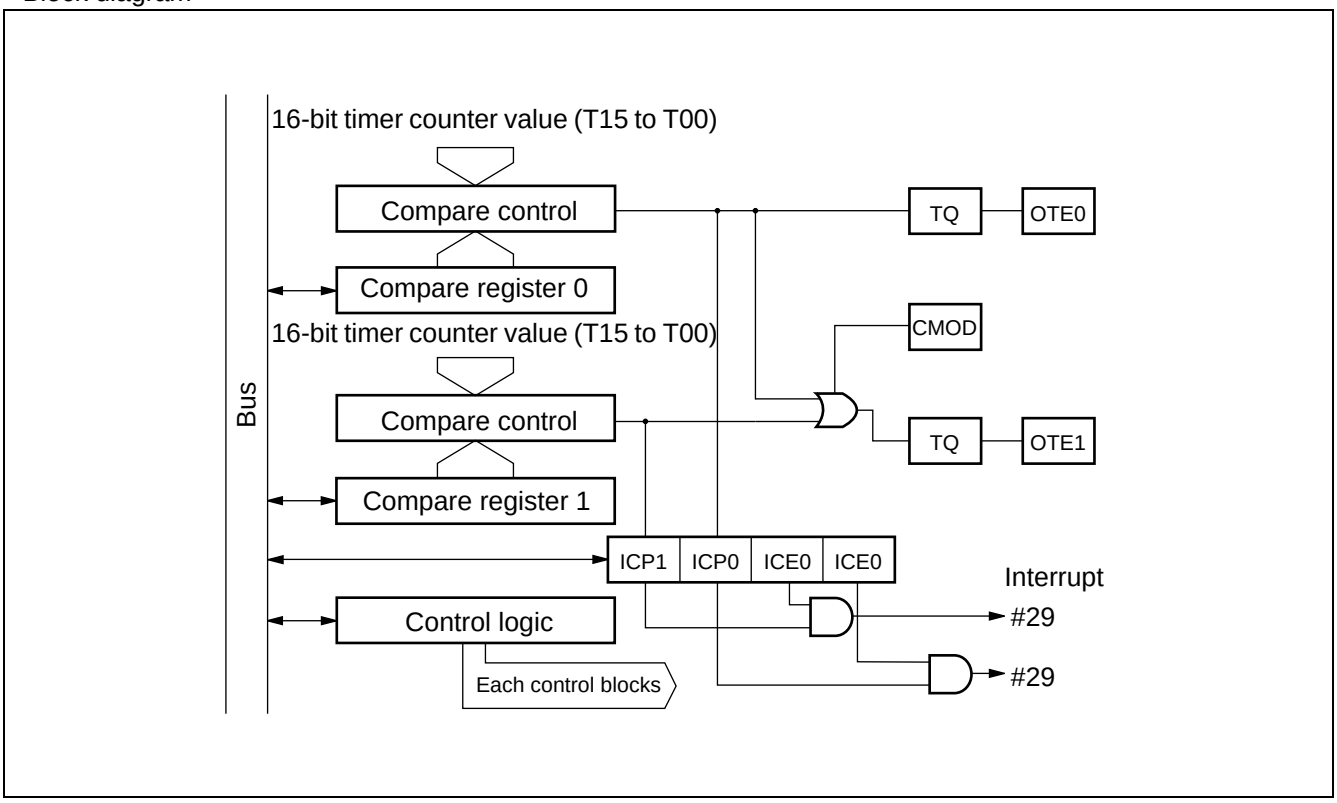
bit	15	14	13	12	11	10	9	8	Initial Value
00004F$_H$	—	—	—	CMOD	OTE1	OTE0	OTD1	OTD0	---00000$_B$
	—	—	—	R/W	R/W	R/W	R/W	R/W	Read/Write

Control register (OCSL)

bit	7	6	5	4	3	2	1	0	Initial Value
00004E$_H$	IOP1	IOP0	IOE1	IOE0	—	—	CST1	CST0	0000--00$_B$
	R/W	R/W	R/W	R/W	—	—	R/W	R/W	Read/Write

- : Unused

• Block diagram



(3) Input capture

The input capture consists of input capture and control registers. Each input capture has its corresponding external input pin.

This module has a function that detects a rising edge, falling edge or both edges and holds a value of the 16-bit free-run timer in a register at the time of detection. It can also generate an interrupt when detecting an edge.

The detection edge of an external input can be selected from among three types. Rising edge/falling edge/ both edges.

It can generate an interrupt when it detects the valid edge of the external input.

• Register list

Input capture data register (IPCP0, IPCP1)

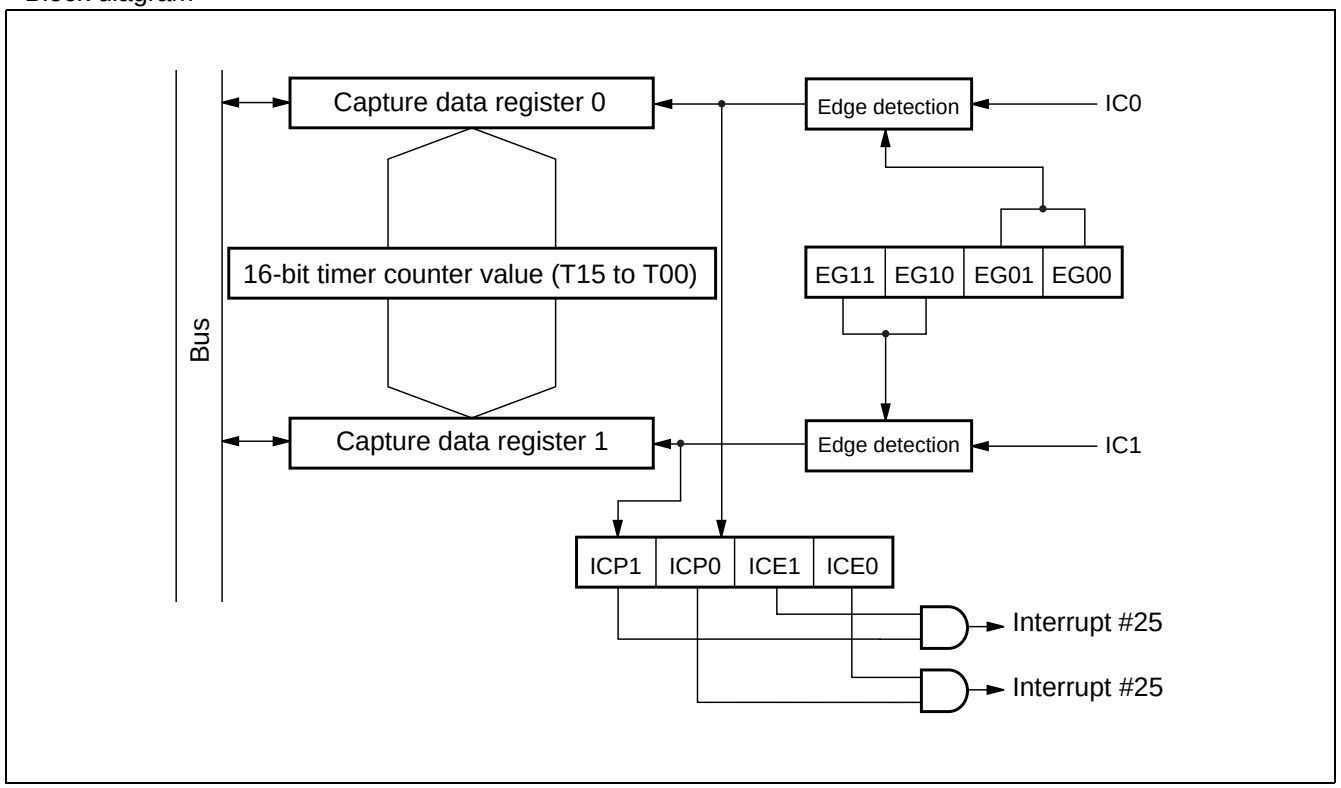
	bit	15	14	13	12	11	10	9	8	
000045H 000047H		CP15	CP14	CP13	CP12	CP11	CP10	CP09	CP08	Initial Value XXXXXXXXB
		R	R	R	R	R	R	R	R	Read/Write

	bit	7	6	5	4	3	2	1	0	
000044H 000046H		CP07	CP06	CP05	CP04	CP03	CP02	CP01	CP00	Initial Value XXXXXXXXB
		R	R	R	R	R	R	R	R	Read/Write

Control status register (ICS01)

	bit	7	6	5	4	3	2	1	0	
000048H		ICP1	ICP0	ICE1	ICE0	EG11	EG10	EG01	EG00	Initial Value 00000000B
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Read/Write

• Block diagram



10. 16-bit reload timer

The 16-bit reload timer provides two functions either one which can be selected, the internal clock mode that performs the count down by synchronizing with 3-type internal clocks and the event count mode that performs the count down by detecting the arbitration. This timer defines an underflow as a transition of the count value from 0000_H to $FFFF_H$. Therefore, when the equation (counted value = reload register setting value+1) holds, an underflow occurs. Either mode can be selected for the count operation from the reload mode which repeats the count by reloading the count setting value at the underflow occurrence or the one-shot mode which stops the count at the underflow occurrence. The interrupt can be generated at the counter underflow occurrence so as to correspond to the DTC.

(1) Register list

• TMCSR Timer control status register

Timer control status register (upper) (TMCSR0H to TMCSR2H)

bit	15	14	13	12	11	10	9	8	Initial Value
000051_H / 000055_H / 000059_H	—	—	—	—	CSL1	CSL0	MOD2	MOD1	- - - - 0000_B
	—	—	—	—	R/W	R/W	R/W	R/W	Read/Write

Timer control status register (lower) (TMCSR0L to TMCSR2L)

bit	7	6	5	4	3	2	1	0	Initial Value
000050_H / 000054_H / 000058_H	MOD0	OUTE	OUTL	RELD	INTE	UF	CNTE	TRG	00000000_B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Read/Write

• 16-bit timer register/16-bit reload register TMR0 to TMR2/TMRLR0 to TMRLR2 (upper)

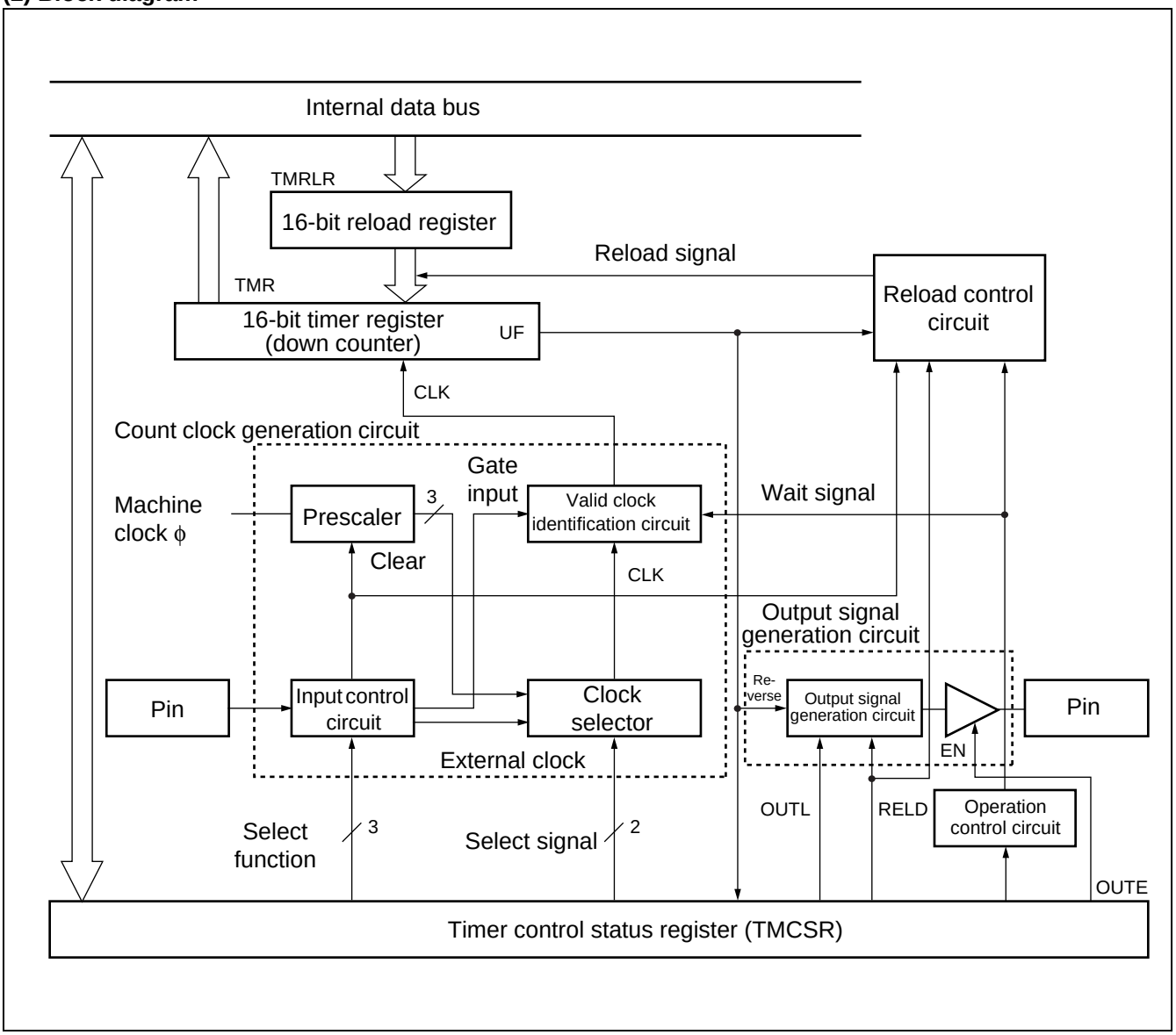
bit	15	14	13	12	11	10	9	8	Initial Value
000053_H / 000057_H / $00005B_H$	D15	D14	D13	D12	D11	D10	D9	D8	$XXXXXXXX_B$
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Read/Write

TMR0 to TMR2/TMRLR0 to TMRLR2 (lower)

bit	7	6	5	4	3	2	1	0	Initial Value
000052_H / 000056_H / $00005A_H$	D7	D6	D5	D4	D3	D2	D1	D0	$XXXXXXXX_B$
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Read/Write

- : Unused

(2) Block diagram



11. Watch timer

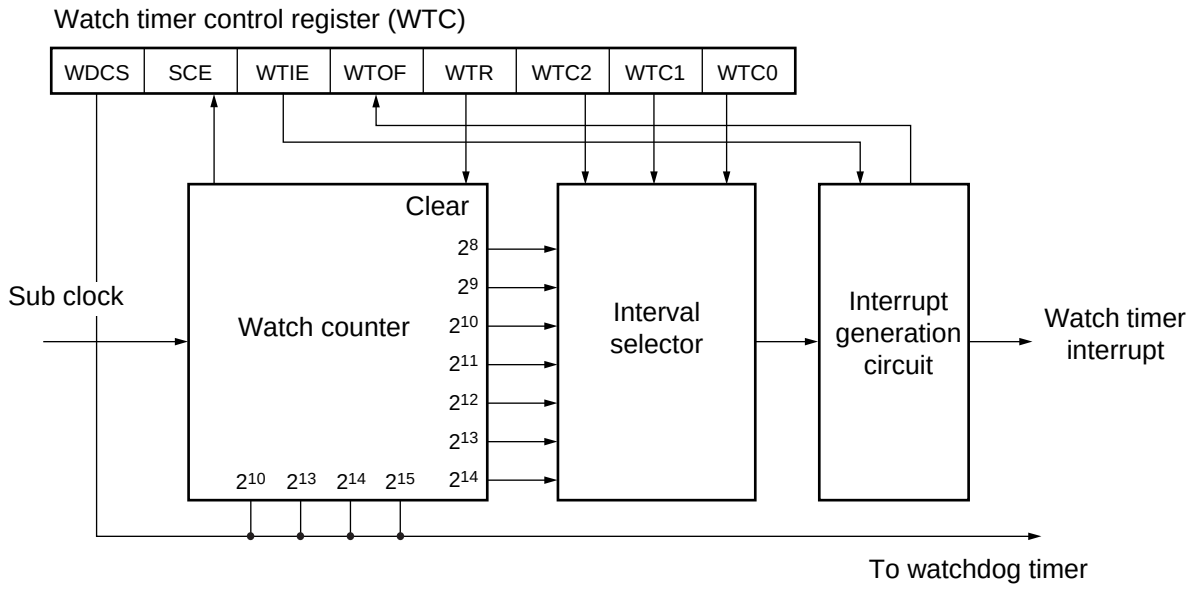
The watch timer is a 15-bit timer using the subclock. It can generate the interrupt request for each interval time. The watch timer can also be used as the clock source of the watchdog timer by setting so.

(1) Register list

Watch timer control register (WTC)

bit	7	6	5	4	3	2	1	0	Initial Value
0000AA$_H$	WDCS	SCE	WTIE	WTOF	WTR	WTC2	WTC1	WTC0	1X011000$_B$
	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	Read/Write

(2) Block diagram



12. Watchdog timer

The watchdog timer is a timer counter provided for preventing program malfunction. The watchdog timer is a 2-bit counter operating with an output of the timebase timer or watch timer as count clock and resets the CPU when the counter is not cleared within the interval time.

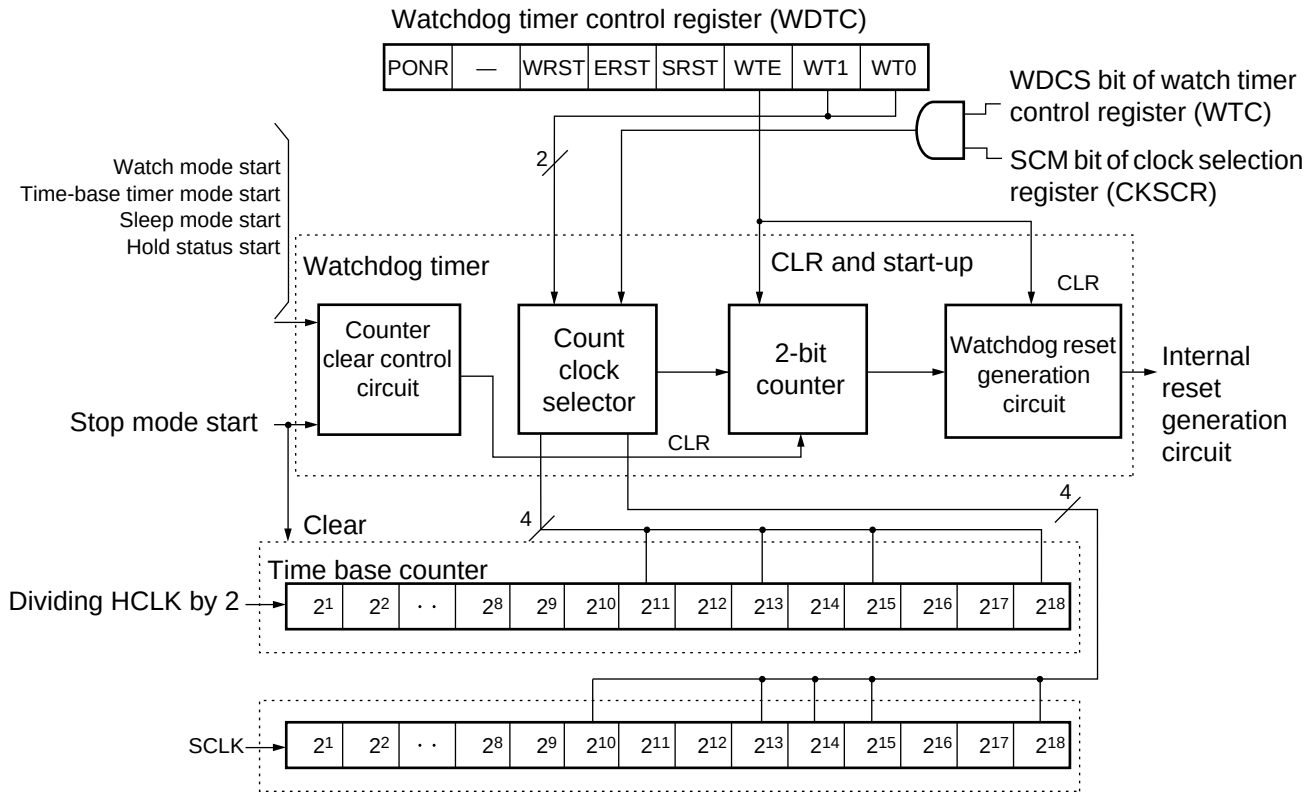
(1) Register list

Watchdog timer control register (WDTC)

bit	7	6	5	4	3	2	1	0	Initial Value
0000A8H	PONR		WRST	ERST	SRST	WTE	WT1	WT0	XXXXX111B
	R		R	R	R	W	W	W	Read/Write

– : Unused

(2) Block diagram



HCLK: Oscillation clock
SCLK: Sub clock

13. Time-base timer

The time-base timer has a function that enables a selection of four interval times using 18-bit free-run counter (time-base counter) with synchronizing to the internal count clock (two division of original oscillation). Furthermore, the function of timer output of oscillation stabilization wait or function supplying operation clocks for watchdog timer are provided.

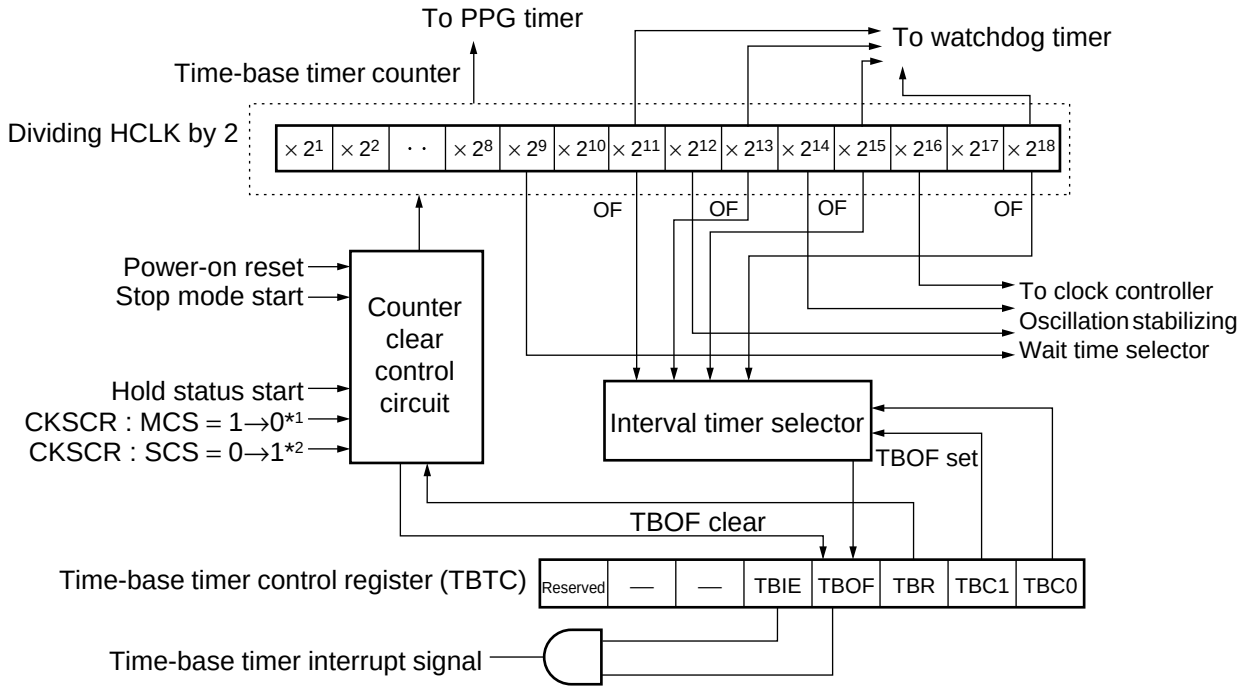
(1) Register list

Time-base timer control register (TBTC)

bit	15	14	13	12	11	10	9	8	Initial Value
0000A9H	Reserved	—	—	TBIE	TBOF	TBR	TBC1	TBC0	1 - - 00100B
	R/W	—	—	R/W	R/W	W	R/W	R/W	Read/Write

- : Unused

(2) Block diagram



— : Unused
OF : Overflow
HCLK : Oscillation clock
*1 : The machine clock is switched from main/sub clock to PLL clock.
*2 : The machine clock is switched from sub clock to main clock.

14. Clock generator

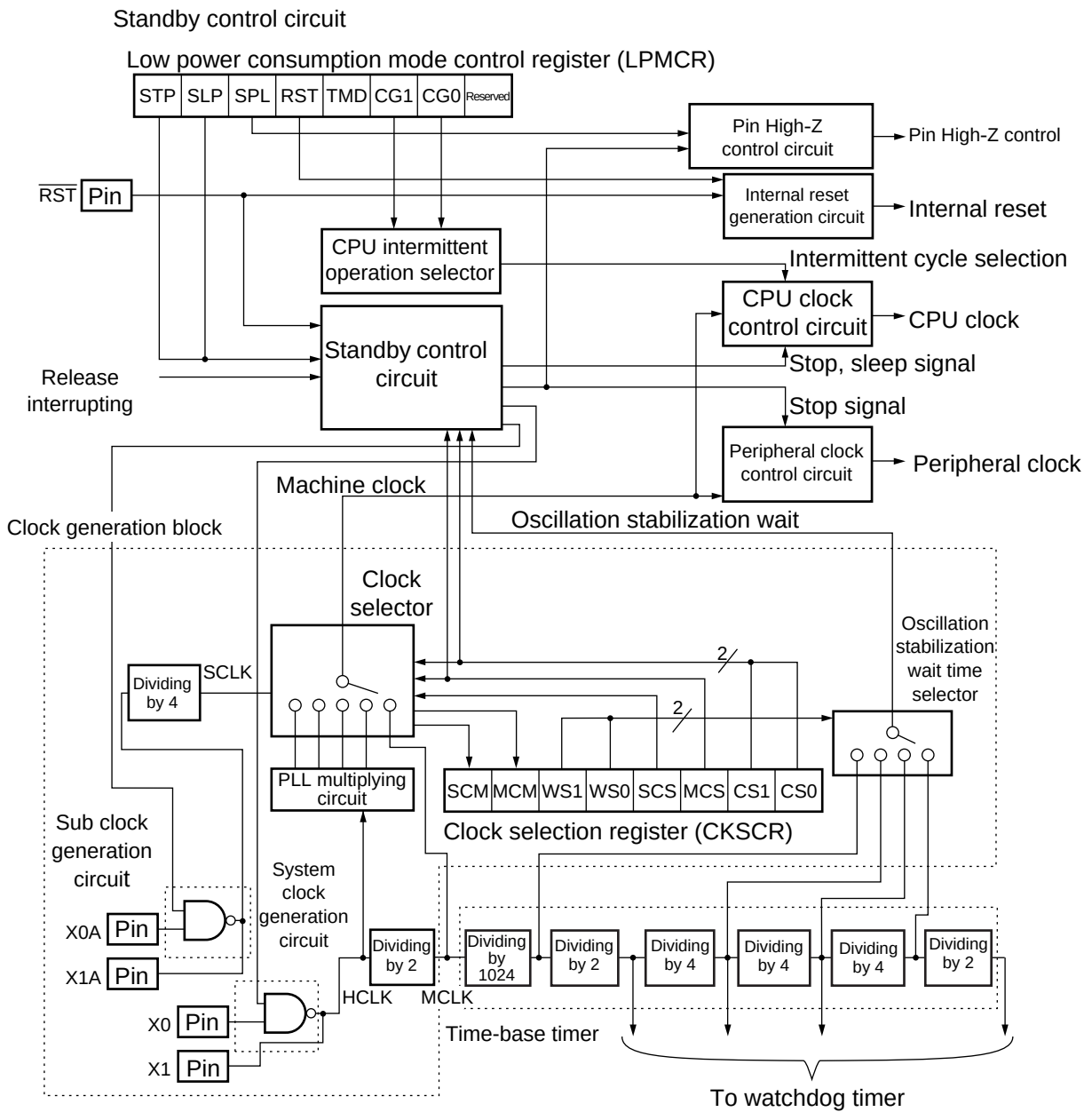
The clock generator controls operation of the internal clock which is the operation clock for the CPU and peripheral devices. This internal clock is used as machine clock and its one cycle as machine cycle. In addition, the clock generated by original oscillation is used as oscillation clock and that by internal PLL oscillation as PLL clock.

(1) Register list

Clock selection register (CKSCR)

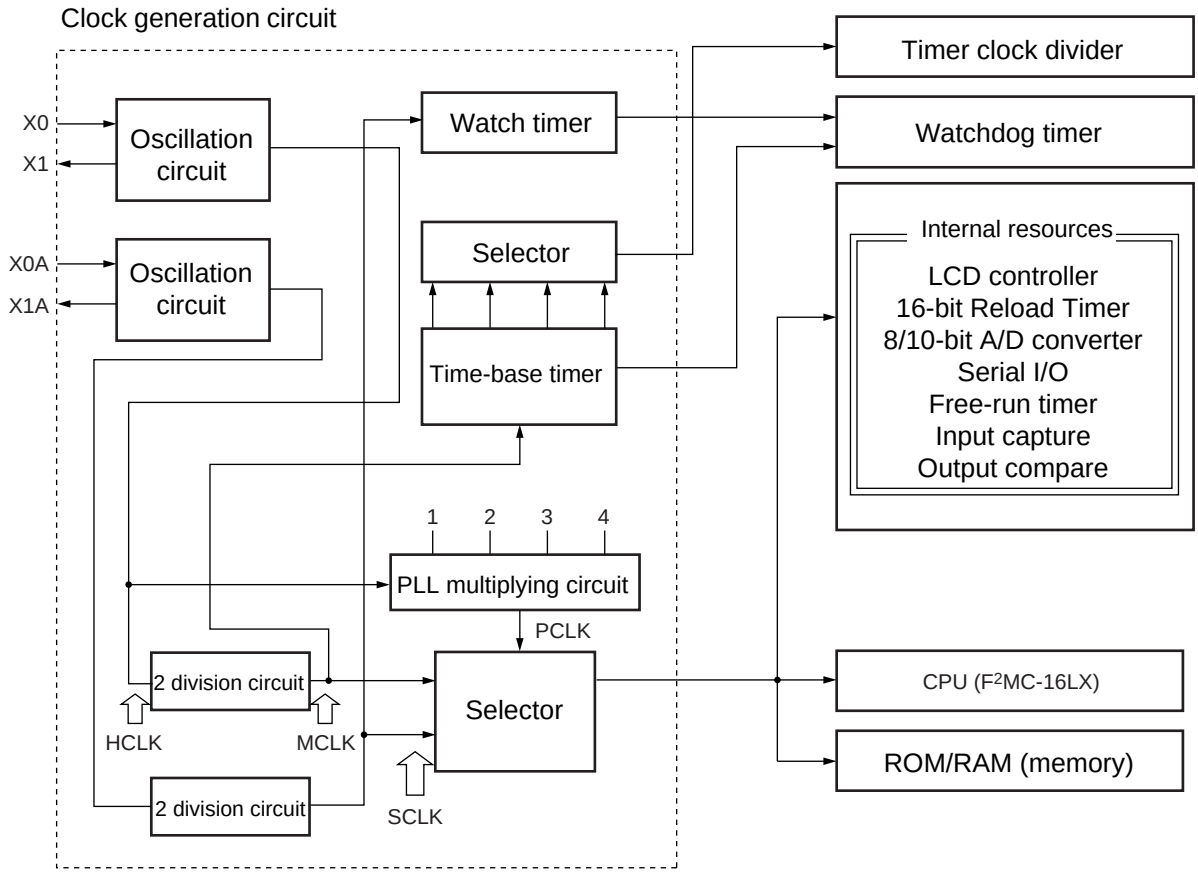
bit	15	14	13	12	11	10	9	8	Initial Value
0000A1H	SCM	MCM	WS1	WS0	SCS	MCS	CS1	CS0	11111100B
	R	R	R/W	R/W	R/W	R/W	R/W	R/W	Read/Write

(2) Block diagram



HCLK : Oscillation clock
MCLK : Main clock
SCLK : Sub clock

(3) Clock supply map



HCLK : Oscillation clock
MCLK : Main clock
PCLK : PLL clock
SCLK : Sub clock

15. Low power consumption mode

The low-power consumption mode has the following CPU operation modes by selecting the operation clock and operating the control of the clock.

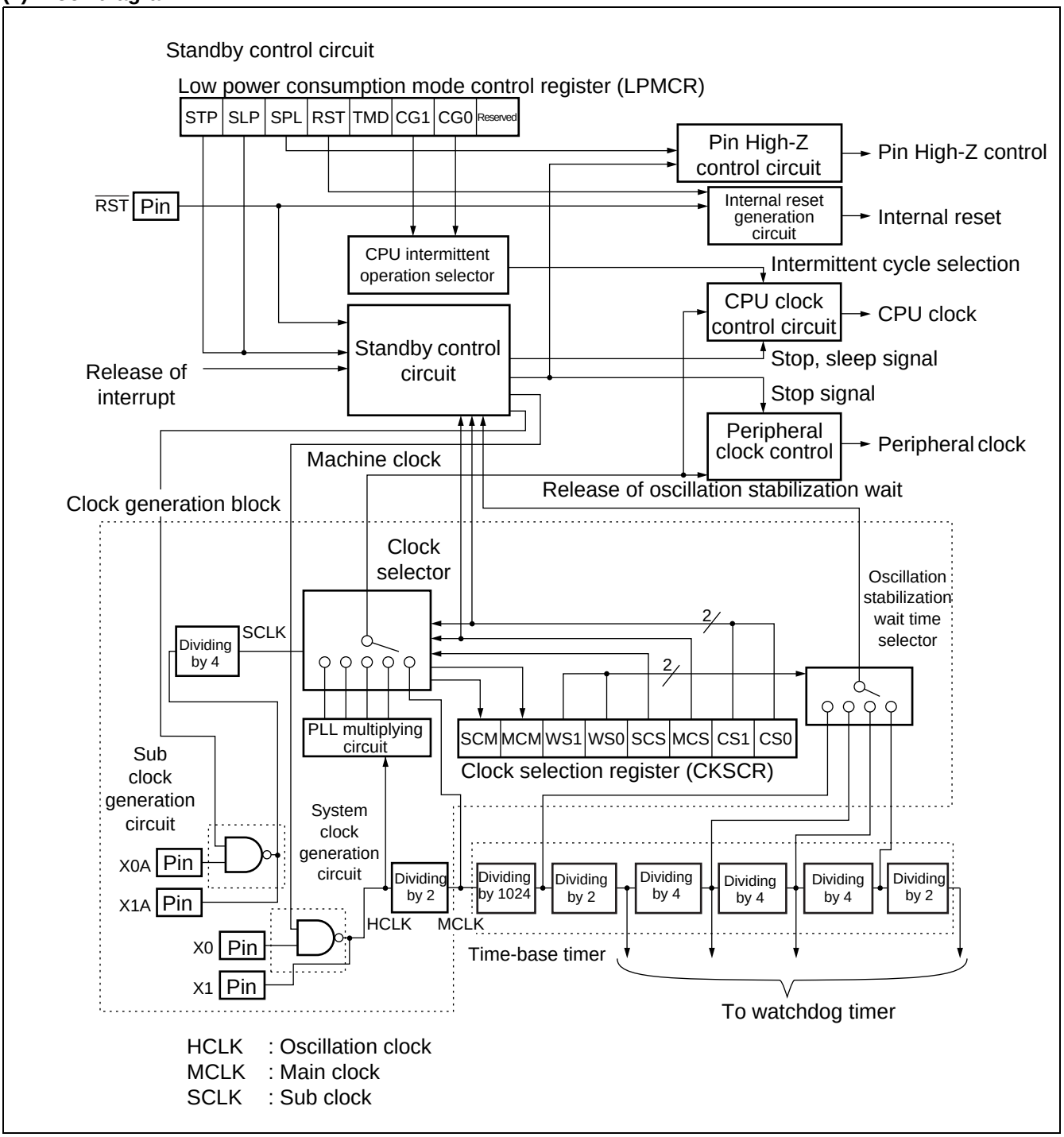
Clock mode
(PLL clock mode, main clock mode and sub clock mode)
CPU intermittent operation mode
(PLL clock intermittent operation mode, main clock intermittent operation mode and subclock intermittent operation mode)
Standby mode
(Sleep mode, time base timer mode, stop mode and watch mode)

(1) Register list

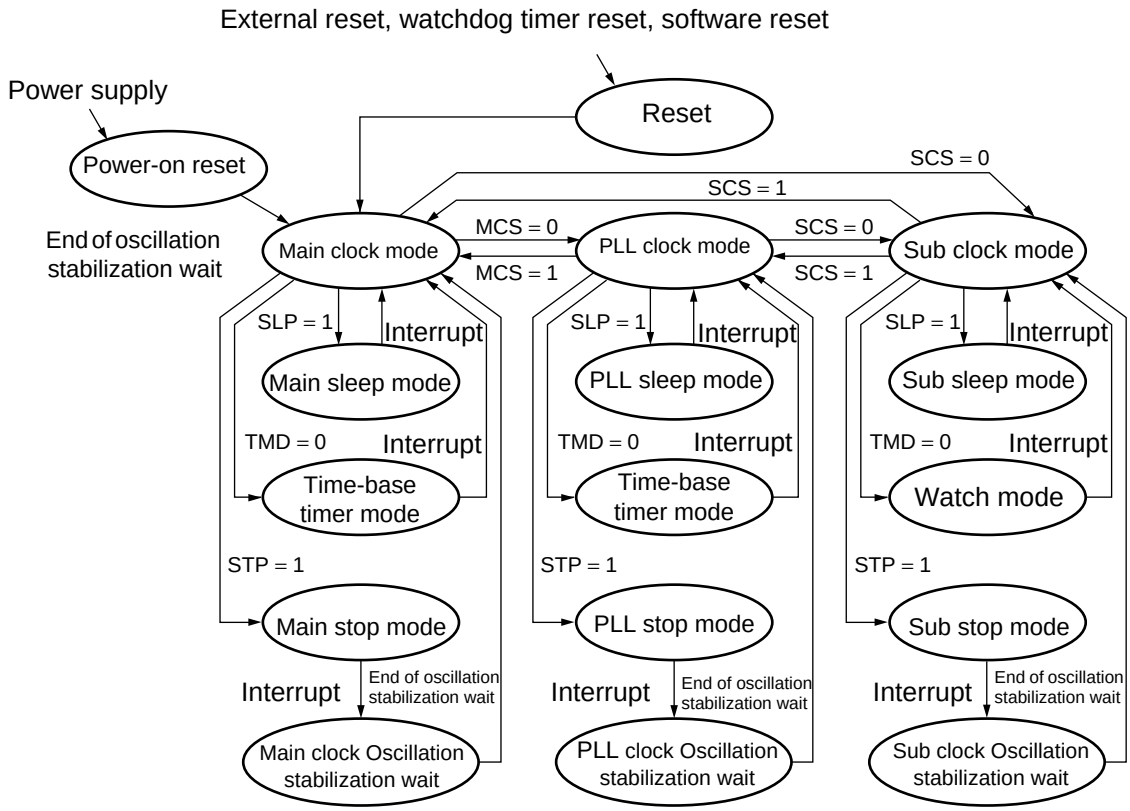
Low power consumption mode control register (LPMCR)

bit	7	6	5	4	3	2	1	0	Initial Value
0000A0H	STP	SLP	SPL	RST	TMD	CG1	CG0	Reserved	00011000B
	W	W	R/W	W	R/W	R/W	R/W	R/W	Read/Write

(2) Block diagram



(3) Figure of status transition



16. Timer clock output

The timer clock output circuit divides the oscillation clock by the time-base timer and generates and outputs the set division clock. Selectable from 32/64/128/256 division of the oscillation clock.

The timer clock output circuit is inactive in reset or stop mode. It is active in normal run, sleep, or pseudo-timer mode.

	PLL_Run	Main_Run	Sleep	Pseudo clock	STOP	Reset
Operation status	○	○	○	○	×	×

Note : When the time-base timer is cleared while using the timer clock output circuit, the clock is not correctly output. For detail of the time-base timer s clear condition, see the section of time-base timer in the MB90800 Hardware Manual.

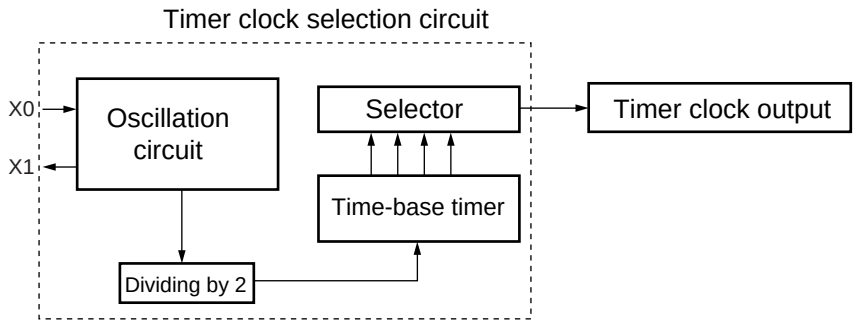
(1) Register list

Watch clock output control register (TMCS)

bit	15	14	13	12	11	10	9	8	Initial Value
0000AF$_H$	—	—	—	—	—	TEN	TS1	TS0	XXXXX000$_B$
	—	—	—	—	—	R/W	R/W	R/W	Read/Write

- : Unused

(2) Block diagram



17. ROM mirroring function selection module

ROM mirroring function selection module provides the setting so that ROM data located in FF bank can be read by access to 00 bank.

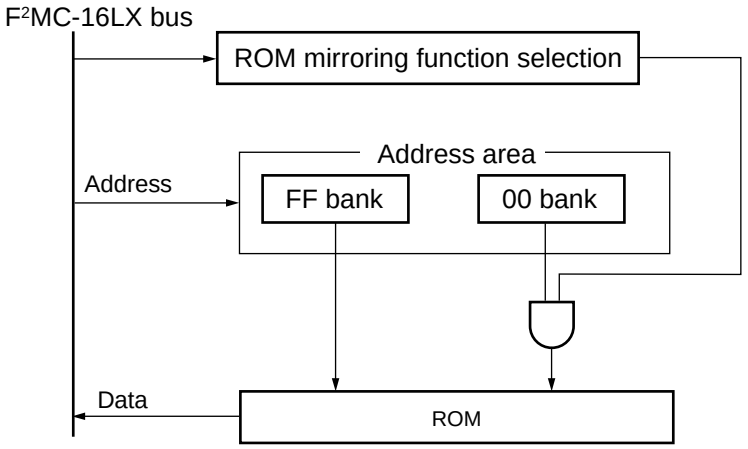
(1) Register list

ROM mirror function select register (ROMM)

bit	15	14	13	12	11	10	9	8	Initial Value
00006F$_H$	—	—	—	—	—	—	—	MI	XXXXXXX1$_B$
	—	—	—	—	—	—	—	R/W	Read/Write

- : Unused

(2) Block diagram



Note : Do not access to ROM mirroring function selection register in the middle of the operation of the address 008000$_H$ to 00FFFF$_H$.

18. Interrupt controller

Interrupt control register is in the interrupt controller. The register corresponds to all I/O of interrupt function. The register has following functions;

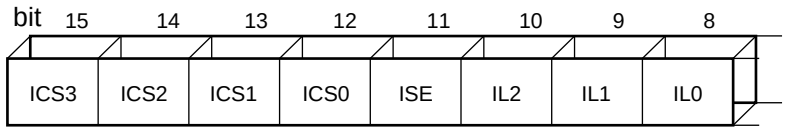
Setting of Interrupt level at correspondent peripheral circuit.

(1) Register list (at writing)

Interrupt control register — Initial Value

Address :

ICR01 $0000B1_H$
ICR03 $0000B3_H$
ICR05 $0000B5_H$
ICR07 $0000B7_H$
ICR09 $0000B9_H$
ICR11 $0000BB_H$
ICR13 $0000BD_H$
ICR15 $0000BF_H$



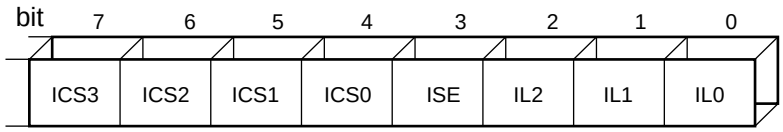
00000111_B

W W W W R/W R/W R/W R/W — Read/Write

Interrupt control register — Initial Value

Address :

ICR00 $0000B0_H$
ICR02 $0000B2_H$
ICR04 $0000B4_H$
ICR06 $0000B6_H$
ICR08 $0000B8_H$
ICR10 $0000BA_H$
ICR12 $0000BC_H$
ICR14 $0000BE_H$

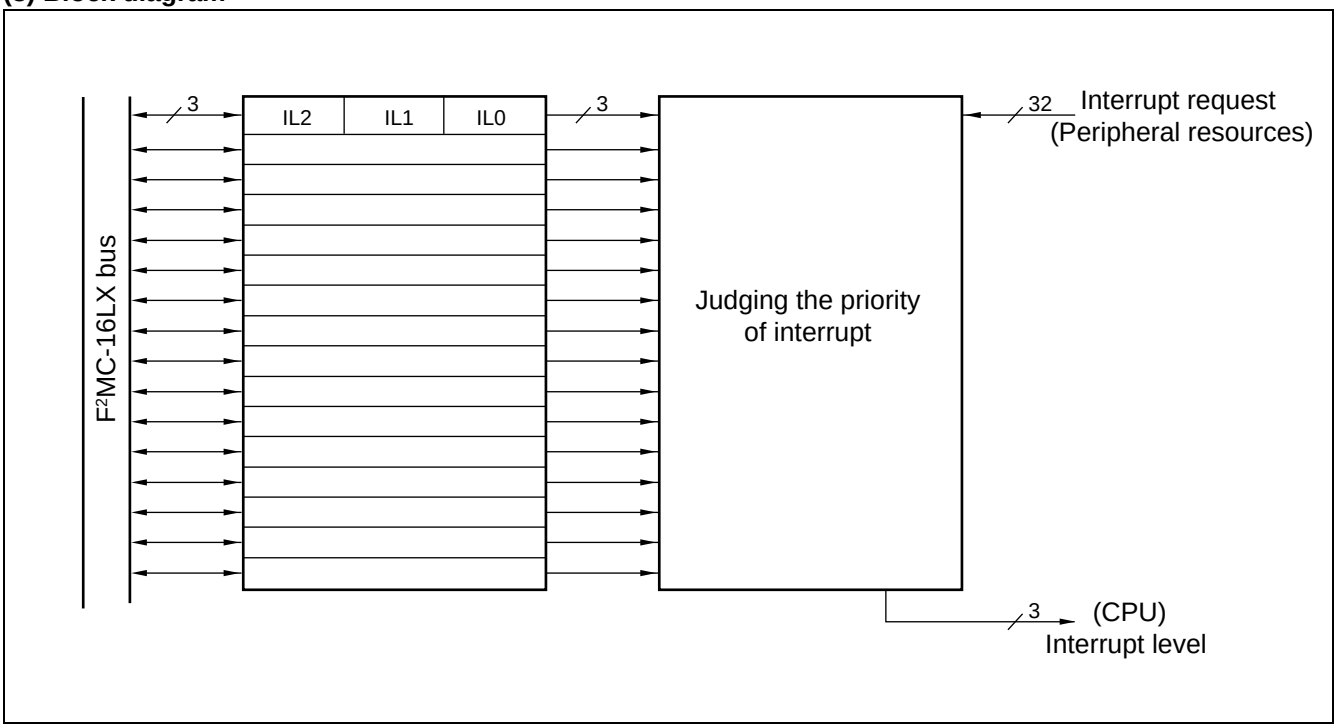


00000111_B

W W W W R/W R/W R/W R/W — Read/Write

Note : Do not access using read modify write instruction because it causes the malfunction.

(3) Block diagram



■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} – 0.3	V_{SS} + 4.0	V	
	AV_{CC}	V_{SS} – 0.3	V_{SS} + 4.0	V	$V_{CC} \geq AV_{CC}$*2
Input voltage*1	V_I	V_{SS} – 0.3	V_{SS} + 4.0	V	*3
		V_{SS} – 0.3	V_{SS} + 6.0	V	N-ch open-drain (5 V withstand voltageI/O) *4
Output voltage*1	V_O	V_{SS} – 0.3	V_{SS} + 4.0	V	*3
L level maximum output current	I_{OL11}	—	10	mA	Other than P74, P75, P40 to P47*5
	I_{OL12}	—	30	mA	P74, P75, P40 to P47 (Heavy-current output port) *5
L level average output current	I_{OLAV1}	—	3	mA	Other than P74, P75, P40 to P47*6
	I_{OLAV2}	—	15	mA	P74, P75, P40 to P47 (Heavy-current output port) *6
L level maximum total output current	ΣI_{OL}	—	120	mA	
L level average total output current	ΣI_{OLAV}	—	60	mA	*7
H level maximum output current	I_{OH11}	—	– 10	mA	Other than P74, P75, P40 to P47*5
	I_{OH12}	—	– 12	mA	P40 to P47 (Heavy-current output port) *5
H level average output current	I_{OHAV}	—	– 3	mA	*6
H level maximum total output current	ΣI_{OH}	—	– 120	mA	
H level average total output current	ΣI_{OHAV}	—	– 60	mA	*7
Power consumption	Pd	—	351	mW	
Operating temperature	T_A	– 40	+ 85	°C	
Storage temperature	T_{STG}	– 55	+ 150	°C	

*1 : The parameter is based on $V_{SS} = AV_{SS} = 0.0$ V.

*2 : AV_{CC} should not be exceeding V_{CC} at power-on etc.

*3 : V_I, V_O, should not exceed Vcc + 0.3 V.

*4 : Applicable to pins : P74, P75

*5 : A peak value of an applicable one pin is specified as a maximum output current.

*6 : An average current value of an applicable one pin within 100 ms is specified as an average output current. (Average value is found by multiplying operating current by operating rate.)

*7 : An average current value of all pins within 100 ms is specified as an average total output current. (Average value is found by multiplying operating current by operating rate.)

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

3. DC Characteristics

(V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V, T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
H level output voltage	V_{OH}	Output pins other than P40 to P47, P74, P75	I_{OH} = – 4.0 mA	V_{CC} – 0.5	—	Vcc	V	
	V_{OH1}	P40 to P47	I_{OH} = – 8.0 mA	V_{CC} – 0.5	—	Vcc	V	Heavy-current output port
L level output voltage	V_{OL}	Output pins other than P40 to P47, P74, P75	I_{OL} = 4.0 mA	Vss	—	Vss + 0.4	V	
	V_{OL1}	P40 to P47	I_{OL} = 15.0 mA	Vss	—	Vss + 0.6	V	Heavy-current output port
	V_{OL2}	P74, P75	I_{OL} = 15.0 mA	—	0.5	Vss + 0.8	V	Open-drain pin
Open-drain output application voltage	V_{D1}	P74, P75	—	Vss – 0.3	—	Vss + 5.5	V	
Input leak current	I_{IL}	All output pins	V_{CC} = 3.3 V, $V_{SS} < V_I < V_{CC}$	– 10	—	+ 10	µA	
Pull-up resistor	R_{UP}	$\overline{RST}$	Vcc = 3.3 V, T_A = + 25 °C	25	50	100	kΩ	
Pull-down resistor	R_{DOWN}	MD2	Vcc = 3.3 V, T_A = + 25 °C	25	50	100	kΩ	Except Flash memory products
Open drain output current	I_{leak}	P74, P75	—	—	0.1	10	µA	
Power supply current	I_{CC}	V_{CC}	V_{CC} = 3.3 V, Internal frequency 25 MHz At normal operating	—	48	60	mA	
			V_{CC} = 3.3 V, Internal frequency 25 MHz At Flash writing	—	60	75	mA	Flash memory products
			V_{CC} = 3.3 V, Internal frequency 25 MHz At Flash erasing	—	60	75	mA	Flash memory products
	I_{CCS}		V_{CC} = 3.3 V, Internal frequency 25 MHz at sleep mode	—	22.5	30	mA	

(Continued)

(Continued)

(V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V, T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I_{CCTS}	V_{CC}	V_{CC} = 3.3 V, Internal frequency 3 MHz at timer mode	—	0.75	7	mA	
	I_{CCL}		V_{CC} = 3.3 V, Internal frequency 8 kHz at subclock operation, (T_A = + 25 °C)	—	15	140	µA	MASK ROM products
				—	0.5	0.9	mA	Flash memory products
	I_{CCLS}		V_{CC} = 3.3 V, Internal frequency 8 kHz at subclock sleep operation, (T_A = + 25 °C)	—	13	40	µA	
	I_{CCT}		V_{CC} = 3.3 V, Internal frequency 8 kHz at watch mode (T_A = + 25 °C)	—	1.8	40	µA	
	I_{CCH}		At Stop mode, (T_A = + 25 °C)	—	0.8	40	µA	
LCD division resistance	R_{LCD}	V_{CC} – V3	At LCR = 0 setting	100	200	400	kΩ	*
		V_{CC} – V3	At LCR = 1 setting	12.5	25	50		
		V0 – V1, V1 – V2, V2 – V3	At LCR = 0 setting	50	100	200		
		V0 – V1, V1 – V2, V2 – V3	At LCR = 1 setting	6.25	12.5	25		
COM0 to COM3 output impedance	R_{VCOM}	COM0 to COM3	V1 to V3 = 3.3 V	—	—	2.5	kΩ	
SEG0 to SEG47 output impedance	R_{VSEG}	SEG0 to SEG47		—	—	15	kΩ	
LCD leak current	I_{LCDC}	V0 to V3, COM0 to COM3, SEG0 to SEG47	—	– 5	—	+ 5	µA	

* : LCD internal divided resistor can be select two type resistor by internal divided resistor selecting bit (LCR) of LCDC range register (LCRR) .

4. AC Characteristics

(1) Clock timing

(V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V, T_A = – 40 °C to + 85 °C)

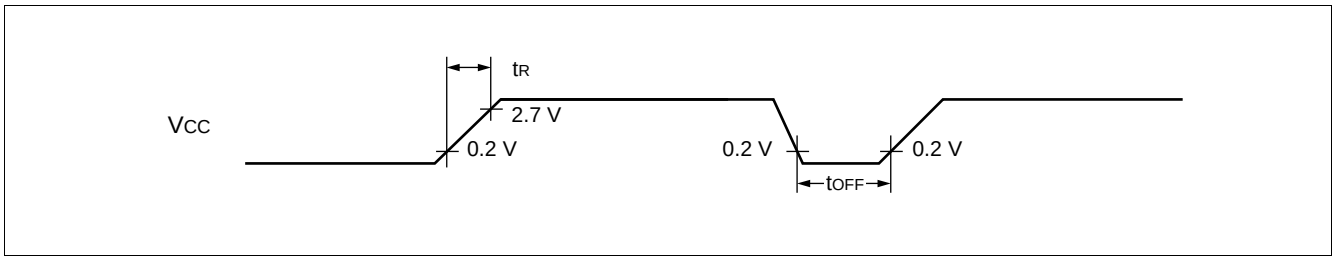
Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	f_{CH}	X0, X1	—	3	—	16	MHz	External crystal oscillation
				3		16		× 1/2 (at PLL stop) At oscillation circuit
				4		16		Multiply by 1 At oscillation circuit
				4		12.5		Multiply by 2 At oscillation circuit
				4		8.33		Multiply by 3 At oscillation circuit
				4		6.25		Multiply by 4 At oscillation circuit
		X0		3		25		× 1/2 (at PLL stop) At external clock
				4		25		Multiply by 1 At external clock
				4		12.5		Multiply by 2 At external clock
				4		8.33		Multiply by 3 At external clock
				4		6.25		Multiply by 4 At external clock
	f_{CL}	X0A, X1A		—	32.768	—	kHz	
Clock cycle time	t_{HCYL}	X0, X1		40	—	333	ns	
	t_{LCYL}	X0A, X1A		—	30.5	—	µs	
Input clock pulse width	P_{WH} P_{WL}	X0		5	—	—	ns	Set duty ratio 50% ± 3%
	P_{WLH} P_{WLL}	X0A		—	15.2	—	µs	Set duty ratio at 30% to 70% as a guideline.
Input clock rise time and fall time	tcr tcf	X0		—	—	5	ns	At external clock
Internal operating clock frequency	f_{CP}	—		1.5	—	25	MHz	When main clock is used
	f_{CP1}	—		—	8.192	—	kHz	When sub clock is used
Internal operating clock cycle time	t_{CP}	—		40	—	666	ns	When main clock is used
	t_{CP1}	—		—	122.1	—	µs	When sub clock is used

(3) Power-on reset

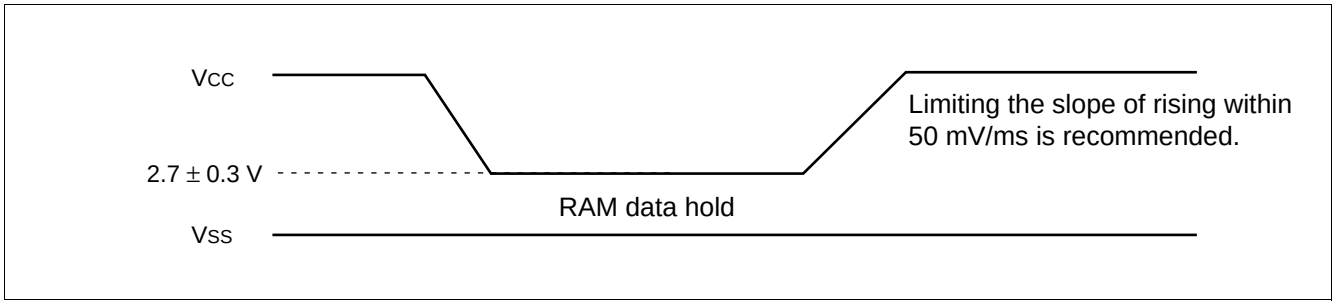
(V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V, T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Condi-tions	Value		Unit	Remarks
				Min	Max		
Power supply rising time	t_R	V_{CC}	—	—	30	ms	At normal operating
Power supply shutdown time	t_{OFF}	V_{CC}		1	—	ms	Wait time until power on

Notes :
- V_{CC} should be set under 0.2 V before power-on rising up.
- These value are for power-on reset.
- In the device, there are internal registers which is initialized only by a power-on reset. If these initialization is executing, power-on procedure must be obeyed by these value.



Note : Sudden change of power supply voltage may activate the power-on reset function. When changing power supply voltages during operation, raise the power smoothly by suppressing variation of voltages as shown below.



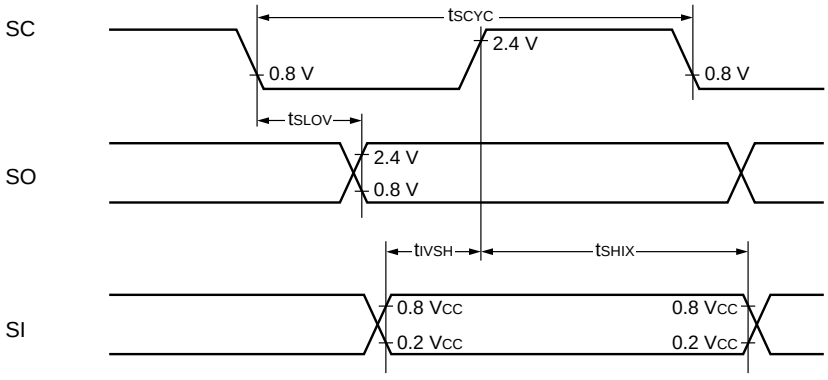
(4) Serial I/O

(V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V, T_A = – 40 °C to + 85 °C)

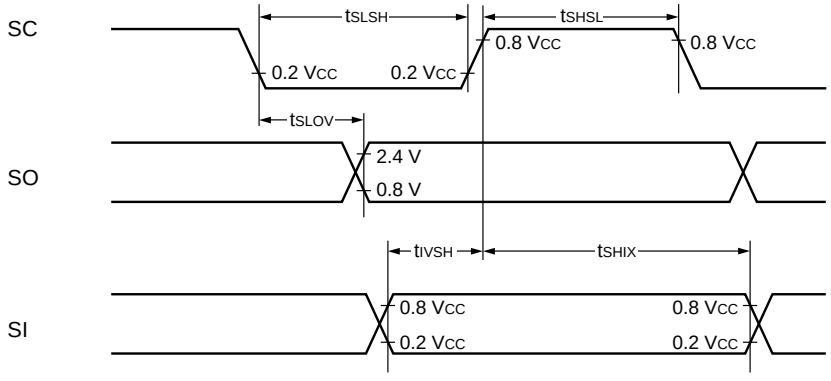
Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SC0 to SC3	Internal shift clock mode output pin : C_L = 80 pF + 1TTL	8 t_{CP}	—	ns
SCK ↓ → SOT delay time	t_{SLOV}	SC0 to SC3, SO0 to SO3		–80	+ 80	ns
Valid SIN → SCK ↑	t_{IVSH}	SC0 to SC3, SI0 to SI3		100	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIX}			60	—	ns
Serial clock H pulse width	t_{SHSL}	SC0 to SC3	External shift clock mode output pin : C_L = 80 pF + 1TTL	4 t_{CP}	—	ns
Serial clock L pulse width	t_{SLSH}			4 t_{CP}	—	ns
SCK ↓ → SOT delay time	t_{SLOV}	SC0 to SC3, SO0 to SO3		—	150	ns
Valid SIN → SCK ↑	t_{IVSH}	SC0 to SC3, SI0 to SI3		60	—	ns
SCK ↑ → valid SIN hold time	t_{SHIX}			60	—	ns

Notes : • The above rating is in CLK synchronous mode.
• C_L is a load capacitance value on pins for testing.
• t_{CP} is machine cycle frequency (ns) . Refer to (1) Clock timing .

• Internal shift clock mode



• External shift clock mode



(8) I²C timing

($AV_{CC} = V_{CC} = 3.3\ V \pm 0.3\ V$, $V_{SS} = AV_{SS} = 0.0\ V$, $T_A = -40\ °C$ to $+85\ °C$)

Parameter	Symbol	Conditions	Standard-mode		Unit
			Min	Max	
SCL clock frequency	f_{SCL}	When power supply voltage of external pull-up resistor is 5.0 V R = 1.0 kΩ, C = 50 pF*2 When power supply voltage of external pull-up resistor is 3.6 V R = 1.0 kΩ, C = 50 pF*2	0	100	kHz
Hold time (repeated) START condition SDA ↓ → SCL ↓	t_{HDSTA}		4.0	—	µs
L width of the SCL clock	t_{LOW}		4.7	—	µs
H width of the SCL clock	t_{HIGH}		4.0	—	µs
Set-up time for a repeated START condition SCL ↑ → SDA ↓	t_{SUSTA}		4.7	—	µs
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	3.45 *3	µs
Data set-up time SDA ↓ ↑ → SCL ↑	t_{SUDAT}	When power supply voltage of external pull-up resistor is 5.0 V f_{CP}*1 ≤ 20 MHz, R = 1.0 kΩ, C = 50 pF*2 When power supply voltage of external pull-up resistor is 3.6 V f_{CP}*1 ≤ 20 MHz, R = 1.0 kΩ, C = 50 pF*2	250 *4	—	ns
		When power supply voltage of external pull-up resistor is 5.0 V f_{CP}*1 > 20 MHz, R = 1.0 kΩ, C = 50 pF*2 When power supply voltage of external pull-up resistor is 3.6 V f_{CP}*1 > 20 MHz, R = 1.0 kΩ, C = 50 pF*2	200 *4	—	ns
Set-up time for STOP condition SCL ↑ → SDA ↑	t_{SUSTO}	When power supply voltage of external pull-up resistor is 5.0 V R = 1.0 kΩ, C = 50 pF*2 When power supply voltage of external pull-up resistor is 3.6 V R = 1.0 kΩ, C = 50 pF*2	4.0	—	µs
Bus free time between a STOP and START condition	t_{BUS}		4.7	—	µs

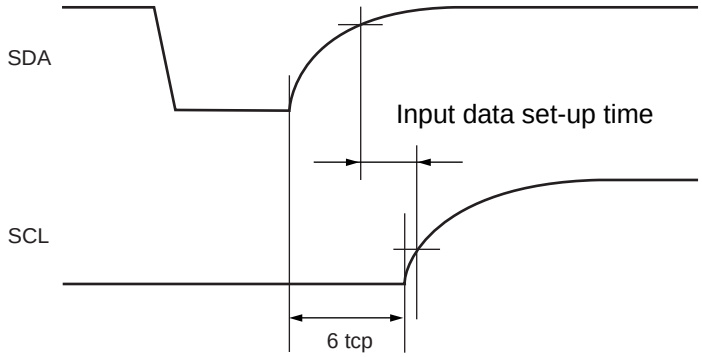
*1 : f_{CP} is internal operation clock frequency. Refer to (1) Clock timing .

*2 : R, C : Pull-up resistor and load capacitor of the SCL and SDA lines.

*3 : The maximum t_{HDDAT} only has to be met if the device does not stretch the L width (t_{LOW}) of the SCL signal.

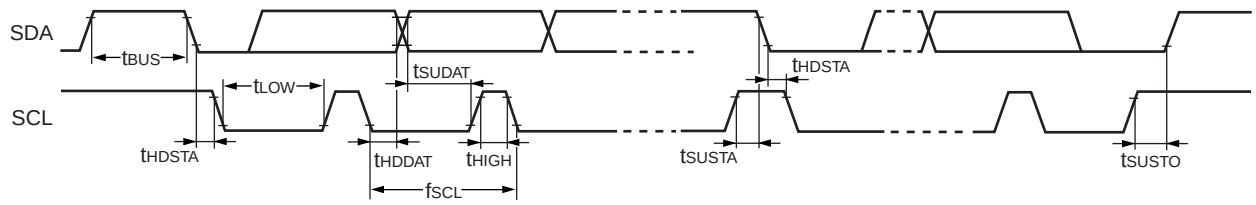
*4 : Refer to • Note of SDA and SCL set-up time .

• Note of SDA and SCL set-up time



Note : The rating of the input data set-up time in the device connected to the bus cannot be satisfied depending on the load capacitance or pull-up resistor.
Be sure to adjust the pull-up resistor of SDA and SCL if the rating of the input data set-up time cannot be satisfied.

• Timing definition



5. A/D Converter

(1) A/D Converter Electrical Characteristics

(V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V, T_A = – 40°C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Resolution	—	—	—	—	—	10	bit	
Total error	—	—		—	—	± 3.0	LSB	
Nonlinear error	—	—		—	—	± 2.5	LSB	
Differential linear error	—	—		—	—	± 1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN11		AV_{SS} – 1.5LSB	AVss + 0.5LSB	AV_{SS} + 2.5LSB	V	1 LSB = (AV_{CC} - AV_{SS})/ 1024
Full-scale transition voltage	V_{FST}	AN0 to AN11		AVcc – 3.5LSB	AVcc – 1.5LSB	AVcc + 0.5LSB	V	
Conversion time	—	—		8.64*1	—	—	µs	
Sampling time	—	—		2	—	—	µs	
Analog port input current	I_{AIN}	AN0 to AN11		—	—	10	µA	
Analog input voltage	V_{AIN}	AN0 to AN11		0	—	AVcc	V	
Reference voltage	—	AVcc		3.0	—	AVcc	V	
Power supply current	I_A	AVcc		—	1.4	3.5	mA	
	I_{AH}	AVcc		—	—	5*2	µA	
Reference voltage supplying current	I_R	AVcc		—	94	150	µA	
	I_{RH}	AVcc		—	—	5*2	µA	
Interchannel disparity	—	AN0 to AN11		—	—	4	LSB	

*1 : At operating, main clock 25 MHz.

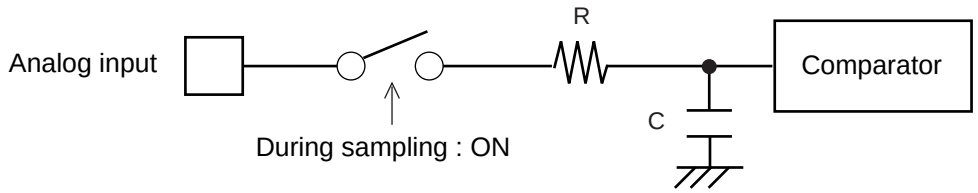
*2 : If A/D converter is not operating, a current when CPU is stopped is applicable (at Vcc – CPU = AVcc = 3.3 V)

(2) Notes on Using A/D Converter

- **About the external impedance of analog input and its sampling time**

A/D converter with sample & hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, consider the relation-ship between the external impedance and minimum sampling time and either adjust the resistor value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. And, if the sampling time cannot be sufficient, connect a capacitor of about 0.1 µF to the analog input pin.

- Analog input circuit model

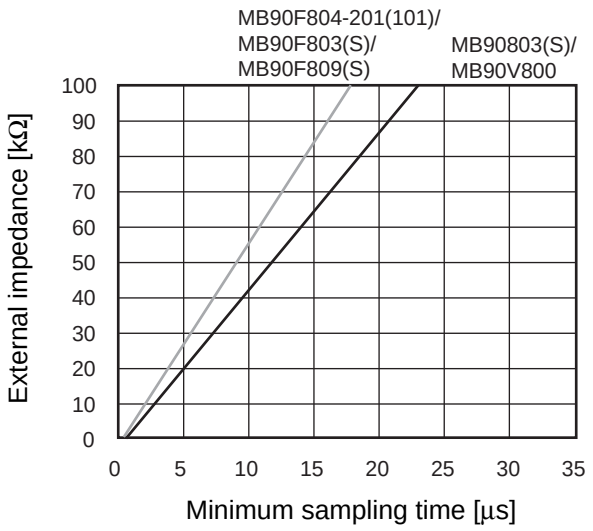


	R	C
MB90803 (S)	1.9 kΩ (Max)	32.3 pF (Max)
MB90F804-201(101)/F803(S)/F809(S)	1.9 kΩ (Max)	25.0 pF (Max)
MB90V800	1.9 kΩ (Max)	32.3 pF (Max)

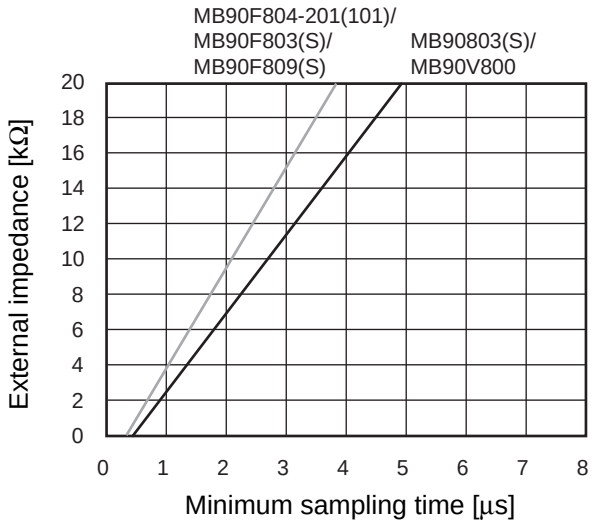
Note : The values are reference values.

- The relationship between external impedance and minimum sampling time

(External impedance = 0 kΩ to 100 kΩ)



(External impedance = 0 kΩ to 20 kΩ)



- **About errors**

As | AV_{CC} – AV_{SS} | becomes smaller, values of relative errors grow larger.

6. Definition of A/D Converter Terms

Resolution

Analog variation that is recognized by an A/D converter.

The 10-bit can resolve analog voltage into $2^{10} = 1024$.

Total error

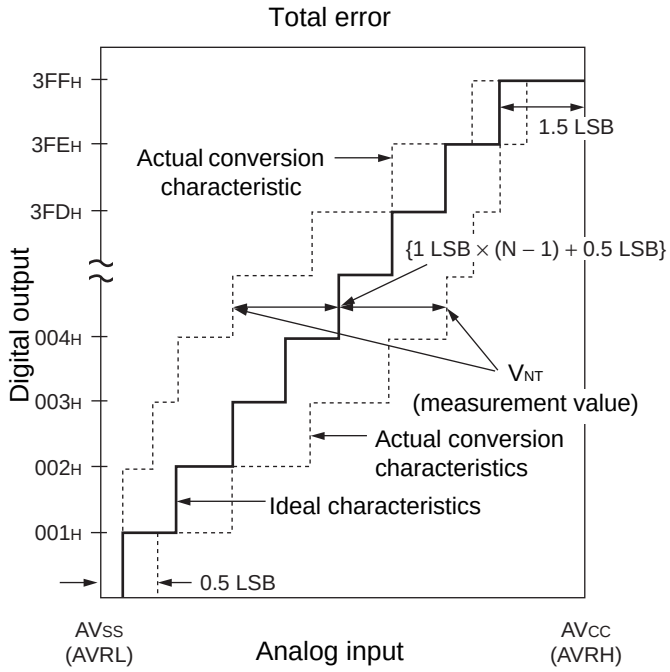
This shows the difference between the actual voltage and the ideal value and means a total of error because of offset error, gain error, non-linearity error and noise.

Linearity error

Deviation between a line across zero-transition line (00 0000 0000↔00 0000 0001) and full-scale transition line (11 1111 1110↔11 1111 1111) and actual conversion characteristics.

Differential linear error

Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.



$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$1\text{LSB(Ideal value)} = \frac{AV_{CC} - AV_{SS}}{1024}\ [\text{V}]$$

N : A/D converter digital output value

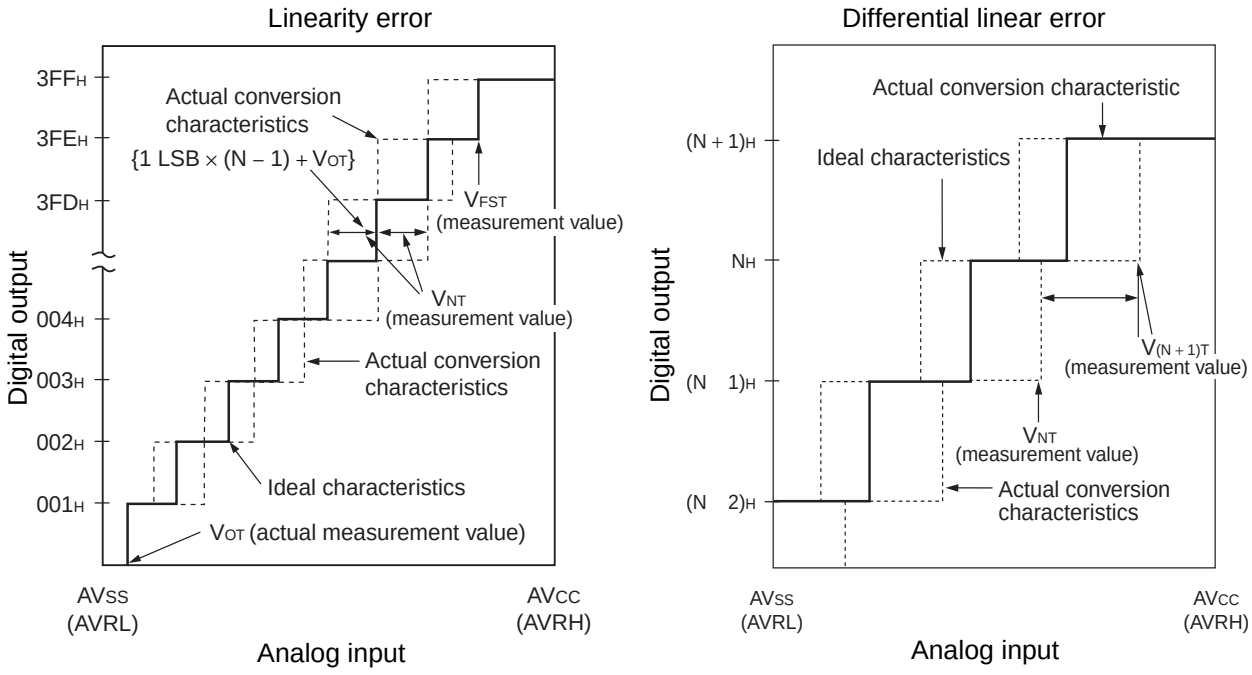
V_{OT}(Ideal value) = AV_{SS} + 0.5 LSB [V]

V_{FST}(Ideal value) = AV_{CC} – 1.5 LSB [V]

V_{NT}: A voltage at which digital output transitions from $(N - 1)_H$ to N_H.

(Continued)

(Continued)



$$\text{Linear error in digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ \text{[LSB]}$$

$$\text{Differential linear error in digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\text{LSB}\ \text{[LSB]}$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ \text{[V]}$$

N : A/D converter digital output value

V_{OT} : Voltage at which digital output transits from 000_H to 001_H.

V_{FST} : Voltage at which digital output transits from $3FE_H$ to $3FF_H$.

7. Flash Memory (MB90F804-101/201, MB90F809/S)

Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	T_A = + 25 °C Vcc = 3.0 V	—	1	15	s	Excludes 00_H programming prior to erasure.
Chip erase time		—	9	—		
Word (16-bit width) programming time		—	16	3600	µs	Except for the over head time of the system.
Program/erase cycle	—	10000	—	—	cycle	
Flash memory data retention time	Average T_A = + 85 °C	20	—	—	year	*

* : This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85 °C).

8. Dual Operation Flash Memory (MB90F803/S)

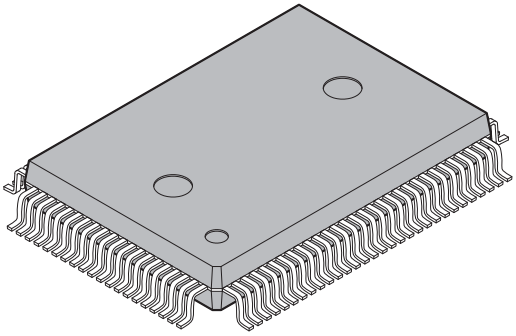
Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time (4 Kbytes sector)	T_A = +25 °C Vcc = 3.0 V	—	0.2	0.5	s	Excludes 00_H programming prior to erasure.
Sector erase time (16 Kbytes sector)		—	0.5	7.5		
Chip erase time		—	4.6	—		
Word (16-bit width) programming time		—	64	3600	µs	Except for the over head time of the system.
Program/erase cycle	—	10000	—	—	cycle	
Flash memory data retention time	Average T_A = + 85 °C	20	—	—	year	*

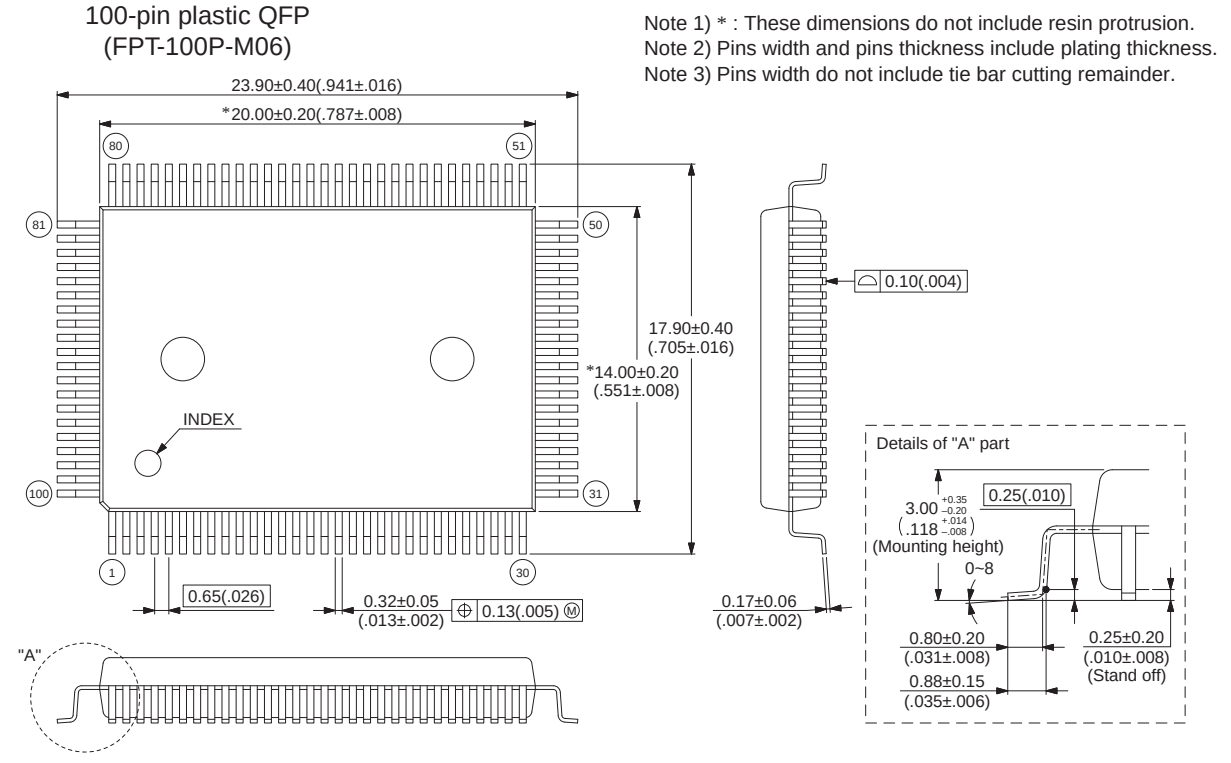
* : This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85 °C).

■ ORDERING INFORMATION

Part number	Package	Remarks
MB90F804-101PF-G MB90F804-201PF-G MB90F803PF-G MB90F803SPF-G MB90F809PF-G MB90F809SPF-G	100-pin plastic QFP (FPT-100P-M06)	With sub clock: Products without "S" suffix 201 option products Without sub clock: Products with "S" suffix 101 option products
MB90803PF-G MB90803SPF-G		

■ PACKAGE DIMENSION

100-pin plastic QFP		
	Lead pitch	0.65 mm
	Package width · package length	14.00 · 20.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	3.35 mm MAX
	Code (Reference)	P-QFP100-14· 20-0.65
(FPT-100P-M06)		



Please check the latest Package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

■ MAIN CHANGES IN THIS EDITION

Page	Section	Change Results
17	■ MEMORY MAP	Corrected “Address #2” for part number MB90F809/S. $FC8000_H$ $FD0000_H$

The vertical lines marked in the left side of the page show the changes.

MEMO

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