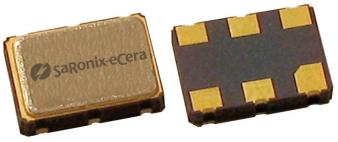
3.3V CMOS Ultra-Low Jitter Voltage Control VCXO

YN



Actual Size = 5 x 7mm

Product Features

- Cost-effective design
- LVCMOS compatible output
- Commercial and industrial operation
- ±50 ppM stability (or as specified)
- ±50 to ±100 ppM absolute (net) pull range
- RoHS Compliant

Product Description

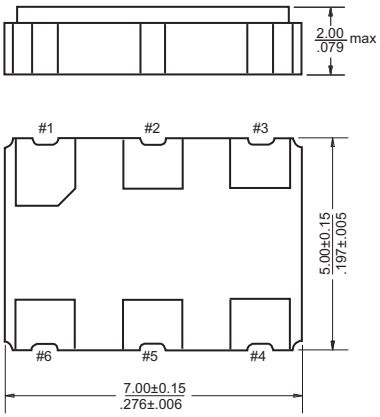
The YN is a voltage controlled crystal oscillator with wide pullability over a broad range of operating conditions and frequencies. The device is constructed with a hermetically sealed, quartz crystal resonator and low noise clock IC. The device, available on tape and reel, is contained in a 5x7mm ceramic package.

Applications

The YN Series VCXO is an ideal component in phase locked loop circuits that perform clock smoothing, clock/data recovery, or frequency translation and card synchronization functions, such as:

- SD/HD Video decoding
- SONET/SDH timing control and line cards
- T3/E3 Platforms
- Satellite and microwave communications
- Wireless base stations
- xDSL and DSLAM
- VoIP

Packaging Outline



Pin Functions

Pad	Function
1	Control voltage
2	Output Enable/Disable
3	Ground
4	Output
5	No Connect
6	Supply voltage

Dimensions are in mm/inches.

New Part Number Example

YN (A) C50 (B) 0001 (C)

A = Product Family
B = Frequency Code
C = Specification Code

Note: After July 1, 2007, a Saronix - eCera part number following the above format will be assigned upon confirmation of exact customer requirements.

Legacy Ordering Information (for reference only)

S T1317 B A B - 125.0000 (T)

SaRonix

Model

Stability Tolerance
B = ±50 ppm, 0 to +70°C
E = ±50 ppm, -40 to +85°C

Pullability (minimum APR)
A = ±50 ppm
B = ±100 ppm

Linearity
B = 10%

Frequency (MHz)

Packaging
blank = bulk packaged
(T) = Tape & Reel*
*full reel increments only (500pcs)

* Availability varies by frequency.

Electrical Performance

Parameter	Min.	Typ.	Max.	Units	Notes
Output frequency (F_N)	32.0		125.0	MHz	As specified
Supply voltage	+2.97	+3.3	+3.63	V	
Supply current			35	mA	
Frequency stability			±50	ppM	See #1 and #2 below
Operating temperature	-40		+85	°C	As specified
Output logic 0, V_{OL}			10% V_{DD}	V	Capacitive load
Output logic 0, V_{OL}			20% V_{DD}	V	AC coupled load
Output logic 1, V_{OH}	90% V_{DD}			V	Capacitive load
Output logic 1, V_{OH}	80% V_{DD}			V	AC coupled load
Output load			30	pF	Up to 80 MHz
Output load			95	Ω AC	Up to 125 MHz
Duty cycle	45		55	%	measured 50% V_{DD} (0 to +70°C)
Duty cycle	40		60	%	measured 50% V_{DD} (-40 to +85°C)
Rise and fall time			4	ns	measured 20/80% V_{DD}
Jitter, total			100	ps pk-pk	
Jitter, total			20	ps RMS	
Phase noise		-95		dBc/Hz	100 Hz offset
Phase noise		-110		dBc/Hz	1 kHz offset
Phase noise		-100		dBc/Hz	10 kHz offset

Notes:
1. As specified. Stability includes all combinations of operating temperature, load changes, rated input (supply) voltage changes, shock and vibration, with control voltage held at center.
2. ±12 ppM max due to aging (10 years at 40°C average ambient operating temperature).

Frequency Modulation Function

Parameter	Min.	Typ.	Max.	Units	Notes
Absolute pull range (APR)	±50 to ±100			ppM	See #1 below
Control voltage range	+0.3		+3.0	V_{DC}	As rated
Center control voltage		+1.65		V	For RMT center frequency
Monotonic linearity			10	%	Positive transfer slope
Input impedance	50			kΩ	Control voltage pin
Modulation bandwidth	50			kHz	-3dB

Notes:
1. As specified. APR is relative to the nominal output frequency F_N; APR is inclusive (net) of frequency deviation due to stability.

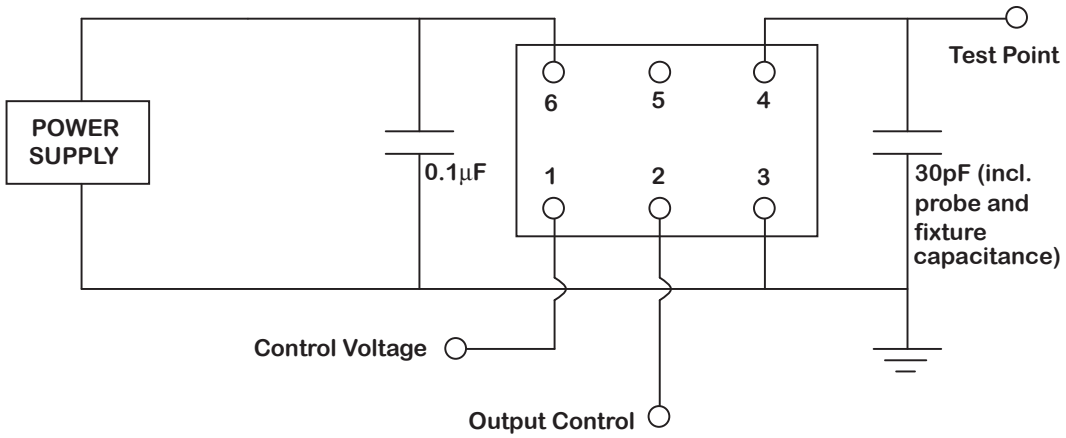
Output Enable / Disable Function

Parameter	Min.	Typ.	Max.	Units	Notes
Input voltage, output enable	3.0			V	or open
Input voltage, output high impedance			0.3	V	Output is high impendance

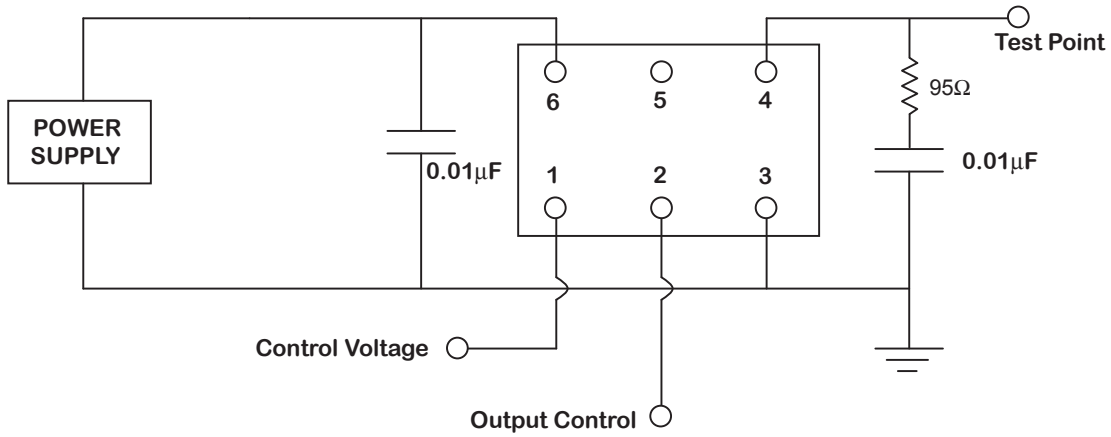
Absolute Maximum Ratings

Parameter	Min.	Typ.	Max.	Units	Notes
Storage temperature	-55		+125	°C	
Control voltage range	-0.5		V_{DD} +0.5	V	

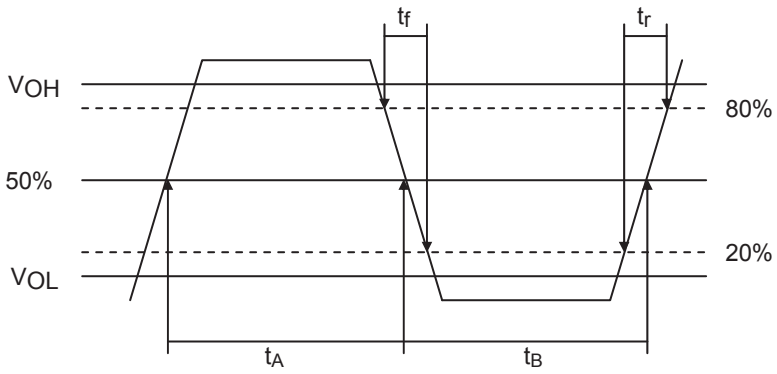
Test Circuit



Test Circuit (AC Coupled Load)

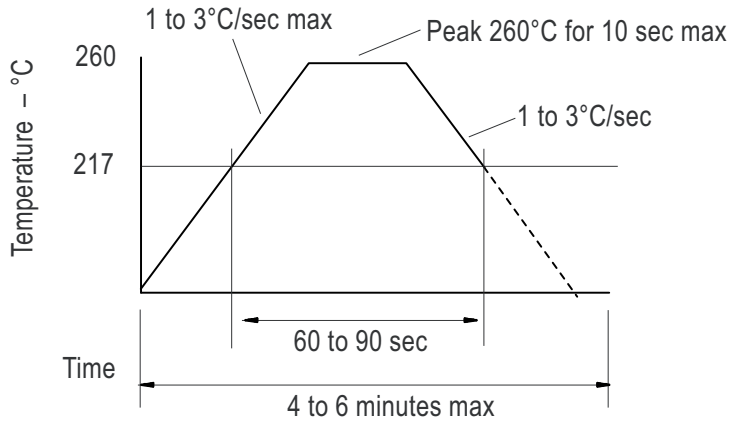


Output Waveform



Duty cycle = 100% × (t_A) / (t_A + t_B)

Solder Reflow Guide

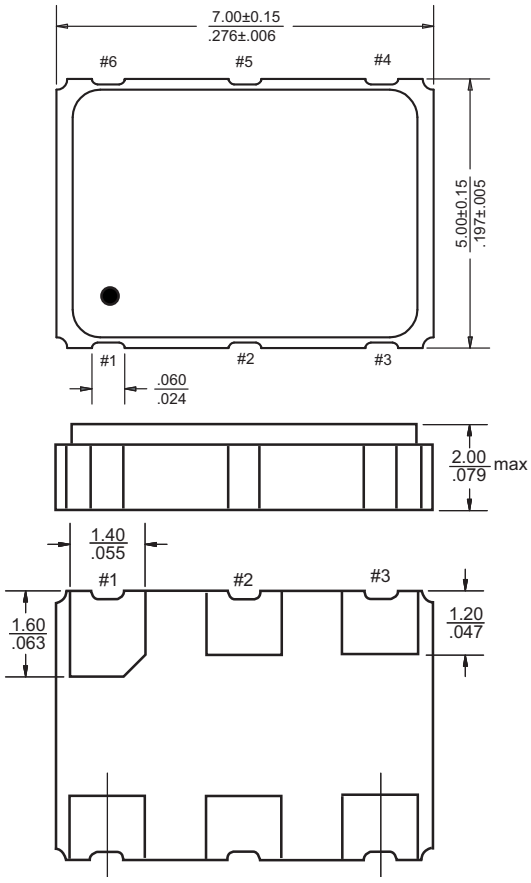


Reliability Test Ratings

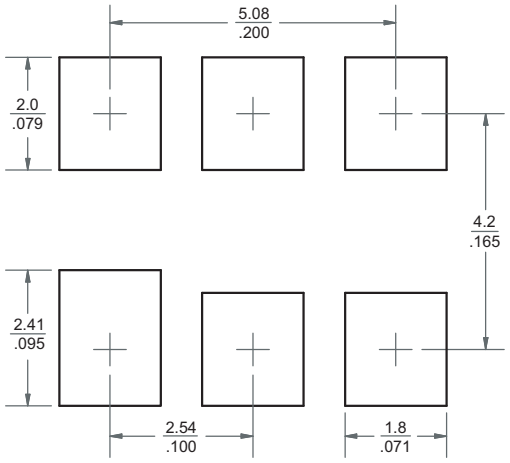
This product is rated to meet the following test conditions:

Type	Parameter	Test Condition
Mechanical	Shock	MIL-STD-883, Method 2002, Condition B
Mechanical	Solderability	JESD22-B102-D Method 2 (Preconditioning E)
Mechanical	Terminal strength	MIL-STD-883, Method 2004, Condition D
Mechanical	Solvent resistance	MIL-STD-202, Method 215
Environmental	Thermal shock	MIL-STD-883, Method 1011, Condition A
Environmental	Moisture resistance	MIL-STD-883, Method 1004
Environmental	Vibration	MIL-STD-883, Method 2007, Condition A
Environmental	Resistance to soldering heat	J-STD-020C Table 5-2 Pb-free devices (2 cycles max)

Mechanical Drawings



Recommended Land Pattern*



*External high-frequency power decoupling is recommended.(see test circuit for minimum recommendation). To ensure optimal performance, do not route traces beneath the package.

Scale: None. Dimensions are in mm/inches.