Hot Swap Controller (Negative Supply Rail)

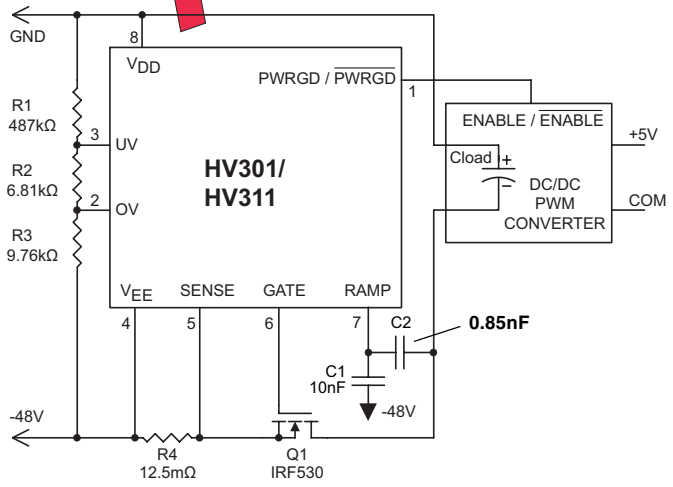
Features

- ±10V to ±90V Operation
- Built-in “normally on” turn-on clamp eliminates components
- UV/OV Lock Out & Power-on-Reset for Debouncing
- Sense resistor program ground circuit breaker
- Programmable circuit breaker holdoff
- Inrush control using either: i) servo or ii) feedback cap
- Feedback to Ramp pin means no Gate clamp needed
- Application solution for input voltage step (diode “ORing”)
- Programmable Auto-Retry (tens of seconds if desired)
- Auto-Retry or Latched Operation
- Enable through Open Drain interface to UV or OV
- Low Power, <0.6mA PWRGD Flag Operation, <0.4mA Sleep Mode
- Small SOIC-8 Package

Applications

- -48V Central Office Switching
- -24V Cellular and Fixed Wireless Systems
- -24V PBX Systems
- Line Cards
- -48V Powered Ethernet for VoIP
- Distributed Power Systems
- Power Supply Control
- +48V Storage Networks
- Electronic Circuit Breaker

Typical Application Circuit



NOTES: 1. Undervoltage Shutdown (UV) set to 35V.
2. Overvoltage Shutdown (OV) set to 65V.
3. Current Limit set to ~1A.
4. CB set to 8A.

Ordering Information

Active State of Power Good Signal	Package Options
	8 Pin SO
HIGH	HV301LG
LOW	HV311LG

General Description

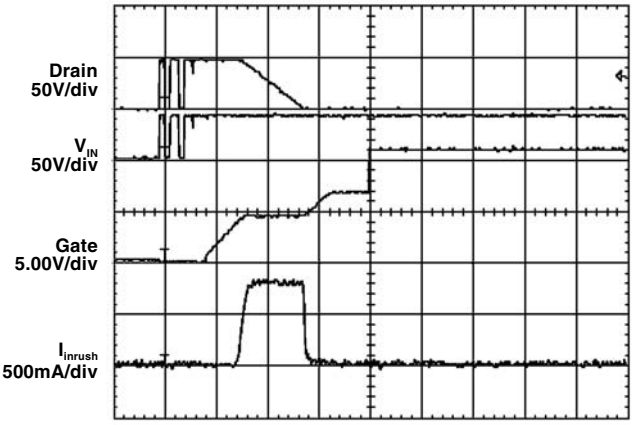
The Supertex HV301 and HV311 Hot Swap Controllers provide control of power supply connection during insertion of cards or modules into live backplanes. They may be used in systems where active control is implemented in the negative lead of supplies ranging from ±10V to ±90V.

During initial power application the gate of the external pass device is clamped low to suppress contact bounce glitches by a “normally on” circuit which does not require initialization of the IC. Thereafter the UV/OV supervisors and power-on-reset work together to suppress gate turn on until mechanical bounce has ended. The HV301/311 then control the current inrush limit to a programmed level using one of two possible methods, i) servo control or ii) a drain to ramp capacitor. The above methods eliminate the need for extra hold-off or current limiting components. The devices also include an electronic circuit breaker, programmed by a sense resistor.

After the load capacitance has fully charged, the HV301/311 will transition into a low power mode, and enable the open drain PWRGD. In low power mode the HV301/311 continues to monitor the input voltage and monitor the current level. If a load fault occurs, the electronic circuit breaker will trip, the pass element will be turned off, and the PWRGD will return to an

(continued on Page 3)

Waveforms



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Electrical Characteristics (-10V - V_{EE} - -90V, -40°C - +85°C unless otherwise noted)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
Supply (Referenced to V_{DD} pin)						
V_{EE}	Supply Voltage	-90		-10	V	
I_{EE}	Supply Current		600	700	µA	V_{EE} = -48V, Mode = Limiting
I_{EE}	Sleep Mode Suppy Current		400	450	µA	V_{EE} = -48V, Mode = Sleep
OV and UV Control (Referenced to V_{EE} pin)						
V_{UVH}	UV High Threshold		1.26		V	Low to High Transition
V_{UVL}	UV Low Threshold		1.16		V	High to Low Transition
V_{UVHY}	UV Hysteresis		100		mV	
I_{UV}	UV Input Current			1.0	nA	V_{UV} = V_{EE} +1.9V
V_{OVH}	OV High Threshold		1.26		V	Low to High Transition
V_{OVL}	OV Low Threshold		1.16		V	High to Low Transition
V_{OVHY}	OV Hysteresis		100		mV	
I_{OV}	OV Input Current			1.0	nA	V_{OV} = V_{EE} + 0.5V
Current Limit (Referenced to V_{EE} pin)						
$V_{SENSE-CL}$	Current Limit Threshold Voltage	40	50	60	mV	V_{UV} = V_{EE} + 1.9V, V_{OV} = V_{EE} + 0.5V
$V_{SENSE-CB}$	Circuit Breaker Threshold Voltage	80	100	120	mV	V_{UV} = V_{EE} + 1.9V, V_{OV} = V_{EE} + 0.5V
Gate Drive Output (Referenced to V_{EE} pin)						
V_{GATE}	Maximum Gate Drive Voltage	8.5	10	12	V	V_{UV} = V_{EE} + 1.9V, V_{OV} = V_{EE} + 0.5V
I_{GATEUP}	Gate Drive Pull-Up Current	500			µA	V_{UV} = V_{EE} + 1.9V, V_{OV} = V_{EE} + 0.5V
$I_{GATEDOWN}$	Gate Drive Pull-Down Current	40			mA	V_{UV} = V_{EE}, V_{OV} = V_{EE} + 0.5V
Ramp Timing Control (Test Conditions: C_{LOAD}=100mF, C_{RAMP}=10nF, V_{UV}=V_{EE}+1.9V, V_{OV}=V_{EE}+0.5V, External MOSFET is IRF530*)						
I_{RAMP}	Ramp Pin Output Current		10		µA	V_{SENSE} = 0V
t_{POR}	Time from UV to Gate Turn On	2.0			ms	(See Note 1)
t_{RISE}	Time from Gate Turn On to V_{SENSE} Limit	400			µs	
t_{LIMIT}	Duration of Current Limit Mode		5.0		ms	
t_{PWRGD}	Time from Current Limit to PWRGD		5.0		ms	
V_{RAMP}	Voltage on Ramp Pin in Current Limit Mode		3.6		V	(See Note 2)
$t_{STARTLIMIT}$	Start Up Time Limit	80	100	120	ms	
t_{CBTRIP}	Circuit Breaker Delay Time	2.0		5.0	µs	May be exteneded by external RC circuit
t_{AUTO}	Automatic Restart Delay TIme	12			s	
Power Good Output (Referenced to V_{EE} pin)						
$V_{PWRGD(hi)}$	Applied voltage to PWRGD	90			V	PWRGD=Inactive
$V_{PWRGD(lo)}$	PWRGD Low Voltage		0.5	0.8	V	I_{PWRGD} = 1mA, PWRGD=Active
Dynamic Characteristics						
$t_{GATEHLOV}$	OV Comparator Transition			500	ns	
$t_{GATEHLUV}$	UV Comparator Transition			500	ns	

Note 1: This timing depends on the threshold voltage of the external N-Channel MOSFET. The higher its threshold is, the longer this timing.

Note 2: This voltage depends on the characteristics of the external N-Channel MOSFET. V_{th} = 3V for an IRF530.

* IRF530 is a registered trademark of International Rectifier.

General Description, cont'd.

inactive state. Thereafter a programmable auto-retry timer will hold the device off to allow the pass element to cool before resetting and restarting. The auto-retry can be disabled using a single resistor if desired.

The HV301/311 includes a current mode servo-circuit which can be used as a return to limit during input voltage steps such as would be seen in a diode "ORed" situation when power switches back to regulated supply from battery operation. The HV301/311 allows independent programming of the trigger level of this phenomenon so that it may be set at a different level to the current limit level if desired. Under all circumstances the maximum servo period is limited to 100ms to protect the pass element.

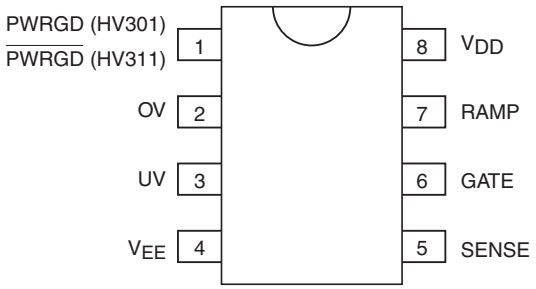
PWRGD Logic

Model	Condition	PWRGD	
HV301	INACTIVE (Not Ready)	0	V_{EE}
	ACTIVE (Ready)	1	HI Z
HV311	INACTIVE (Not Ready)	1	HI Z
	ACTIVE (Ready)	0	V_{EE}

Absolute Maximum Ratings

V_{EE} reference to V_{DD} pin	+0.3V to -100V
V_{PWRGD} referenced to V_{EE} Voltage	-0.3V to +100V
V_{UV} and V_{OV} referenced to V_{EE} Voltage	-0.3V to +12V
Operating Ambient Temperature	-40°C to +85°C
Operating Junction Temperature	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C

Pinout



Pin Description

PWRGD – The Power Good Output Pin is held inactive on initial power application and will go active when the external MOSFET is fully turned on. This pin may be used as an enable control when connected directly to a PWM power module.

OV – This Over Voltage sense pin, when raised above its high threshold will immediately cause the GATE pin to be pulled low. The GATE pin will remain low until the voltage on this pin falls below the low threshold limit, initiating a new start-up cycle.

UV – This Under Voltage sense pin, when below its low threshold limit will immediately cause the GATE pin to be pulled low. The GATE pin will remain low until the voltage on this pin rises above the high threshold limit, initiating a new start-up cycle.

V_{EE} – This pin is the negative terminal of the power supply input to the circuit.

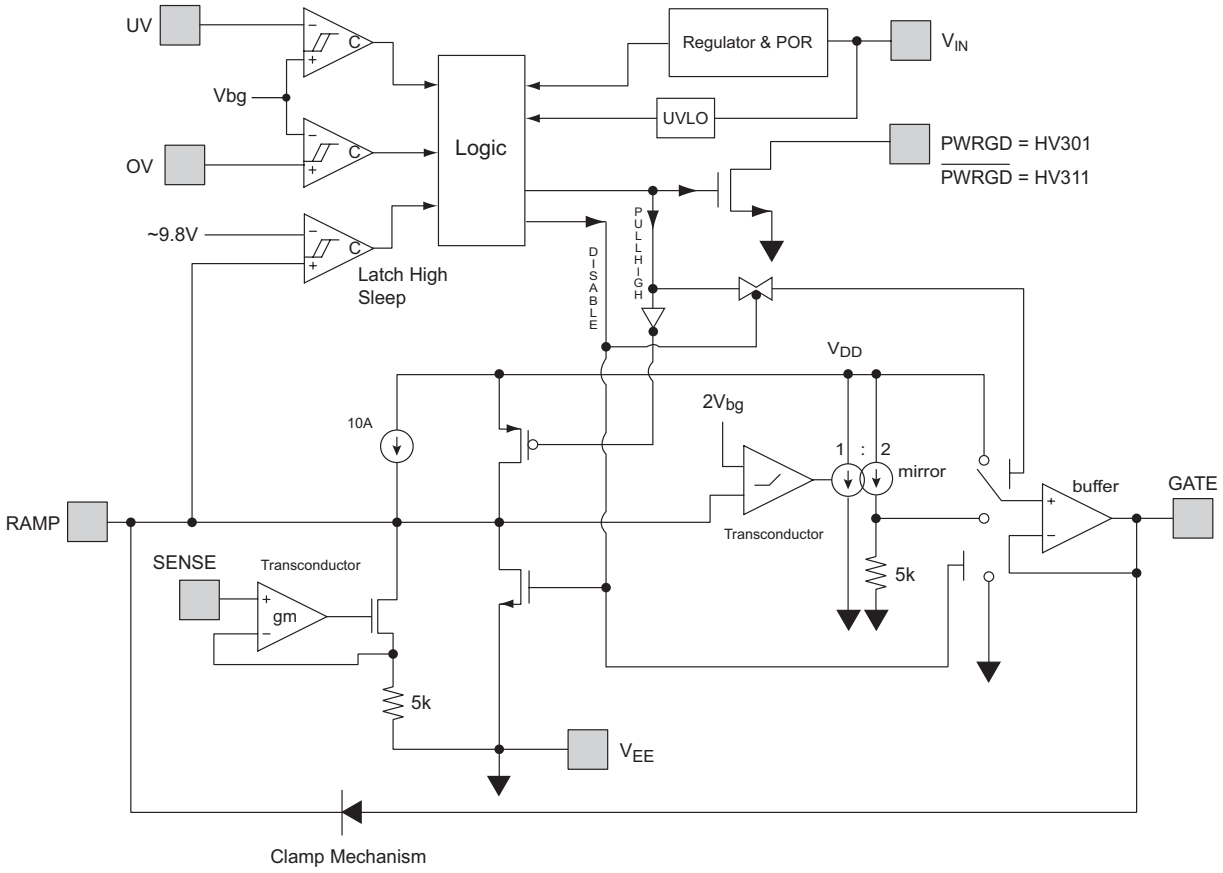
V_{DD} – This pin is the positive terminal of the power supply input to the circuit.

RAMP – This pin provides a current output so that a timing ramp voltage is generated when a capacitor is connected.

GATE – This is the Gate Driver Output for the external N-Channel MOSFET.

SENSE – The current sense resistor connected from this pin to V_{EE} Pin programs the circuit breaker trip limit.

Functional Block Diagram



Functional Description

Insertion into Hot Backplanes

Telecom, data networks and some computer applications require the ability to insert and remove circuit cards from systems without powering down the entire system. All circuit cards have some filter capacitance on the power rails, which is especially true in circuit cards or network terminal equipment utilizing distributed power systems. The insertion can result in high inrush currents that can cause damage to connector and circuit cards and may result in unacceptable disturbances on the system backplane power rails.

The HV301 and HV311 are designed to facilitate the insertion of these circuit cards or connection of terminal equipment by eliminating these inrush currents and powering up these circuits in a controlled manner after full connector insertion has been achieved. The HV301 or HV311 is intended to provide this function on supply rails in the range of ±10 to ±90 Volts.

Description of Operation

During initial power application, a unique proprietary circuit holds off the external MOSFET, preventing an input glitch while an internal regulator establishes an internal operating voltage of approximately 10V. Until the proper internal voltage is achieved all circuits are held reset, the PWRGD output is inactive and the gate to source voltage of the external MOSFET is clamped low.

Once the internal under voltage lock out (UVLO) has been satisfied, the circuit checks the input supply under voltage (UV) and over voltage (OV) sense circuits to ensure that the input voltage is within programmed limits. These limits are determined by the selected values of resistors R1, R2 and R3, which form a voltage divider.

Assuming the above conditions are satisfied and while continuing to hold the PWRGD output inactive and the external MOSFET GATE voltage low, the current source feeding the RAMP pin is turned on. The external capacitor connected to it begins to charge, thus starting an initial time delay determined by the value of the capacitor. During this time if the OV or UV limits are exceeded, an immediate reset occurs and the capacitor connected to the RAMP pin is discharged.

When the voltage on the RAMP pin reaches an internally set threshold voltage, the gate drive circuit begins to turn on the external MOSFET. In servo mode, once the gate threshold is reached, the resulting output current generates a voltage drop on the sense resistor connected between the SENSE and V_{EE} pins, causing a decrease in the available current charging the capacitor on the RAMP pin. This continuous feedback mechanism allows the output current to rise inverse exponentially over a period of a few hundred microseconds to the sense resistor programmed current limit set point.

When the voltage drop on the sense resistor reaches 50mV the

Functional Description, cont'd.

RAMP pin current is reduced to zero and the voltage on the RAMP pin will be fixed, indicating that the circuit is in current limit mode. Depending on the value of the load capacitor and the programmed current limit, charging may continue for some time, but may not exceed a nominal 100ms preset time limit. Once the load capacitor has been charged, the output current will drop, reducing the voltage on the SENSE pin, which in turn will increase the RAMP pin current, thus causing the voltage on the capacitor connected to the RAMP pin to continue rising, thereby providing yet another programmed delay. If due to output overload conditions during startup, PWRGD does not achieve an active state within 100ms or the Circuit Breaker is tripped, the circuit is reset, pulling down the GATE to V_{EE}, discharging the capacitor connected to the RAMP pin, changing PWRGD to an inactive state. A timeout or circuit breaker fault will initiate an Auto-Retry if enabled.

On the other hand, in feedback capacitor mode, a current source of 10µA from the RAMP pin limits the dv/dt of the feedback capacitor which, in turn, programs Inrush according to Inrush=10µA-C_{load}/C_2.

When the ramp voltage is within 1.2V of the regulated internal supply voltage, the controller will force the GATE terminal to a nominal 10V, the PWRGD pin will change to an active state, the Circuit Breaker is enabled and the circuit will transition to a low power sleep mode.

When the voltage on the SENSE pin rises to 100mV, indicating an over current condition, the circuit breaker will trip in less than 5µs. This time may be extended by the addition of external components.

At any time during the start up cycle or thereafter, crossing the UV and OV limits (including hysteresis) will cause an immediate reset of all internal circuitry. When the input supply voltage returns to a value within the programmed UV and OV limits a new start up sequence will be initiated.

Design Information

Setting Under Voltage and Over Voltage Shut Down

The UV and OV pins are connected to comparators with nominal 1.21V thresholds and 100mV of hysteresis (1.21V ± 50mV). They are used to detect under voltage and over voltage conditions at the input to the circuit. Whenever the OV pin rises above its high threshold (1.26V) or the UV pin falls below its low threshold (1.16V) the GATE voltage is immediately pulled low, the PWRGD pin changes to its inactive state and the external capacitor connected to the RAMP pin is discharged.

Calculations can be based on either the desired input voltage operating limits or the input voltage shutdown limits. In the following equations the shutdown limits are assumed.

The under voltage and over voltage shut down thresholds can be programmed by means of the three resistor divider formed by R1, R2 and R3. Since the input currents on the UV and OV pins are negligible the resistor values may be calculated as follows:

$$UV_{OFF} = V_{UVL} = 1.16 = \left|V_{EEUV(off)}\right| \times \frac{R2 + R3}{R1 + R2 + R3}$$

$$OV_{OFF} = V_{OVH} = 1.26 = \left|V_{EEOV(off)}\right| \times \frac{R3}{R1 + R2 + R3}$$

Where $|V_{EEUV(off)}|$ and $|V_{EEOV(off)}|$ relative to V_{EE} are Under & Over Voltage Shut Down Threshold points.

If we select a divider current of 100µA at a nominal operating input voltage of 50 Volts then

$$R1 + R2 + R3 = \frac{50\text{V}}{100\mu\text{A}} = 500\text{k}\Omega$$

From the second equation for an OV shut down threshold of 65V the value of R3 may be calculated.

$$OV_{OFF} = 1.26 = \frac{65 \times R3}{500\text{k}\Omega}$$

$$R3 = \frac{1.26 \times 500\text{k}\Omega}{65} = 9.69\text{k}\Omega$$

The closest 1% value is 9.76kΩ.

From the first equation for a UV shut down threshold of 35V the value of R2 can be calculated.

$$UV_{OFF} = 1.16 = \frac{35 \times (R2 + R3)}{500\text{k}\Omega}$$

$$R2 = \frac{1.16 \times 500\text{k}\Omega}{35} - 9.76\text{k}\Omega = 6.81\text{k}\Omega$$

The closest 1% value is 6.81kΩ.

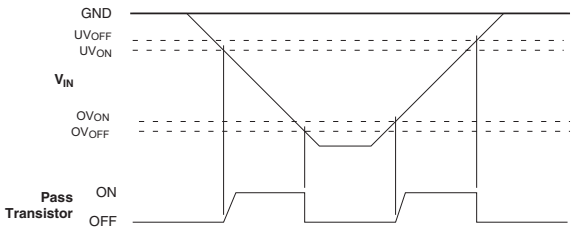
Then

$$R1 = 500\text{k}\Omega - R2 - R3 = 483\text{k}\Omega$$

The closest 1% value is 487kΩ.

Design Information, cont'd.

Undervoltage/Overvoltage Operation



From the calculated resistor values the OV and UV start up threshold voltages can be calculated as follows:

$$UV_{ON} = V_{UVH} = 1.26 = \left|V_{EEUV(on)}\right| \times \frac{R2 + R3}{R1 + R2 + R3}$$

$$OV_{ON} = V_{OVL} = 1.16 = \left|V_{EEOV(on)}\right| \times \frac{R3}{R1 + R2 + R3}$$

Where $|V_{EEUV(on)}|$ and $|V_{EEOV(on)}|$ are Under & Over Voltage Start Up Threshold points relative to V_{EE}.

Then

$$\left|V_{EEUV(on)}\right| = 1.26 \times \frac{R1 + R2 + R3}{R2 + R3}$$

$$\left|V_{EEUV(on)}\right| = 1.26 \times \frac{487\text{k}\Omega + 6.81\text{k}\Omega + 9.76\text{k}\Omega}{6.81\text{k}\Omega + 9.76\text{k}\Omega} = 38.29\text{V}$$

And

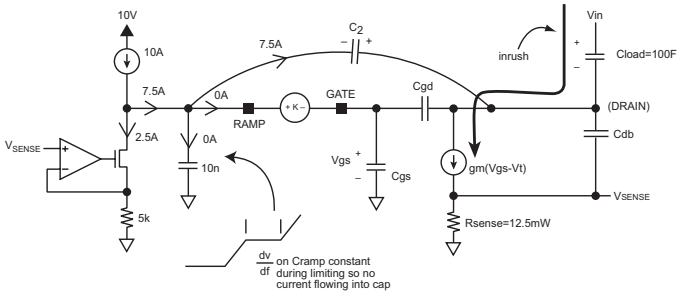
$$\left|V_{EEOV(on)}\right| = 1.16 \times \frac{R1 + R2 + R3}{R3}$$

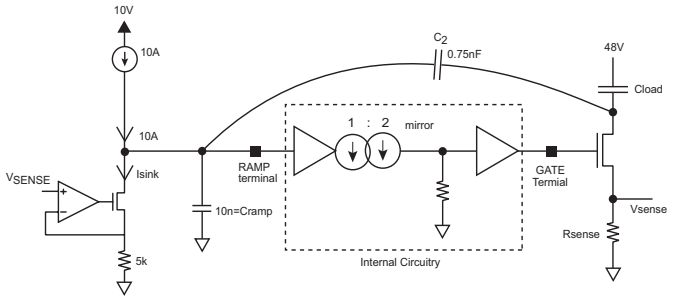
$$\left|V_{EEOV(on)}\right| = 1.16 \times \frac{487\text{k}\Omega + 6.81\text{k}\Omega + 9.76\text{k}\Omega}{9.76\text{k}\Omega} = 59.85\text{V}$$

Therefore, the circuit will start when the input supply voltage is in the range of 38.29V to 59.85V.

Programming Inrush and I_{CB}

Method 1: Inrush independent of I_{CB}





1. Choose circuit breaker trip point eg. 8A as follows

   $$\text{Rsense} = \frac{100mV}{I_{CB}} = \frac{100mV}{8} = 12.5m\Omega$$

2. Choose inrush level, for example Inrush = 1A

3. Calculate Isink $= \frac{\text{Inrush} * \text{Rsense}}{5k\Omega} = \frac{1A \times 12.5m\Omega}{5k\Omega} = 2.5\mu\text{A}$

4. Calculate C_2 discharge limit
   = 10µA - Isink = 7.5µA (typical) = iC_2

4a. Adjust for Auto-retry disable, if used →

   $\cong \frac{Vt_{max}}{R_{disable}}$ e.g. $\frac{4V}{2.5M\Omega}$ = 1.6µA

   ⇒ e.g. iC_2 = 10µA - Isink - 1.6µA

   In this example we assume Auto-retry is enabled so ignore 1.6µA, ∴ iC_2 = 10µA - Isink = 7.5µA

5. Note: $i = C\frac{dv}{dt}$ $\quad iC_2 = C_2 \times \frac{dv}{dt}$ $\quad \text{Inrush} = C_{load} \times \frac{dv}{dt}$

   Note V_{IN} is fixed and V_{RAMP} is constant during limiting

   ⇒ $\frac{dv}{dt}$ across $C_{load} = \frac{dv}{dt}$ across C_2 (as they share a common node and their other terminals are fixed during inrush)

   $$\frac{iC_2}{C_2} = \frac{Inrush}{C_{load}} \Rightarrow \text{Inrush} = \frac{iC_2 \times C_{load}}{C_2}$$

   by conservation of charge on RAMP Node iC_2 = 7.5µA

   $$\text{Inrush} = \frac{7.5\mu A \times C_{load}}{C_2} \Rightarrow C_2 = \frac{7.5\mu A \times C_{load}}{Inrush}$$

   $$= \frac{7.5\mu A \times 100nF}{1A} = 750\text{pF} = 0.75\text{nF}$$

   Note that RAMP is protected by AC divider and Gate is clamped internally.

Design Information, cont'd.

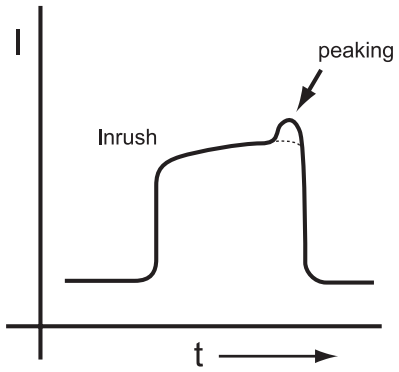
Programming Inrush and I_{CB}, continued:

Method 2: Inrush = 1/2 I_{CB}

1. Choose $I_{CB} = \frac{100mV}{R_{SENSE}}$, e.g. 2A $\Rightarrow$ $R_{SENSE} = 50m\Omega$

2. Inrush = $\frac{50mv}{R_{SENSE}}$, e.g. $\frac{50mV}{50m\Omega} = 1A$

3. Add compensation components from gate to drain if necessary to reduce peaking.

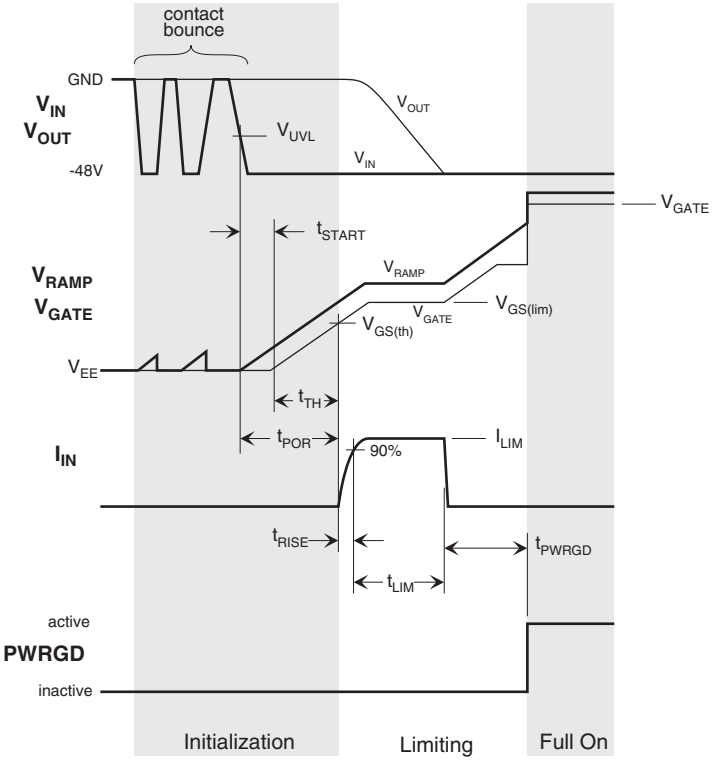


i) start with 2nF from gate to source

ii) increase to 10nF if needed

iii) add 1k Series resistor from gate to capacitor if needed

Timing



The timing functions are defined by the following equations:

$$t_{START} = 2.4\frac{C_{RAMP}}{I_{RAMP}}$$

$$t_{TH} = V_{GS(th)}\frac{C_{RAMP}}{I_{RAMP}}$$

$$t_{POR} = t_{START} + t_{TH}$$

$$t_{RISE} \approx \frac{C_{RAMP}}{g_{fs}\left(\frac{I_{RAMP}}{0.9I_{LIMIT}} - \frac{R_{SENSE}}{R_{FB}}\right)}$$

$$t_{LIMIT} \approx V_{IN}\frac{C_{LOAD}}{I_{LIMIT}}$$

$$t_{PWRGD} = \left(V_{INT} - V_{GS(\text{LIMIT})} - 1.2\right)\frac{C_{RAMP}}{I_{RAMP}}$$

Design Information, cont'd.

These equations assume that the load is purely capacitive and the following definitions apply.

C_{RAMP} is the external capacitor connected to the RAMP pin.

I_{RAMP} is the output current from the RAMP pin, nominally 10µA, when the voltage drop on R_{SENSE} resistor is zero.

V_{INT} is the internally regulated supply voltage and can range from 8.5V to 12V.

$V_{GS(th)}$ is the gate threshold voltage of the external pass transistor and may be obtained from its datasheet.

$V_{GS(\text{limit})}$ is the external pass transistor gate-source voltage required to obtain the limit current. It is dependent on the pass transistor's characteristics and may be obtained from the transfer characteristics on the transistor datasheet.

g_{fs} is the transconductance of the external pass transistor and may be obtained from its datasheet.

R_{FB} is the internal feedback resistor and is nominally 5kΩ.

I_{LIMIT} is the load current when the voltage drop on the R_{SENSE} resistor is 50mV.

These equations may be used to calculate the minimum value of C_{RAMP} for the most critical system performance characteristics.

For maximum contact bounce duration protection choose a value for t_{POR} and use the following equation:

$$C_{RAMP} = \frac{t_{POR} \times I_{RAMP}}{2.4 + V_{GS(th)}}$$

If control of PWRGD active delay is the critical system parameter, then choose a value for t_{PWRGD} and use the following equation:

$$C_{RAMP} = \frac{t_{PWRGD} \times I_{RAMP}}{V_{INT} - V_{GS(\text{limit})} - 1.2}$$

Start up Overload Protection

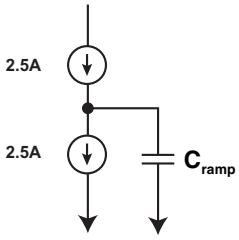
Start up must be achieved within a nominal 100ms as indicated by the PWRGD pin transition to the active state or the circuit will reset and an automatic restart will initiate after 12s delay. If there is an output overload or short circuit during start up, the circuit will be in a current mode for the 100ms time limit.

Circuit Breaker

The circuit breaker will trip in less than 5µs when the voltage on the SENSE pin reaches a nominal 100mV (2.0 x I_{LIMIT}). A resistor in series with the SENSE pin and a capacitor connected between the SENSE and V_{EE} pins may be added to delay the rate of voltage rise on the SENSE pin, thus permitting a current overshoot and delaying Circuit Breaker activation.

Automatic Restart

The Automatic Restart delay time is directly proportional to the capacitance at the RAMP pin. Automatic Restart sequence is activated whenever the 100ms timeout is reached during start up or the Circuit Breaker is tripped in low power sleep operating mode.



Auto-retry can be approximated as an SSS-timer with 2.5µA charge up and charge down currents through 28V, to a count of 256. Therefore,

$$T_{AUTORETRY} = \frac{2 \times 8 \times 256}{2.5\mu A} \times C_{ramp}$$

Due to the 2.5µA max charge current a resistor which draws more than 2.5µA below 8V will disable the autoretry. Try to keep this resistor as big as possible, e.g. 2.5mý, for most MOSFETs with max V_t of 4V this will vary the 10µA current source by only 4/2.5mý=1.6µA.

Application Information

Supported External Pass Devices

The HV301 and HV311 are designed to support N-Channel MOSFETs and IGBTs.

Selection of External Pass Devices

Since the current limit is likely to be set just slightly higher than maximum continuous load current in a typical system, the continuous current rating of the device will have to be at least equal to the current limit value.

The $R_{DS(ON)}$ of the device is likely to be selected based on allowable voltage drop after the hot swap action has been completed. Thus the continuous power dissipation rating of the device can be determined from the following equation:

$$P_{CONT} = R_{DS(ON)} \times I^2_{LIMIT}$$

The peak power rating may be calculated from the following equation:

$$P_{PEAK} = V_{IN} \times I_{LIMIT}$$

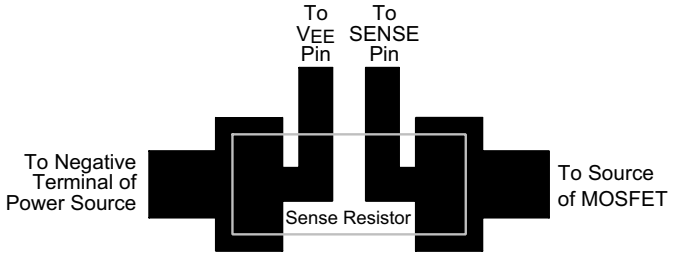
Given these values an external pass transistor may be selected from the manufacturers data sheet.

Selection of Current Sense Resistor

The power rating of the sense resistor must be greater than $I^2_{load} \times R$, where I_{load} is the normal maximum operating load.

Kelvin Connection to Sense Resistor

Physical layout of the printed circuit board is critical for correct current sensing. Ideally trace routing between the current sense resistor and the V_{EE} and SENSE pins should be direct and as short as possible with zero current in the sense traces. The use of Kelvin connection from SENSE pin and V_{EE} pin to the respective ends of the current sense resistor is recommended.



Paralleling External Pass Transistors

Due to variations in threshold voltages and gain characteristics between samples of transistors reliable 50% current sharing is not achievable. Some measure of paralleling may be accomplished by adding resistors in series with the source of each device; however, it will cause increased voltage drop and power dissipation.

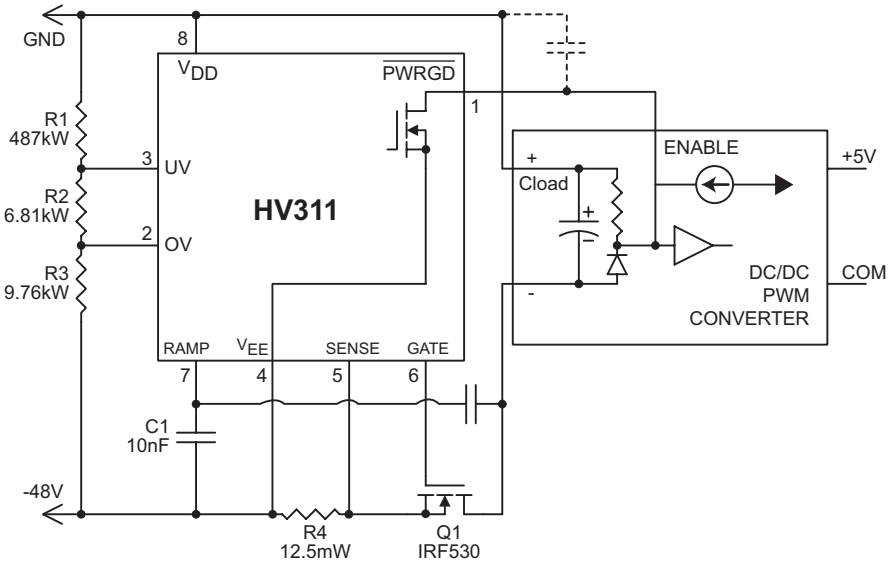
Paralleling of external Pass devices is not recommended!

If a sufficiently high current rated external pass transistor cannot be found then increased current capability may be achieved by connecting independent hot swap circuits in parallel, since they act as current sources during the load capacitor charging time when the circuits are in current limit. For this application the HV301 with active high PWRGD is recommended where the PWRGD pins of multiple hot swap circuits can be connected in a wired OR configuration.

PWRGD Output

It is critical to have a detailed understanding of the ENABLE input circuitry of the load (DC/DC PWM Converter) in order to make the correct choice between the HV301 and HV311.

Many DC/DC PWM Converters reference their ENABLE inputs to the negative input terminal. If the ENABLE input is active LOW then the HV311 can be directly connected as shown below (**Application Circuit 1**) since the open drain PWRGD output is in a High-Z state until the external MOSFET is fully turned on and the potential on the negative input of the converter is essentially the same as the V_{EE} pin of the HV311.

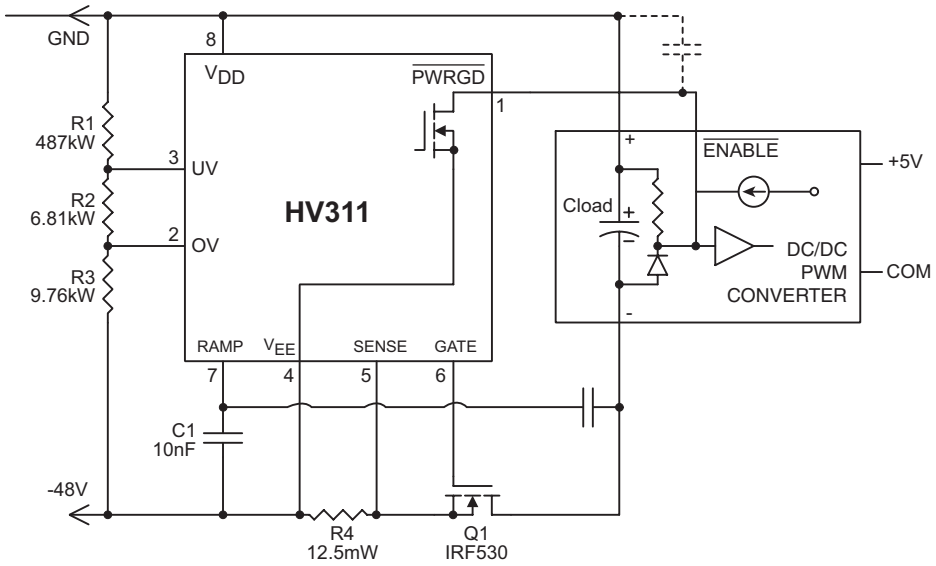


Note: capacitor may be needed to slow PWRGD dv/dt if gate oscillations around are observed when V_{IN} is close to OVLO.

Application Circuit 1

However, if the DC/DC PWM Converter with the ENABLE input circuit configuration was active HIGH, then the apparent choice of the HV301 would result in the creation of a current path through the protective diode clamp of the ENABLE input and the PWRGD output MOSFET of the HV301. For this situation the HV311 should be used as shown below in **Application Circuit 2**.

In some applications the PWRGD signal is used to activate load circuitry on the isolated output side of the DC/DC PWM Converter. In this situation an optocoupler is needed to provide the required isolation as shown below in **Application Circuit 3**.



Note: capacitor may be needed to slow PWRGD dv/dt if gate oscillations around are observed when V_{IN} is close to OVLO.

Application Circuit 2

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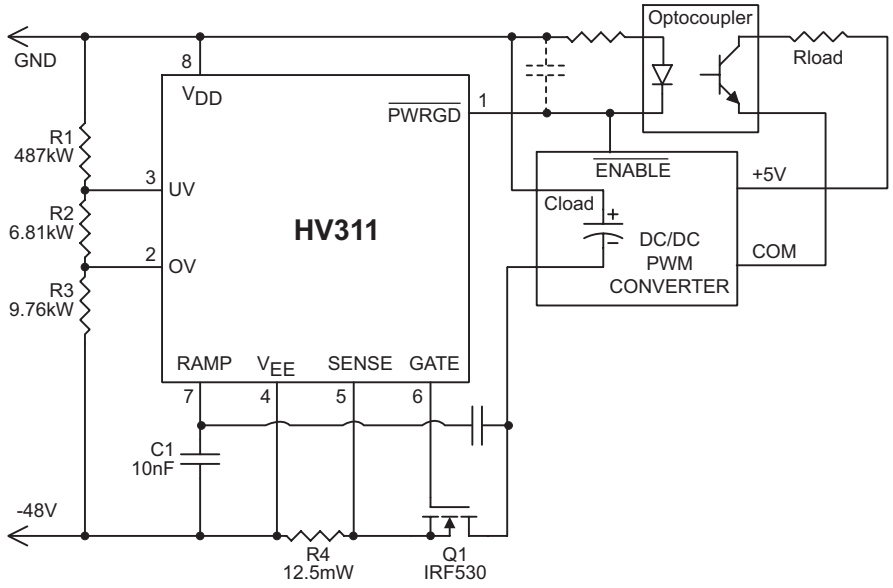


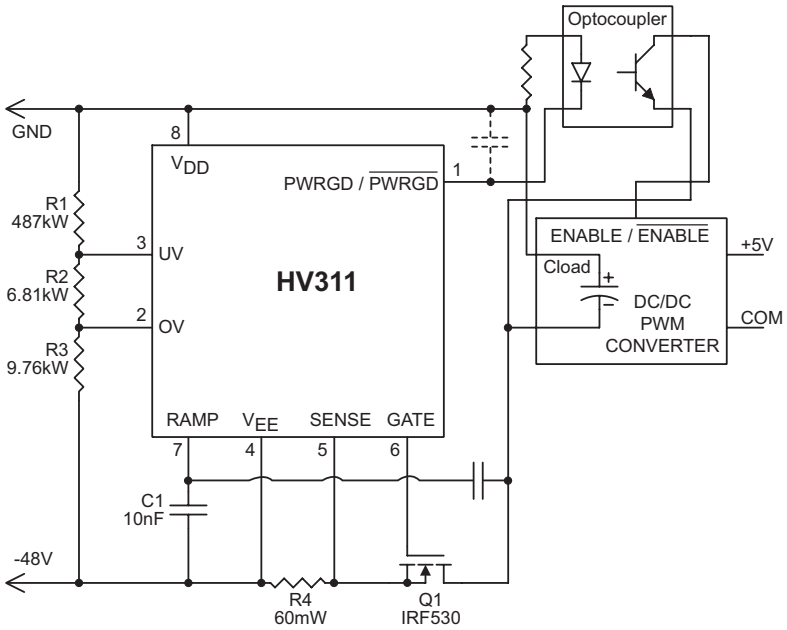
Note: capacitor may be needed to slow PWRGD dv/dt if gate oscillations around are observed when V_{IN} is close to OVLO.

Application Circuit 3

When the details of the load ENABLE circuitry is not known, using an optocoupler always provides a safe solution (**Application Circuit 4**).

Filtering Voltage Spikes on Input Supply

In some systems over voltage spikes of very short duration may exist. For these systems a small capacitor may be added from the OV pin to the V_{EE} pin to filter the voltage spikes (**Application Circuit 5**).



Note: capacitor may be needed to slow PWRGD dv/dt if gate oscillations around are observed when V_{IN} is close to OVLO.

Application Circuit 4

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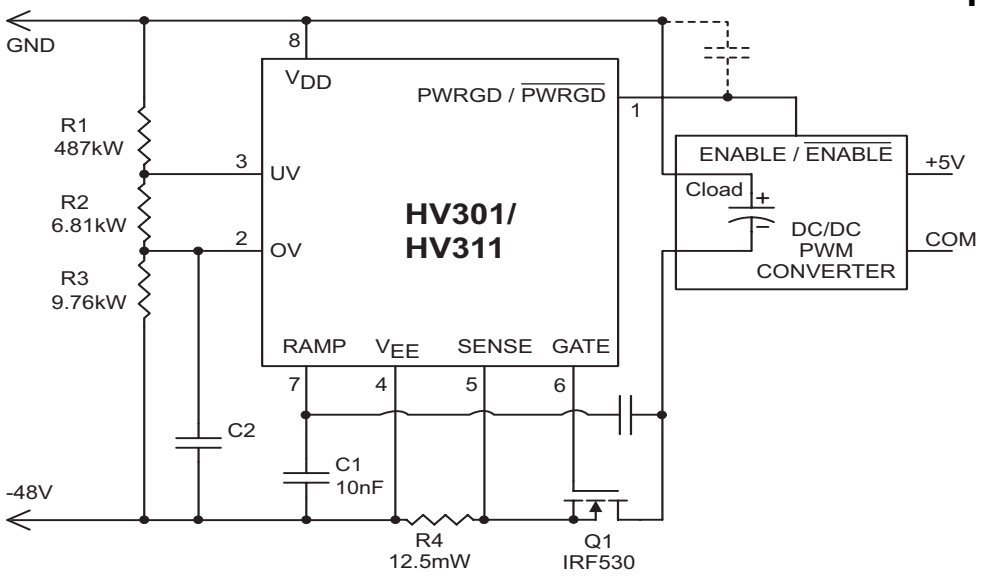


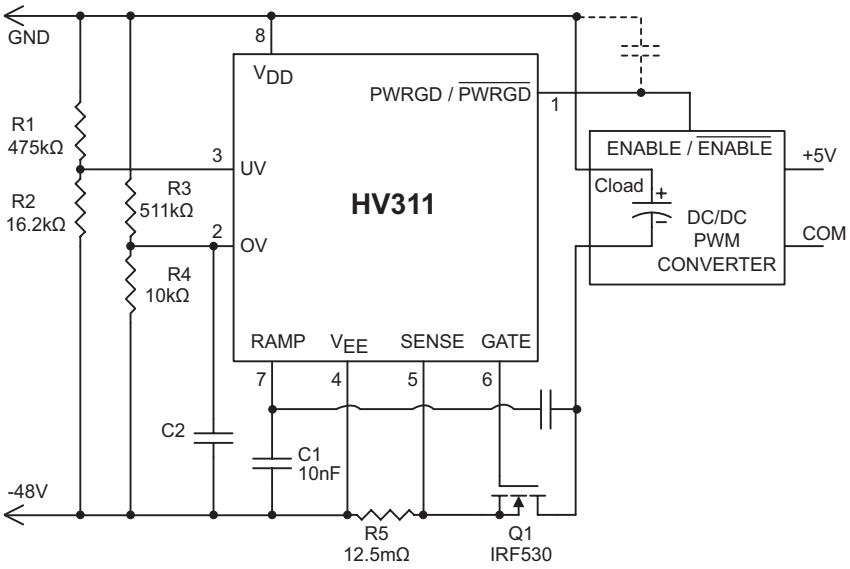
Note: capacitor may be needed to slow PWRGD dv/dt if gate oscillations around are observed when V_{IN} is close to OVLO.

Application Circuit 5

Unfortunately this will also cause some delay in responding to UV conditions. If this UV delay is not acceptable, then separate resistor dividers can be provided for OV and UV with a capacitor connected from OV pin to the V_{EE} pin (**Application Circuit 6**).

Using Short Connector Pin

In some systems short connector pins are used to guarantee that the power pins are fully mated before the hot swap control circuit is enabled. For these systems the positive (V_{DD}) end of the R1, R2, and R3 resistor divider should be connected to the short pin (**Application Circuit 7**).



Note: capacitor may be needed to slow PWRGD dv/dt if gate oscillations around are observed when V_{IN} is close to OVLO.

Application Circuit 5

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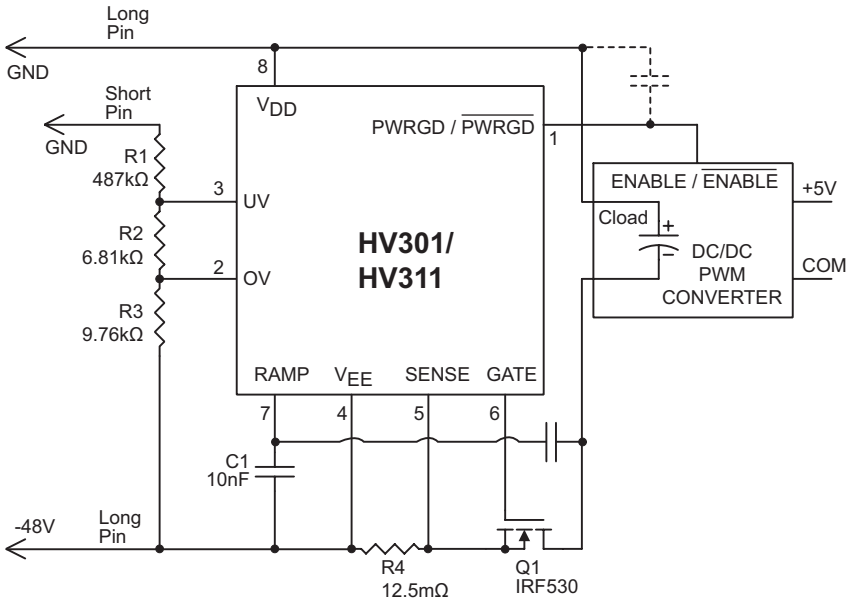
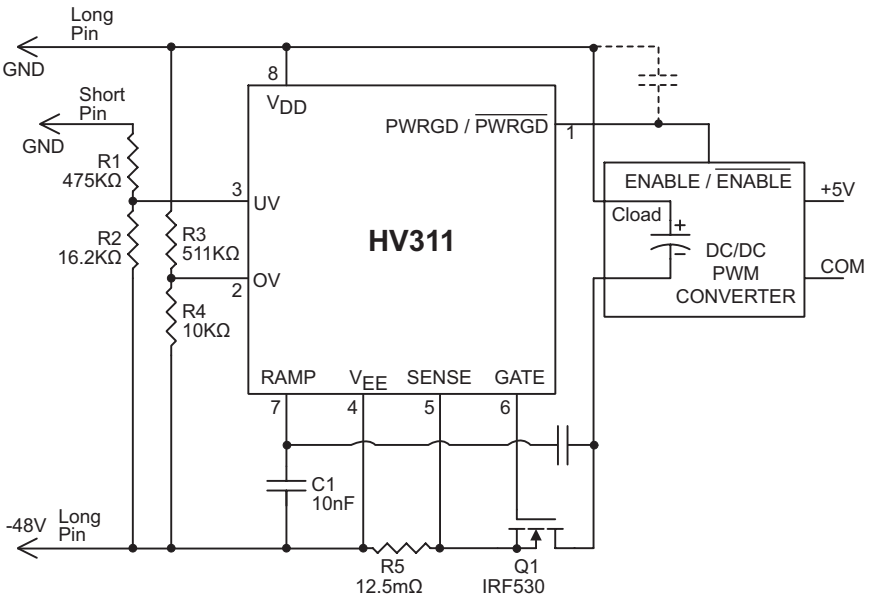


Note: capacitor may be needed to slow PWRGD dv/dt if gate oscillations around are observed when V_{IN} is close to OVLO.

Application Circuit 6

If separate resistor dividers are used for OV and UV, then only the positive (V_{DD}) end of the UV resistor divider should be connected to the short pin (**Application Circuit 8**).

If a system requires the use of a short connector pin on the negative supply lead to guarantee that the power pins are fully mated before the hot swap control circuit is enabled and a single resistor divider string (R1, R2 and R3) is used, then a 6.2V to 10V zener diode must be connected from the UV pin to the V_{EE} pin, as seen below in **Application Circuit 9**.



Note: capacitor may be needed to slow PWRGD dv/dt if gate oscillations around are observed when V_{IN} is close to OVLO.

Application Circuit 8

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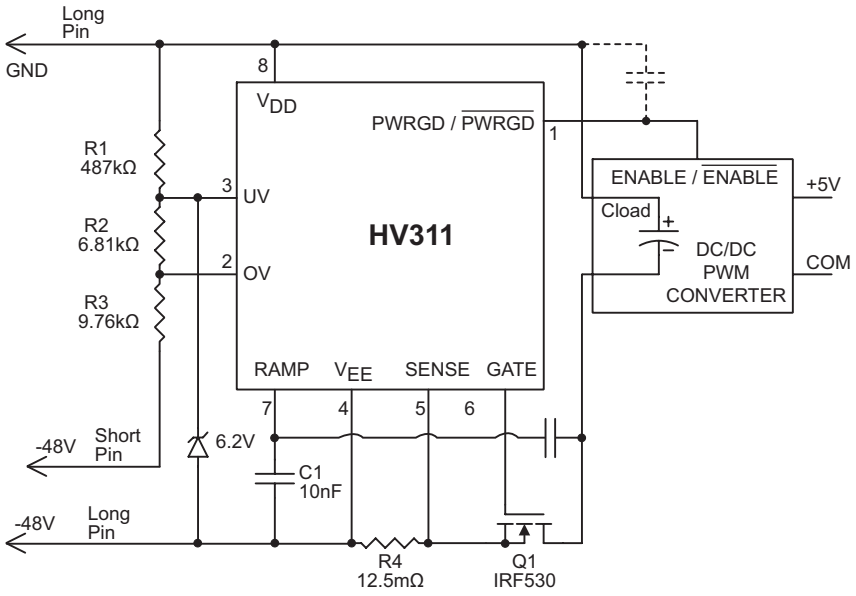


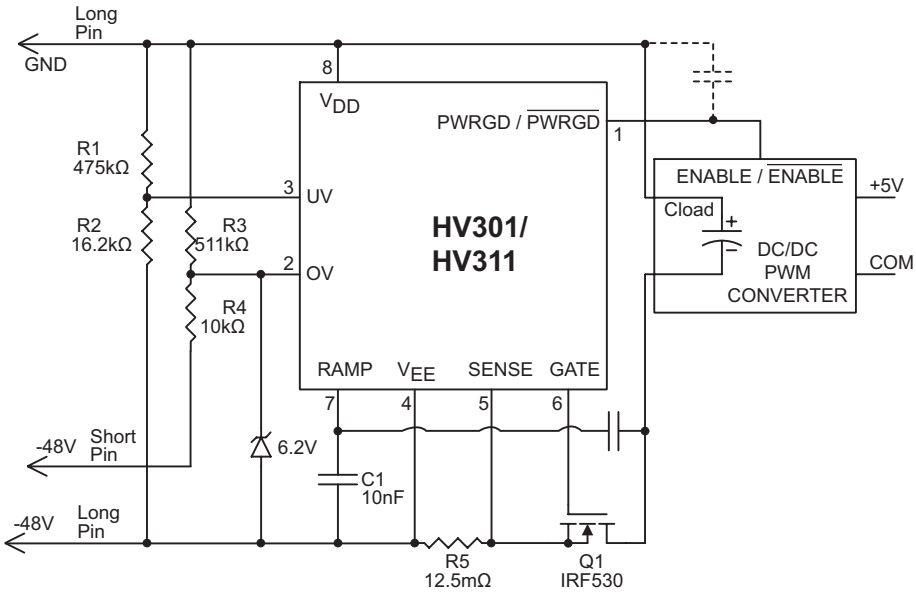
Note: capacitor may be needed to slow PWRGD dv/dt if gate oscillations around are observed when V_{IN} is close to OVLO.

Application Circuit 9

If a system requires the use of a short connector pin on the negative supply lead to guarantee that the power pins are fully mated before the hot swap control circuit is enabled and uses separate resistor dividers for UV and OV, then a 6.2V to 10V zener diode must be connected from the OV pin to the V_{EE} pin and only the OV divider should be connected to the short pin (**Application Circuit 10**).

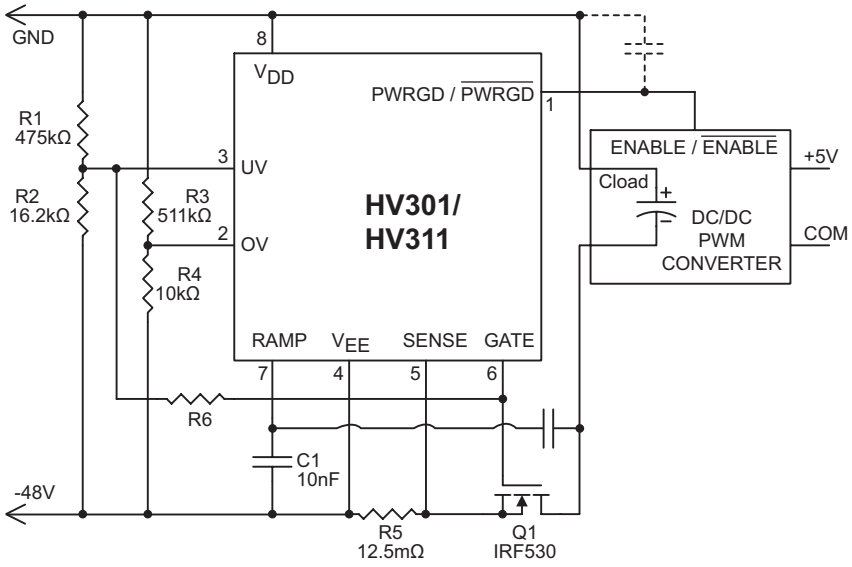
Increasing Under Voltage Hysteresis

If the internally fixed under voltage hysteresis is insufficient for a particular system application, then it may be increased by using separate resistor dividers for OV and UV and providing a resistor feedback path from the GATE pin to the UV pin (**Application Circuit 11**).



Note: capacitor may be needed to slow PWRGD dv/dt if gate oscillations around are observed when V_{IN} is close to OVLO.

Application Circuit 10



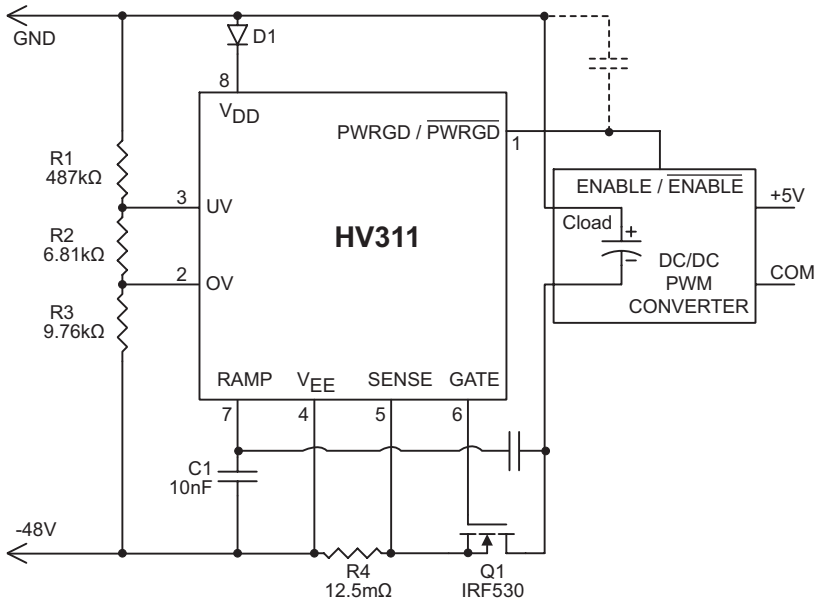
Note: capacitor may be needed to slow PWRGD dv/dt if gate oscillations around are observed when V_{IN} is close to OVLO.

Application Circuit 11

Reverse Polarity Protection

The UV and OV pins are protected against reverse polarity input supplies by internal clamping diodes and the fault currents are sufficiently limited by the impedance of the external resistor divider, however, a low current diode with a 100V breakdown rating must be inserted in series with the V_{DD} pin.

This method (shown in **Application Circuit 12**) will protect the hot swap control circuit however, due to the intrinsic diode in the external MOSFET, the load will not be protected from reverse polarity voltages.



Note: capacitor may be needed to slow PWRGD dv/dt if gate oscillations around are observed when V_{IN} is close to OVLO.

Application Circuit 12

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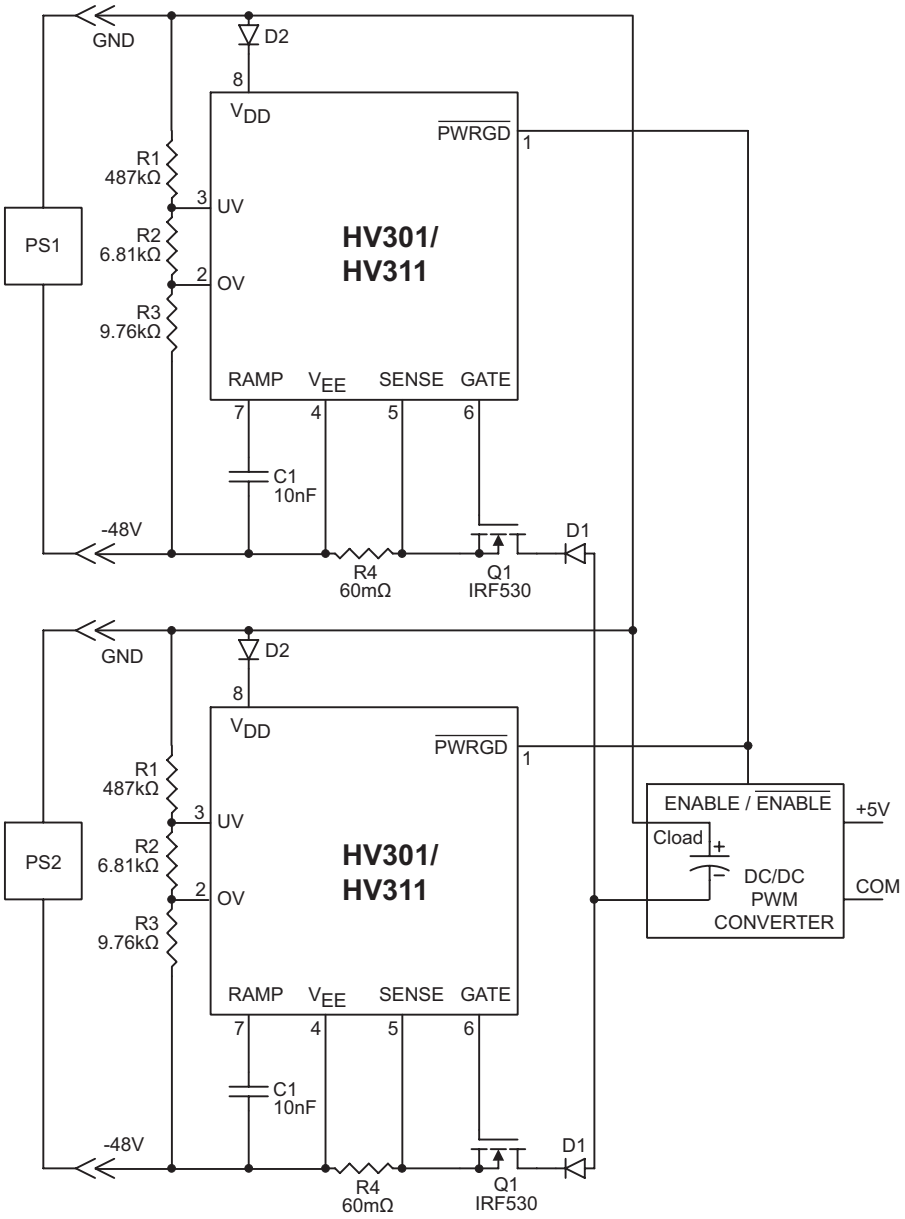
Redundant Supplies

Many systems use redundant primary power supplies or battery backup. When redundant AC powered sources are used they are generally diode OR'ed to the load on the hot terminal.

For these systems, the use of independent hot swap controllers is recommended with the diode OR'ing provided after the hot swap controllers. The HV311 is ideally suited for such applications since two or more active low PWRGD signals can be connected to a single active low ENABLE pin, thus enabling the load as long as at least one primary power source is available. By adding low current 100V diodes in series with the V_{DD} pins, full reverse polarity protection on either power source is also provided (**Application Circuit 13**).



Note: capacitor may be needed to slow PWRGD dv/dt if gate oscillations around are observed when V_{IN} is close to OVLO.

Application Circuit 13

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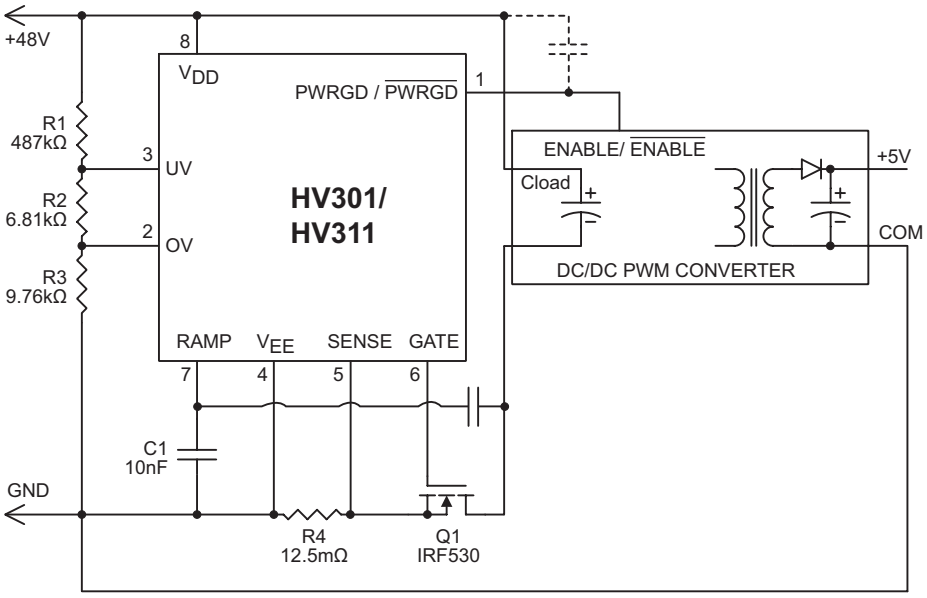
Use with Negative Ground

The HV301 and HV311 may be used with many positive ground systems where DC/DC PWM Converters have isolated outputs and their inputs need not be ground referenced (**Application Circuit 14**).

Current Limit Stability (Method 2 (Servo) Only)

The closed loop current mode control system used in the HV301/HV311 is very stable, especially when driving MOSFETs with high gate capacitances (C_{ISS}). However, a peaking in I_{LIMIT} near the end of the current limit may be noted with some MOSFETs. The current control loop can be frequency compensated to eliminate this peaking by adding a series connected capacitor and resistor between the gate and source of the external MOSFET. The recommended starting values for C and R are 10nF and 1K. These compensation values should be verified by board level testing, which may yield satisfactory results with reduced component values.



Note: capacitor may be needed to slow PWRGD dv/dt if gate oscillations around are observed when V_{IN} is close to OVLO.

Application Circuit 14

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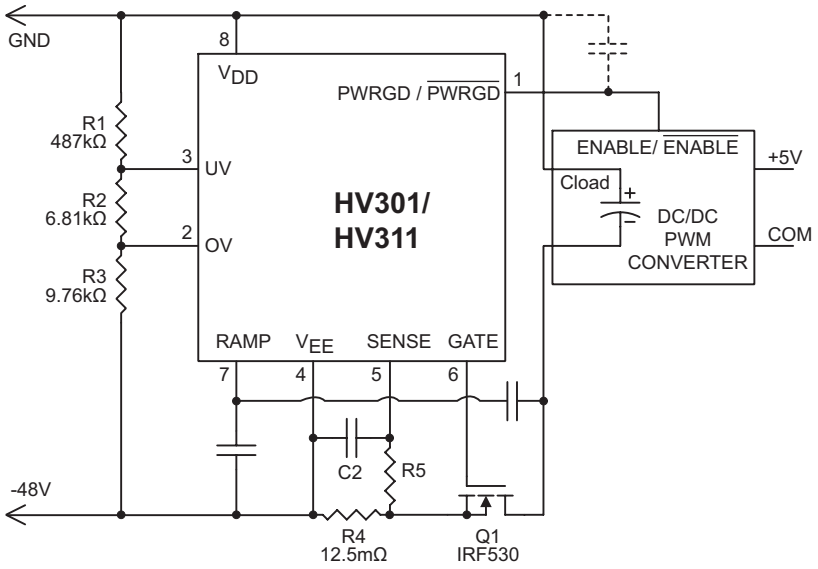
Extending Circuit Breaker Delay

Connecting a resistor in series with the SENSE pin and a capacitor between the SENSE and V_{EE} pins as shown in the following diagram may be used to extend the Circuit Breaker delay time beyond the 5µs internally set delay time (**Application Circuit 15**).

The time delay achievable by this method is limited since this delay circuit will also effect the current control feedback loop and will result in a current overshoot during the external pass device turn on transition to current limit. If the time delay required for the Circuit Breaker causes excessive current overshoot during the turn on transition then the following circuit may be used, where the RC filter is switched on after the completion of the current limit control function of the hot swap controller.

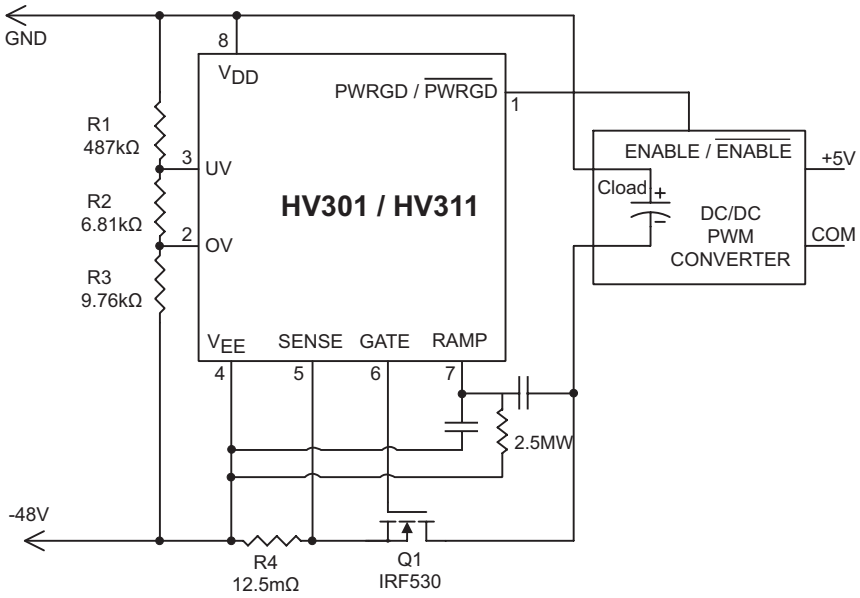


Application Circuit 15

Note: capacitor may be needed to slow PWRGD dv/dt if gate oscillations around are observed when V_{IN} is close to OVLO.

Latched Operation

For those applications that need to disable the automatic retry capability, the following circuit disables the auto retry feature.



Application Circuit 17

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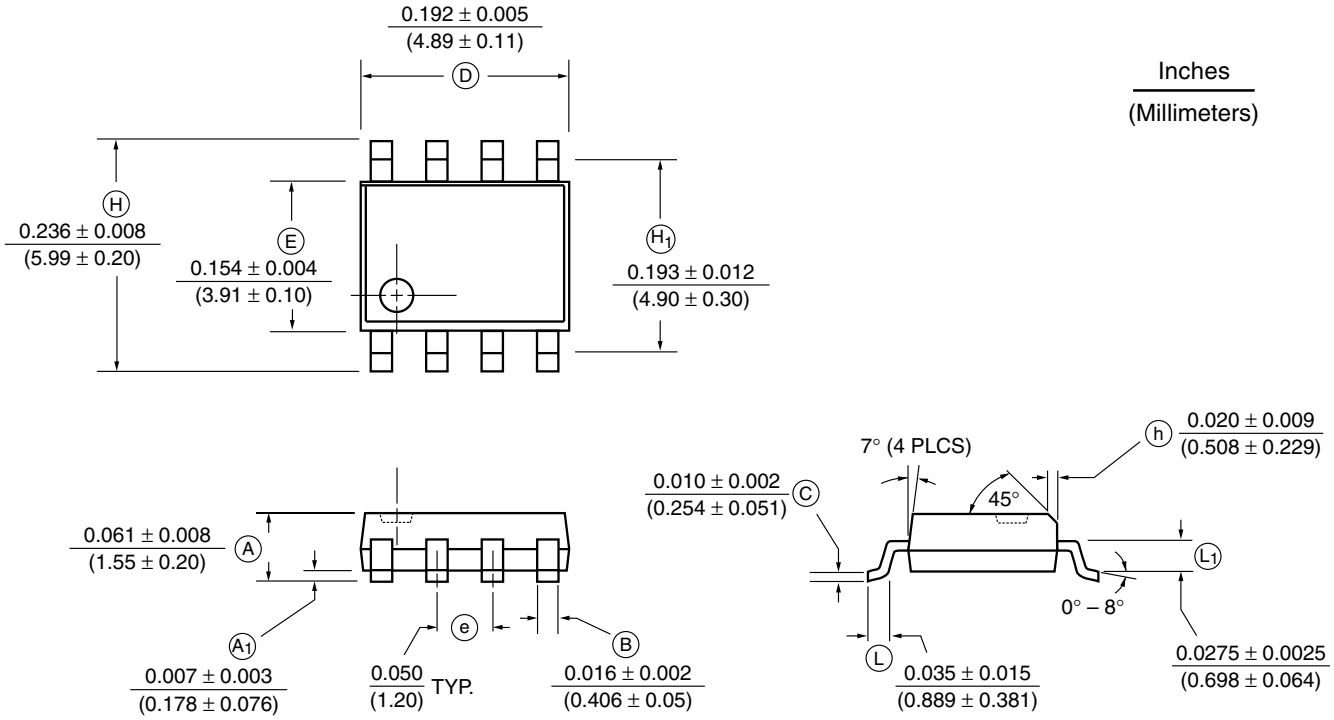
Note: capacitor may be needed to slow PWRGD dv/dt if gate oscillations around are observed when V_{IN} is close to OVLO.

Package Dimensions



Circled letters (e.g. Ⓑ denote JEDEC reference dimensons.

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Technical Update / Alert

This alert applies to the HV301, HV302, HV311, and HV312 Hotswap Controllers

The internal circuit breaker may trip unintentionally in situations when the voltage at the V_{DD} pin rises slowly as power is applied.

This unintended tripping of the circuit breaker causes the power-on sequence to be delayed by an additional Automatic Restart Delay. The extra delay can be observed by viewing the voltage waveform at the RAMP pin.

Subsequent to this delay, this device will perform a regular start-up, thereby providing power to the load.

The inadvertant tripping of the circuit breaker does not occur when the input voltage slew rate is greater than 400V per ms. In a typical hotswap application, the rise of the input voltage occurs in a couple of microseconds, and the slew rate is well in excess of of the value necessary to cause tripping of the circuit breaker.

If technical assistance is required, please contact our applications department by e-mail at apps@supertex.com, or by telephone at 408-222-4895.

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