**Flash**

**2.5V Only 4 Mbit Serial Flash Memory with Dual Output**

## ■ FEATURES

- Single supply voltage 2.3~3.3V
- Standard, Dual SPI
- Speed
  - Read max frequency: 33MHz
  - Fast Read max frequency: 50MHz; 86MHz; 100MHz
  - Fast Read Dual max frequency: 50MHz / 86MHz/ 100MHz (100MHz / 172MHz/ 200MHz equivalent Dual SPI)
- Low power consumption
  - Active current: 25 mA
  - Standby current: 5μA
  - Deep Power Down current: 3μA
- Reliability
  - 100,000 typical program/erase cycles
  - 20 years Data Retention
- Program
  - Byte programming time: 7μs (typical)
  - Page programming time: 0.8 ms (typical)
- Erase
  - Chip erase time 3 sec (typical)
  - Block erase time 0.4 sec (typical)
  - Sector erase time 40 ms (typical)
- Page Programming
  - 256 byte per programmable page
- SPI Serial Interface
  - SPI Compatible: Mode 0 and Mode 3
- End of program or erase detection
- Write Protect ( $\overline{WP}$ )
- Hold Pin ( $\overline{HOLD}$ )
- All Pb-free products are RoHS-Compliant

## ■ ORDERING INFORMATION

| Product ID | Speed | Package | | COMMENTS |
|---|---|---|---|---|
| F25S04PA –50PG | 50MHz | 8-lead SOIC | 150 mil | Pb-free |
| F25S04PA –86PG | 86MHz | 8-lead SOIC | 150 mil | Pb-free |
| F25S04PA –100PG | 100MHz | 8-lead SOIC | 150 mil | Pb-free |
| F25S04PA –50PAG | 50MHz | 8-lead SOIC | 200 mil | Pb-free |
| F25S04PA –86PAG | 86MHz | 8-lead SOIC | 200 mil | Pb-free |
| F25S04PA –100PAG | 100MHz | 8-lead SOIC | 200 mil | Pb-free |
| F25S04PA –50DG | 50MHz | 8-lead PDIP | 300 mil | Pb-free |
| F25S04PA –86DG | 86MHz | 8-lead PDIP | 300 mil | Pb-free |
| F25S04PA –100DG | 100MHz | 8-lead PDIP | 300 mil | Pb-free |
| F25S04PA –50HG | 50MHz | 8-lead DFN | 5x6 mm | Pb-free |
| F25S04PA –86HG | 86MHz | 8-lead DFN | 5x6 mm | Pb-free |
| F25S04PA –100HG | 100MHz | 8-lead DFN | 5x6 mm | Pb-free |

## ■ GENERAL DESCRIPTION

The F25S04PA is a 4Megabit, 2.5V only CMOS Serial Flash memory device. The device supports the standard Serial Peripheral Interface (SPI), and a Dual SPI. ESMT's memory devices reliably store memory data even after 100,000 programming and erase cycles.

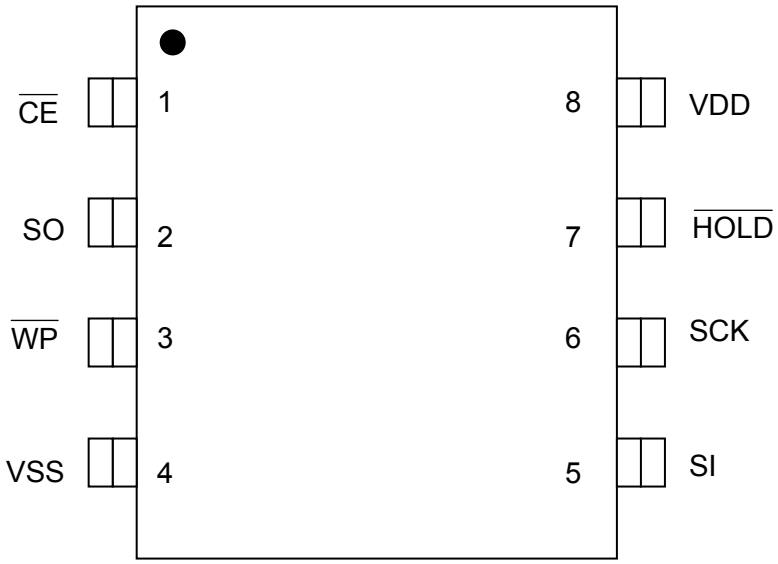
The memory array can be organized into 2,048 programmable pages of 256 byte each. 1 to 256 byte can be programmed at a time with the Page Program instruction.

The device features sector erase architecture. The memory array is divided into 128 uniform sectors with 4K byte each; 8 uniform blocks with 64K byte each. Sectors can be erased individually without affecting the data in other sectors. Blocks can be erased individually without affecting the data in other blocks. Whole chip erase capabilities provide the flexibility to revise the data in the device. The device has Sector, Block or Chip Erase but no page erase.

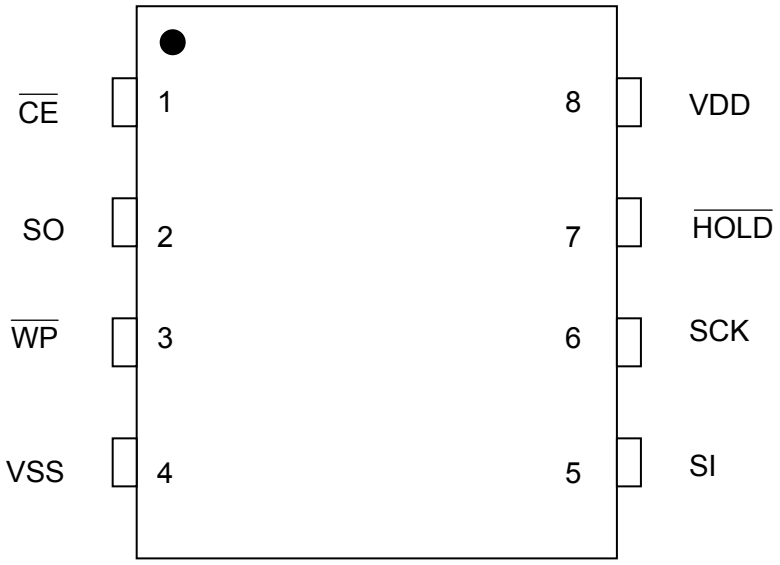
The sector protect/unprotect feature disables both program and erase operations in any combination of the sectors of the memory.

## ■ PIN CONFIGURATIONS

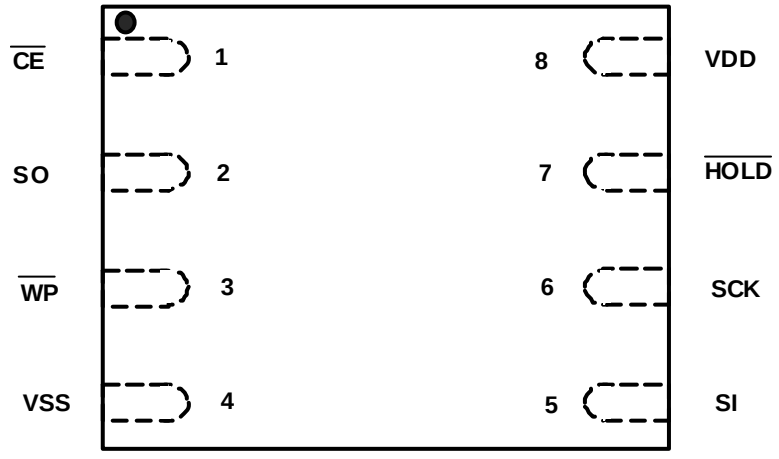
### 8- LEAD SOIC



**8- LEAD PDIP**



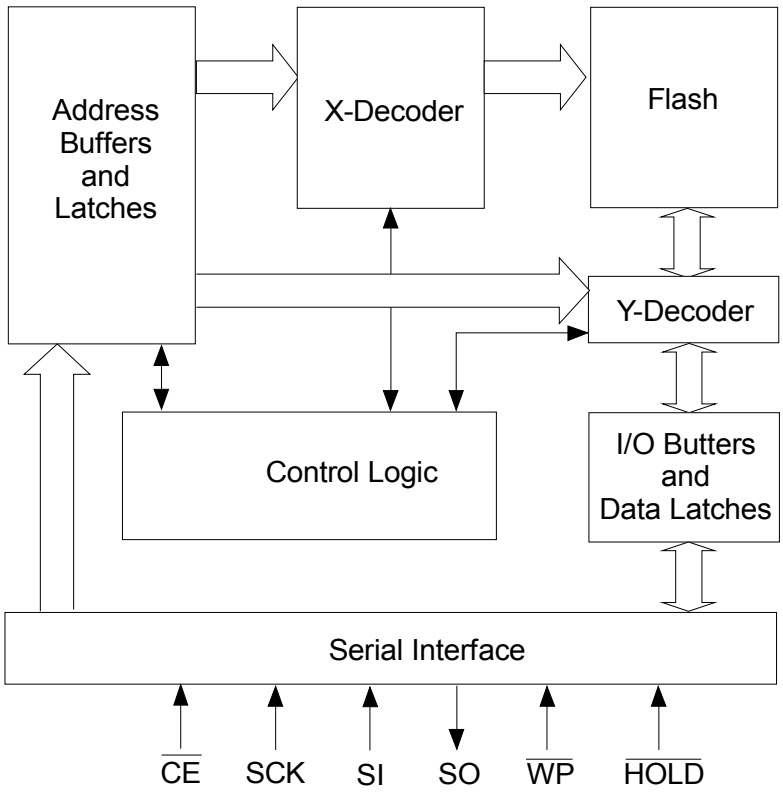

**8- LEAD DFN**



## ■ PIN DESCRIPTION

| Symbol | Pin Name | Functions |
|---|---|---|
| SCK | Serial Clock | To provide the timing for serial input and output operations |
| SI | Serial Data Input | To transfer commands, addresses or data serially into the device.<br>Data is latched on the rising edge of SCK. |
| SO | Serial Data Output | To transfer data serially out of the device.<br>Data is shifted out on the falling edge of SCK. |
| $\overline{CE}$ | Chip Enable | To activate the device when $\overline{CE}$ is low. |
| $\overline{WP}$ | Write Protect | The Write Protect ( $\overline{WP}$ ) pin is used to enable/disable BPL bit in the status register. |
| $\overline{HOLD}$ | Hold | To temporality stop serial communication with SPI flash memory without resetting the device. |
| VDD | Power Supply | To provide power. |
| VSS | Ground | |

## ■ FUNCTIONAL BLOCK DIAGRAM



## ■ SECTOR STRUCTURE

**Table 1: F25S04PA Sector Address Table**

| Block | Sector | Sector Size (Kbytes) | Address range | Block Address | | |
|---|---|---|---|---|---|---|
| | | | | A18 | A17 | A16 |
| 7 | 127 | 4KB | 07F000H – 07FFFFH | 1 | 1 | 1 |
| | : | : | : | | | |
| | 112 | 4KB | 070000H – 070FFFH | | | |
| 6 | 111 | 4KB | 06F000H – 06FFFFH | 1 | 1 | 0 |
| | : | : | : | | | |
| | 96 | 4KB | 060000H – 060FFFH | | | |
| 5 | 95 | 4KB | 05F000H – 05FFFFH | 1 | 0 | 1 |
| | : | : | : | | | |
| | 80 | 4KB | 050000H – 050FFFH | | | |
| 4 | 79 | 4KB | 04F000H – 04FFFFH | 1 | 0 | 0 |
| | : | : | : | | | |
| | 64 | 4KB | 040000H – 040FFFH | | | |
| 3 | 63 | 4KB | 03F000H – 03FFFFH | 0 | 1 | 1 |
| | : | : | : | | | |
| | 48 | 4KB | 030000H – 030FFFH | | | |
| 2 | 47 | 4KB | 02F000H – 02FFFFH | 0 | 1 | 0 |
| | : | : | : | | | |
| | 32 | 4KB | 020000H – 020FFFH | | | |
| 1 | 31 | 4KB | 01F000H – 01FFFFH | 0 | 0 | 1 |
| | : | : | : | | | |
| | 16 | 4KB | 010000H – 010FFFH | | | |
| 0 | 15 | 4KB | 00F000H – 00FFFFH | 0 | 0 | 0 |
| | : | : | : | | | |
| | 0 | 4KB | 000000H – 000FFFH | | | |

## ■ STATUS REGISTER

The software status register provides status on whether the flash memory array is available for any Read or Write operation, whether the device is Write enabled, and the state of the memory Write protection. During an internal Erase or Program operation, the status register may be read only to determine the completion of an operation in progress. Table 2 describes the function of each bit in the software status register.

**Table 2: Software Status Register**

| Bit | Name | Function | Default at Power-up | Read/Write |
|---|---|---|---|---|
| 0 | BUSY | 1 = Internal Write operation is in progress<br>0 = No internal Write operation is in progress | 0 | R |
| 1 | WEL | 1 = Device is memory Write enabled<br>0 = Device is not memory Write enabled | 0 | R |
| 2 | BP0 | Indicate current level of block write protection (See Table 3) | 0 | R/W |
| 3 | BP1 | Indicate current level of block write protection (See Table 3) | 0 | R/W |
| 4 | BP2 | Indicate current level of block write protection (See Table 3) | 0 | R/W |
| 5 | TB | Top / Bottom write protect | 0 | R/W |
| 6 | RESERVED | Reserved for future use | 0 | N/A |
| 7 | BPL | 1 = BP2,BP1,BP0 and TB are read-only bits<br>0 = BP2,BP1,BP0 and TB are read/writable | 0 | R/W |

Note:
1. Only BP0, BP1, BP2, TB and BPL are writable.
2. BP0, BP1, BP2, TB and BPL are non-volatile; others volatile.
3. All area are protected at power-on (BP2=BP1=BP0=1)

### WRITE ENABLE LATCH (WEL)

The Write-Enable-Latch bit indicates the status of the internal memory Write Enable Latch. If this bit is set to "1", it indicates the device is Write enabled. If the bit is set to "0" (reset), it indicates the device is not Write enabled and does not accept any memory Write (Program/ Erase) commands. This bit is automatically reset under the following conditions:

- Power-up
- Write Disable (WRDI) instruction completion
- Page Program instruction completion
- Sector Erase instruction completion
- Block Erase instruction completion
- Chip Erase instruction completion
- Write Status Register instructions

### BUSY

The Busy bit determines whether there is an internal Erase or Program operation in progress. A "1" for the Busy bit indicates the device is busy with an operation in progress. A "0" indicates the device is ready for the next valid operation.

### Top/Bottom Block Protect (TB)

The Top/Bottom bit (TB) controls if the Block-Protection (BP2, BP1, BP0) bits protect from the Top (TB=0) or the Bottom (TB=1) of the array as show in Table 3, The TB bit can be set with Write Status Register (WRSR) instruction. The TB bit can not be written to if the Block- Protection-Look (BPL) bit is 1 or $\overline{WP}$ is low.

**Table 3: F25S04PA Block Protection Table**

| Protection Level | Status Register Bit | | | | Protected Memory Area | |
|---|---|---|---|---|---|---|
| | TB | BP2 | BP1 | BP0 | Block Range | Address Range |
| 0 | X | 0 | 0 | 0 | None | None |
| Upper 1/8 | 0 | 0 | 0 | 1 | Block 7 | 070000H – 07FFFFH |
| Upper 1/4 | 0 | 0 | 1 | 0 | Block 6~7 | 060000H – 07FFFFH |
| Upper 1/2 | 0 | 0 | 1 | 1 | Block 4~7 | 040000H – 07FFFFH |
| Lower 1/8 | 1 | 0 | 0 | 1 | Block 0 | 000000H – 00FFFFH |
| Lower 1/4 | 1 | 0 | 1 | 0 | Block 0~1 | 000000H – 01FFFFH |
| Lower 1/2 | 1 | 0 | 1 | 1 | Block 0~3 | 000000H – 03FFFFH |
| All Blocks | X | 1 | X | X | Block 0~7 | 000000H – 07FFFFH |

### Block Protection (BP2, BP1, BP0)

The Block-Protection (BP2, BP1, BP0) bits define the size of the memory area, as defined in Table 3, to be software protected against any memory Write (Program or Erase) operations. The Write Status Register (WRSR) instruction is used to program the BP2, BP1, BP0 bits as long as $\overline{WP}$ is high or the Block-Protection-Look (BPL) bit is 0. Chip Erase can only be executed if Block-Protection bits are all 0. After power-up, BP2, BP1 and BP0 are set to 0.

### Block Protection Lock-Down (BPL)

$\overline{WP}$ pin driven low ($V_{IL}$), enables the Block-Protection-Lock-Down (BPL) bit. When BPL is set to 1, it prevents any further alteration of the TB, BPL, BP2, BP1, and BP0 bits. When the $\overline{WP}$ pin is driven high ($V_{IH}$), the BPL bit has no effect and its value is “Don’t Care”. After power-up, the BPL bit is reset to 0.

## ■ HOLD OPERATION

$\overline{HOLD}$ pin is used to pause a serial sequence underway with the SPI flash memory without resetting the clocking sequence. To activate the $\overline{HOLD}$ mode, $\overline{CE}$ must be in active low state. The $\overline{HOLD}$ mode begins when the SCK active low state coincides with the falling edge of the $\overline{HOLD}$ signal. The HOLD mode ends when the $\overline{HOLD}$ signal's rising edge coincides with the SCK active low state.

If the falling edge of the $\overline{HOLD}$ signal does not coincide with the SCK active low state, then the device enters Hold mode when the SCK next reaches the active low state.

Similarly, if the rising edge of the $\overline{HOLD}$ signal does not coincide with the SCK active low state, then the device exits in Hold mode when the SCK next reaches the active low state. See Figure 1 for Hold Condition waveform.

Once the device enters Hold mode, SO will be in high impedance state while SI and SCK can be $V_{IL}$ or $V_{IH}$.

If $\overline{CE}$ is driven active high during a Hold condition, it resets the internal logic of the device. As long as $\overline{HOLD}$ signal is low, the memory remains in the Hold condition. To resume communication with the device, $\overline{HOLD}$ must be driven active high, and $\overline{CE}$ must be driven active low. See Figure 22 for Hold timing.

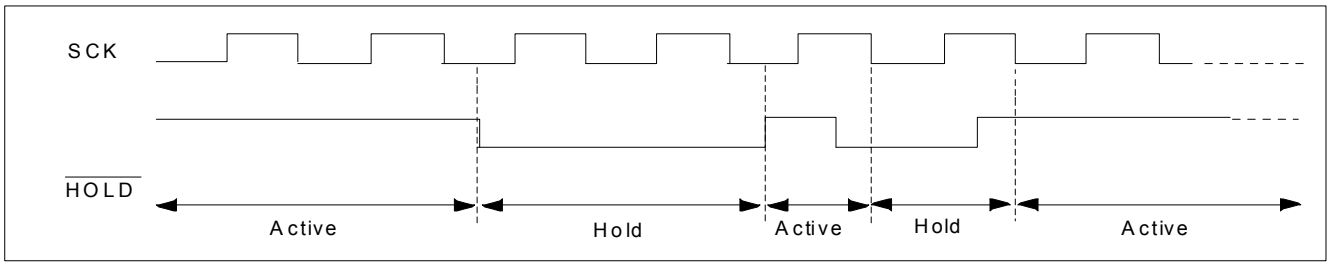



**Figure 1: HOLD Condition Waveform**

## ■ WRITE PROTECTION

The device provides software Write Protection.

The Write-Protect pin ($\overline{WP}$) enables or disables the lock-down function of the status register. The Block-Protection bits (BP2, BP1, BP0, and BPL) in the status register provide Write protection to the memory array and the status register. See Table 4 for Block-Protection description.

### Write Protect Pin ($\overline{WP}$)

The Write-Protect ($\overline{WP}$) pin enables the lock-down function of the BPL bit (bit 7) in the status register. When $\overline{WP}$ is driven low, the execution of the Write Status Register (WRSR) instruction is determined by the value of the BPL bit (see Table 4). When $\overline{WP}$ is high, the lock-down function of the BPL bit is disabled.

**Table 4: Conditions to Execute Write-Status-Register (WRSR) Instruction**

| $\overline{WP}$ | BPL | Execute WRSR Instruction |
|---|---|---|
| L | 1 | Not Allowed |
| L | 0 | Allowed |
| H | X | Allowed |

## ■ INSTRUCTIONS

Instructions are used to Read, Write (Erase and Program), and configure the F25S04PA. The instruction bus cycles are 8 bits each for commands (Op Code), data, and addresses. Prior to executing any Page Program, Write Status Register, Sector Erase, Block Erase, or Chip Erase instructions, the Write Enable (WREN) instruction must be executed first. The complete list of the instructions is provided in Table 5. All instructions are synchronized off a high to low transition of $\overline{CE}$. Inputs will be accepted on the rising edge of SCK starting with the most significant bit. $\overline{CE}$ must be driven low before an instruction is entered and must be driven high after the last bit of the instruction has been shifted in (except for Read, Read ID, Read Status Register, Read Electronic Signature instructions). Any low to high transition on $\overline{CE}$, before receiving the last bit of an instruction bus cycle, will terminate the instruction in progress and return the device to the standby mode.

Instruction commands (Op Code), addresses, and data are all input from the most significant bit (MSB) first.

**Table 5: Device Operation Instructions**

| Operation | Max. Freq | Bus Cycle [1~3] 1 | | 2 | | 3 | | 4 | | 5 | | 6 | | N | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $S_{IN}$ | $S_{OUT}$ | $S_{IN}$ | $S_{OUT}$ | $S_{IN}$ | $S_{OUT}$ | $S_{IN}$ | $S_{OUT}$ | $S_{IN}$ | $S_{OUT}$ | $S_{IN}$ | $S_{OUT}$ | $S_{IN}$ | $S_{OUT}$ |
| Read | 33 MHz | 03H | Hi-Z | $A_{23}$-$A_{16}$ | Hi-Z | $A_{15}$-$A_8$ | Hi-Z | $A_7$-$A_0$ | Hi-Z | X | $D_{OUT0}$ | X | $D_{OUT1}$ | X | cont. |
| Fast Read | | 0BH | Hi-Z | $A_{23}$-$A_{16}$ | Hi-Z | $A_{15}$-$A_8$ | Hi-Z | $A_7$-$A_0$ | Hi-Z | X | X | X | $D_{OUT0}$ | X | cont. |
| Fast Read Dual Output[11,12] | | 3BH | | $A_{23}$-$A_{16}$ | | $A_{15}$-$A_8$ | | $A_7$-$A_0$ | | X | | $D_{OUT0\sim1}$ | | cont. | |
| Sector Erase[4] (4K Byte) | | 20H | Hi-Z | $A_{23}$-$A_{16}$ | Hi-Z | $A_{15}$-$A_8$ | Hi-Z | $A_7$-$A_0$ | Hi-Z | - | - | - | - | - | - |
| Block Erase[4,] (64K Byte) | | D8H | Hi-Z | $A_{23}$-$A_{16}$ | Hi-Z | $A_{15}$-$A_8$ | Hi-Z | $A_7$-$A_0$ | Hi-Z | - | - | - | - | - | - |
| Chip Erase | | 60H / C7H | Hi-Z | - | - | - | - | - | - | - | - | - | - | - | - |
| Page Program (**PP**) | 50MHz | 02H | Hi-Z | $A_{23}$-$A_{16}$ | Hi-Z | $A_{15}$-$A_8$ | Hi-Z | $A_7$-$A_0$ | Hi-Z | $D_{IN0}$ | Hi-Z | $D_{IN1}$ | Hi-Z | Up to 256 bytes | Hi-Z |
| Read Status Register (**RDSR**) [6] | ~ | 05H | Hi-Z | X | $D_{OUT}$ | - | - | - | - | - | - | - | - | - | - |
| Write Status Register (**WRSR**) | | 01H | Hi-Z | $D_{IN}$ | Hi-Z | - | - | -. | - | - | - | - | - | - | - |
| Write Enable (**WREN**) [9] | 100MHz | 06H | Hi-Z | - | - | - | - | - | - | - | - | - | - | - | - |
| Write Disable (**WRDI**) | | 04H | Hi-Z | - | - | - | - | - | - | - | - | - | - | - | - |
| Deep Power Down (**DP**) | | B9h | Hi-Z | - | - | - | - | - | - | - | - | - | - | - | - |
| Release from Deep Power Down (**RDP**) | | ABH | Hi-Z | - | - | - | - | - | - | - | - | - | - | - | - |
| Read Electronic Signature (**RES**) [7] | | ABH | Hi-Z | X | X | X | X | X | X | X | 12H | - | - | - | - |
| Jedec Read ID (**JEDEC-ID**) [8] | | 9FH | Hi-Z | X | 8CH | X | 20H | X | 13H | - | - | - | - | - | - |
| Read ID (**RDID**) [10] | | 90H | Hi-Z | 00H | Hi-Z | 00H | Hi-Z | 00H | Hi-Z | X | 8CH | X | 12H | - | - |
| | | | | | | | | 01H | Hi-Z | X | 12H | X | 8CH | - | - |

Note:

1. Operation: $S_{IN}$ = Serial In, $S_{OUT}$ = Serial Out, Bus Cycle 1 = Op Code
2. X = Dummy Input Cycles ($V_{IL}$ or $V_{IH}$); - = Non-Applicable Cycles (Cycles are not necessary); cont. = continuous
3. One bus cycle is eight clock periods.
4. Sector Earse addresses: use $A_{MS}$ -$A_{12}$, remaining addresses can be $V_{IL}$ or $V_{IH}$
   Block Earse addresses: use $A_{MS}$ -$A_{16}$, remaining addresses can be $V_{IL}$ or $V_{IH}$
5. To continue programming to the next sequential address location, enter the 8-bit command, followed by the data to be programmed.
6. The Read-Status-Register is continuous with ongoing clock cycles until terminated by a low to high transition on $\overline{CE}$.
7. The Read-Electronic-Signature is continuous with on going clock cycles until terminated by a low to high transition on $\overline{CE}$.
8. The Jedec-Read-ID is output first byte 8CH as manufacture ID; second byte 20H as top memory type; third byte 13H as memory capacity.
9. The Write-Enable (WREN) instruction and the Write-Status-Register (WRSR) instruction must work in conjunction of each other. The WRSR instruction must be executed immediately (very next bus cycle) after the WREN instruction to make both

instructions effective. WREN can enable WRSR, user just need to execute it. A successful WRSR can reset WREN.

10. The Manufacture ID and Device ID output will repeat continuously until $\overline{CE}$ terminates the instruction.
11. Dual commands use bidirectional IO pins. $D_{OUT}$ and cont. are serial data out; others are serial data in.
12. Dual output data:
    $IO_0 = (D_6, D_4, D_2, D_0), (D_6, D_4, D_2, D_0)$
    $IO_1 = (D_7, D_5, D_3, D_1), (D_7, D_5, D_3, D_1)$
    $D_{OUT0}$ $D_{OUT1}$

**Read (33MHz)**

The Read instruction supports up to 33 MHz, it outputs the data starting from the specified address location. The data output stream is continuous through all addresses until terminated by a low to high transition on $\overline{CE}$. The internal address pointer will automatically increment until the highest memory address is reached. Once the highest memory address is reached, the address pointer will automatically increment to the beginning (wrap-around) of the address space, i.e. for 4Mbit density, once the data from address location 7FFFFH had been read, the next output will be from address location 00000H.

The Read instruction is initiated by executing an 8-bit command, 03H, followed by address bits [$A_{23}$ -$A_0$]. $\overline{CE}$ must remain active low for the duration of the Read cycle. See Figure 2 for the Read sequence.

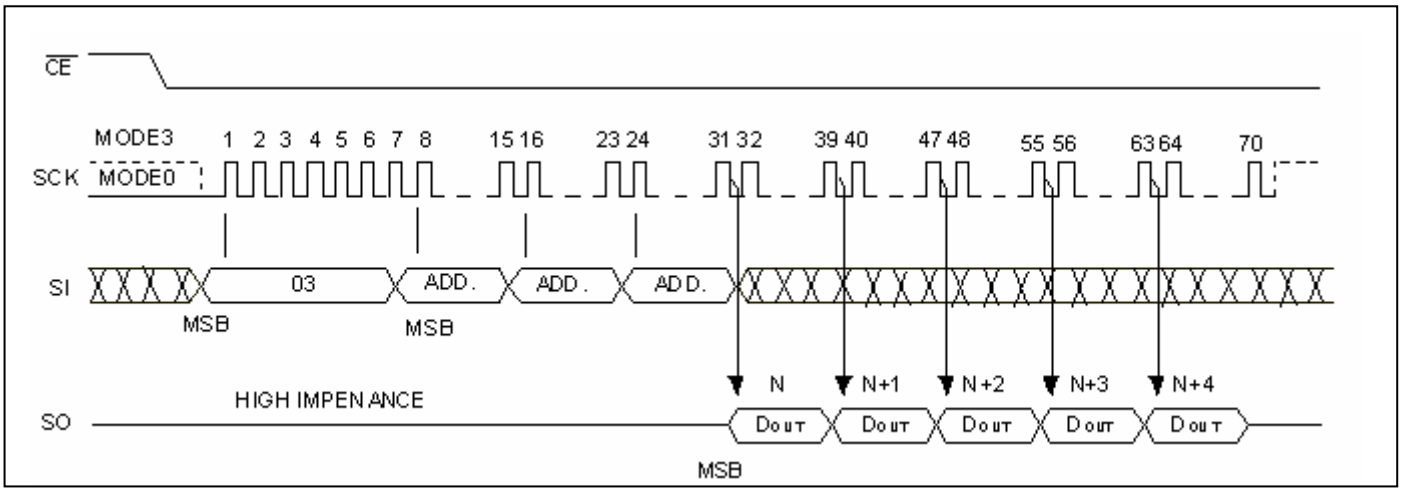



**Figure 2: Read Sequence**

**Fast Read (50 MHz ~ 100 MHz)**

The Fast Read instruction supporting up to 100 MHz is initiated by executing an 8-bit command, 0BH, followed by address bits [$A_{23}$ -$A_0$] and a dummy byte. $\overline{CE}$ must remain active low for the duration of the Fast Read cycle. See Figure 3 for the Fast Read sequence.

Following a dummy byte (8 clocks input dummy cycle), the Fast Read instruction outputs the data starting from the specified address location. The data output stream is continuous through all addresses until terminated by a low to high transition on $\overline{CE}$. The internal address pointer will automatically increment until the highest memory address is reached. Once the highest memory address is reached, the address pointer will automatically increment to the beginning (wrap-around) of the address space, i.e. for 4Mbit density, once the data from address location 7FFFFH has been read, the next output will be from address location 000000H.

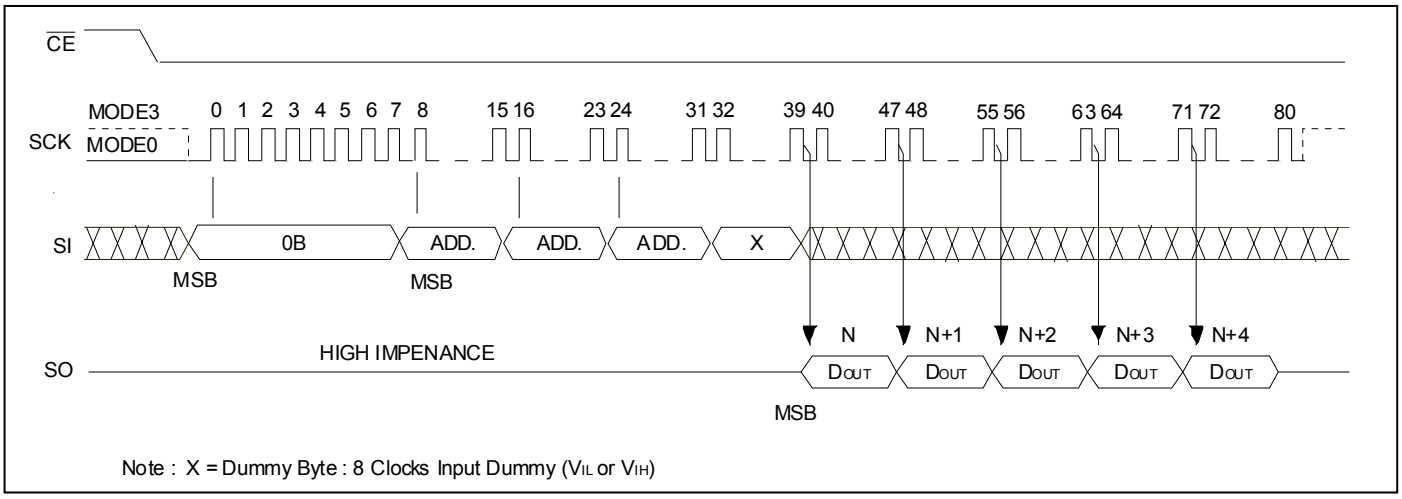



**Figure 3: Fast Read Sequence**

**Fast Read Dual Output (50 MHz ~ 100 MHz)**

The Fast Read Dual Output (3BH) instruction is similar to the standard Fast Read (0BH) instruction except the data is output on SI and SO pins. This allows data to be transferred from the device at twice the rate of standard SPI devices. This instruction is for quickly downloading code from Flash to RAM upon power-up or for applications that cache code- segments to RAM for execution.

The Fast Read Dual Output instruction is initiated by executing an 8-bit command, 3BH, followed by address bits [$A_{23}$ -$A_0$] and a dummy byte. $\overline{CE}$ must remain active low for the duration of the Fast Read Dual Output cycle. See Figure 4 for the Fast Read Dual Output sequence.

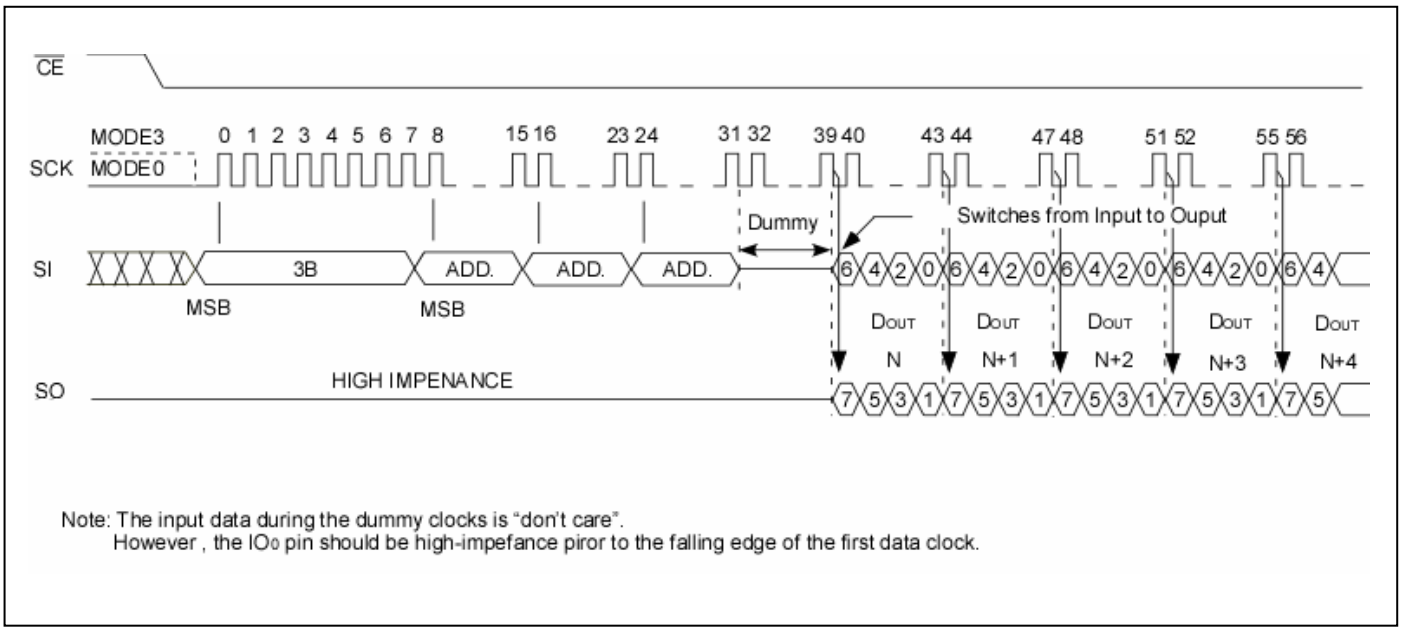



**Figure 4: Fast Read Dual Output Sequence**

**Page Program (PP)**

The Page Program instruction allows many bytes to be programmed in the memory. The bytes must be in the erased state (FFH) when initiating a Program operation. A Page Program instruction applied to a protected memory area will be ignored.

Prior to any Write operation, the Write Enable (WREN) instruction must be executed. $\overline{CE}$ must remain active low for the duration of the Page Program instruction. The Page Program instruction is initiated by executing an 8-bit command, 02H, followed by address bits [$A_{23}$-$A_0$]. Following the address, at least one byte Data is input (the maximum of input data can be up to 256 bytes). If the 8 least significant address bits [$A_7$-$A_0$] are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits [$A_7$-$A_0$] are all zero).

If more than 256 bytes Data are sent to the device, previously latched data are discarded and the last 256 bytes Data are guaranteed to be programmed correctly within the same page. If less than 256 bytes Data are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page.

$\overline{CE}$ must be driven high before the instruction is executed. The user may poll the Busy bit in the software status register or wait $T_{PP}$ for the completion of the internal self-timed Page Program operation. While the Page Program cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the Busy bit. It is recommended to wait for a duration of $T_{BP}$ before reading the status register to check the BUSY bit. The BUSY bit is a 1 during the Page Program cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Page Program cycle has finished, the Write-Enable-Latch (WEL) bit in the Status Register is cleared to 0. See Figure 7 for the Page Program sequence.

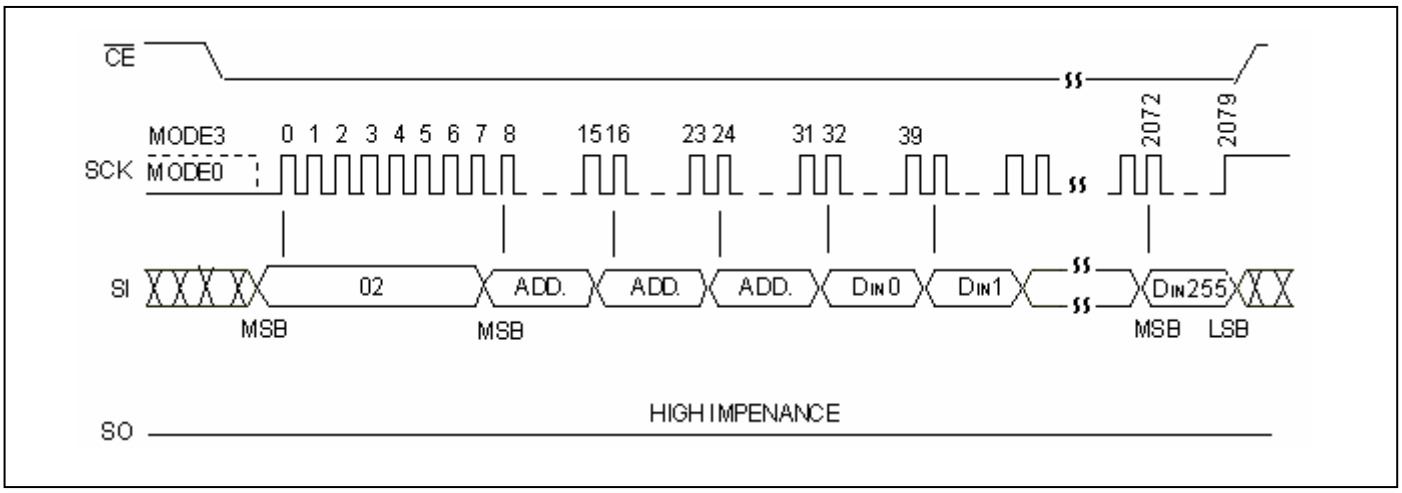



**Figure 7: Page Program Sequence**

### 64K Byte Block Erase

The 64K-byte Block Erase instruction clears all bits in the selected block to FFH. A Block Erase instruction applied to a protected memory area will be ignored. Prior to any Write operation, the Write Enable (WREN) instruction must be executed. $\overline{CE}$ must remain active low for the duration of the any command sequence. The Block Erase instruction is initiated by executing an 8-bit command, D8H, followed by address bits [$A_{23}$ -$A_0$]. Address bits [$A_{MS}$ -$A_{16}$] ($A_{MS}$ = Most Significant address) are used to determine the block address ($BA_X$), remaining address bits can be $V_{IL}$ or $V_{IH}$. $\overline{CE}$ must be driven high before the instruction is executed. The user may poll the Busy bit in the Software Status Register or wait $T_{BE}$ for the completion of the internal self-timed Block Erase cycle. See Figure 8 for the Block Erase sequence.

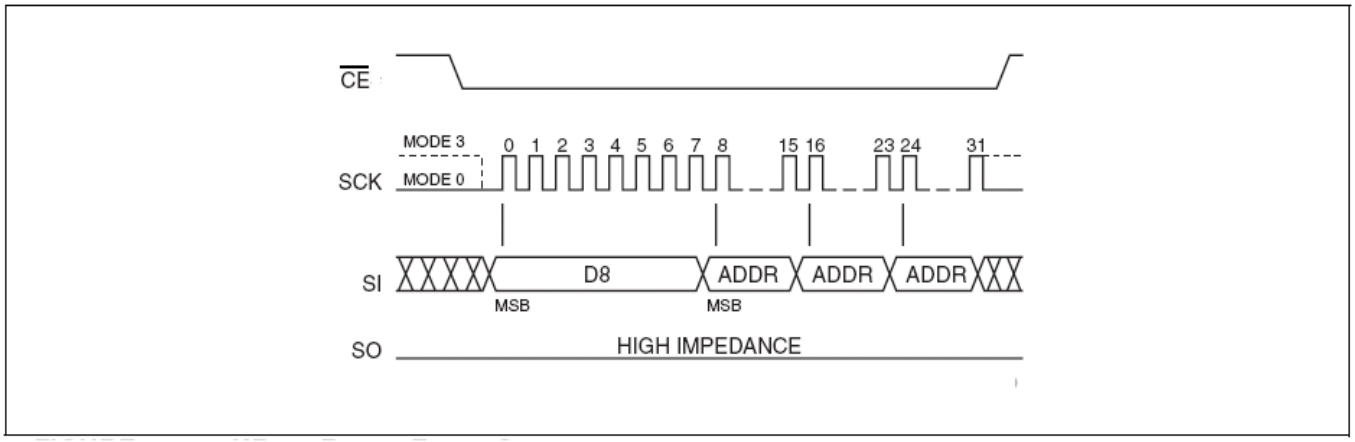



**Figure 8: 64K-byte Block Erase Sequence**

### 4K Byte Sector Erase

The Sector Erase instruction clears all bits in the selected sector to FFH. A Sector Erase instruction applied to a protected memory area will be ignored. Prior to any Write operation, the Write Enable (WREN) instruction must be executed. $\overline{CE}$ must remain active low for the duration of the any command sequence. The Sector Erase instruction is initiated by executing an 8-bit command, 20H, followed by address bits [$A_{23}$ -$A_0$]. Address bits [$A_{MS}$ -$A_{12}$] ($A_{MS}$ = Most Significant address) are used to determine the sector address ($SA_X$), remaining address bits can be $V_{IL}$ or $V_{IH}$. $\overline{CE}$ must be driven high before the instruction is executed. The user may poll the Busy bit in the Software Status Register or wait $T_{SE}$ for the completion of the internal self-timed Sector Erase cycle. See Figure 9 for the Sector Erase sequence.

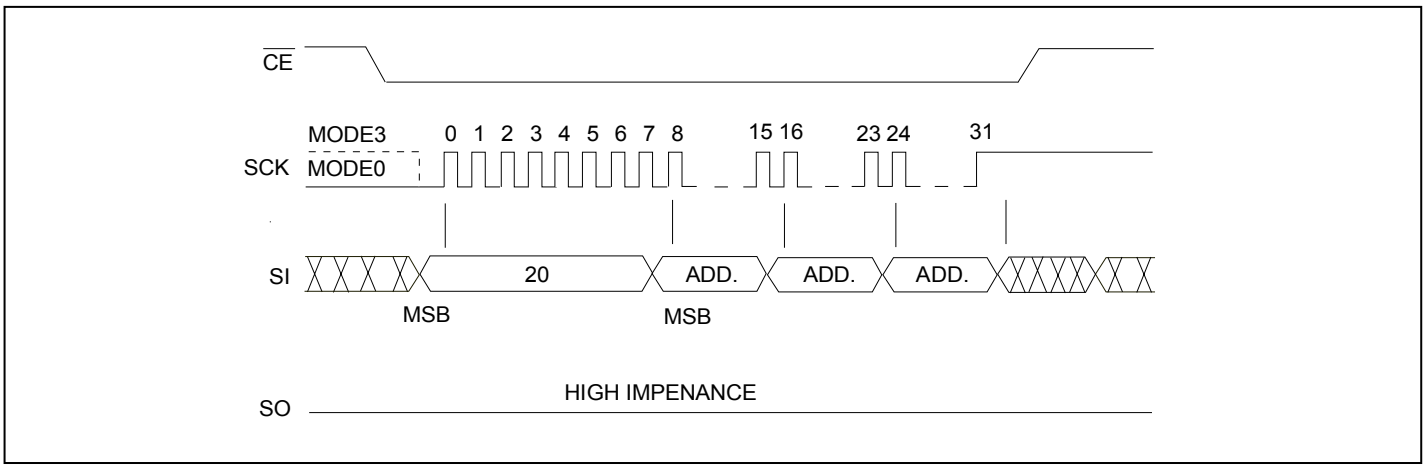



**Figure 9: 4K-byte Sector Erase Sequence**

### Chip Erase

The Chip Erase instruction clears all bits in the device to FFH. A Chip Erase instruction will be ignored if any of the memory area is protected. Prior to any Write operation, the Write Enable (WREN) instruction must be executed. $\overline{CE}$ must remain active low for the duration of the Chip-Erase instruction sequence. The Chip Erase instruction is initiated by executing an 8-bit command, 60H or C7H. $\overline{CE}$ must be driven high before the instruction is executed. The user may poll the Busy bit in the Software Status Register or wait $T_{CE}$ for the completion of the internal self-timed Chip Erase cycle. See Figure 10 for the Chip Erase sequence.

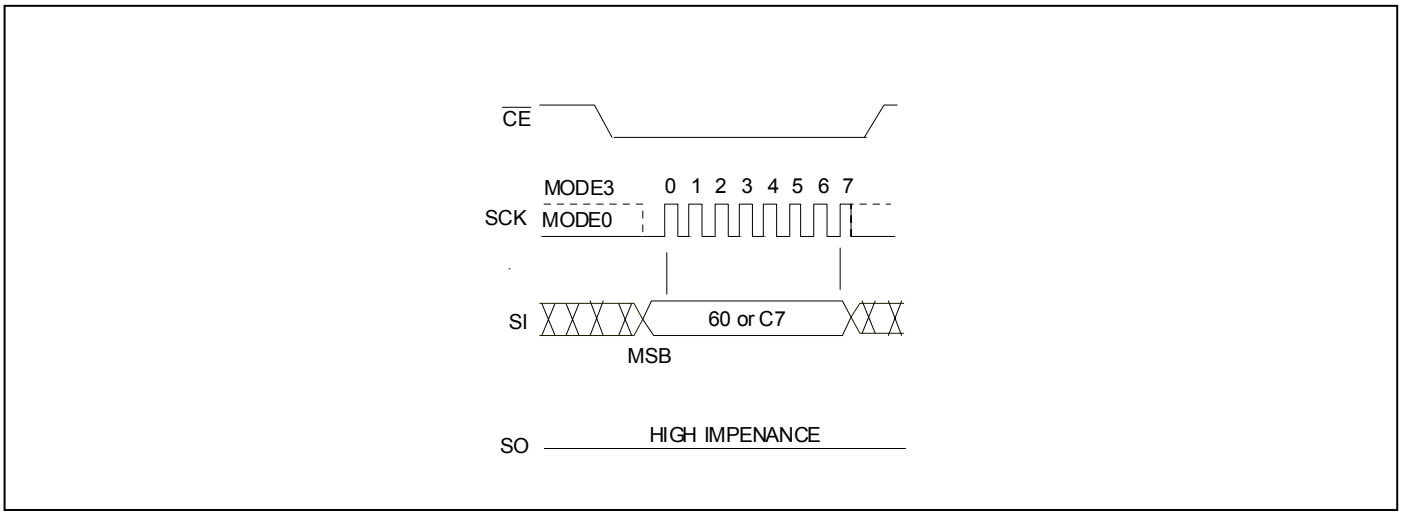



**Figure 10: Chip Erase Sequence**

### Read Status Register (RDSR)

The Read Status Register (RDSR) instruction allows reading of the status register. The status register may be read at any time even during a Write (Program/Erase) operation.
When a Write operation is in progress, the Busy bit may be checked before sending any new commands to assure that the new commands are properly received by the device.

$\overline{CE}$ must be driven low before the RDSR instruction is entered and remain low until the status data is read. Read Status Register is continuous with ongoing clock cycles until it is terminated by a low to high transition of the $\overline{CE}$. See Figure 11 for the RDSR instruction sequence.

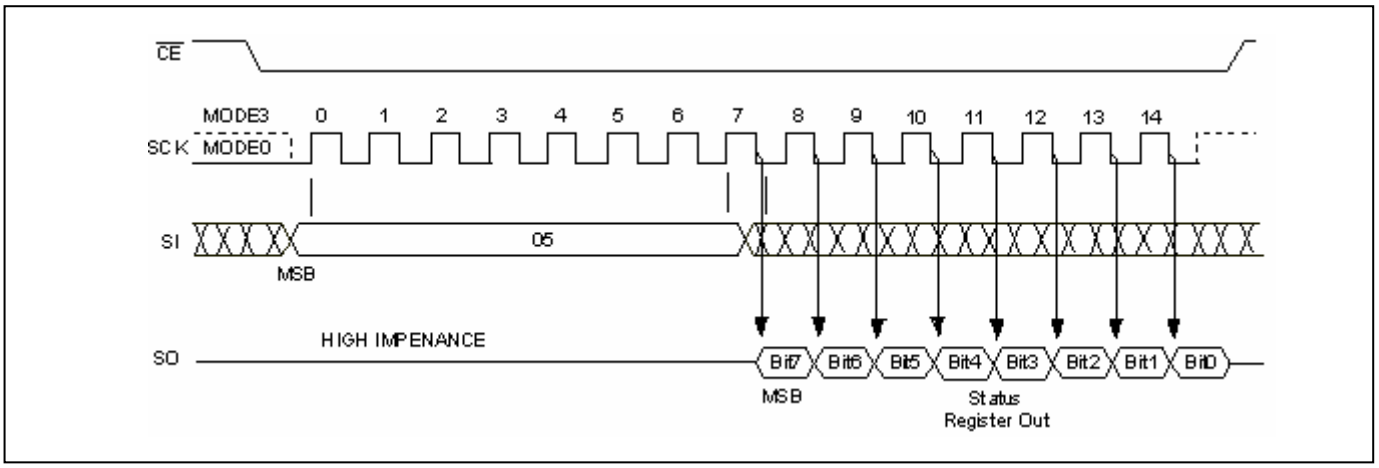



**Figure 11: Read Status Register (RDSR) Sequence**

### Write Enable (WREN)

The Write Enable (WREN) instruction sets the Write-Enable-Latch bit in the Software Status Register to 1 allowing Write operations to occur.
The WREN instruction must be executed prior to any Write (Program/Erase) operation. $\overline{CE}$ must be driven high before the WREN instruction is executed.

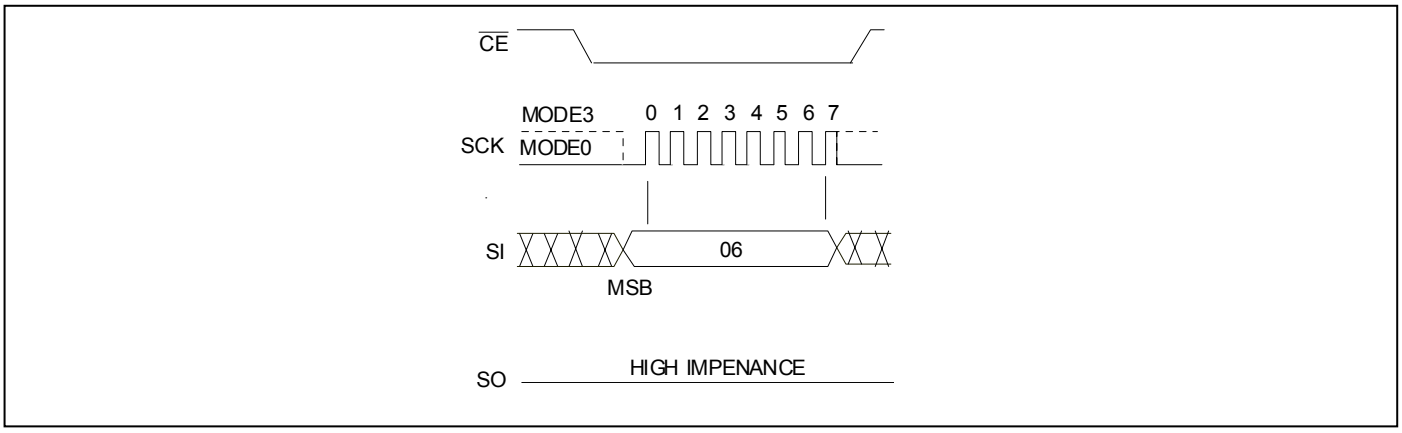



**Figure 12: Write Enable (WREN) Sequence**

### Write Disable (WRDI)

The Write Disable (WRDI) instruction resets the Write-Enable-Latch bit to 0 disabling any new Write operations from occurring. $\overline{CE}$ must be driven high before the WRDI instruction is executed.

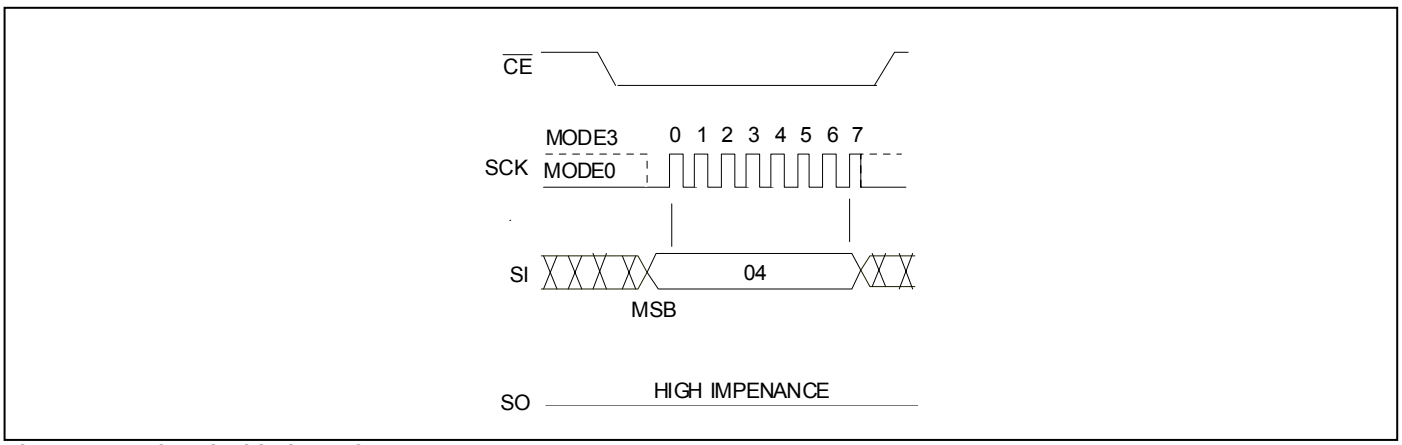



**Figure 13: Write Disable (WRDI) Sequence**

$\overline{CE}$

**Write-Status-Register (WRSR)**

The Write Status Register instruction writes new values to the BP2, BP1, BP0, and BPL bits of the status register. $\overline{CE}$ must be driven low before the command sequence of the WRSR instruction is entered and driven high before the WRSR instruction is executed. See Figure 14 for WREN and WRSR instruction sequences.

Executing the Write Status Register instruction will be ignored when $\overline{WP}$ is low and BPL bit is set to "1". When the $\overline{WP}$ is low, the BPL bit can only be set from "0" to "1" to lock down the status register, but cannot be reset from "1" to "0".

When $\overline{WP}$ is high, the lock-down function of the BPL bit is disabled and the BPL, TB, BP0, BP1,and BP2 bits in the status register can all be changed. As long as BPL bit is set to 0 or $\overline{WP}$ pin is driven high ($V_{IH}$) prior to the low-to-high transition of the $\overline{CE}$ pin at the end of the WRSR instruction, the bits in the status register can all be altered by the WRSR instruction. In this case, a single WRSR instruction can set the BPL bit to "1" to lock down the status register as well as altering the TB, BP0; BP1 and BP2 bits at the same time. See Table 4 for a summary description of $\overline{WP}$ and BPL functions.

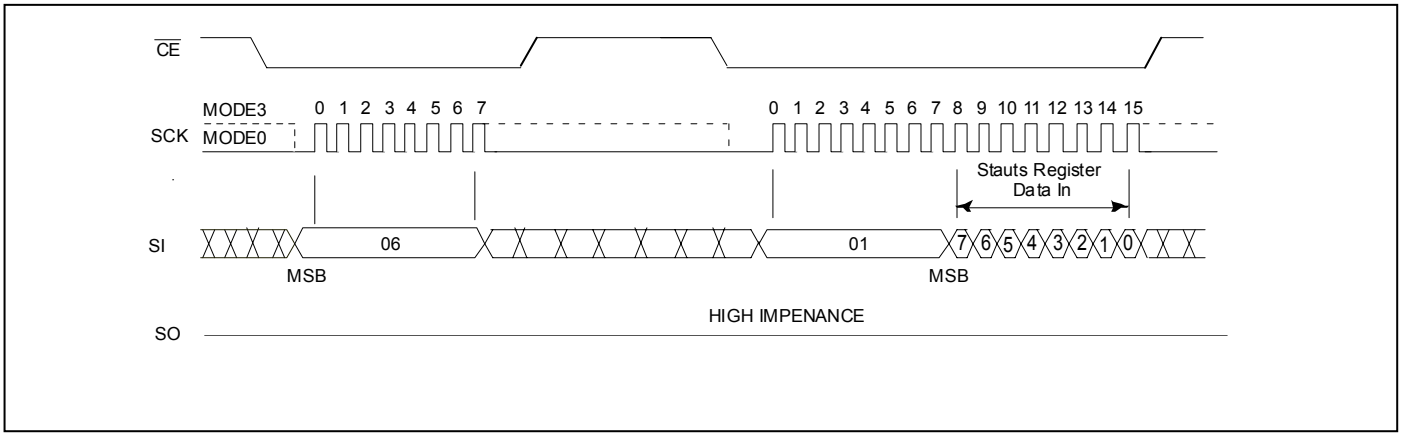



**Figure 14: Write-Enable (WREN) and Write-Status-Register (WRSR)**

### Deep Power Down (DP)

The Deep Power Down instruction is for minimizing power consumption (the standby current is reduced from $I_{SB1}$ to $I_{SB2}$.).

This instruction is initiated by executing an 8-bit command, B9H, and then $\overline{CE}$ must be driven high. After $\overline{CE}$ is driven high, the device will enter to deep power down within the duration of $T_{DP}$.

Once the device is in deep power down status, all instructions will be ignored except the Release from Deep Power Down instruction (RDP) and Read Electronic Signature instruction (RES). The device always power-up in the normal operation with the standby current ($I_{SB1}$). See Figure 15 for the Deep Power Down instruction.

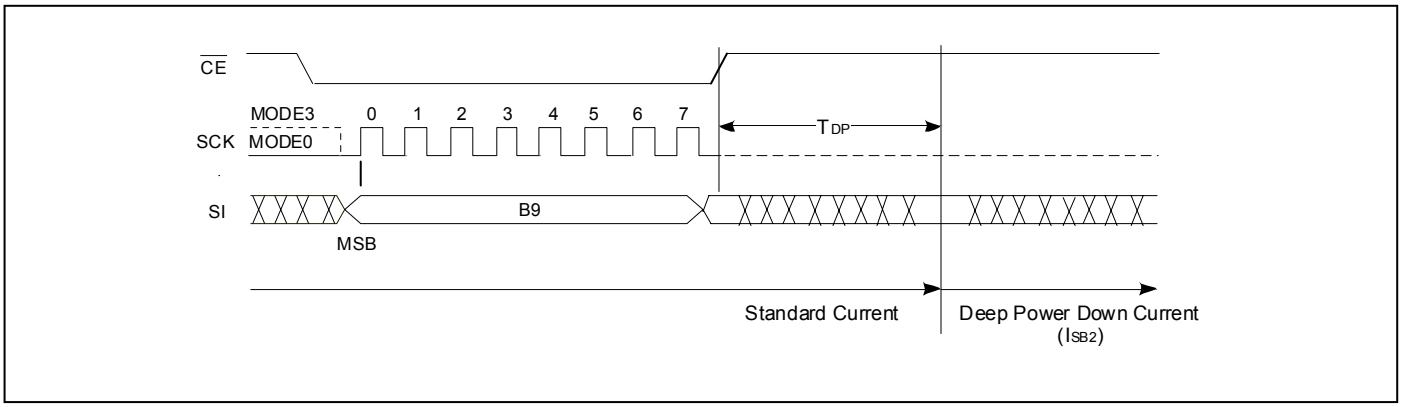



**Figure 15: Deep Power Down Instruction**

### Release from Deep Power Down (RDP) and Read-Electronic-Signature (RES)

The Release form Deep Power Down and Read-Electronic-Signature instruction is a multi-purpose instruction.

The instruction can be used to release the device from the deep power down status. This instruction is initiated by driving $\overline{CE}$ low and executing an 8-bit command, ABH, and then drive $\overline{CE}$ high. See Figure 16 for RDP instruction. Release from the deep power down will take the duration of $T_{RES1}$ before the device will resume normal operation and other instructions are accepted. $\overline{CE}$ must remain high during $T_{RES1}$.

The instruction also can be used to read the 8-bit Electronic-Signature of the device on the SO pin. It is initiated by driving $\overline{CE}$ low and executing an 8-bit command, ABH, followed by 3 dummy bytes. The Electronic-Signature byte is then output from the device. The Electronic-Signature can be read continuously until $\overline{CE}$ go high. See Figure 17 for RES sequence. After driving $\overline{CE}$ high, it must remain high during for the duration of $T_{RES2}$, and then the device will resume normal operation and other instructions are accepted.

The instruction is executed while an Erase, Program or WRSR cycle is in progress is ignored and has no effect on the cycle in progress.

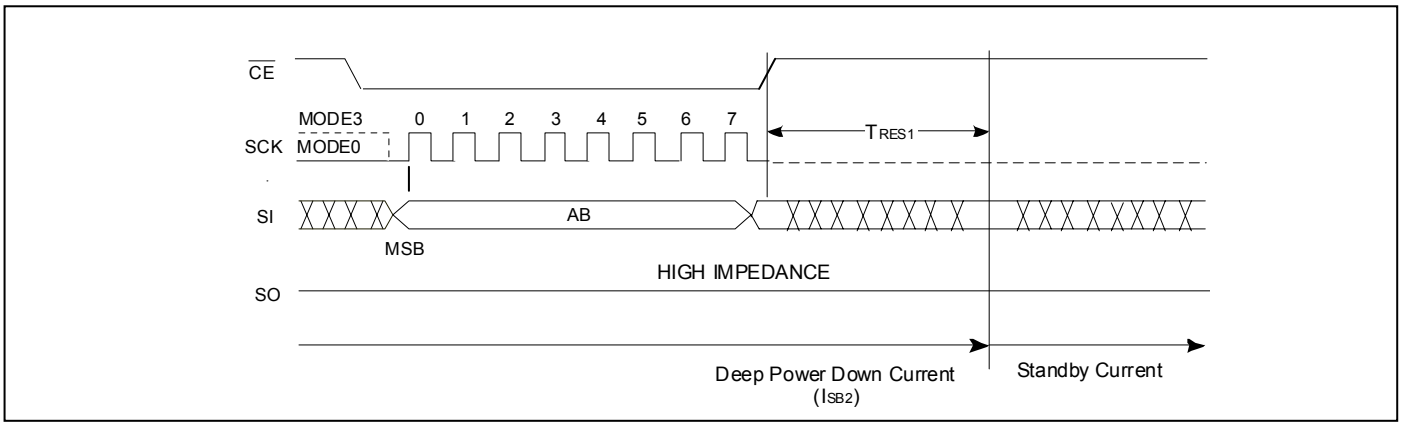



**Figure 16: Release from Deep Power Down (RDP) Instruction**

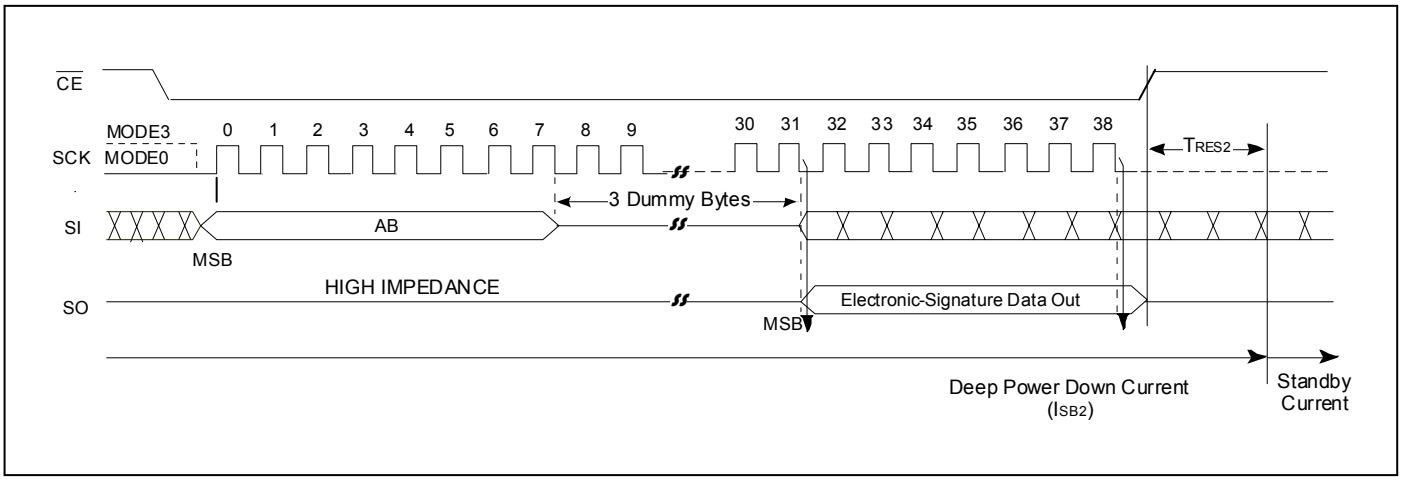



**Figure 17: Read Electronic -Signature (RES) Sequence**

**Table 6: Electronic Signature Data**

| Command | Electronic Signature Data |
|---|---|
| RES | 12H |

**JEDEC Read-ID**

The JEDEC Read-ID instruction identifies the device as F25S04PA and the manufacturer as ESMT. The device information can be read from executing the 8-bit command, 9FH. Following the JEDEC Read-ID instruction, the 8-bit manufacturer's ID, 8CH, is output from the device. After that, a 16-bit device ID is shifted out on the SO pin. Byte1, 8CH, identifies the manufacturer as ESMT. Byte2, 20H, identifies the memory type as SPI Flash. Byte3, 13H, identifies the device as F25S04PA. The instruction sequence is shown in Figure 18. The JEDEC Read ID instruction is terminated by a low to high transition on $\overline{CE}$ at any time during data output. If no other command is issued after executing the JEDEC Read-ID instruction, issue a 00H (NOP) command before going into Standby Mode ( $\overline{CE}$ =$V_{IH}$).

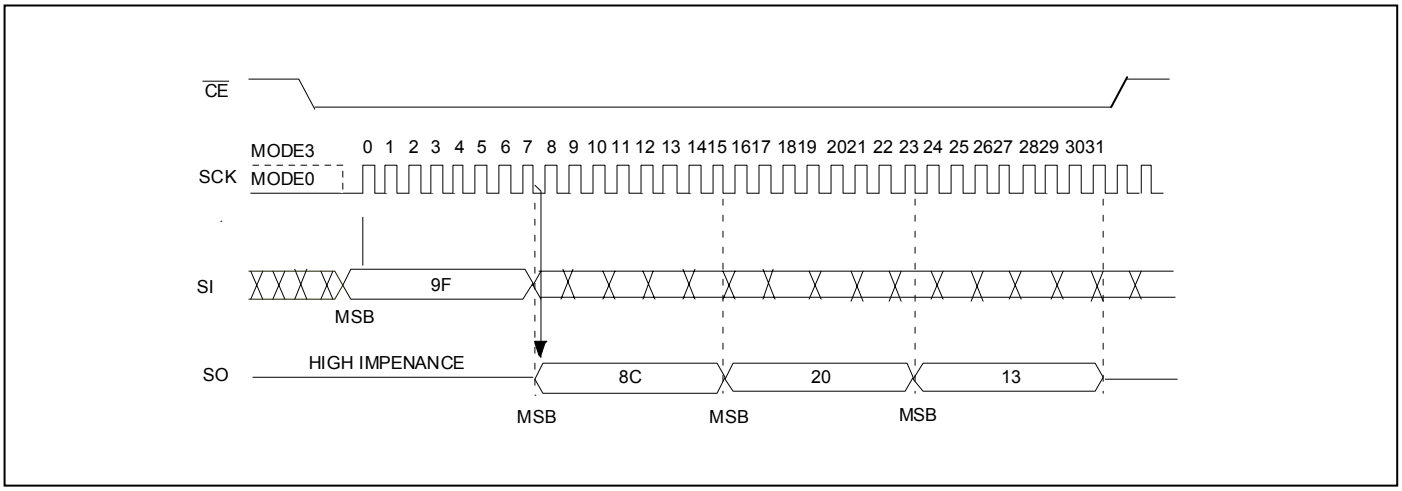



**Figure 18: JEDEC Read-ID Sequence**

**Table 7: JEDEC READ-ID Data**

| Manufacturer's ID (Byte 1) | Device ID | |
|---|---|---|
| | Memory Type (Byte 2) | Memory Capacity (Byte 3) |
| 8CH | 20H | 13H |

**Read-ID (RDID)**

The Read-ID instruction (RDID) identifies the devices as F25 S04PA and manufacturer as ESMT. This command is backward compatible to all ESMT SPI devices and should be used as default device identification when multiple versions of ESMT SPI devices are used in one design. The device information can be read from executing an 8-bit command, 90H, followed by address bits [$A_{23}$ -$A_0$]. Following the Read-ID instruction, the manufacturer's ID is located in address 00000H and the device ID is located in address 00001H.

Once the device is in Read-ID mode, the manufacturer's and device ID output data toggles between address 00000H and 00001H until terminated by a low to high transition on $\overline{CE}$ .

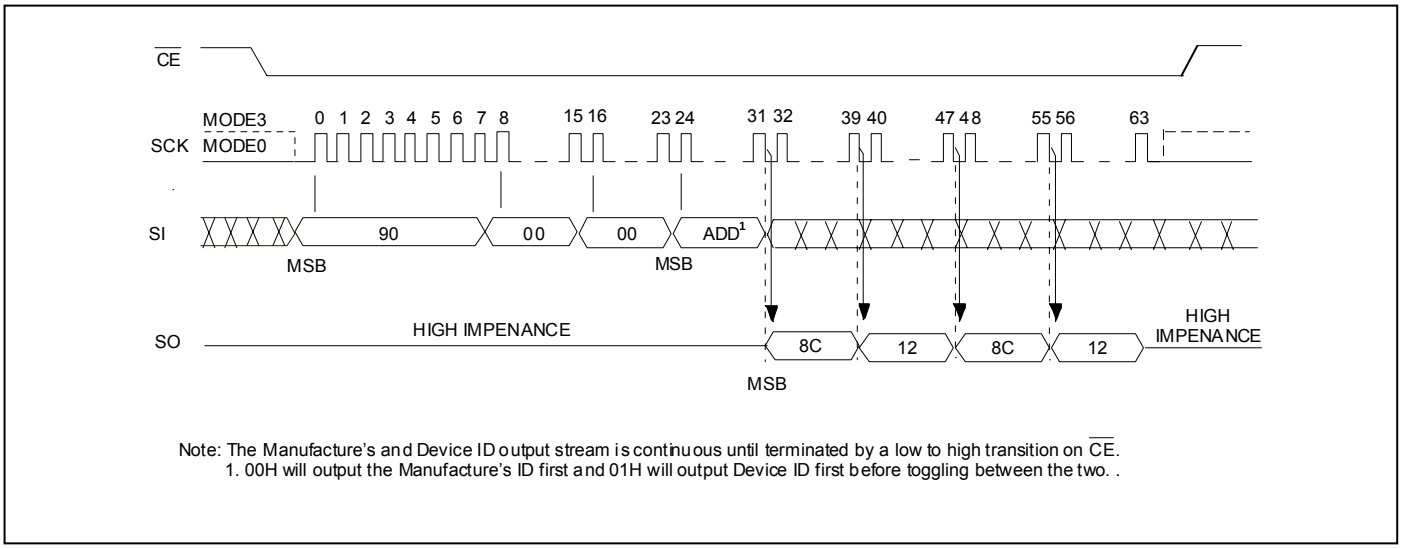



**Figure 19: Read-ID Sequence**

**Table 8: Product ID Data**

| Address | Byte1 | Byte2 |
|---|---|---|
| 00000H | 8CH | 12H |
| | Manufacturer's ID | Device ID<br>ESMT F25S04PA |
| 00001H | 12H | 8CH |
| | Device ID<br>ESMT F25S04PA | Manufacturer's ID |

## ■ ELECTRICAL SPECIFICATIONS

**Absolute Maximum Stress Ratings**
(Applied conditions are greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this datasheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Storage Temperature . . . . . -65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential . . . . . -0.5V to VDD+0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential . . . . . -2.0V to VDD+2.0V
Package Power Dissipation Capability ($T_A$ = 25°C) . . . . . 1.0W
Surface Mount Lead Soldering Temperature (3 Seconds) . . . . . 240°C
Output Short Circuit Current (Note 1). . . . . 50 mA

( Note 1: Output shorted for no more than one second. No more than one output shorted at a time. )

### AC CONDITIONS OF TEST

Input Rise/Fall Time . . . . . 5 ns
Output Load . . . . . $C_L$ = 15 pF for ≧75MHz
. . . . . .$C_L$ = 30 pF for ≦50MHz
See Figures 28 and 29

### OPERATING RANGE

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Operating Supply Voltage | $V_{DD}$ | 2.3 ~ 3.3 | V |
| Ambient Operating Temperature | $T_A$ | 0 ~ 70 | ℃ |

### Table 9: DC OPERATING CHARACTERISTICS

| Symbol | Parameter | | Limits | | | Test Condition |
|---|---|---|---|---|---|---|
| | | | Min | Max | Unit | |
| $I_{DDR1}$ | Read Current @33 MHz | Standard | | 3 | mA | $\overline{CE}$ =0.1 $V_{DD}$/0.9 $V_{DD}$, SO=open |
| | | Dual | | 4 | | |
| $I_{DDR2}$ | Read Current @ 50MHz | Standard | | 6 | mA | $\overline{CE}$ =0.1 $V_{DD}$/0.9 $V_{DD}$, SO=open |
| | | Dual | | 8 | | |
| $I_{DDR3}$ | Read Current @ 86MHz | Standard | | 10 | mA | $\overline{CE}$ =0.1 $V_{DD}$/0.9 $V_{DD}$, SO=open |
| | | Dual | | 12 | | |
| $I_{DDR4}$ | Read Current @ 100MHz | Standard | | 20 | mA | $\overline{CE}$ =0.1 $V_{DD}$/0.9 $V_{DD}$, SO=open |
| | | Dual | | 25 | | |
| $I_{DDW}$ | Program and Erase Current | | | 15 | mA | $\overline{CE}$ =$V_{DD}$ |
| $I_{SB1}$ | Standby Current | | | 5 | µA | $\overline{CE}$ =$V_{DD}$, $V_{IN}$ =$V_{DD}$ or $V_{SS}$ |
| $I_{SB2}$ | Deep Power Down Current | | | 5 | µA | $\overline{CE}$ =$V_{DD}$, $V_{IN}$ =$V_{DD}$ or $V_{SS}$ |
| $I_{LI}$ | Input Leakage Current | | | ±2 | µA | $V_{IN}$=GND to $V_{DD}$, $V_{DD}$=$V_{DD}$ Max |
| $I_{LO}$ | Output Leakage Current | | | ±2 | µA | $V_{OUT}$=GND to $V_{DD}$, $V_{DD}$=$V_{DD}$ Max |
| $V_{IL}$ | Input Low Voltage | | -0.5 | 0.3 x $V_{DD}$ | V | $V_{DD}$=$V_{DD}$ Min |
| $V_{IH}$ | Input High Voltage | | 0.7 x $V_{DD}$ | $V_{DD}$ +0.4 | V | $V_{DD}$=$V_{DD}$ Max |
| $V_{OL}$ | Output Low Voltage | | | 0.4 | V | $I_{OL}$= 1.6mA, $V_{DD}$=$V_{DD}$ Min |
| $V_{OH}$ | Output High Voltage | | $V_{DD}$-0.2 | | V | $I_{OH}$=-100 µA, $V_{DD}$=$V_{DD}$ Min |

**Table 10: RECOMMENDED SYSTEM POWER-UP TIMINGS**

| Symbol | Parameter | Minimum | Unit |
|---|---|---|---|
| $T_{PU-READ}$[1] | $V_{DD}$ Min to Read Operation | 10 | µs |
| $T_{PU-WRITE}$[1] | $V_{DD}$ Min to Write Operation | 10 | µs |

**Table 11: CAPACITANCE ($T_A$ = 25°C, f=1 MHz, other pins open)**

| Parameter | Description | Test Condition | Maximum |
|---|---|---|---|
| $C_{OUT}$[1] | Output Pin Capacitance | $V_{OUT}$ = 0V | 8 pF |
| $C_{IN}$[1] | Input Capacitance | $V_{IN}$ = 0V | 6 pF |

Note 1: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

**Table 12: AC OPERATING CHARACTERISTICS**

| Symbol | Parameter | Normal 33MHz | | Fast 50 MHz | | Fast 86 MHz | | Fast 100 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $F_{CLK}$ | Serial Clock Frequency | | 33 | | 50 | | 86 | | 100 | MHz |
| $T_{SCKH}$[2] | Serial Clock High Time | 13 | | 9 | | 5 | | 4 | | ns |
| $T_{SCKL}$[2] | Serial Clock Low Time | 13 | | 9 | | 5 | | 4 | | ns |
| $T_{CLCH}$ | Clock Rise Time (Slew Rate) | 0.1 | | 0.1 | | 0.1 | | 0.1 | | V/ns |
| $T_{CHCL}$ | Clock Fall Time (Slew Rate) | 0.1 | | 0.1 | | 0.1 | | 0.1 | | V/ns |
| $T_{CES}$[1] | $\overline{CE}$ Active Setup Time | 5 | | 5 | | 5 | | 5 | | ns |
| $T_{CEH}$[1] | $\overline{CE}$ Active Hold Time | 5 | | 5 | | 5 | | 5 | | ns |
| $T_{CHS}$[1] | $\overline{CE}$ Not Active Setup Time | 5 | | 5 | | 5 | | 5 | | ns |
| $T_{CHH}$[1] | $\overline{CE}$ Not Active Hold Time | 5 | | 5 | | 5 | | 5 | | ns |
| $T_{CPH}$ | $\overline{CE}$ High Time | 100 | | 100 | | 100 | | 100 | | ns |
| $T_{CHZ}$ | $\overline{CE}$ High to High-Z Output | | 6 | | 6 | | 6 | | 6 | ns |
| $T_{CLZ}$ | SCK Low to Low-Z Output | 0 | | 0 | | 0 | | 0 | | ns |
| $T_{DS}$ | Data In Setup Time | 2 | | 2 | | 2 | | 2 | | ns |
| $T_{DH}$ | Data In Hold Time | 5 | | 5 | | 5 | | 5 | | ns |
| $T_{HLS}$ | $\overline{HOLD}$ Low Setup Time | 5 | | 5 | | 5 | | 5 | | ns |
| $T_{HHS}$ | $\overline{HOLD}$ High Setup Time | 5 | | 5 | | 5 | | 5 | | ns |

**Table 12: AC OPERATING CHARACTERISTICS - Continued**

| Symbol | Parameter | Normal 33MHz | | Fast 50 MHz | | Fast 86 MHz | | Fast 100 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $T_{HLH}$ | $\overline{HOLD}$ Low Hold Time | 5 | | 5 | | 5 | | 5 | | ns |
| $T_{HHH}$ | $\overline{HOLD}$ High Hold Time | 5 | | 5 | | 5 | | 5 | | ns |
| $T_{HZ}$[3] | $\overline{HOLD}$ Low to High-Z Output | | 6 | | 6 | | 6 | | 6 | ns |
| $T_{LZ}$[3] | $\overline{HOLD}$ High to Low-Z Output | | 6 | | 6 | | 6 | | 6 | ns |
| $T_{OH}$ | Output Hold from SCK Change | 0 | | 0 | | 0 | | 0 | | ns |
| $T_V$ | Output Valid from SCK | | 12 | | 8 | | 8 | | 8 | ns |
| $T_{WHSL}$[4] | Write Protect Setup Time before $\overline{CE}$ Low | | 20 | | 20 | | 20 | | 20 | ns |
| $T_{SHWL}$[4] | Write Protect Hold Time after $\overline{CE}$ High | | 100 | | 100 | | 100 | | 100 | ns |
| $T_W$ | Write Status Register Time | (typ.) 3 | 15 | (typ.) 3 | 15 | (typ.) 3 | 15 | (typ.) 3 | 15 | ms |
| $T_{DP}$[3] | $\overline{CE}$ High to Deep Power Down Mode | | 3 | | 3 | | 3 | | 3 | us |
| $T_{RES1}$[3] | $\overline{CE}$ High to Standby Mode ( for DP) | | 3 | | 3 | | 3 | | 3 | us |
| $T_{RES2}$[3] | $\overline{CE}$ High to Standby Mode (for RES) | | 1.8 | | 1.8 | | 1.8 | | 1.8 | us |

Note:
1. Relative to SCK.
2. $T_{SCKH} + T_{SCKL}$ must be less than or equal to 1/ $F_{CLK}$.
3. Value guaranteed by characterization, not 100% tested in production.
4. Only applicable as a constraint for a Write status Register instruction when Block- Protection-Look (BPL) bit is set at 1.

## ERASE AND PROGRAMMING PERFORMANCE

| Parameter | Symbol | Limit | | Unit |
|---|---|---|---|---|
| | | Typ[2] | Max[3] | |
| Sector Erase Time | $T_{SE}$ | 40 | 100 | ms |
| Block Erase Time | $T_{BE}$ | 0.4 | 2 | s |
| Chip Erase Time | $T_{CE}$ | 3 | 7 | s |
| Byte Programming Time | $T_{BP}$ | 7 | 10 | us |
| Page Programming Time | $T_{PP}$ | 0.8 | 3 | ms |
| Chip Programming Time | | 3 | 5 | s |
| Erase/Program Cycles[1] | | 100,000 | - | Cycles |
| Data Retention | | 20 | - | Years |

**Notes:**
1. Not 100% Tested, Excludes external system level over head.
2. Typical values measured at 25°C, 2.5V.
3. Maximum values measured at 85°C, 2.3V.

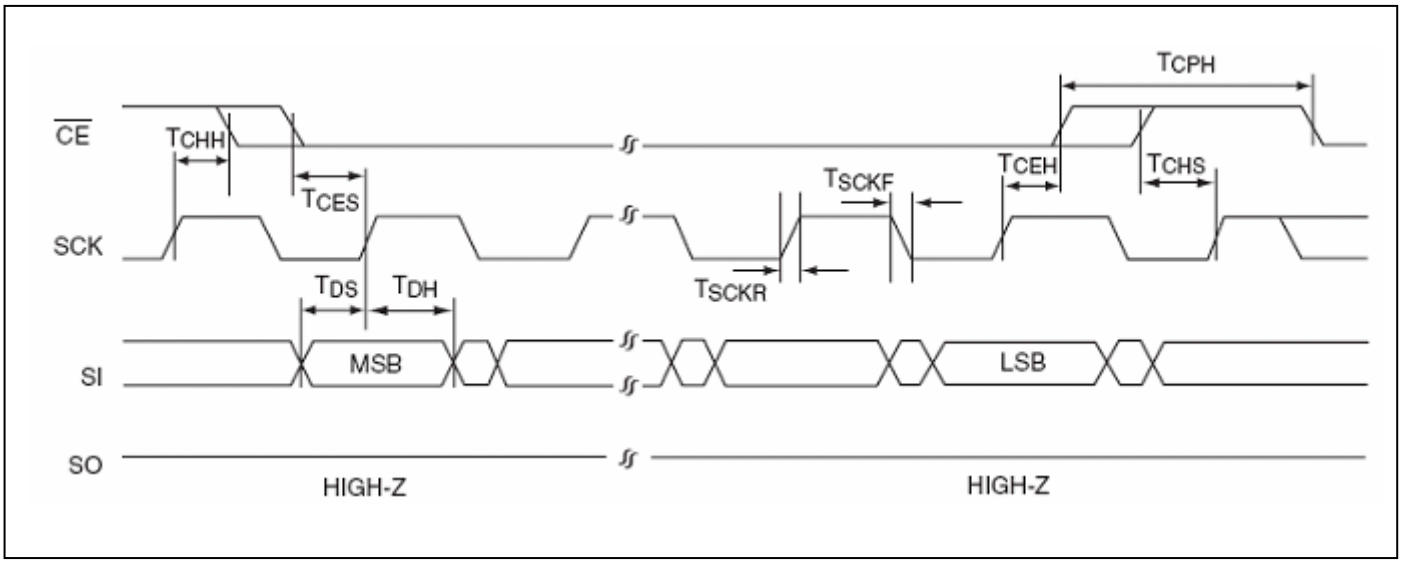



**Figure 20: Serial Input Timing Diagram**

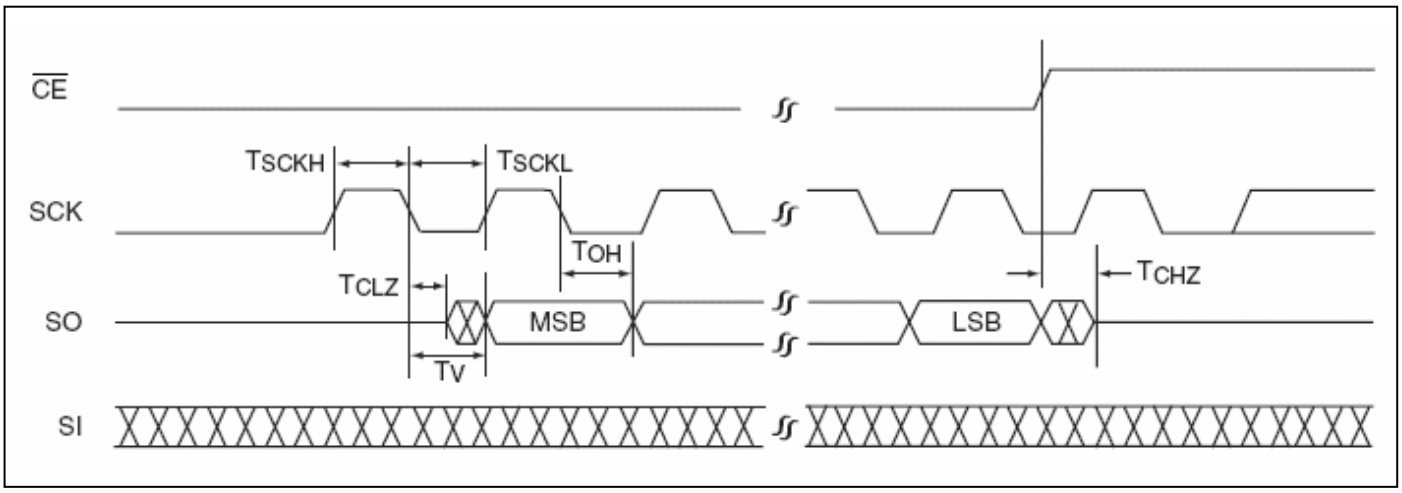



**Figure 21: Serial Output Timing Diagram**

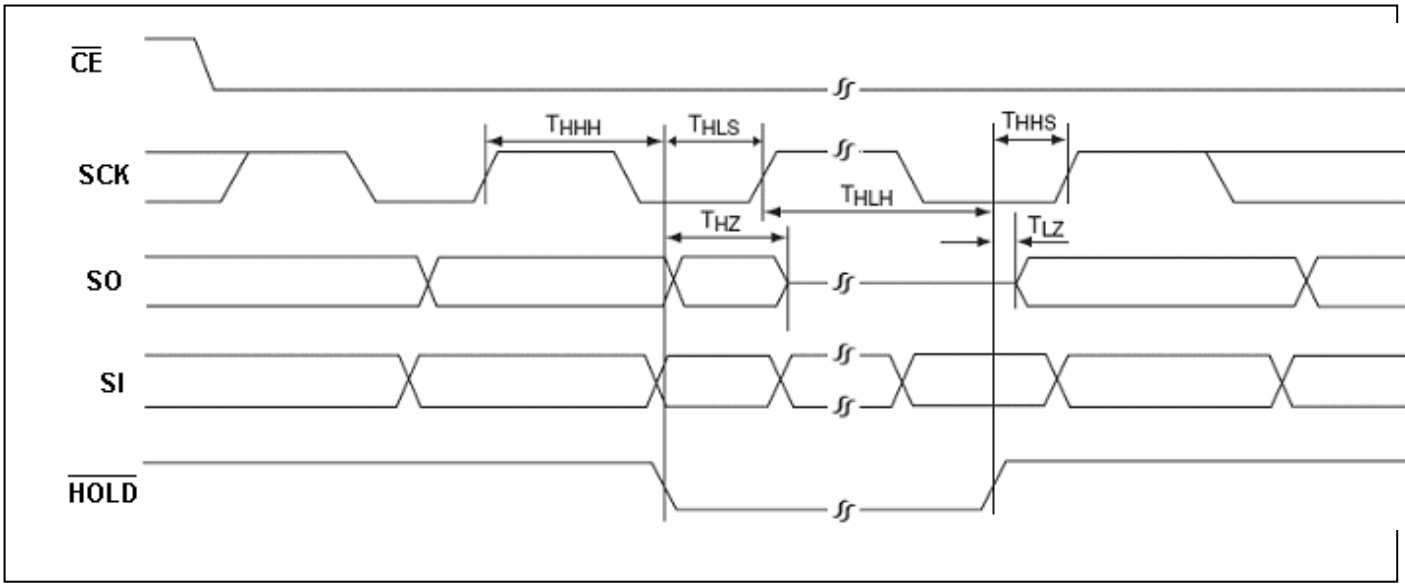



**Figure 22: HOLD Timing Diagram**

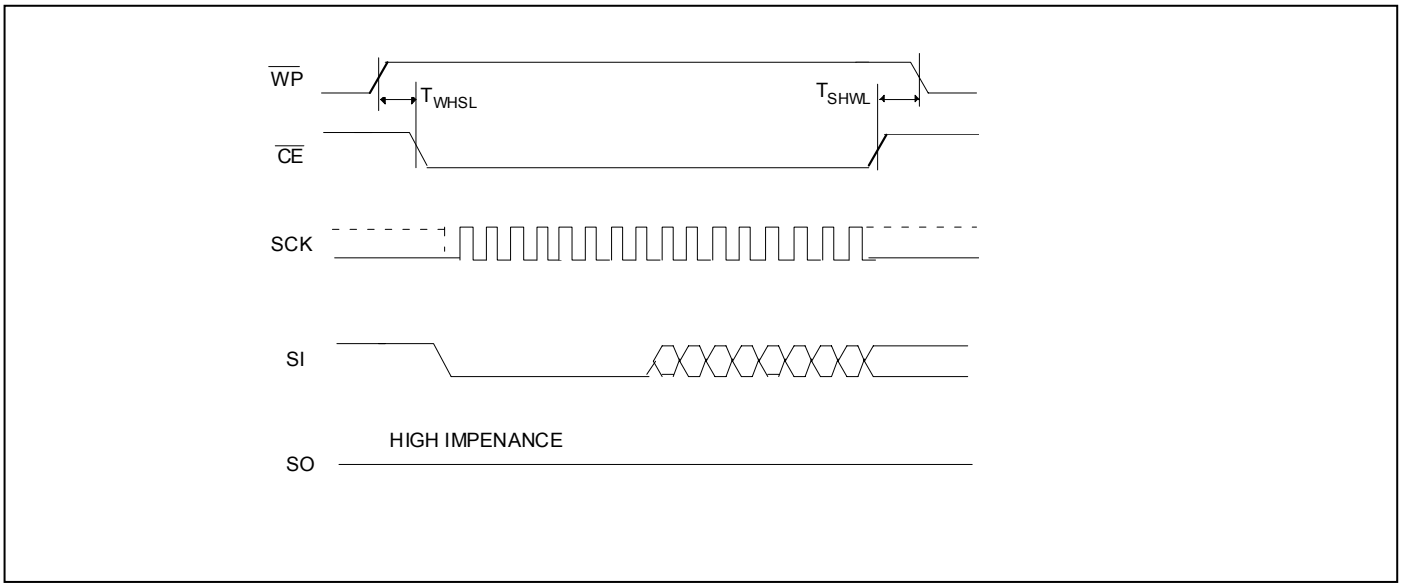



**Figure 23: Write Protect setup and hold timing during WRSR when SRWD = 1**

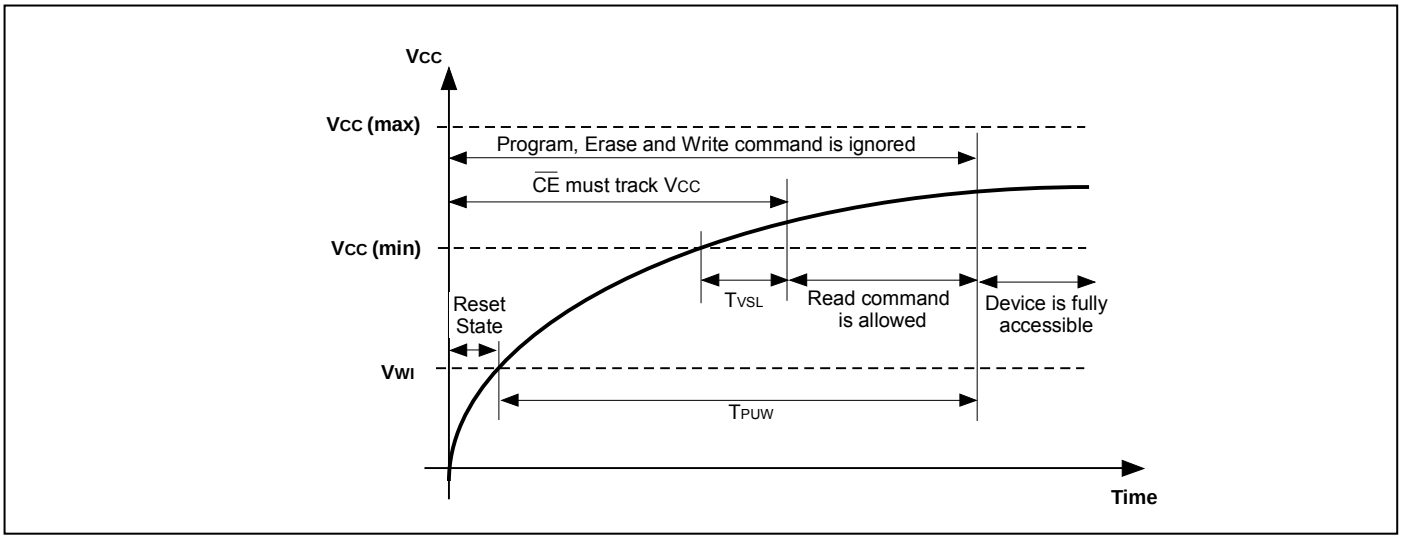



**Figure 24: Power-Up Timing Diagram**

**Table 13: Power-Up Timing and $V_{WI}$ Threshold**

| Parameter | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{CC}$(min) to $\overline{CE}$ low | $T_{VSL}$ | 10 | | us |
| Time Delay before Write instruction | $T_{PUW}$ | 1 | 10 | ms |
| Write Inhibit Threshold Voltage | $V_{WI}$ | 1 | 2 | V |

**Note:** These parameters are characterized only.

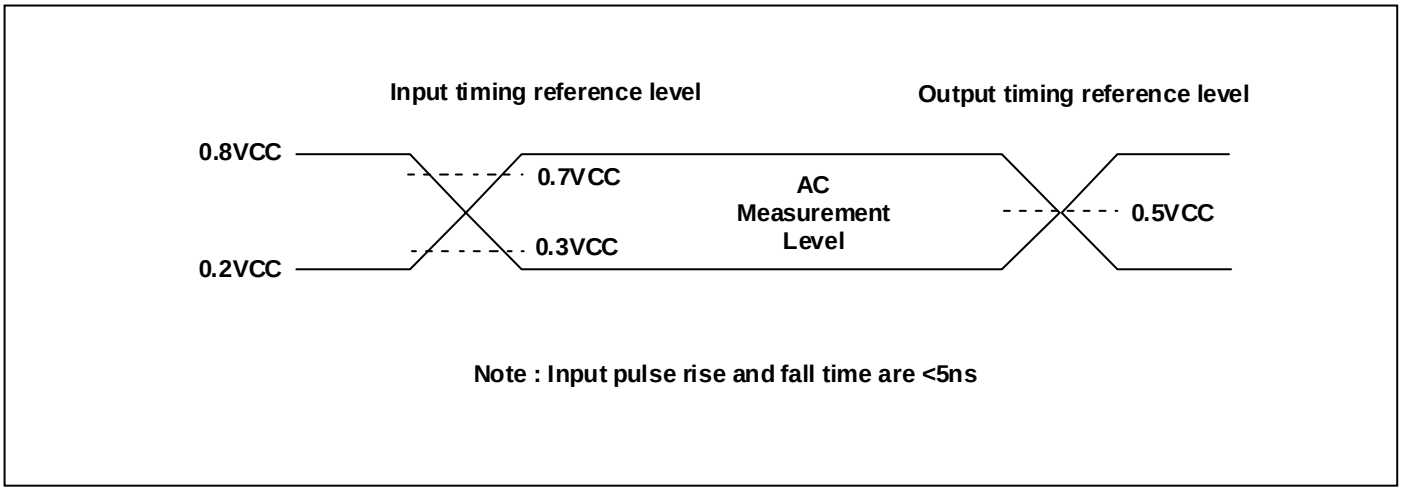



**Figure 25: AC Input/Output Reference Waveforms**

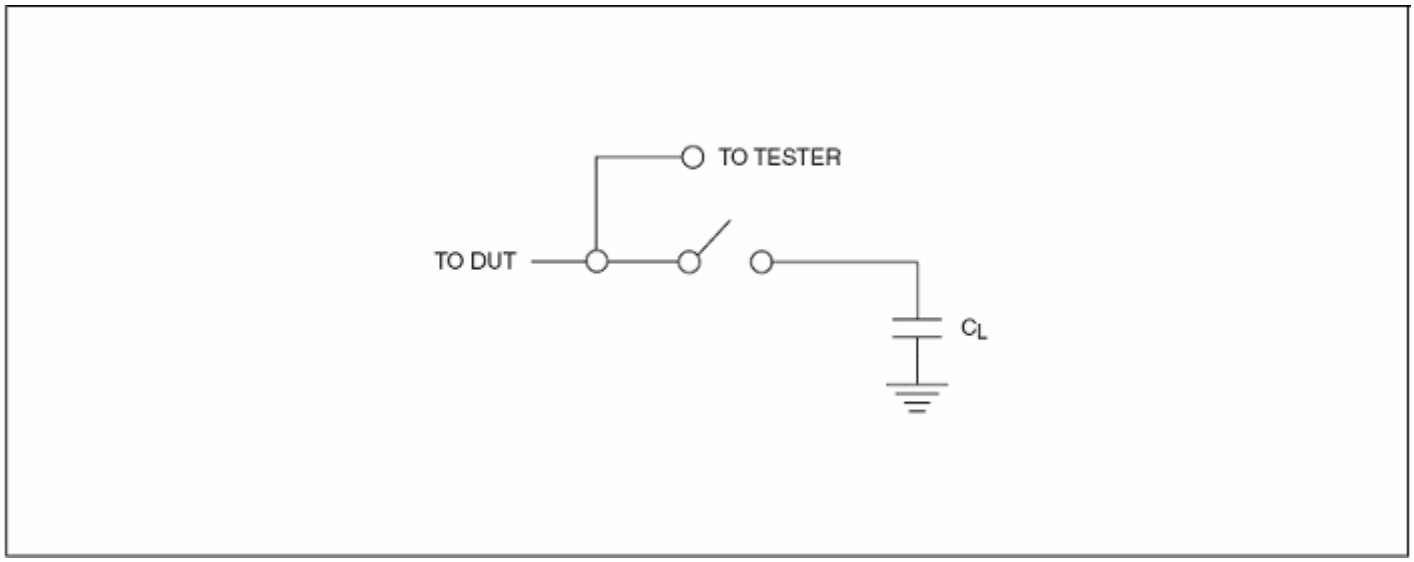
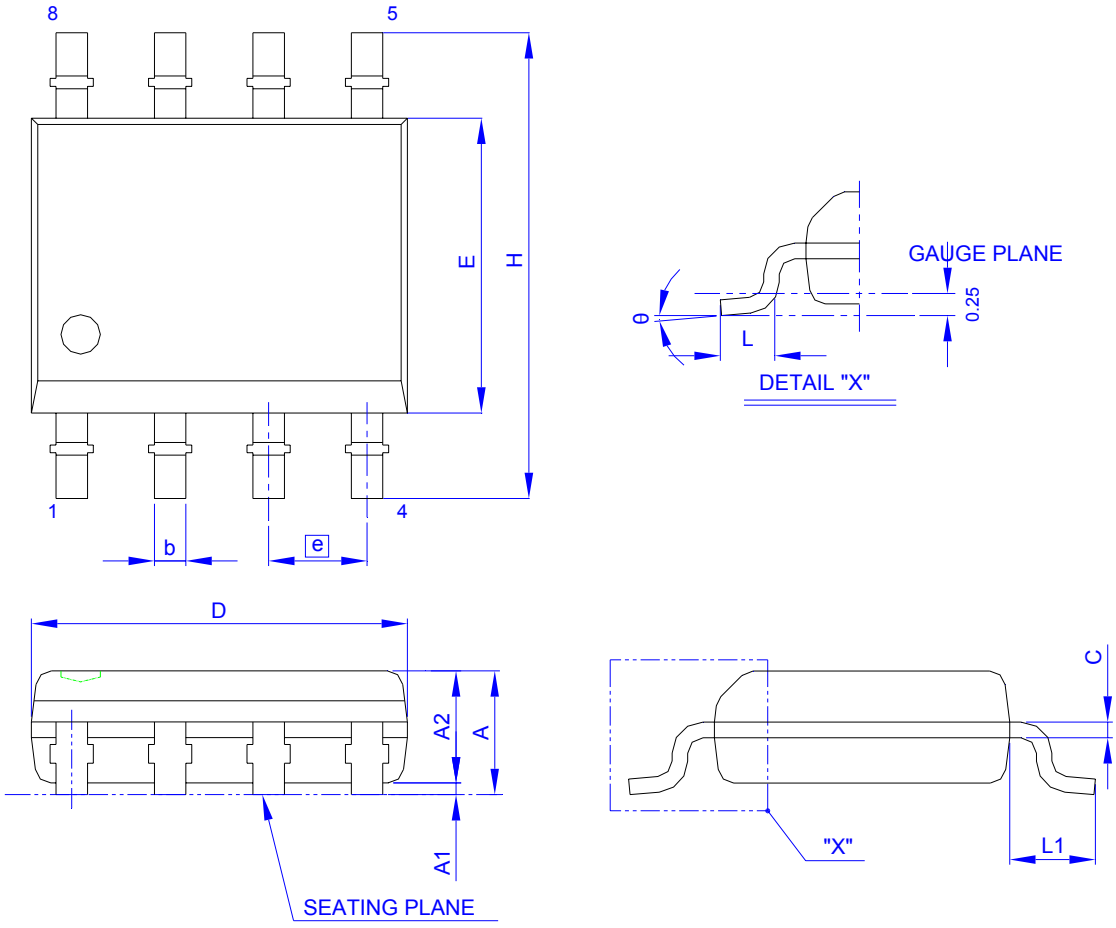



**Figure 26: A Teat Load Example**

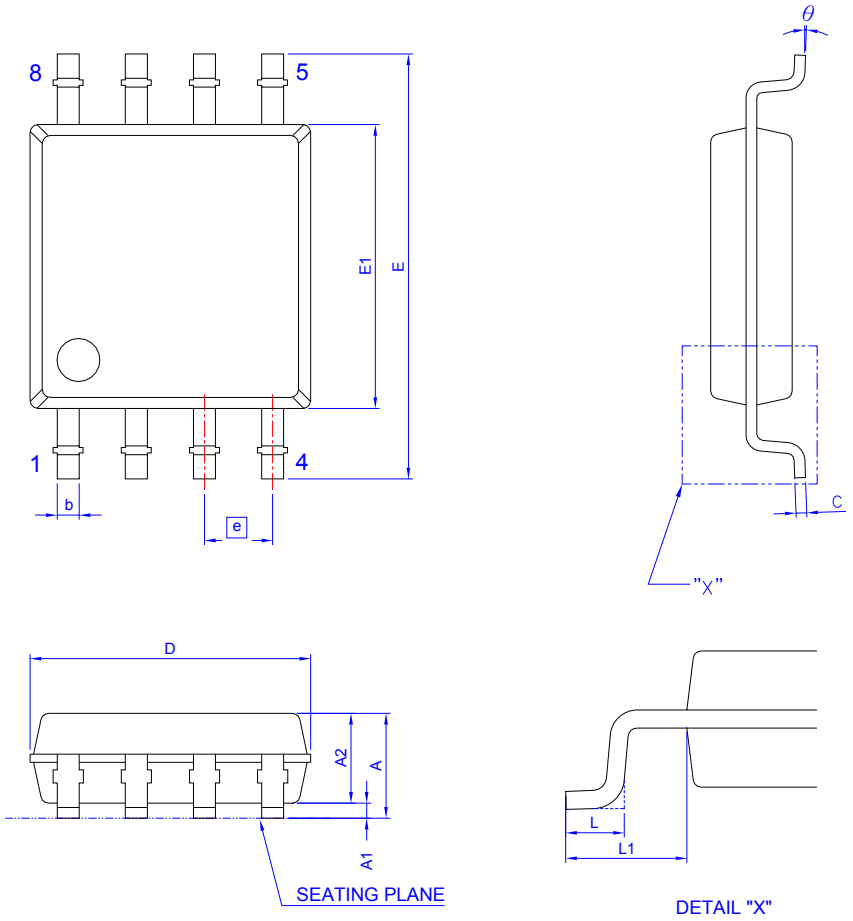
## PACKAGING DIAGRAMS
## 8-LEAD SOIC ( 150 mil )




| Symbol | Dimension in mm | | | Dimension in inch | | | Symbol | Dimension in mm | | | Dimension in inch | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Norm | Max | Min | Norm | Max | | Min | Norm | Max | Min | Norm | Max |
| A | 1.35 | 1.60 | 1.75 | 0.053 | 0.063 | 0.069 | D | 4.80 | 4.90 | 5.00 | 0.189 | 0.193 | 0.197 |
| $A_1$ | 0.10 | 0.15 | 0.25 | 0.004 | 0.006 | 0.010 | E | 3.80 | 3.90 | 4.00 | 0.150 | 0.154 | 0.157 |
| $A_2$ | 1.25 | 1.45 | 1.55 | 0.049 | 0.057 | 0.061 | L | 0.40 | 0.66 | 1.27 | 0.016 | 0.026 | 0.050 |
| b | 0.33 | 0.406 | 0.51 | 0.013 | 0.016 | 0.020 | e | 1.27 BSC | | | 0.050 BSC | | |
| c | 0.19 | 0.203 | 0.25 | 0.0075 | 0.008 | 0.010 | $L_1$ | 1.00 | 1.05 | 1.10 | 0.039 | 0.041 | 0.043 |
| H | 5.80 | 6.00 | 6.20 | 0.228 | 0.236 | 0.244 | θ | 0° | --- | 8° | 0° | --- | 8° |

**Controlling dimension : millimenter**

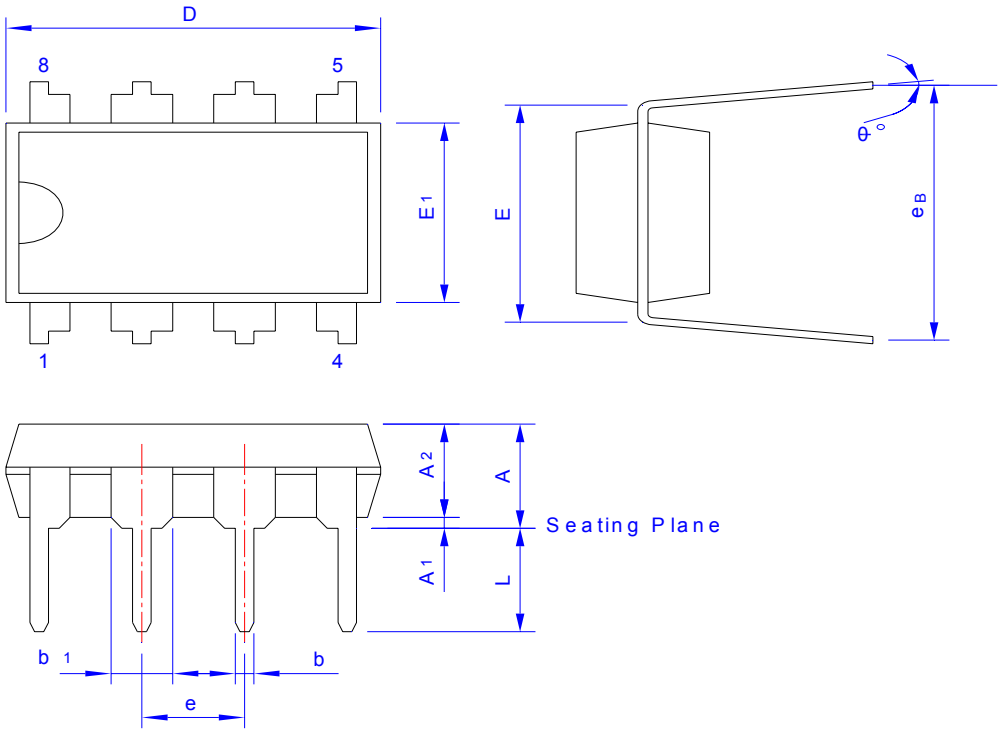
## PACKING DIMENSIONS
## 8-LEAD SOIC 200 mil ( official name – 209 mil )




| Symbol | Dimension in mm | | | Dimension in inch | | | Symbol | Dimension in mm | | | Dimension in inch | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Norm | Max | Min | Norm | Max | | Min | Norm | Max | Min | Norm | Max |
| A | --- | --- | 2.16 | --- | --- | 0.085 | E | 7.70 | 7.90 | 8.10 | 0.303 | 0.311 | 0.319 |
| $A_1$ | 0.05 | 0.15 | 0.25 | 0.002 | 0.006 | 0.010 | $E_1$ | 5.18 | 5.28 | 5.38 | 0.204 | 0.208 | 0.212 |
| $A_2$ | 1.70 | 1.80 | 1.91 | 0.067 | 0.071 | 0.075 | L | 0.50 | 0.65 | 0.80 | 0.020 | 0.026 | 0.032 |
| b | 0.36 | 0.41 | 0.51 | 0.014 | 0.016 | 0.020 | e | 1.27 BSC | | | 0.050 BSC | | |
| c | 0.19 | 0.20 | 0.25 | 0.007 | 0.008 | 0.010 | $L_1$ | 1.27 | 1.37 | 1.47 | 0.050 | 0.054 | 0.058 |
| D | 5.13 | 5.23 | 5.33 | 0.202 | 0.206 | 0.210 | θ | 0° | --- | 8° | 0° | --- | 8° |

**Controlling dimension : millimenter**

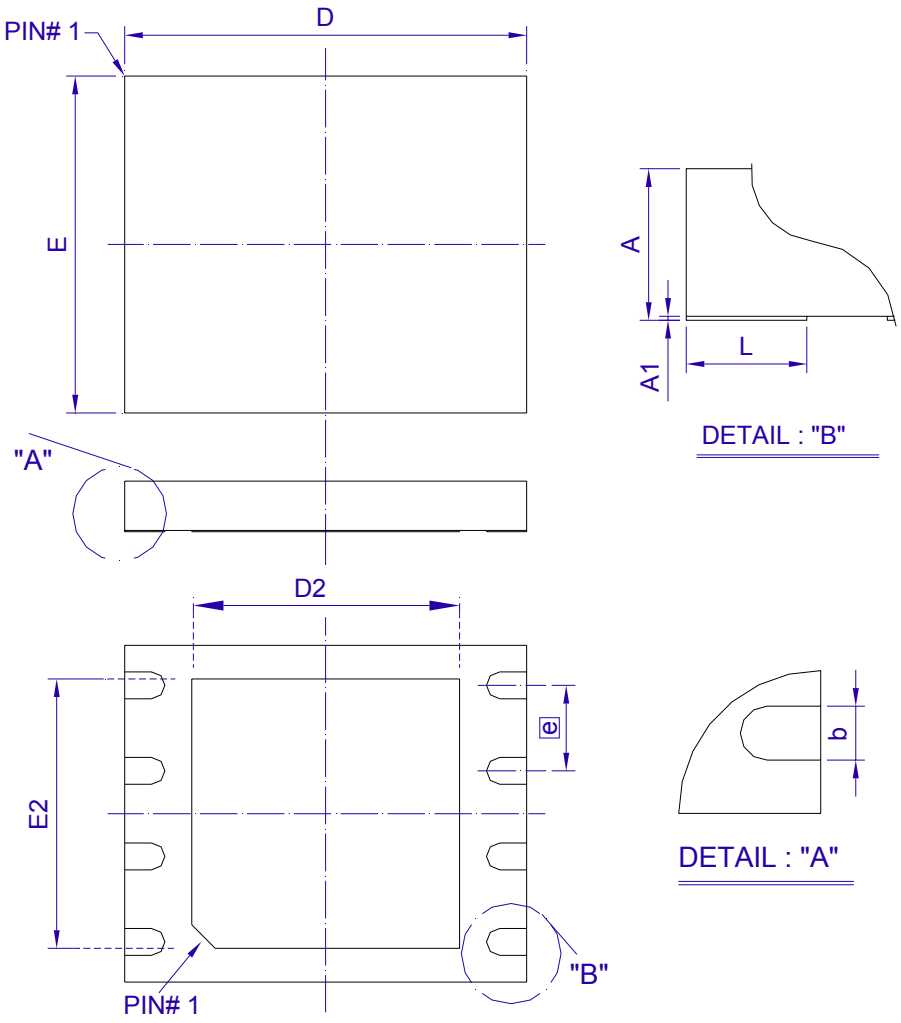
## PACKING DIMENSIONS
## 8-LEAD P-DIP ( 300 mil )




| Symbol | Dimension in mm | | | Dimension in inch | | |
|---|---|---|---|---|---|---|
| | Min | Norm | Max | Min | Norm | Max |
| A | | | 5.00 | | | 0.21 |
| $A_1$ | 0.38 | | | 0.015 | | |
| $A_2$ | 3.18 | 3.30 | 3.43 | 0.125 | 0.130 | 0.135 |
| D | 9.02 | 9.27 | 10.16 | 0.355 | 0.365 | 0.400 |
| E | 7.62 BSC. | | | 0.300 BSC. | | |
| $E_1$ | 6.22 | 6.35 | 6.48 | 0.245 | 0.250 | 0.255 |
| L | 9.02 | 9.27 | 10.16 | 0.115 | 0.130 | 0.150 |
| e | 2.54 TYP. | | | 0.100 TYP. | | |
| $e_B$ | 8.51 | 9.02 | 9.53 | 0.335 | 0.355 | 0.375 |
| b | 0.46 TYP. | | | 0.018 TYP. | | |
| $b_1$ | 1.52 TYP. | | | 0.060 TYP. | | |
| $\theta^o$ | $0^o$ | $7^o$ | $15^o$ | $0^o$ | $7^o$ | $15^o$ |

**Controlling dimension : Inch.**

## PACKING DIMENSIONS
## 8-LEAD DFN ( 5x6 mm )




| Symbol | Dimension in inch | | | Dimension in mm | | |
|---|---|---|---|---|---|---|
| | Min | Norm | Max | Min | Norm | Max |
| A | 0.028 | 0.030 | 0.031 | 0.70 | 0.75 | 0.80 |
| A1 | 0.000 | 0.001 | 0.002 | 0.00 | 0.02 | 0.05 |
| b | 0.014 | 0.016 | 0.018 | 0.35 | 0.40 | 0.45 |
| D | 0.232 | 0.236 | 0.240 | 5.90 | 6.00 | 6.10 |
| D2 | -- | -- | 0.161 | -- | -- | 4.10 |
| E | 0.193 | 0.197 | 0.201 | 4.90 | 5.00 | 5.10 |
| E2 | -- | -- | 0.161 | -- | -- | 4.10 |
| e | 0.050 BSC | | | 1.27 BSC | | |
| L | 0.022 | 0.024 | 0.026 | 0.55 | 0.60 | 0.65 |

**Controlling dimension : millimeter**

## Revision History

| Revision | Date | Description |
|---|---|---|
| 0.1 | 2009.02.20 | Original |
| 0.2 | 2009.05.14 | 1. Add DFN package<br>2. Modify the test condition of $V_{OL}$ |

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