

TC74VHCV245FT, TC74VHCV245FK

Octal Schmitt Bus Transceiver

The TC74VHCV245 is an advanced high speed CMOS OCTAL BUS TRANSCEIVER fabricated with silicon gate CMOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

It is intended for two-way asynchronous communication between data busses. The direction of data transmission is determined by the level of the DIR input.

The enable input (\overline{G}) can be used to disable the device so that the busses are effectively isolated.

Input pin and bus terminal have hysteresis between the positive-going and negative-going thresholds. Thus the TC74VHCV245 is capable of squaring up transitions of slowly changing input signals and provides an improved noise immunity. Input protection and output circuit ensure that 0 to 5.5 V can be applied to the input and output ^(Note) pins without regard to the supply voltage. These structure prevents device destruction due to mismatched supply and input/output voltages such as battery back up, etc.

Note: Output in off-state.

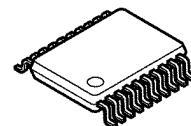
Features (Note)

- High speed: $t_{pd} = 3.8 \text{ ns}$ (typ.) at $V_{CC} = 5 \text{ V}$
- Low power dissipation: $I_{CC} = 2 \mu\text{A}$ (max) at $T_a = 25^\circ\text{C}$
- Wide operating voltage range: $V_{CC}(\text{opr}) = 1.8 \text{ V}$ to 5.5 V
- Output current: $|I_{OH}|/I_{OL} = 16 \text{ mA}$ (min) ($V_{CC} = 4.5 \text{ V}$)
- Available in TSSOP and VSSOP (US)
- Power-down protection provided on all inputs and outputs
- Pin and function compatible with the 74 series
(74AC/VHC/HC/F/ALS/LS etc.) 245 type

Note: Do not apply a signal to any bus pins when it is in the output mode. Damage may result.

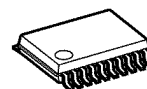
All floating (high impedance) bus pins must have their input levels fixed by means of pull-up or pull-down resistors.

TC74VHCV245FT



TSSOP20-P-0044-0.65A

TC74VHCV245FK

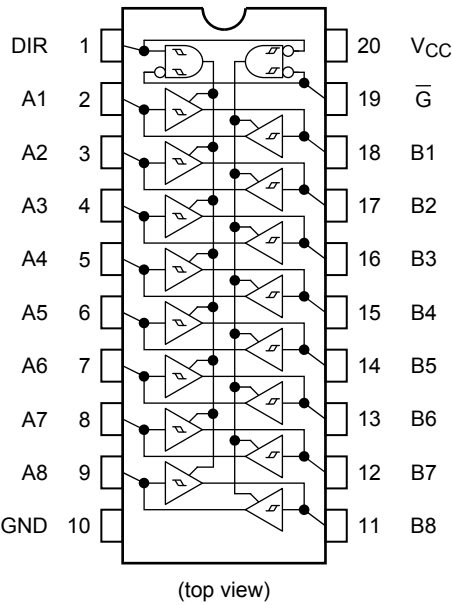


VSSOP20-P-0030-0.50

Weight

TSSOP20-P-0044-0.65A	: 0.08 g (typ.)
VSSOP20-P-0030-0.50	: 0.03 g (typ.)

Pin Assignment



Truth Table

Inputs		Function		Output
\overline{G}	DIR	A Bus	B Bus	
L	L	Output	Input	A = B
L	H	Input	Output	B = A
H	X	Z		Z

X: Don't care

Z: High impedance

Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CC}	-0.5 to 7.0	V
DC iInput voltage (DIR, \overline{G})	V_{IN}	-0.5 to 7.0	V
DC bus I/O voltage	$V_{I/O}$	-0.5 to 7.0 (Note 2)	V
		-0.5 to $V_{CC} + 0.5$ (Note 3)	
Input diode current	I_{IK}	-50	mA
Output diode current	I_{OK}	± 50 (Note 4)	mA
DC output current	I_{OUT}	± 50	mA
Power dissipation	P_D	180	mW
DC V_{CC} /ground current	I_{CC}/I_{GND}	± 100	mA
Storage temperature	T_{stg}	-65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note 2: off-state

Note 3: High or low state. I_{OUT} absolute maximum rating must be observed.

Note 4: $V_{OUT} < GND$, $V_{OUT} > V_{CC}$

Operating Ranges (Note 1)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CC}	1.8 to 5.5	V
iInput voltage (DIR, \overline{G})	V_{IN}	0 to 5.5	V
Bus I/O voltage	$V_{I/O}$	0 to 5.5 (Note 2)	V
		0 to V_{CC} (Note 3)	
Operating temperature	T_{opr}	-40 to 85	°C
Input rise and fall time	dt/dv	0 to 20($V_{CC}=3.3 \pm 0.3V$) 0 to 1($V_{CC}=5 \pm 0.5V$)	ms/V

Note 1: The operating ranges are required to ensure the normal operation of the device. Unused inputs and bus inputs must be tied to either V_{CC} or GND. Please connect both bus inputs and the bus outputs with V_{CC} or GND when the I/O of the bus terminal changes by the function. In this case, please note that the output is not short-circuited.

Note 2: off-state

Note 3: High or low state

Electrical Characteristics
DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit	
				VCC (V)	Min	Typ.	Max	Min		Max
Positive threshold voltage	V _P	—		1.8	—	—	1.65	—	1.65	V
				2.3	—	—	1.85	—	1.85	
				3.0	—	—	2.20	—	2.20	
				4.5	—	—	3.15	—	3.15	
				5.5	—	—	3.85	—	3.85	
Negative threshold voltage	V _N	—		1.8	0.15	—	—	0.15	—	V
				2.3	0.45	—	—	0.45	—	
				3.0	0.90	—	—	0.90	—	
				4.5	1.35	—	—	1.35	—	
				5.5	1.65	—	—	1.65	—	
Hysteresis voltage	V _H	—		1.8	0.15	—	1.05	0.15	1.05	V
				2.3	0.20	—	1.10	0.20	1.10	
				3.0	0.30	—	1.20	0.30	1.20	
				4.5	0.40	—	1.40	0.40	1.40	
				5.5	0.50	—	1.60	0.50	1.60	
High-level output voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50 μA	1.8	1.7	1.8	—	1.7	—	V
				3.0	2.9	3.0	—	2.9	—	
			I _{OH} = -8 mA I _{OH} = -16 mA	4.5	4.4	4.5	—	4.4	—	
				3.0	2.58	—	—	2.48	—	
				4.5	3.94	—	—	3.80	—	
Low-level output voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50 μA	1.8	—	0.0	0.1	—	0.1	V
				3.0	—	0.0	0.1	—	0.1	
			I _{OL} = 8 mA I _{OL} = 16 mA	4.5	—	0.0	0.1	—	0.1	
				3.0	—	—	0.36	—	0.44	
				4.5	—	—	0.44	—	0.55	
3-state output off-state current	I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0 to 5.5V		1.8 to 5.5	—	—	±0.5	—	±5.0	μA
Power-off leakage current	I _{OFF}	V _{IN} /V _{OUT} = 5.5 V		0	—	—	0.5	—	5.0	μA
Input leakage current	I _{IN}	V _{IN} = 5.5 V or GND		0 to 5.5	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I _{CC}	V _{IN} = V _{CC} or GND		5.5	—	—	2.0	—	20.0	μA

AC Characteristics (input: $t_r = t_f = 3 \text{ ns}$)

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = -40 to 85°C		Unit
			VCC (V)	CL (pF)	Min	Typ.	Max	Min	Max	
Propagation delay time	t_{pLH} t_{pHL}	—	2.5± 0.2	15	—	5.9	13.0	1.0	15.0	ns
				50	—	8.7	15.9	1.0	18.0	
			3.3 ± 0.3	15	—	4.6	8.4	1.0	10.0	
				50	—	6.9	11.9	1.0	13.5	
			5.0 ± 0.5	15	—	3.8	5.5	1.0	6.5	
				50	—	5.4	7.5	1.0	8.5	
3-state output enable time	t_{pZL} t_{pZH}	RL = 1 kΩ	2.5 ± 0.2	15	—	7.0	19.9	1.0	22.0	ns
				50	—	9.6	22.7	1.0	26.0	
			3.3 ± 0.3	15	—	5.3	13.2	1.0	15.5	
				50	—	7.4	16.7	1.0	19.0	
			5.0 ± 0.5	15	—	4.1	8.5	1.0	10.0	
				50	—	5.7	10.6	1.0	12.0	
3-state output disable time	t_{pLZ} t_{pHZ}	RL = 1 kΩ	2.5 ± 0.2	50	—	15.0	23.1	1.0	25.0	ns
			3.3 ± 0.3	50	—	11.6	15.8	1.0	18.0	
			5.0 ± 0.5	50	—	9.3	9.7	1.0	11.0	
Output to output skew	t_{osLH} t_{osHL}	(Note1)	2.5 ± 0.2	50	—	—	2.0	—	2.0	ns
			3.3 ± 0.3	50	—	—	1.5	—	1.5	
			5.0 ± 0.5	50	—	—	1.0	—	1.0	
Input capacitance	C _{IN}	DIR, \overline{G}			—	4	10	—	10	pF
Bus input capacitance	C _{I/O}	An, Bn			—	6	—	—	—	pF
Power dissipation capacitance	C _{PD}	(Note2)			—	26	—	—	—	pF

Note 1: Parameter guaranteed by design.

$$t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|$$

Note 2: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per bit)}$$

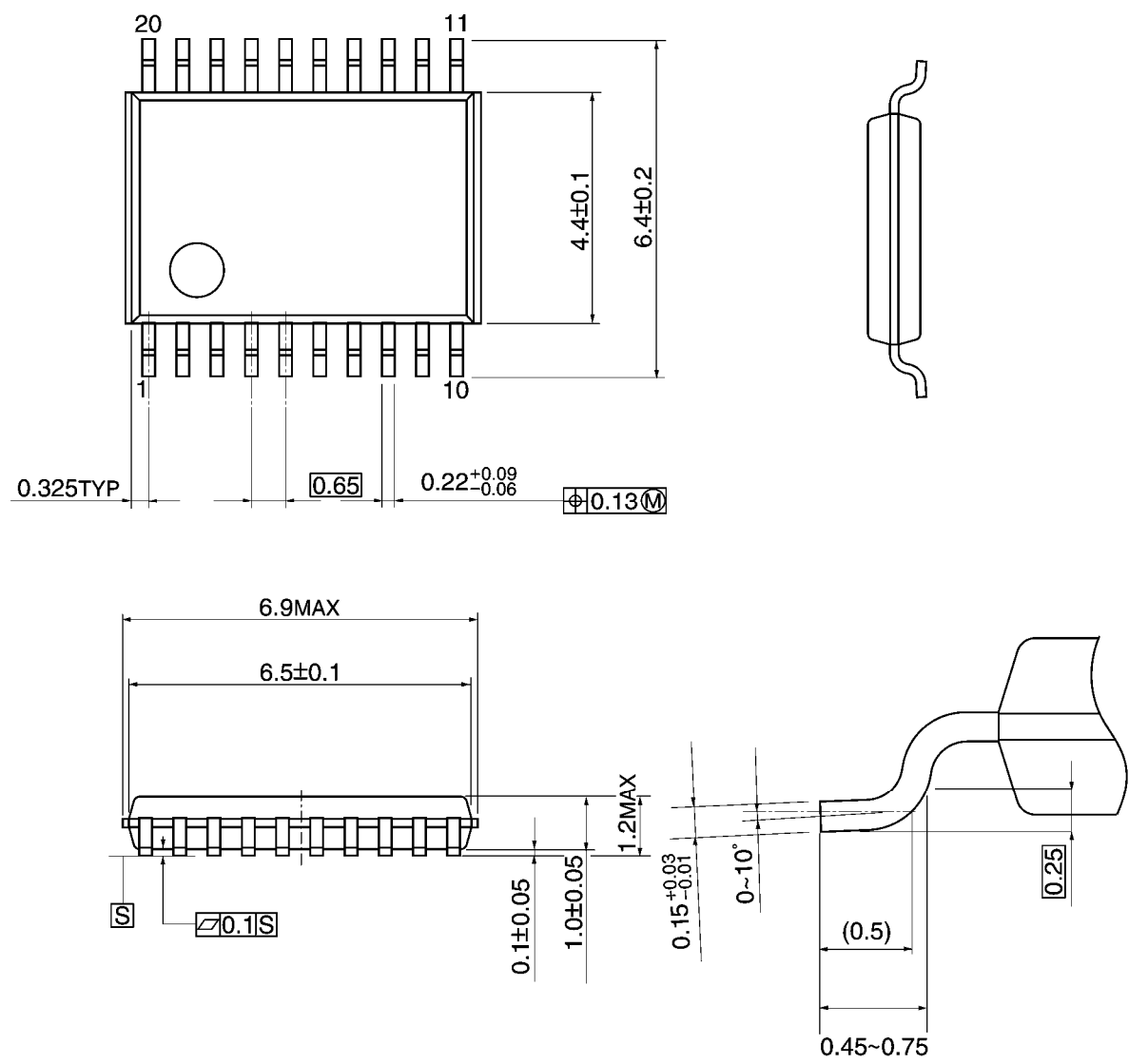
Noise Characteristics (input: $t_r = t_f = 3 \text{ ns}$)

Characteristics	Symbol	Test Condition	Ta = 25°C			Unit
			VCC (V)	Typ.	Max	
Quiet output maximum dynamic V _{OL}	V _{OLP}	C _L = 50 pF	3.3 5.0	0.5 1.0	— —	V
Quiet output minimum dynamic V _{OL}	V _{OLV}	C _L = 50 pF	3.3 5.0	-0.1 -0.3	— —	V
Minimum high level dynamic input voltage	V _{IHD}	C _L = 50 pF	5.0	—	3.5	V
Maximum low level dynamic input voltage	V _{ILD}	C _L = 50 pF	5.0	—	1.5	V

Package Dimensions

TSSOP20-P-0044-0.65A

Unit: mm

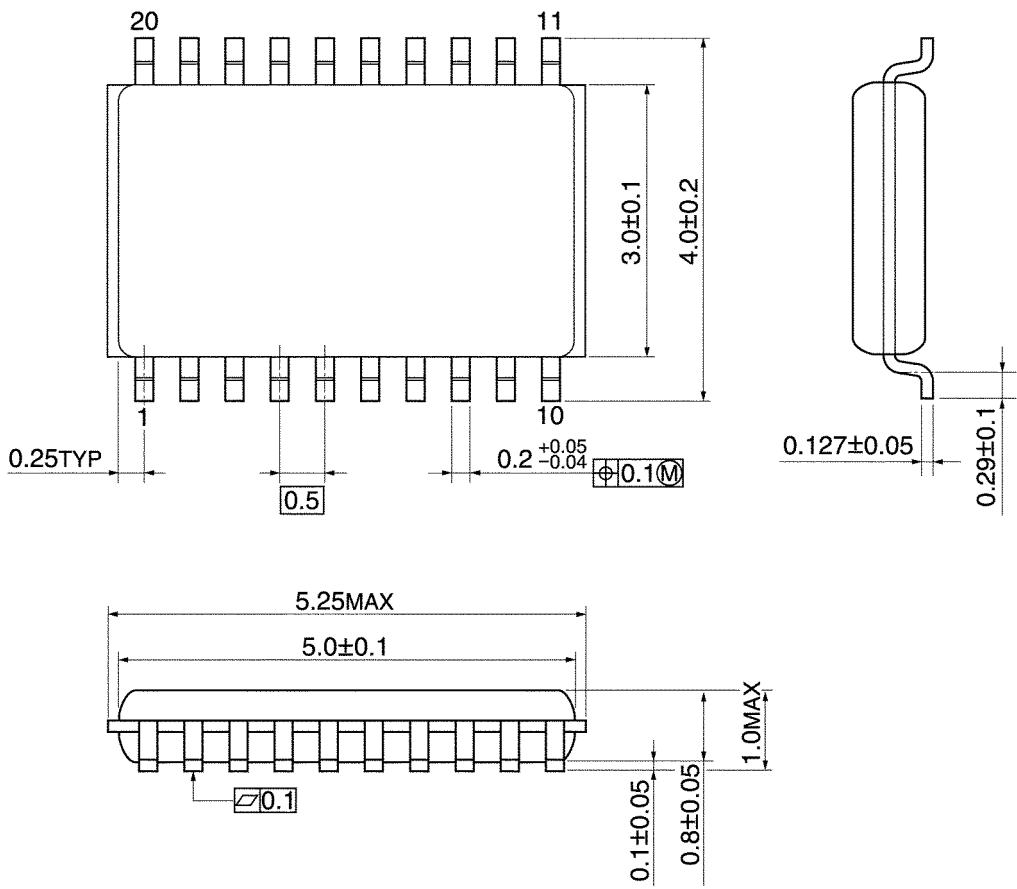


Weight: 0.08 g (typ.)

Package Dimensions

VSSOP20-P-0030-0.50

Unit: mm



Weight: 0.03 g (typ.)

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