

7 A V-I Chip EMI Filter

Description

The QPI-12 EMI filter is specifically designed to attenuate conducted common-mode (CM) and differential-mode (DM) noise of Vicor's V•I Chip products to comply with the CISPR22 standard requirements for conducted noise measurements. The filter is designed to operate up to 80 Vdc and supports 7 A loads up to 60°C without derating.

Designed for the telecom bus range, the V•I Chip EMI Filter supports the PICMG® 3.0 specification for filtering system boards to the EN55022 Class B limits.

Features

- >40 dB CM attenuation at 1 MHz
- >60 dB DM attenuation at 1 MHz
- 80 Vdc (max input)
- 100 Vdc surge 100 ms
- 1,500 Vdc hipot hold off to shield plane
- 7 A rating
- 12.4 x 25 x 4.5 mm SiP (System-in-Package)
- Low profile LGA package
- -40° to +100°C PCB temperature (see *Figure 6*)
- Efficiency >99%
- TÜV Certified

Applications

- Telecom and ATCA boards
- V•I Chip input power filter



Figure 1 – QPI-12, less than 1/2 in².

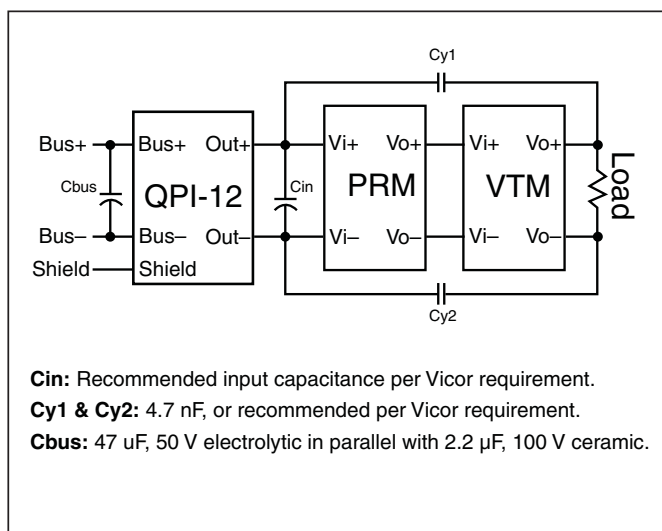


Figure 2 – QPI-12 Typical application schematic

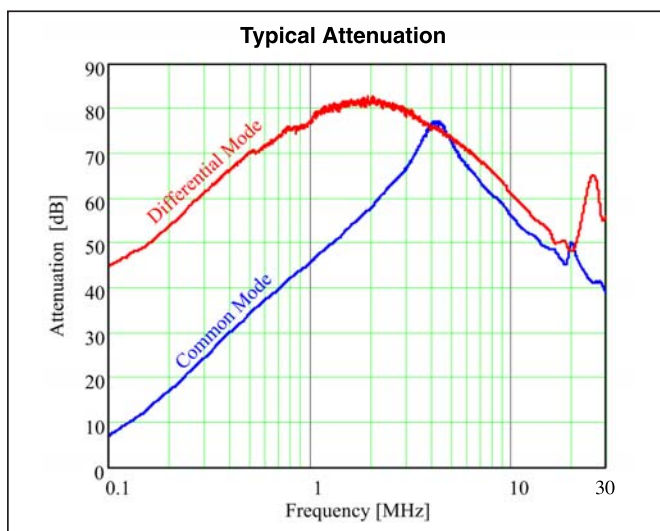


Figure 3 – QPI-12 network analyzer attenuation curves

Absolute Maximum Ratings – Exceeding these parameters may result in permanent damage to the product.

Pins	Parameter	Notes	Min	Max	Units
Bus+ to Bus–	Input voltage	Continuous	-80	80	Vdc
Bus+ to Bus–	Input voltage	100 ms transient	-100	100	Vdc
BUS+/BUS– to shield plane	BUS inputs to shield hipot		-1500	1500	Vdc
QPI+ to QPI–	Input to output current	Continuous @ 25°C		7	Adc
Package	Power dissipation	@ 25°C		1.50	W
Package	Operating temperature	PCB to filter interface		100	°C
Package	Thermal resistance	Free air		75	°C/W
Package	Thermal resistance	PCB Layout Fig. 7		30	°C/W
Package	Storage temperature		-55	125	°C
Package	Reflow temperature	20 s exposure		245	°C
All Pins	ESD	HBM	-2	+2	kV

Electrical Characteristics – Parameter limits apply over the operating PCB temperature range unless otherwise noted

Parameter	Notes	Min	Typ	Max	Units
Bus+ to Bus- input range	Measured at 7 A			76	Vdc
Bus+ to Out+ voltage drop	Measured at 7 A ⁽¹⁾		110		mVdc
Bus- to Out- voltage drop	Measured at 7 A ⁽¹⁾		110		mVdc
Common mode attenuation	VBUS = 48 V Frequency = 1.0 MHz	40			dB
Differential mode attenuation	VBUS = 48 V Frequency = 1.0 MHz	60			dB
Input bias current at 80 V	Input current from Bus+ to Bus-			10	μA

Note 1: See Figure 6 for current derating curve.

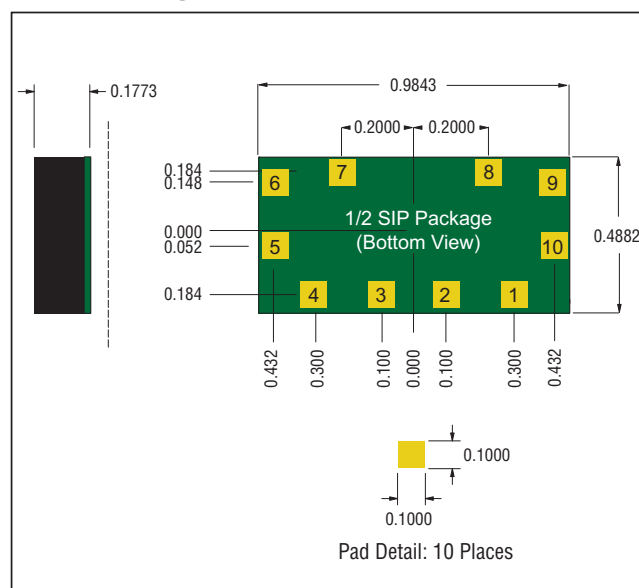
Pad Description

Pin Number	Name	Description
8, 9	Bus+	Positive bus potential
1, 10	Bus–	Negative bus potential
6, 7	Out+	Positive input to the converter
4, 5	Out–	Negative input to the converter
2, 3	Shield	Shield connects to system chassis or safety ground.

Ordering Information

Part Number	Description
QPI-12LZ	QPI-12 LGA Package, RoHS Compliant
QPI-12LZ-01	QPI-12 LGA, RoHS Compliant Open Frame Package

SiP Package Outline



EMI Performance

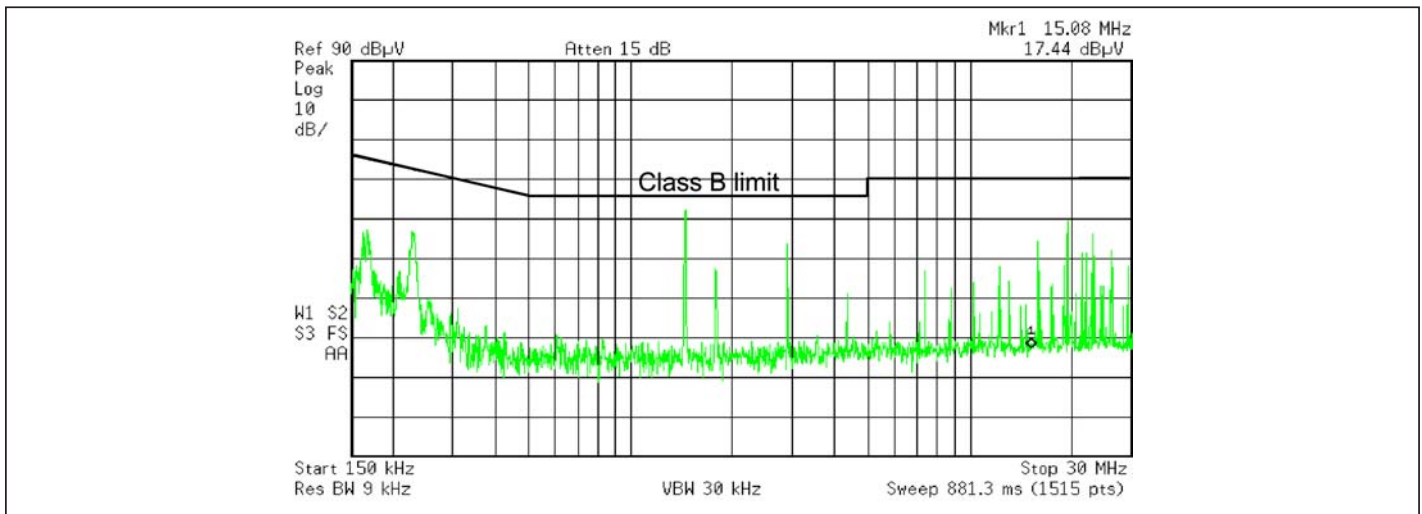


Figure 4 – Total conducted noise of P048K048T24IF & V048K120T025 with QPI-12 connected as shown in Figure 2. Output load = 170W: $C_{y1} = C_{y2} = 4.7 \text{ nF}$ & CBUS = 47 μF electrolytic in parallel with 2.2 μF ceramic.

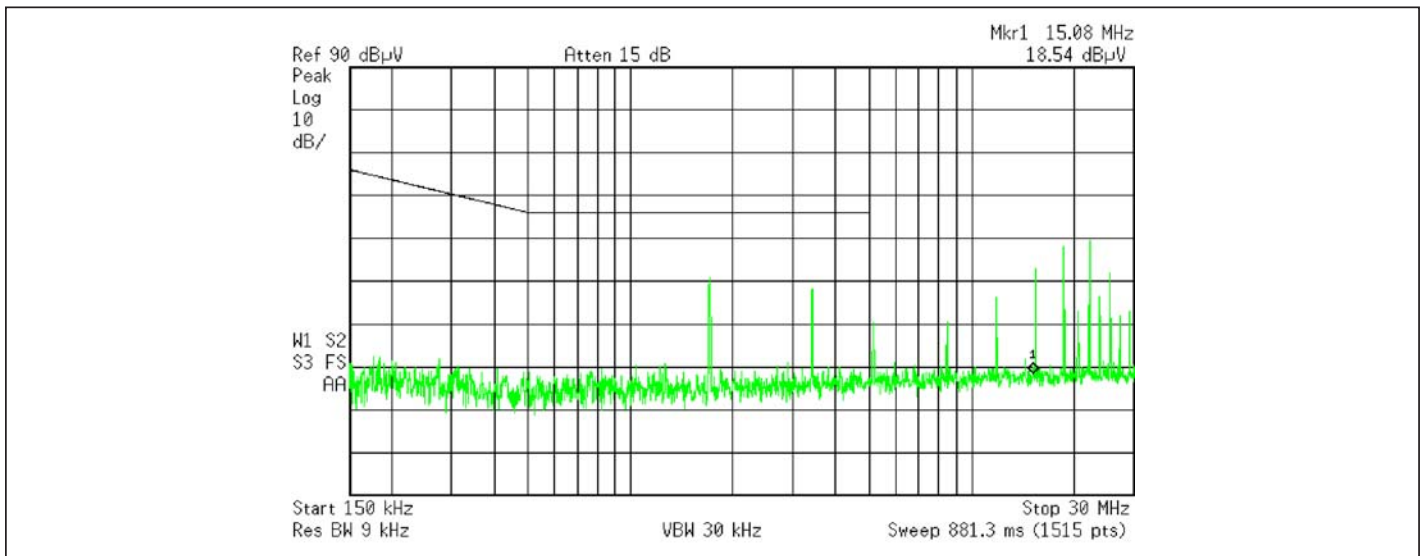


Figure 5 – Total conducted noise of BCM (B048A120T20) with QPI-12. Output load = 144 W. Same setup as in Figure 2, with the BCM replacing the VTM/PRM pair.

When laying out the QPI-12L, care must be taken such that the input and output signal polygons do not overlap each other on lower layers.

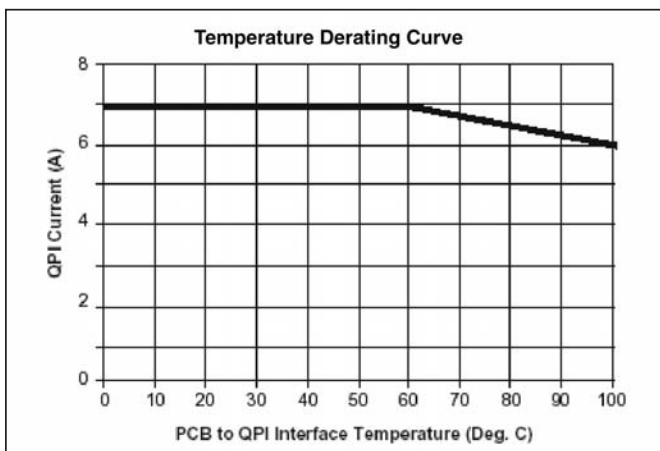


Figure 6 – Current vs. PCB temperature derating curve.

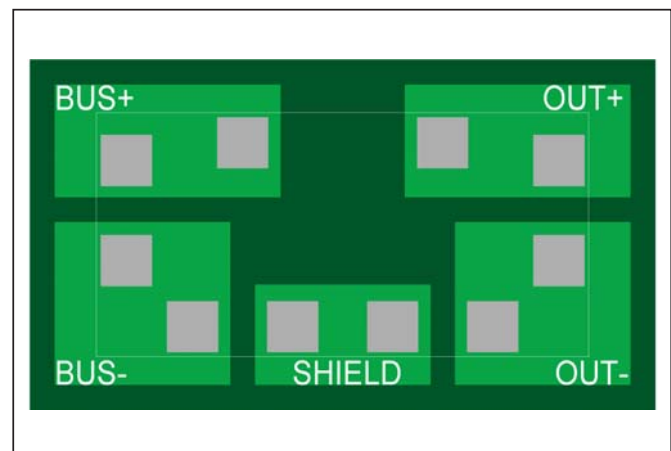


Figure 7 – Typical QPI-12L polygon layout.

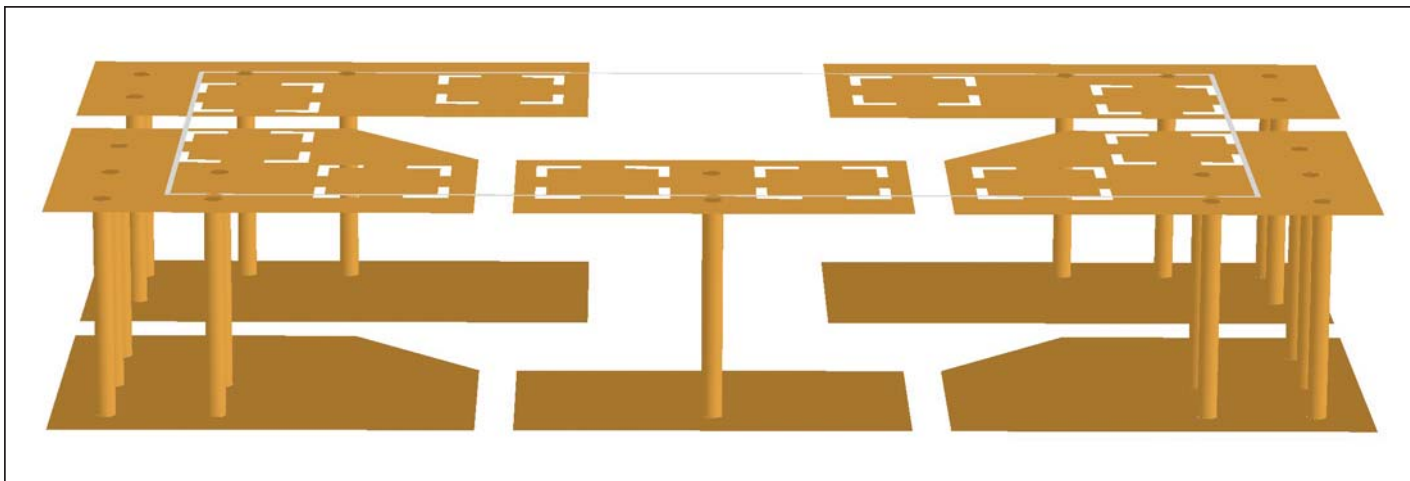


Figure 5 – Recommended mounting on a 2 layer board

QPI-12 PCB Layout Recommendations

The filtering performance of the QPI-11 and -12 is sensitive to capacitive coupling between its input and output pins. Parasitic plane capacitance must be kept below 1 pico-Farad between inputs and outputs using the layout shown above and the recommendations described below to achieve maximum conducted EMI performance.

To avoid capacitive coupling between input and output pins, there should not be any planes or large traces that run under both input and output pins, such as a ground plane or power plane. For example, if there are two signal planes or large traces where one trace runs under the input pins, and the other under the output pins, and both planes overlap in another area, they will cause capacitive coupling between input and output pins. Also, planes that run under both input and outputs pins, but do not cross, can cause capacitive coupling if they are capacitively by-passed together.

Figure 5 shows the recommended pcb layout on a 2 layer board. Here, the top layer planes are duplicated on the bottom layer so that there can be no overlapping of input and output planes. This method can be used for boards of greater layer count.

Post Solder Cleaning

Picor lidded QP SIPs are not hermetically sealed and must not be exposed to liquid, including but not limited to cleaning solvents, aqueous washing solutions or pressurized sprays.

When soldering, it is recommended that no-clean flux solder be used, as this will insure that potentially corrosive mobile ions will not remain on, around, or under the module following the soldering process.

For applications requiring water wash compatibility the “-01” open frame version should be used.

Vicor’s comprehensive line of power solutions includes high-density AC-DC & DC-DC modules and accessory components, fully configurable AC-DC & DC-DC power supplies, and complete custom power systems.

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Vicor Corporation
25 Frontage Road, Andover, MA, USA 01810
Tel: 800-735-6200 Fax: 978-475-6715

Email
Sales Support: vicorexp@vicorpower.com
Technical Support: apps@vicorpower.com