GENERAL DESCRIPTION

The XRT86SH328 has a total of 56 independent T1 framers (or 42 independent framers for E1). This Voyager Device maps 28 T1 payloads up to STS-3/ STM-1. The purpose of the 56 framers is to allow back-to-back transmit and receive framers on each of the 28 channel Egress and Ingress data paths. The channel numbering system references the framers according to the block diagram shown in **Figure 1**.

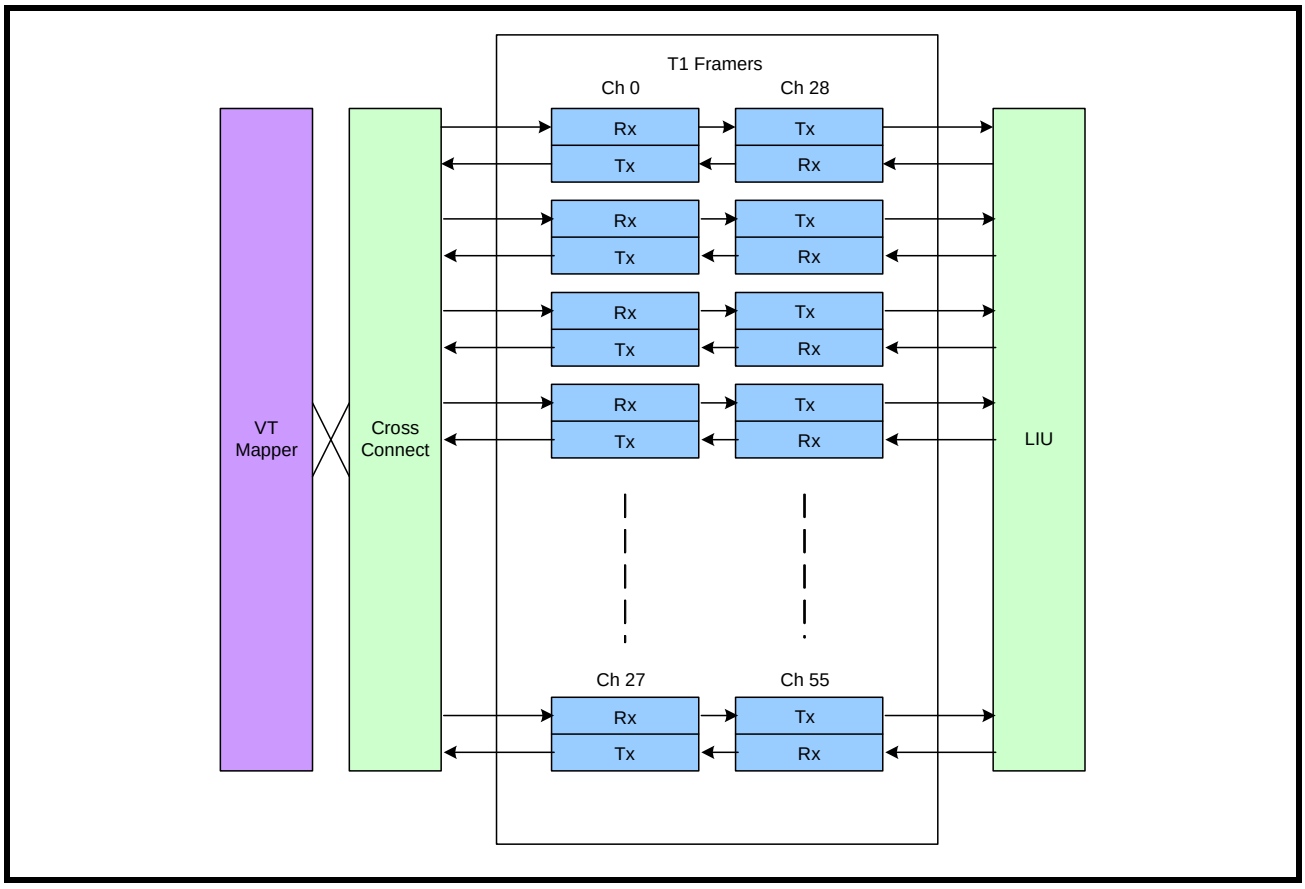
The XRT86SH328 provides T1 framing and error accumulation in accordance with ANSI/ITU_T specifications. Each framer has its own framing synchronizer and transmit-receive slip buffers. The slip buffers can be independently enabled or disabled as required and can be configured to frame to the common T1 signal formats.

Each Framer block contains its own Transmit and Receive T1 Framing function. There is 1 Transmit HDLC controller per channel which encapsulates contents of the Transmit HDLC buffers into LAPD Message frames. There is 1 Receive HDLC controller per channel which extracts the payload content of Receive LAPD Message frames from the incoming T1 data stream and write the contents into the Receive HDLC buffers.

The XRT86SH328 fully meets all of the latest T1 specifications: ANSI E1.107-1988, ANSI E1.403-1995, ANSI E1.231-1993, ANSI E1.408-1990, AT&T TR 62411 (12-90) TR54016, and ITU G-703, G.704, G706 and G.733, AT&T Pub. 43801, and ETS 300 011, 300 233, JT G.703, JT G.704, JT G706, I.431. Extensive test and diagnostic functions include Loop-backs, Boundary scan, Pseudo Random bit sequence (PRBS) test pattern generation, Performance Monitor, Bit Error Rate (BER) meter, forced error insertion, and LAPD unchannelized data payload processing according to ITU-T standard Q.921.

Applications and Features (next page)

FIGURE 1. XRT86SH328 21-CHANNEL T1 FRAMERS (56 TOTAL T1 FRAMERS)



APPLICATIONS

- High-Density T1 interfaces for Multiplexers, Switches, LAN Routers and Digital Modems
- SONET/SDH terminal or Add/Drop multiplexers (ADMs)
- T1 add/drop multiplexers (MUX)
- Channel Service Units (CSUs):
- Digital Access Cross-connect System (DACs)
- Digital Cross-connect Systems (DCS)
- Frame Relay Switches and Access Devices (FRADS)
- ISDN Primary Rate Interfaces (PRA)
- PBXs and PCM channel bank
- T3 channelized access concentrators and M13 MUX
- Wireless base stations
- ATM equipment with integrated E1 interfaces
- Multichannel T1 Test Equipment
- T1 Performance Monitoring
- Voice over packet gateways
- Routers

FEATURES

- Fifty-Six independent, full duplex T1 Tx and Rx Framer/LIUs
- Two 512-bit (two-frame) elastic store, PCM frame slip buffers (FIFO) on TX and Rx
- Supports Robbed Bit Signaling (RBS)
- Supports ISDN Primary Rate Interface (ISDN PRI) signaling
- Integrated HDLC controller per channel for transmit and receive, each controller having two 65-byte buffers (buffer 0 / buffer 1)
- HDLC Controllers Support SS7
- Timeslot assignable HDLC
- Automatic Performance Report Generation (PMON Status) can be inserted into the transmit LAPD interface every 1 second or for a single transmission
- Alarm Indication Signal with Customer Installation signature (AIS-CI)
- Remote Alarm Indication with Customer Installation (RAI-CI)
- Gapped Clock interface mode for Transmit and Receive.
- Intel/Motorola and Power PC interfaces for configuration, control and status monitoring
- Parallel search algorithm for fast frame synchronization
- Direct access to D and E channels for fast transmission of data link information
- PRBS, QRSS, and Network Loop Code generation and detection
- Each framer block encodes and decodes the T1 Frame serial data
- Detects and forces Red (SAI), Yellow (RAI) and Blue (AIS) Alarms

- Detects OOF, LOF, LOS errors and COFA conditions
- Loopbacks: Local (LLB) and Line remote (LB)
- Performance monitor with one second polling
- Boundary scan (IEEE 1149.1) JTAG test port
- Accepts external 8kHz Sync reference
- 1.8V Inner Core Voltage
- 3.3V I/O operation with 5V tolerant inputs
- 568-pin BGA package with -40°C to +85°C operation

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT86SH328IB	568 Ball BGA	-40°C to +85°C

DESCRIPTION OF THE CONTROL REGISTERS - T1 MODE

TABLE 1: REGISTER SUMMARY

FUNCTION	SYMBOL	HEX
Control Registers (0xN100 - 0xN1FF)		
Clock and Select Register	CSR	0xN100
Line Interface Control Register	LICR	0xN101
Reserved	-	0xN102 - 0xN106
Framing Select Register	FSR	0xN107
Alarm Generation Register	AGR	0xN108
Synchronization MUX Register	SMR	0xN109
Transmit Signaling and Data Link Select Register	TSDLSR	0xN10A
Framing Control Register	FCR	0xN10B
Receive Signaling & Data Link Select Register	RSDLSR	0xN10C
Receive Signaling Change Register 0	RSCR0	0xN10D
Receive Signaling Change Register 1	RSCR1	0xN10E
Receive Signaling Change Register 2	RSCR2	0xN10F
Reserved - E1 mode only	-	0xN110 - 0xN111
Receive In-Frame Register	RIFR	0xN112
Data Link Control Register	DLCR	0xN113
Transmit Data Link Byte Count Register	TDLBCR	0xN114
Receive Data Link Byte Count Register	RDLBCR	0xN115
Slip Buffer Control Register	SBCR	0xN116
Reserved	-	0xN117
Interrupt Control Register	ICR	0xN11A
Reserved	-	0xN11B
Customer Installation Alarm Generation Register	CIAGR	0xN11C
Performance Report Control Register	PRCR	0xN11D
Reserved	-	0xN11E
Reserved	-	0xN120
BERT Control & Status - Register 0	PRBSCSR0	0xN121
Reserved	-	0xN122
BERT Control & Status - Register 1	PRBSCSR1	0xN123
Loopback Code Control Register - Code 0	LCCR0	0xN124
Transmit Loopback Code Register	TLCR	0xN125

TABLE 1: REGISTER SUMMARY

FUNCTION	SYMBOL	HEX
Receive Loopback Activation Code Register - Code 0	RLACR0	0xN126
Receive Loopback Deactivation Code Register - Code 0	RLDCR0	0xN127
Defect Detection Enable Register	DDER	0xN129
Loopback Code Control Register - Code 1	LCCR1	0xN12A
Receive Loopback Activation Code Register - Code 1	RLACR1	0xN12B
Receive Loopback Deactivation Code Register - Code 1	RLDCR1	0xN12C
Loopback Code Control Register - Code 2	LCCR2	0xN12D
Receive Loopback Activation Code Register - Code 2	RLACR2	0xN12E
Receive Loopback Deactivation Code Register - Code 2	RLDCR2	0xN12F
Reserved - E1 mode only	-	0xN130 - 0xN13F
Transmit SPRM Control Register and NPRM	TSPRMCR	0xN142
BERT Control Register	BCR	0xN163
Time Slot (payload) Control (0xN300 - 0xN3FF)		
Transmit Channel Control Register 0-23	TCCR 0-23	0xN300 - 0xN317
Transmit User Code Register 0-23	TUCR 0-23	0xN320 - 0xN337
Transmit Signaling Control Register 0-23	TSCR 0-23	0xN340 - 0xN357
Receive Channel Control Register 0-23	RCCR 0-23	0xN360 - 0xN377
Receive User Code Register 0-23	RUCR 0-23	0xN380 - 0xN397
Receive Signaling Control Register 0-23	RSCR 0-23	0xN3A0 - 0xN3B7
Receive Substitution Signaling Register 0-23	RSSR 0-23	0xN3C0 - 0xN3D7
Receive Signaling Array (0xN500 - 0xN51F)		
Receive Signaling Array Register 0	RSAR0-23	0xN500 - 0xN517
LAPDn Buffer 0		
LAPD Buffer 0 Control Register	LAPDBCR0	0xN600 - 0xN660
LAPDn Buffer 1		
LAPD Buffer 1 Control Register	LAPDBCR1	0xN700 - 0xN760
Performance Monitor		
Receive Line Code Violation Counter: MSB	RLCVCU	0xN900
Receive Line Code Violation Counter: LSB	RLCVCL	0xN901
Receive Frame Alignment Error Counter: MSB	RFAECU	0xN902
Receive Frame Alignment Error Counter: LSB	RFAECL	0xN903

TABLE 1: REGISTER SUMMARY

FUNCTION	SYMBOL	HEX
Receive Severely Errored Frame Counter	RSEFC	0xN904
Receive Synchronization Bit (CRC-6) Error Counter: MSB	RSBBECU	0xN905
Receive Synchronization Bit (CRC-6) Error Counter: LSB	RSBBECL	0xN906
Receive FEBE Event Count Register: MSB	FEBECU	0xN907
Receive FEBE Event Count Register: LSB	FEBECL	0xN908
Receive Slip Counter	RSC	0xN909
Receive Loss of Frame Counter	RLFC	0xN90A
Receive Change of Frame Alignment Counter	RCOAC	0xN90B
LAPD Frame Check Sequence Error counter 1	LFCSEC1	0xN90C
PRBS bit Error Counter: MSB	PBECU	0xN90D
PRBS bit Error Counter: LSB	PBECL	0xN90E
Transmit Slip Counter	TSC	0xN90F
Excessive Zero Violation Counter: MSB	EZVCU	0xN910
Excessive Zero Violation Counter: LSB	EZVCL	0xN911
Interrupt Generation/Enable Register Address Map (0xNB00 - 0xNB41)		
Block Interrupt Status Register	BISR	0xNB00
Block Interrupt Enable Register	BIER	0xNB01
Alarm & Error Interrupt Status Register	AEISR	0xNB02
Alarm & Error Interrupt Enable Register	AEIER	0xNB03
Framer Interrupt Status Register	FISR	0xNB04
Framer Interrupt Enable Register	FIER	0xNB05
Data Link Status Register	DLSR1	0xNB06
Data Link Interrupt Enable Register	DLIER1	0xNB07
Slip Buffer Interrupt Status Register	SBISR	0xNB08
Slip Buffer Interrupt Enable Register	SBIER	0xNB09
Receive Loopback code Interrupt and Status Register - Code 0	RLCISR0	0xNB0A
Receive Loopback code Interrupt Enable Register - Code 0	RLCIER0	0xNB0B
Reserved - E1 Mode Only	-	0xNB0C - 0xNB0D
Excessive Zero Status Register	EXZSR	0xNB0E
Excessive Zero Enable Register	EXZER	0xNB0F
SS7 Status Register for LAPD	SS7SR	0xNB10
SS7 Enable Register for LAPD	SS7ER	0xNB11
RxLOS/CRC Interrupt Status Register	RLCISR	0xNB12

TABLE 1: REGISTER SUMMARY

FUNCTION	SYMBOL	HEX
RxLOS/CRC Interrupt Enable Register	RLCIER	0xNB13
Receive Loopback code Interrupt and Status Register - Code 1	RLCISR1	0xNB14
Receive Loopback code Interrupt Enable Register - Code 1	RLCIER1	0xNB15
Receive Loopback code Interrupt and Status Register - Code 2	RLCISR2	0xNB1A
Receive Loopback code Interrupt Enable Register - Code 2	RLCIER2	0xNB1B
Customer Installation Alarm Status Register	CIASR	0xNB40
Customer Installation Alarm Interrupt Enable Register	CIAIER	0xNB41
LIU Line Interface Unit Global Register Address Map (0x0100 - 0x01FF)		
LIU Global Configuration Register 0	LIU_GLOBAL0	0x0100
LIU Global Configuration Register 1	LIU_GLOBAL1	0x0101
LIU Global Configuration Register 2	LIU_GLOBAL2	0x0102
LIU Global Configuration Register 3	LIU_GLOBAL3	0x0103
LIU Global Configuration Register 4	LIU_GLOBAL4	0x0104
LIU Global Configuration Register 5	LIU_GLOBAL5	0x0105
LIU Global Configuration Register 6	LIU_GLOBAL6	0x0106
Reserved	-	0x0107 - 0x01FF
LIU Line Interface Unit Channel Register Address Map (0xN000 - 0xN011		
LIU Channel Configuration Register 0	LIU_Channel0	0xN000
LIU Channel Configuration Register 1	LIU_Channel1	0xN001
LIU Channel Configuration Register 2	LIU_Channel2	0xN002
LIU Channel Configuration Register 3	LIU_Channel3	0xN003
LIU Channel Configuration Register 4	LIU_Channel4	0xN004
LIU Channel Configuration Register 5	LIU_Channel5	0xN005
LIU Channel Configuration Register 6	LIU_Channel6	0xN006
LIU Channel Configuration Register 7	LIU_Channel7	0xN007
LIU Channel Configuration Register 8	LIU_Channel8	0xN008
LIU Channel Configuration Register 9	LIU_Channel9	0xN009
LIU Channel Configuration Register 10	LIU_Channel10	0xN00A
LIU Channel Configuration Register 11	LIU_Channel11	0xN00B
LIU Channel Configuration Register 12	LIU_Channel12	0xN00C
LIU Channel Configuration Register 13	LIU_Channel13	0xN00D
LIU Channel Configuration Register 14	LIU_Channel14	0xN00E
LIU Channel Configuration Register 15	LIU_Channel15	0xN00F

TABLE 1: REGISTER SUMMARY

FUNCTION	SYMBOL	HEX
LIU Channel Configuration Register 16	LIU_Channel16	0xN010
LIU Channel Configuration Register 17	LIU_Channel17	0xN011

1.0 REGISTER DESCRIPTIONS - T1 MODE

TABLE 2: CLOCK SELECT REGISTER (CSR) **HEX ADDRESS: 0XN100**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	LCV Insert	R/W	0	**Line Code Violation Insertion** This bit is used to force a Line Code Violation (LCV) on the transmit output. A “0” to “1” transition on this bit will cause a single LCV to be inserted on the transmit output.
6	Set T1 Mode	R/W	0	**T1/E1 Mode select** This bit is used to program the individual channel to operate in either T1 or E1 mode. 0 = Configures the selected channel to operate in E1 mode. 1 = Configures the selected channel to operate in T1 mode.
5	Sync All Transmit-ters to 8kHz	R/W	0	**Sync All Transmit Framers to 8kHz** This bit permits the user to configure each of the 56 Transmit T1 Framer blocks to synchronize their “transmit output” frame alignment with the 8kHz signal that is derived from the MCLK PLL, as described below. 0 - Disables the “Sync all Transmit Framers to 8kHz” feature for all channels. 1 - Enables the “Sync all Transmit Framers to 8kHz” feature for all channels. ***NOTE:*** *Writing to this bit in register 0x0100 will enable this feature for all channels.* ***NOTE:*** *This bit is only active if the MCLK PLL is used as the “Timing Source” for the Transmit T1 Framer” blocks. CSS[1:0] of this register allows users to select the transmit source of the framer.*
4:2	Reserved	R/W	00	**Reserved**

TABLE 2: CLOCK SELECT REGISTER (CSR) **HEX ADDRESS: 0XN100**

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>1:0</td><td>CSS[1:0]</td><td>R/W</td><td>01</td><td>Clock Source Select
These bits select the timing source for the Transmit T1 Framer block.

<table>
<tr><th>CSS[1:0]</th><th>TRANSMIT SOURCE FOR THE TRANSMIT T1 FRAMER BLOCK</th></tr>
<tr><td>00/11</td><td>Loop-Timing Mode:The Transmit T1 Framer block will derive its timing from the Received or Recovered Clock signal in 28-Channel Combo Mode only.</td></tr>
<tr><td>01</td><td>Local-Timing Mode: The Transmit T1 Framer block will either use up-stream timing or the TxDS1CLK_n input as its timing source.NOTE: For Aggregation Applications, the user MUST configure all active T1 Framer blocks to operate in this timing mode.</td></tr>
<tr><td>10</td><td>Local-Timing Mode: MCLK PLL Input. This timing option is only available if the user has configured the 28-Channel T1 Framer/LIU Combo Mode.</td></tr>
</table>
</td></tr>
</table>

TABLE 3: LINE INTERFACE CONTROL REGISTER (LICR) **HEX ADDRESS: 0XN101**

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>7</td><td>FORCE_LOS</td><td>R/W</td><td>0</td><td>Force Transmit LOS (To the Line Side)
This bit permits the user to configure the transmit direction circuitry (within the channel) to transmit the LOS pattern.
0 - Configures the transmit direction circuitry to transmit “normal” traffic.
1 - Configures the transmit direction circuitry to transmit the LOS Pattern.</td></tr>
<tr><td>6</td><td>Reserved</td><td>R/W</td><td>0</td><td>Reserved</td></tr>
<tr><td>5:4</td><td>LB[1:0]</td><td>R/W</td><td>00</td><td>Framer Loopback Selection
These bits are used to select any of the following loop-back modes for the framer section.
<table>
<tr><th>LB[1:0]</th><th>TYPES OF LOOPBACK SELECTED</th></tr>
<tr><td>00</td><td>Normal Mode (No LoopBack)</td></tr>
<tr><td>01</td><td>Framer Local LoopBack:
When framer local loopback is enabled, the transmit PCM input data is looped back to the receive PCM output data.</td></tr>
<tr><td>10</td><td>Framer Far-End (Remote) Line LoopBack:
When framer remote loopback is enabled, the receive digital data is looped back to the transmit output data.</td></tr>
<tr><td>11</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>3:0</td><td>Reserved</td><td>R/W</td><td>0</td><td>Reserved</td></tr>
</table>

TABLE 4: FRAMING SELECT REGISTER (FSR) **HEX ADDRESS: 0XN107**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Signaling update on Superframe Boundaries	R/W	0	**Enable Robbed-Bit Signaling Update on Superframe Boundary on Both Transmit and Receive Direction** This bit enables or disables robbed-bit signaling update on the superframe boundary for both the transmit and receive side of the framer. **On the Receive Side:** If signaling update is enabled, signaling data on the receive side (Signaling Array Register - RSAR) will be updated on the superframe boundary, otherwise, signaling data will be updated as soon as it is received. **On the Transmit Side:** If signaling update is enabled, any signaling data changes on the transmit side will be transmitted on the superframe boundary, otherwise, signaling data will be transmitted as soon as it is changed. 0 - Disables the signaling update feature for both transmit and receive. 1 - Enables the signaling update feature for both transmit and receive.
6	Force CRC Errors	R/W	0	**Force CRC Errors** This bit permits the user to force the Transmit T1 Framer block to transmit CRC errors within the outbound T1 data-stream, as depicted below. 0 - Disables CRC error transmission on the outbound T1 stream. 1 **-** Enables CRC error transmission on the outbound T1 stream.
5	J1_MODE	R/W	0	**J1 Mode** This bit is used to configure the device in J1 mode. Once the device is configured in J1 mode, the following two changes will happen: **1.** CRC calculation is done in J1 format. The J1 CRC6 calculation is based on the actual values of all 4632 bits in a T1 multiframe including Fe bits instead of assuming all Fe bits to be a one in T1 format. **2.** Receive and Transmit Yellow Alarm signal format is interpreted per the J1 standard. (J1-SF or J1-ESF) 0 - Configures the device in T1 mode. (Default) 1 - Configures the device in J1 mode. ***NOTE:*** *Users can select between J1-SF or J1-ESF by setting this bit and the T1 Framing Mode Select Bits[2:0] (Bits 2-0 within this register).*
4	ONEONLY	R/W	0	**Allow Only One Sync Candidate** This bit is used to specify one of the synchronization criteria that the Receive T1 Framer block employs. 0 - Allows the Receive T1 Framer to select any one of the winners in the matching process when there are two or more valid synchronization patterns appear in the required time frame. 1 - Allows the Receive T1 Framer to declare success of match when there is only one candidate left in the required time frame.

TABLE 4: FRAMING SELECT REGISTER (FSR) **HEX ADDRESS: 0XN107**

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>3</td><td>FASTSYNC</td><td>R/W</td><td>0</td><td>Faster Sync Algorithm
This bit is used to specify one of the synchronization criteria that the Receive T1 Framer block employs. If this “Faster Sync Algorithm” is enabled, the Receive T1 Framer Block will declare synchronization earlier. The table below specifies the number of consecutive frames with correct F-bits that the T1 Receive framer must receive in order to declare “SYNC” when FASTSYNC is enabled or disabled.

<table>
<tr><th>Framing</th><th>FastSync = 0</th><th>FastSync = 1</th></tr>
<tr><td>ESF</td><td>96</td><td>48</td></tr>
<tr><td>SF</td><td>48</td><td>24</td></tr>
<tr><td>N</td><td>48</td><td>24</td></tr>
<tr><td>SLC ® 96</td><td>48</td><td>24</td></tr>
</table>
0 - Disables FASTSYNC feature.
1 - Enables FASTSYNC feature.</td></tr>
<tr><td>2-0</td><td>FSl[2:0]</td><td>R/W</td><td>000</td><td>T1 Framing Mode Select [2:0]
These three bits permit the user to select the exact T1 framing format that the channel is to operate in.
Bit 2 is MSB and Bit 0 is LSB. The following table shows the five different framing formats that can be selected by configuring these three bits accordingly.
NOTE: Changing Framing formats 'on the fly' will cause the Receive T1 Framer block to undergo a “Reframe” event.

<table>
<tr><th>Framing</th><th>FS[2]</th><th>FS[1]</th><th>FS[0]</th></tr>
<tr><td>ESF</td><td>0</td><td>X</td><td>X</td></tr>
<tr><td>SF</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>N</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>T1DM</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>SLC®96</td><td>1</td><td>0</td><td>0</td></tr>
</table></td></tr>
</table>

TABLE 5: ALARM GENERATION REGISTER (AGR) **HEX ADDRESS: 0XN108**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Yellow Alarm - One Second Rule	R/W	0	**One-Second Yellow Alarm Rule Enforcement** This bit is used to enforce the one-second yellow alarm rule according to the yellow alarm (RAI) transmission duration per the ANSI standards. **If the one second alarm rule is enforced, the following will happen:** **1.** RAI will be transmitted for at least one second for both ESF and SF. **2.** There must be a minimum of one second delay between termination of the first RAI and the initiation of a subsequent RAI. **3.** ALARM_ENB bit (see description of bit 6 of this register) controls the duration of RAI. **4.** YEL[0] & YEL[1] (see description of bits 5-4 of this register) controls the format of RAI. **If the one second alarm rule is NOT enforced, the following will happen:** **1.** RAI will be transmitted for at least one second for ESF and SF. **2.** Minimum one second delay between termination of the first RAI and the initiation of the subsequent RAI is NOT enforced. **3.** YEL[0] and YEL[1] bits (see description of bits 5-4 of this register) are used to control the duration AND the format of RAI transmission. 0 - The one-second yellow alarm rule is NOT enforced. 1 - The one-second yellow alarm rule is enforced.
6	ALARM_ENB	R/W	0	**Yellow Alarm Transmission Enable** This bit is used to control the duration of yellow alarm (RAI) when the one-second yellow alarm rule is enforced (bit 7 of this register set to'1'). When the one-second yellow alarm rule is not enforced (bit 7 of this register set to'0'), the duration of the RAI is controlled by the YEL[0] and YEL[1] bits (bits 5-4 of this register). **If the one-second alarm rule is enforced:** 0 - Stop the transmission of yellow alarm (see description of bits 5-4). 1 - Start the transmission of yellow alarm (see description of bits 5-4). ***NOTE:*** *This bit has no function if the one second alarm rule is not enforced.*

TABLE 5: ALARM GENERATION REGISTER (AGR) **HEX ADDRESS: 0XN108**

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>5-4</td><td>YEL[1:0]</td><td>R/W</td><td>00</td><td>
Yellow Alarm (RAI) Duration and Format
The exact function of these bits depends on whether or not the one-second yellow alarm rule is enforced. (Bit 7 of this register). The decoding of these bits are explained in Table 6 and Table 7 below.

TABLE 6: YELLOW ALARM DURATION AND FORMAT WHEN ONE SECOND RULE IS NOT ENFORCED
<table>
<tr><th>YEL[1:0]</th><th>YELLOW ALARM DURATION AND FORMAT</th></tr>
<tr><td>00</td><td>Disable the transmission of yellow alarm</td></tr>
<tr><td>01</td><td>SF or N mode:
RAI is transmitted as bit 2 = 0 (second MSB) in all DS0 data channel.
T1DM mode:
RAI is transmitted as Y-bit = 0 (6th bit in the SYNC byte).
ESF mode:
1. If YEL[0] bit is set ’high’ for a duration shorter or equal to the time required to transmit 255 patterns of 1111_1111_0000_0000 on the 4-kbit/s data link bits (M1-M12), RAI is transmitted for 255 patterns.of 1111_1111_0000_0000 (approximately 1 second)
2. If YEL[0] bit is set ’high’ for a duration longer than the time required to transmit 255 patterns of 1111_1111_0000_0000 on the 4-kbit/s data link bits (M1-M12), RAI transmission continues until YEL[0] bit is set ’low’.
3. If YEL[0] bit forms another pulse during the RAI transmission, it resets the pattern counter and extends the RAI duration for another 255 patterns of 1111_1111_0000_0000. (approximately 1 second)</td></tr>
<tr><td>10</td><td>SF mode:
RAI is transmitted as a “1” in the Fs bit of frame 12 (This is RAI for J1 SF standard).
T1DM mode:
RAI is transmitted as Y-bit = 0 (6th bit in the SYNC byte).
ESF mode:
RAI is controlled by the duration of YEL[1] bit. This allows continuous RAI of any length.</td></tr>
<tr><td>11</td><td>SF, N, and T1DM mode:
RAI format is the same as described above when YEL[1:0] is set to’01’.
ESF mode:
RAI duration is the same as described above when YEL[1:0] is set to’01’, except that format of RAI is transmitted as 255 patterns of 1111_1111_1111_1111 (sixteen ones) on the 4kbits/s data link bits instead of 255 patterns of 1111_1111_0000_0000.
NOTE: 255 patterns of 1111_1111_1111_111 is the J1 ESF RAI standard)</td></tr>
</table>
</td></tr>
</table>

TABLE 5: ALARM GENERATION REGISTER (AGR) **HEX ADDRESS: 0XN108**

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>5-4</td><td>YEL[1:0]</td><td>R/W</td><td>00</td><td>(Continued)

TABLE 7: YELLOW ALARM FORMAT WHEN ONE SECOND RULE IS ENFORCED
<table>
<tr><th>YEL[1:0]</th><th>YELLOW ALARM FORMAT</th></tr>
<tr><td>00</td><td>Disable the transmission of yellow alarm</td></tr>
<tr><td>01</td><td>SF or N mode:
RAI is transmitted as bit 2 = 0 (second MSB) in all DS0 data channel.
T1DM mode:
RAI is transmitted as Y-bit = 0 (6th bit in the SYNC byte).
ESF mode:
YEL[1:0] controls the format of RAI. When YEL[1:0] is set to’01’, RAI is transmitted as 255 patterns of 1111_1111_0000_0000 on the 4-kbit/s data link (M1-M12) (approximately 1 second).
ALARM_ENB (Bit 6 of this register) controls the duration of RAI as described below:
1. If ALARM_ENB bit is set ’high’ for a duration shorter or equal to the time required to transmit 255 pattern of 1111_1111_0000_0000 on the 4-kbit/s data link (M1-M12), RAI is transmitted for 255 patterns. (approximately 1 second)
2. If ALARM_ENB bit is set ’high’ for a duration longer than the time required to transmit 255 patterns of 1111_1111_0000_0000 on the 4-kbit/s data link (M1-M12), RAI continues until ALARM_ENB bit is set ’low’.
3. If ALARM_ENB forms another pulse during an alarm transmission, it resets the pattern counter and extends the RAI duration for another 255 patterns.(approximately 1 second)
NOTE: A minimum of one second delay between termination of the first RAI and the initiation of a subsequent RAI is enforced.</td></tr>
<tr><td>10</td><td>SF mode:
RAI is transmitted as a “1” in the Fs bit of frame 12 (This is RAI for J1 SF standard).
T1DM mode:
RAI is transmitted as Y-bit = 0 (6th bit in the SYNC byte).
ESF mode:
RAI is controlled by the duration of ALARM_ENB bit. This allows continuous RAI of any length.</td></tr>
<tr><td>11</td><td>SF, N, and T1DM mode:
RAI format is the same as described above when YEL[1:0] is set to’01’.
ESF mode:
RAI duration is the same as described above when YEL[1:0] is set to’01’, except that format of RAI is transmitted as 255 patterns of 1111_1111_1111_1111 on the 4kbits/s data link bits (J1 ESF standard) instead of 255 patterns of 1111_1111_0000_0000.</td></tr>
</table></td></tr>
</table>

TABLE 5: ALARM GENERATION REGISTER (AGR) **HEX ADDRESS: 0XN108**

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>3-2</td><td>Transmit AIS Pattern Select[1:0]</td><td>R/W</td><td>00</td><td>Transmit AIS Pattern Select[1:0]:
These two bits permit the user to do the following.
1. To select the appropriate AIS Pattern that the Transmit T1 Framer block will transmit to the remote terminal equipment, and
2. To command (via Software Control) the Transmit T1 Framer block to transmit that particular AIS Pattern to the remote terminal equipment, as depicted below.

<table>
<tr><th>AISG[1:0]</th><th>TYPES OF AIS PATTERNS TRANSMITTED</th></tr>
<tr><td>00/10</td><td>Disable AIS Alarm Generation
The Transmit T1 Framer block will transmit “normal” T1 traffic to the remote terminal equipment.</td></tr>
<tr><td>01</td><td>Enable Unframed AIS Alarm Generation
Transmit T1 Framer block will transmit an Unframed All Ones Pattern, as an AIS Pattern.</td></tr>
<tr><td>11</td><td>Enable Framed AIS Alarm Generation
Transmit T1 Framer block will transmit a Framed, All Ones Pattern, as the AIS Pattern.</td></tr>
</table>

NOTE: For normal operation (e.g., to configure the Transmit T1 Framer block to transmit normal T1 traffic) the user should set this bit to “[X, 0]”</td></tr>
<tr><td>1-0</td><td>AIS Defect Declaration Criteria [1:0]</td><td>R/W</td><td>00</td><td>AIS Defect Declaration Criteria[1:0]:
These bits permit the user to specify the types of AIS Patterns that the Receive T1 Framer block must detect before it will declare the AIS defect condition.

<table>
<tr><th>AISD[1:0]</th><th>AIS Defect Declaration Criteria</th></tr>
<tr><td>00/10</td><td>AIS Detection Disabled
AIS Defect Condition will NOT be declared.</td></tr>
<tr><td>01</td><td>Enable Unframed and Framed AIS Alarm Detection
ReceiveT1 Framer block will detect both Unframed and Framed AIS pattern</td></tr>
<tr><td>11</td><td>Enable Framed AIS Alarm Detection
Receive T1 Framer block will detect only Framed AIS pattern</td></tr>
</table>
</td></tr>
</table>

TABLE 8: SYNCHRONIZATION MUX REGISTER (SMR) **HEX ADDRESS: 0XN109**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-2	Reserved	-	-	**Reserved**
1	CRC-6 Bits Source Select	R/W	0	**CRC-6 Bits Source Select** This bit permits the user to specify the source of the CRC-6 bits, within the outbound T1 data-stream, as depicted below. 0 - Configures the Transmit T1 Framer block to internally compute and insert the CRC-6 bits within the outbound T1 data-stream. 1 - Configures the Transmit T1 Framer block to externally accept data from the input, and to insert this data into the CRC-6 bits within the outbound T1 data-stream. *This bit is ignored if CRC Multiframe Alignment is disabled*
0	Framing Bits Source Select	R/W	0	**Framing Bits Source Select** This bit is used to specify the source for the Framing bits that will be inserted into the outbound T1 frames. The Framing bits can be generated internally or inserted from the transmit serial input. 0 = Configures the Transmit T1 Framer block to internally generate and insert the Framing bits into the outbound T1 data stream. 1 = Configures the Transmit T1 Framer block to externally accept framing bits from the input, and to insert this data to the outbound T1 data-stream.

TABLE 9: TRANSMIT SIGNALING AND DATA LINK SELECT REGISTER (TSDLSR) **HEX ADDRESS:0XN10A**

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>7-6</td><td>Reserved</td><td>-</td><td>-</td><td>Reserved</td></tr>
<tr><td>5-4</td><td>TxDLBW[1:0]</td><td>R/W</td><td>00</td><td>Transmit Data Link Bandwidth[1:0]
These two bits are used to select the bandwidth for data link message transmission. Data Link messages can be transmitted at a 4kHz rate or at a 2kHz rate on odd or even framing bits depending on the configuration of these three bits. The table below specifies the four different configurations.

<table>
<tr><th>TXDLBW[1:0]</th><th>TRANSMIT DATA LINK BANDWIDTH SELECTED</th></tr>
<tr><td>00</td><td>Data link bits are inserted in every frame. Facility Data Link Bits (FDL) is a 4kHz data link channel.</td></tr>
<tr><td>01</td><td>Data link bits are inserted in every other frame. Facility Data Link Bits (FDL) is a 2kHz data link channel carried by odd framing bits (Frames 1,5,9.....)</td></tr>
<tr><td>10</td><td>Data link bits are inserted in every other frame. Facility Data Link Bits (FDL) is a 2kHz data link channel carried by even framing bits (Frames 3,7,11.....)</td></tr>
<tr><td>11</td><td>Reserved</td></tr>
</table>

NOTE: This bit only applies to T1 ESF framing format. For SLC96 and N framing formats, FDL is a 4kHz data link channel. For T1DM, FDL is a 8kHz data link channel.</td></tr>
<tr><td>3-2</td><td>TxDE[1:0]</td><td>R/W</td><td>00</td><td>Transmit D/E TimeSlot Source Select[1:0]:
These two bits specify the source for transmit D/E time slots. The table below shows the different sources from which D/E time slots can be inserted.

<table>
<tr><th>TXDE[1:0]</th><th>SOURCE FOR TRANSMIT D/E TIMESLOTS</th></tr>
<tr><td>00</td><td>Input - The D/E time slots are inserted from the transmit serial data input.</td></tr>
<tr><td>01</td><td>Transmit LAPD Controller - The D/E time slots are inserted from LAPD Controller.</td></tr>
<tr><td>10/11</td><td>Reserved</td></tr>
</table>
</td></tr>
</table>

TABLE 9: TRANSMIT SIGNALING AND DATA LINK SELECT REGISTER (TSDLSR) **HEX ADDRESS:0XN10A**

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>1-0</td><td>TxDL[1:0]</td><td>R/W</td><td>00</td><td>Transmit Data Link Source Select [1:0]
These two bits specify the source for data link bits that will be inserted in the outbound T1 frames. The table below shows the three different sources from which data link bits can be inserted.

<table>
<tr><th>TXDL[1:0]</th><th>SOURCE FOR DATA LINK BITS</th></tr>
<tr><td>00</td><td>Transmit LAPD Controller / SLC96 Buffer - The Data Link bits are inserted from the Transmit LAPD Controller or SLC96 Buffer.</td></tr>
<tr><td>01</td><td>Input - The Data Link bits are inserted from the transmit serial data input.</td></tr>
<tr><td>10</td><td>Reserved</td></tr>
<tr><td>11</td><td>Data Link bits are forced to 1.</td></tr>
</table>
</td></tr>
</table>

TABLE 10: FRAMING CONTROL REGISTER (FCR) **HEX ADDRESS: 0XN10B**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reframe	R/W	0	**Force Reframe** A '0' to '1' transition will force the Receive T1 Framer to restart the synchronization process. This bit field is automatically cleared (set to 0) after frame synchronization is reached.
6	Framing with CRC Checking	R/W	1	**Framing with CRC Checking in ESF** This bit permits the user to include CRC verification as a part of the "T1/ESF Framing Alignment" process. If the user enables this feature, then the Receive T1 Framer block will also check and verify that the incoming T1 data-stream contains correct CRC data, prior to declaring the "In-Frame" condition. 0 - CRC Verification is NOT included in the "Framing Alignment" process. 1 - Receive T1 Framer block will also check for correct CRC values prior to declaring the "In-Frame" condition.
5-3	LOF Tolerance[2:0]	R/W	010	**LOF Defect Declaration Tolerance[2:0]:** These bits along with the LOF_RANGE[2:0] bits are used to define the LOF Defect Declaration criteria. The Receive T1 Framer block will declare the LOF defect condition anytime it detects "LOF_Tolerance[2:0]" out of "LOF_Range[2:0] framing bit errors within the incoming T1 data-stream. The recommended LOF_TOLR value is 2. ***NOTE:*** *A "0" value for LOF_TOLR is internally blocked. A LOF_TOLR value must be specified.*
2-0	LOF_Range[2:0]	R/W	101	**LOF Defect Declaration Range[2:0]:** These bits along with the "LOF_Tolerance[2:0] bits are used to define the "LOF Defect Declaration" criteria. The Receive T1 Framer block will declare the LOF Defect condition anytime it has received "LOF_Tolerance[2:0] out of "LOF_Range[2:0] framing bit errors, within the incoming T1 data-stream. The recommended LOF_ANG value is 5. ***NOTE:*** *A "0" value for LOF_RANG is internally blocked. A LOF_RANG value must be specified.*

TABLE 11: RECEIVE SIGNALING & DATA LINK SELECT REGISTER (RSDLSR) **HEX ADDRESS: 0XN10C**

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>7-6</td><td>Reserved</td><td>-</td><td>-</td><td>Reserved</td></tr>
<tr><td>5-4</td><td>RxDLBW[1:0]</td><td>R/W</td><td>00</td><td>Receive Data Link Bandwidth[1:0]:
These two bits select the bandwidth for data link message reception. Data Link messages can be received at a 4kHz rate or at a 2kHz rate on odd or even framing bits depending on the configuration of these bits. The table below specifies the different configurations.

<table>
<tr><th>RXDLBW[1:0]</th><th>RECEIVE DATA LINK BANDWIDTH SELECTED</th></tr>
<tr><td>00</td><td>Received Data link bits are extracted in every frame. Facility Data Link Bits (FDL) is a 4kHz data link channel.</td></tr>
<tr><td>01</td><td>Received Data link bits are extracted in every other frame. Facility Data Link Bits (FDL) is a 2kHz data link channel carried by odd framing bits (Frames 1,5,9.....)</td></tr>
<tr><td>10</td><td>Received Data link bits are extracted in every other frame. Facility Data Link Bits (FDL) is a 2kHz data link channel carried by even framing bits (Frames 3,7,11.....)</td></tr>
<tr><td>11</td><td>Reserved</td></tr>
</table>

NOTE: This bit only applies to T1 ESF framing format. For SLC96 and N framing formats, FDL is a 4kHz data link channel. For T1DM, FDL is a 8kHz data link channel.</td></tr>
<tr><td>3-2</td><td>RxDE[1:0]</td><td>R/W</td><td>00</td><td>Receive D/E Time-Slot Destination Select[1:0]:
These bits permit the user to specify the “destination” circuitry that will receive and process the D/E-Time-slot within the incoming T1 data-stream.

<table>
<tr><th>RXDE[1:0]</th><th>DESTINATION CIRCUITRY FOR RECEIVE D/E TIME-SLOT</th></tr>
<tr><td>00</td><td>Output - The D/E time slots are output to the receive serial data output.</td></tr>
<tr><td>01</td><td>Receive LAPD Controller Block - The D/E time slots are output to Receive LAPD Controller Block.</td></tr>
<tr><td>10//11</td><td>Reserved</td></tr>
</table></td></tr>
</table>

TABLE 11: RECEIVE SIGNALING & DATA LINK SELECT REGISTER (RSDLSR) **HEX ADDRESS: 0XN10C**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1-0	RxDL[1:0]	R/W	00	**Receive Data-Link Destination Select[1:0]:** These bits specify the destination circuitry, that is used to process the Data-Link data, within the incoming T1 data-stream.

RXDL[1:0]	DESTINATION CIRCUITRY FOR RECEIVE DATA-LINK
00	**Receive LAPD Controller Block and Output** - The Data Link bits are routed to the Receive LAPD Controller block and the output.
01	**Output**- The Data Link bits are routed to the output.
10	**Reserved**
11	**Data Link bits are forced to 1**.

TABLE 12: RECEIVE SIGNALING CHANGE REGISTER 0 (RSCR 0) **HEX ADDRESS: 0XN10D**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Ch. 0	RUR	0	These bits indicate whether the Channel Associated signaling data, associated with Time-Slots 0 through 7 within the incoming T1 data-stream, has changed since the last read of this register, as depicted below. 0 - CAS data (for Time-slots 0 through 7) has NOT changed since the last read of this register. 1 - CAS data (for Time-slots 0 through 7) HAS changed since the last read of this register. ***NOTES:*** *1. Bit 7 (Time-Slot 0) is NOT active, since it carries the FAS and National Bits.* ***NOTE:*** *2. This register is only active if the incoming T1 data-stream is using Channel Associated Signaling.*
6	Ch. 1	RUR	0	
5	Ch.2	RUR	0	
4	Ch.3	RUR	0	
3	Ch.4	RUR	0	
2	Ch.5	RUR	0	
1	Ch.6	RUR	0	
0	Ch.7	RUR	0	

TABLE 13: RECEIVE SIGNALING CHANGE REGISTER 1 (RSCR 1) **HEX ADDRESS: 0XN10E**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Ch.8	RUR	0	These bits indicate whether the Channel Associated signaling data, associated with Time-Slots 8 through 15 within the incoming T1 data-stream, has changed since the last read of this register, as depicted below. 0 - CAS data (for Time-slots 8 through 15) has NOT changed since the last read of this register. 1 - CAS data (for Time-slots 8 through 15) HAS changed since the last read of this register. ***NOTE:*** *This register is only active if the incoming T1 data-stream is using Channel Associated Signaling.*
6	Ch.9	RUR	0	
5	Ch.10	RUR	0	
4	Ch.11	RUR	0	
3	Ch.12	RUR	0	
2	Ch.13	RUR	0	
1	Ch.14	RUR	0	
0	Ch.15	RUR	0	

TABLE 14: RECEIVE SIGNALING CHANGE REGISTER 2 (RSCR 2) **HEX ADDRESS: 0XN10F**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Ch.16	RUR	0	These bits indicate whether the Channel Associated signaling data, associated with Time-Slots 16 through 23 within the incoming T1 data-stream, has changed since the last read of this register, as depicted below. 0 - CAS data (for Time-slots 16 through 23) has NOT changed since the last read of this register. 1 - CAS data (for Time-slots 16 through 23) HAS changed since the last read of this register. ***NOTE:*** *This register is only active if the incoming T1 data-stream is using Channel Associated Signaling.*
6	Ch.17	RUR	0	
5	Ch.18	RUR	0	
4	Ch.19	RUR	0	
3	Ch.20	RUR	0	
2	Ch.21	RUR	0	
1	Ch.22	RUR	0	
0	Ch.23	RUR	0	

TABLE 15: RECEIVE EXTRA BITS REGISTER (REBR) **HEX ADDRESS: 0XN112**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	In-Frame	RO	0	**In Frame State:** This READ-ONLY bit indicates whether the Receive T1 Framer block is currently declaring the “In-Frame” condition with the incoming T1 data-stream. 0 - Indicates that the Receive T1 Framer block is currently declaring the LOF (Loss of Frame) Defect condition. 1 - Indicates that the Receive T1 Framer block is currently declaring itself to be in the “In-Frame” condition.
6-0	Reserved	-	-	**Reserved**

TABLE 16: DATA LINK CONTROL REGISTER (DLCR) **HEX ADDRESS: 0XN113**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	SLC-96 Data Link Enable	R/W	0	**SLC®96 DataLink Enable** This bit permits the user to configure the channel to support the transmission and reception of the “SLC-96 type” of data-link message. 0 - Channel does not support the transmission and reception of “SLC-96” type of data-link messages. Regular SF framing bits will be transmitted. 1 - Channel supports the transmission and reception of the “SLC-96” type of data-link messages. *This bit is only active if the channel has been configured to operate in either the SLC-96 or the ESF Framing formats.*
6	MOS ABORT Disable	R/W	0	**MOS ABORT Disable:** This bit permits the user to either enable or disable the “Automatic MOS ABORT” feature within Transmit HDLC Controller. If the user enables this feature, then Transmit HDLC Controller block will automatically transmit the ABORT Sequence (e.g., a zero followed by a string of 7 consecutive “1s”) whenever it abruptly transitions from transmitting a MOS type of message, to transmitting a BOS type of message. If the user disables this feature, then the Transmit HDLC Controller Block will NOT transmit the ABORT sequence, whenever it abruptly transitions from transmitting a MOS-type of message to transmitting a BOS-type of message. 0 - Enables the “Automatic MOS Abort” feature 1 - Disables the “Automatic MOS Abort” feature
5	Rx_FCS_DIS	R/W	0	**Receive Frame Check Sequence (FCS) Verification Enable/Disable** This bit permits the user to configure the Receive HDLC Controller Block to compute and verify the FCS value within each incoming LAPD message frame. 0 - Enables FCS Verification 1 - Disables FCS Verification
4	AutoRx	R/W	0	**Auto Receive LAPD Message** This bit configures the Receive HDLC Controller Block to discard any incoming BOS or LAPD Message frame that exactly match which is currently stored in the Receive HDLC buffer. 0 = Disables this “AUTO DISCARD” feature 1 = Enables this “AUTO DISCARD” feature.
3	Tx_ABORT	R/W	0	**Transmit ABORT** This bit configures the Transmit HDLC Controller Block to transmit an ABORT sequence (string of 7 or more consecutive 1’s) to the Remote terminal. 0 - Configures the Transmit HDLC Controller Block to function normally (e.g., not transmit the ABORT sequence). 1 - Configures the Transmit HDLC Controller block to transmit the ABORT Sequence.

TABLE 16: DATA LINK CONTROL REGISTER (DLCR) **HEX ADDRESS: 0XN113**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
2	Tx_IDLE	R/W	0	**Transmit Idle (Flag Sequence Byte)** This bit configures the Transmit HDLC Controller Block to unconditionally transmit a repeating string of Flag Sequence octets (0X7E) in the data link channel to the Remote terminal. In normal conditions, the Transmit HDLC Controller block will repeatedly transmit the Flag Sequence octet whenever there is no MOS message to transmit to the remote terminal equipment. However, if the user invokes this "Transmit Idle Sequence" feature, then the Transmit HDLC Controller block will UNCONDITIONALLY transmit a repeating stream of the Flag Sequence octet (thereby overwriting all outbound MOS data-link messages). 0 - Configures the Transmit HDLC Controller Block to transmit data-link information in a "normal" manner. 1 - Configures the Transmit HDLC Controller block to transmit a repeating string of Flag Sequence Octets (0x7E). ***NOTE:*** *This bit is ignored if the* Transmit *HDLC controller is operating in the BOS Mode - bit 0 (MOS/BOS) within this register is set to 0.*
1	Tx_FCS_EN	R/W	0	**Transmit LAPD Message with Frame Check Sequence (FCS)** This bit permits the user to configure the Transmit HDLC Controller block to compute and append FCS octets to the "back-end" of each outbound MOS data-link message. 0 - Configures the Transmit HDLC Controller block to NOT compute and append the FCS octets to the back-end of each outbound MOS data-link message. 1 - Configures the Transmit HDLC Controller block TO COMPUTE and append the FCS octets to the back-end of each outbound MOS data-link message. ***NOTE:*** *This bit is ignored if the transmit HDLC controller has been configured to operate in the BOS mode - bit 0 (MOS/BOS) within this register is set to 0.*
0	MOS/$\overline{\text{BOS}}$	R/W	0	**Message Oriented Signaling/Bit Oriented Signaling Send** This bit permits the user to send LAPD transmission through HDLC Controller Block using either BOS (Bit-Oriented Signaling) or MOS (Message-Oriented Signaling) frames. 0 - Transmit HDLC Controller block BOS message Send. 1 - Transmit HDLC Controller block MOS message Send. ***NOTE:*** *This is not an Enable bit. This bit must be set to '0' each time a BOS is to be sent or '1' each time a MOS is to be sent.*

TABLE 17: TRANSMIT DATA LINK BYTE COUNT REGISTER (TDLBCR) **HEX ADDRESS: 0XN114**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	TxHDLC BUFAvail/ BUFSel	R/W	0	**Transmit HDLC Buffer Available/Buffer Select** This bit has different functions, depending upon whether the user is writing to or reading from this register, as depicted below. **If the user is writing data into this register bit:** 0 - Configures the Transmit HDLC Controller to read out and transmit the data, residing within “Transmit HDLC Buffer # 0", via the Data Link channel to the remote terminal equipment. 1 - Configures the Transmit HDLC Controller to read out and transmit the data, residing within the “Transmit HDLC Buffer #1”, via the Data Link channel to the remote terminal equipment. **If the user is reading data from this register bit:** 0 - Indicates that “Transmit HDLC Buffer # 0" is the next available buffer. In this case, if the user wishes to write in the contents of a new “outbound” Data Link Message into the Transmit HDLC Message Buffer, he/she should proceed to write this message into “Transmit HDLC Buffer # 0" - Address location: 0xN600. 1 - Indicates that “Transmit HDLC Buffer # 1" is the next available buffer. In this case, if the user wishes to write in the contents of a new “outbound” Data Link Message into the Transmit HDLC Message Buffer, he/she should proceed to write this message into “Transmit HDLC Buffer # 1" - Address location: 0xN700. ***NOTE:*** *If one of these Transmit HDLC buffers contain a message which has yet to be completely read-in and processed for transmission by the Transmit HDLC controller, then this bit will automatically reflect the value corresponding to the next available buffer when it is read. Changing this bit to the in-use buffer is not permitted.*
6-0	TDLBC[6:0]	R/W	0000000	**Transmit HDLC Message - Byte Count** The exact function of these bits depends on whether the Transmit HDLC Controller is configured to transmit MOS or BOS messages to the Remote Terminal Equipment. **In BOS MODE:** These bit fields contain the number of repetitions the BOS message must be transmitted before the Transmit HDLC controller generates the Transmit End of Transfer (TxEOT) interrupt and halts transmission. If these fields are set to 00000000, then the BOS message will be transmitted for an indefinite number of times. **In MOS MODE:** These bit fields contain the length, in number of octets, of the message to be transmitted. The length of MOS message specified in these bits include header bytes such as the SAPI, TEI, Control field, however, it does not include the FCS bytes.

TABLE 18: RECEIVE DATA LINK BYTE COUNT REGISTER (RDLBCR) **HEX ADDRESS: 0XN115**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RBUFPTR	R/W	0	**Receive HDLC Buffer-Pointer** This bit Identifies which Receive HDLC buffer contains the most recently received HDLC message. 0 - Indicates that Receive HDLC Buffer # 0 contains the contents of the most recently received HDLC message. 1 - Indicates that Receive HDLC Buffer # 1 contains the contents of the most recently received HDLC message.
6-0	RDLBC[6:0]	R/W	0000000	**Receive HDLC Message - byte count** The exact function of these bits depends on whether the Receive HDLC Controller Block is configured to receive MOS or BOS messages. **In BOS Mode:** These seven bits contain the number of repetitions the BOS message must be received before the Receive HDLC controller generates the Receive End of Transfer (RxEOT) interrupt. If these bits are set to “0000000”, the message will be received indefinitely and no Receive End of Transfer (RxEOT) interrupt will be generated. **In MOS Mode:** These seven bits contain the size in bytes of the HDLC message that has been received and written into the Receive HDLC buffer. The length of MOS message shown in these bits include header bytes such as the SAPI, TEI, Control field, AND the FCS bytes.

TABLE 19: SLIP BUFFER CONTROL REGISTER (SBCR) **HEX ADDRESS: 0XN116**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-5	Reserved	-	-	**Reserved**
4	SB_FORCESF	R/W	0	**Force Signaling Freeze** This bit permits the user to freeze any signaling update in the Receive Signaling Array Register -RSAR (0xN500-0xN51F) until this bit is cleared. 0 = Signaling in RSAR is updated immediately. 1 = Signaling in RSAR is not updated until this bit is set to ‘0’.
3	SB_SFENB	R/W	0	**Signal Freeze Enable Upon Buffer Slips** This bit enables signaling freeze for one multiframe after the receive buffer slips. If signaling freeze is enabled, then the “Receive Channel” will freeze all signaling updates in RSAR (0xN500-0xN51F) for at least “one-multiframe” period, after a “slip-event” has been detected within the “Receive Slip Buffer”. 0 = Disables signaling freeze for one multi-frame after receive buffer slips. 1 = Enables signaling freeze for one multi-frame after receive buffer slips.
2-0	Reserved	-	-	**Reserved**

TABLE 20: INTERRUPT CONTROL REGISTER (ICR) **HEX ADDRESS: 0XN11A**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-3	Reserved	-	-	**Reserved**
2	INT_WC_RUR	R/W	0	**Interrupt Write-to-Clear or Reset-upon-Read Select** This bit configures all Interrupt Status bits to be either Reset Upon Read or Write-to-Clear 0 = Configures all Interrupt Status bits to be Reset Upon Read (RUR). 1= Configures all Interrupt Status bits to be Write-to-Clear (WC).
1	ENBCLR	R/W	0	**Interrupt Enable Auto Clear** This bit configures all interrupt enable bits to clear or not clear after reading the interrupt status bit. 0= Configures all Interrupt Enable bits to not cleared after reading the interrupt status bit. The corresponding Interrupt Enable bit will stay 'high' after reading the interrupt status bit. 1= Configures all interrupt Enable bits to clear after reading the interrupt status bit. The corresponding interrupt enable bit will be set to 'low' after reading the interrupt status bit.
0	INTRUP_ENB	R/W	0	**Interrupt Enable for Framer_n** This bit enables the entire T1 Framer Block for Interrupt Generation. 0 = Disables the T1 framer block for Interrupt Generation 1 = Enables the T1 framer block for Interrupt Generation

TABLE 21: CUSTOMER INSTALLATION ALARM GENERATION REGISTER (CIAGR) **HEX ADDRESS: 0XN11C**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	EXT_AIS	R/W	0	**DS-1 Insertion Upon SONET/SDH and VT Mapper Validation** This bit is used to prevent AIS insertion unless an alarm is detected in the SONET/SDH or VT Mapper Blocks. 0 = Disabled 1 = Enabled
6	RAI_STAT	R/W	0	**RAI Interrupt Status Enable** This bit is used to enable the RAI interrupt status. 0 = Disabled 1 = Enable RAI Interrupt Status
5	RAI_RBS	R/W	0	**RAI Insertion Without Over Writing Robbed Bit Signaling** This bit is used to prevent the robbed bit signaling bits (if enabled) from being over written by RAI. 0 = RAI Over Writes RBS 1 = RAI does NOT Over Write RBS
4	SAI Enable	R/W	0	**E1 Mode Only**

TABLE 21: CUSTOMER INSTALLATION ALARM GENERATION REGISTER (CIAGR) **HEX ADDRESS: 0XN11C**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
[3:2]	CIAG	R/W	00	**CI Alarm Transmit (Only in ESF)** These two bits are used to enable or disable AIS-CI or RAI-CI generation in T1 ESF mode only. Alarm Indication Signal-Customer Installation (AIS-CI) and Remote Alarm Indication-Customer Installation (RAI-CI) are intended for use in a network to differentiate between an issue within the network or the Customer Installation (CI). **AIS-CI** AIS-CI is an all ones signal with an embedded signature of 01111100 11111111 (right-to left) which recurs at 386 bit intervals in-the DS-1 signal. **RAI-CI** Remote Alarm Indication - Customer Installation (RAI-CI) is a repetitive pattern with a period of 1.08 seconds. It comprises 0.99 seconds of RAI message (00000000 11111111 Right-to-left) and a 90 ms of RAI-CI signature (00111110 11111111 Right to left) to form a RAI-CI signal. RAI-CI applies to T1 ESF framing mode only. 00/11 = Disables RAI-CI or AIS-CI alarms generation 01 = Enables unframed AIS-CI alarm generation 10 = Enables RAI-CI alarm generation
[1:0]	CIAD	R/W	00	**CI Alarm Detect (Only in ESF)** These two bits are used to enable or disable RAI-CI or AIS-CI alarm detection in T1 ESF mode only. 00/11 = Disables the RAI-CI or AIS-CI alarm detection 01 = Enables the unframed AIS-CI alarm detection 10 = Enables the RAI-CI alarm detection

TABLE 22: PERFORMANCE REPORT CONTROL REGISTER (PRCR) **HEX ADDRESS: 0XN11D**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-3	Reserved	-	-	**Reserved.**

TABLE 22: PERFORMANCE REPORT CONTROL REGISTER (PRCR) **HEX ADDRESS: 0XN11D**

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>2</td><td>C/R_BIt</td><td>R/W</td><td>0</td><td>C/R Bit Control
This bit allows user to control the value of C/R bit within an outgoing performance report.
0 - Outgoing C/R bit will be set to’0’
1 - Outgoing C/R bit will be set to’1’</td></tr>
<tr><td>[1:0]</td><td>APCR</td><td>R/W</td><td>00</td><td>Automatic Performance Control/Response Report
These bits automatically generates a summary report of the PMON status so that it can be inserted into an out going LAPD message. Automatic performance report can be generated every time these bits transition from ‘b00’ to ‘b01‘or automatically every one second. The table below describes the different APCR[1:0] bits settings.
<table>
<tr><th>APCR[1:0]</th><th>SOURCE FOR RECEIVE D/E TIMESLOTS</th></tr>
<tr><td>00/11</td><td>No performance report issued</td></tr>
<tr><td>01</td><td>Single performance report is issued when these bits transitions from ‘b00’ to b’01’.</td></tr>
<tr><td>10</td><td>Automatically issues a performance report every one second</td></tr>
</table>
</td></tr>
</table>

TABLE 23: PRBS CONTROL AND STATUS REGISTER 0 (PRBSCSR0) **HEX ADDRESS: 0XN121**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-4	Reserved	R/W	0	**Reserved**
3	BERT_Switch	R/W	0	**BERT Switch** This bit enables or disables the BERT switch function within the XRT86SH328 device. By enabling the BERT switch function, BERT functionality will be switched between the receive and transmit framer. T1 Receive framer will generate the BERT pattern and insert it onto the receive interface, and T1 Transmit Framer will be monitoring the transmit interface for BERT pattern and declare BERT LOCK if it has locked onto the input pattern. If BERT switch is disabled, T1 Transmit framer will generate the BERT pattern and the receive framer will be monitoring the BERT pattern and declare BERT LOCK if it has locked onto the input pattern. 0 = Disables the BERT Switch Feature. 1 = Enables the BERT Switch Feature.
2	BER[1]	R/W	0	**Bit Error Rate** This bit is used to insert PRBS bit error at the rates presented at the table below. The exact function of this bit depends on whether PRBS switch function is enabled or not. (bit 3 within this register). If the PRBS switch function is disabled, bit error will be inserted by the T1 transmit framer out to the line interface if this bit is enabled. If the PRBS switch function is enabled, bit error will be inserted by the T1 receive framer out to the receive backplane interface if this bit is enabled.
1	BER[0]	R/W	0	

BER[1:0]	BIT ERROR RATE
00	Disable Bit Error insertion to the transmit output or receive backplane interface
01	Bit Error is inserted to the transmit output or receive backplane interface at a rate of 1/1000 (one out of one Thousand)
10	Bit Error is inserted to the transmit output or receive backplane interface at a rate of 1/ 1,000,000 (one out of one million)
11	Disable Bit Error insertion to the transmit output or receive backplane interface

TABLE 23: PRBS CONTROL AND STATUS REGISTER 0 (PRBSCSR0) **HEX ADDRESS: 0XN121**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
0	UnFramedPRBS	R/W	0	**Unframed PRBS Pattern** This bit enables or disables unframed PRBS/QRTS pattern generation (i.e. All timeslots and framing bits are all PRBS/QRTS data). The exact function of this bit depends on whether PRBS switch function is enabled or not. (bit 3 within this register). If PRBS switch function is disabled, T1 Transmit Framer will generate an unframed PRBS 15 or QRTS pattern to the line side if this bit is enabled. If PRBS switch function is enabled, T1 Receive Framer will generate an unframed PRBS 15 or QRTS pattern to the receive backplane interface if this bit is enabled. 0 - Enables an unframed PRBS/QRTS pattern generation to the line interface or to the receive backplane interface 1 - Disables an unframed PRBS/QRTS pattern generation to the line interface or to the receive backplane interface

TABLE 24: PRBS CONTROL AND STATUS REGISTER 1 (PRBSCSR1) **HEX ADDRESS: 0XN123**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	PRBSTyp	R/W	0	**PRBS Pattern Type** This bit selects the type of PRBS pattern that the T1 Transmit/ Receive framer will generate or detect. 0 = PRBS $X^{15} + X^{14} +1$ Polynomial generation. 1 = PRBS $X^{23} + X^{18} +1$ Polynomial generation.
6	ERRORIns	R/W	0	**Error Insertion** This bit is used to insert a single error onto the generated BERT pattern selected within this device. A '0' to '1' transition will cause one output bit inverted in the BERT stream. This bit only works if BERT generation is enabled.
5	DATAInv	R/W	0	**BERT Data Invert:** This bit inverts the BERT output data and the Receive BERT input data. 0 - Transmit and Receive Framer will not invert the Transmit BERT and Receive BERT data. 1 - Transmit and Receive Framer will invert the Transmit BERT and Receive BERT data.
4	RxBERTLock	RO	0	**Lock Status** This READ ONLY bit field indicates whether or not the BERT monitor LOCK has occured. 0 = Indicates the Receive BERT has not Locked onto the input patterns. 1 = Indicates the Receive BERT has locked onto the input patterns.

TABLE 24: PRBS CONTROL AND STATUS REGISTER 1 (PRBSCSR1) **HEX ADDRESS: 0XN123**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
3	RxBERTEnb	R/W	0	**Receive BERT Detection/Generation Enable** This bit enables or disables the receive BERT pattern detection or generation. The exact function of this bit depends on whether BERT switch function is enabled or not. (bit 3 in register 0xN121). 0 = Disables the Receive BERT pattern Detection/Generation. 1 - Enables the Receive BERT pattern Detection/Generation.
2	TxPRBSEnb	R/W	0	**Transmit BERT Detection/Generation Enable** This bit enables or disables the Transmit BERT pattern detection or generation. The exact function of this bit depends on whether PRBS switch function is enabled or not. (bit 3 in register 0xN121). 0 = Disables the Transmit BERT pattern Detection/Generation. 1 - Enables the Transmit BERT pattern Detection/Generation.
1	RxBypass	R/W	0	**Receive Framer Bypass** This bit enables or disables the Receive T1 Framer bypass. 0 = Disables the Receive T1 framer Bypass. 1 - Enables the Receive T1 Framer Bypass
0	TxBypass	R/W	0	**Transmit Framer Bypass** This bit enables or disables the Transmit T1 Framer bypass. 0 = Disables the Transmit T1 framer Bypass. 1 - Enables the Transmit T1 Framer Bypass

TABLE 25: LOOPBACK CODE CONTROL REGISTER - CODE 0 (LCCR0) **HEX ADDRESS: 0XN124**

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>7-6</td><td>RXLBCALEN[1:0]</td><td>R/W</td><td>00</td><td>Receive Loopback Code Activation Length
This bit determines the receive loopback code activation length. There are four lengths supported by the XRT86SH328 as presented in the table below:

<table>
<tr><th>RXLBCALEN[1:0]</th><th>RECEIVE LOOPBACK CODE ACTIVATION LENGTH</th></tr>
<tr><td>00</td><td>Selects 4-bit receive loopback code activation Sequence</td></tr>
<tr><td>01</td><td>Selects 5-bit receive loopback code activation Sequence</td></tr>
<tr><td>10</td><td>Selects 6-bit receive loopback code activation Sequence</td></tr>
<tr><td>11</td><td>Selects 7-bit receive loopback code activation Sequence</td></tr>
</table>
</td></tr>
<tr><td>5-4</td><td>RXLBCDLEN[1:0]</td><td>R/W</td><td>00</td><td>Receive Loopback Code Deactivation Length
This bit determines the receive loopback code deactivation length. There are four lengths supported by the XRT86SH328 as presented in the table below

<table>
<tr><th>RXLBCDLEN[1:0]</th><th>RECEIVE LOOPBACK CODE DEACTIVATION LENGTH</th></tr>
<tr><td>00</td><td>Selects 4-bit receive loopback code deactivation Sequence</td></tr>
<tr><td>01</td><td>Selects 5-bit receive loopback code deactivation Sequence</td></tr>
<tr><td>10</td><td>Selects 6-bit receive loopback code deactivation Sequence</td></tr>
<tr><td>11</td><td>Selects 7-bit receive loopback code deactivation Sequence</td></tr>
</table>
</td></tr>
</table>

TABLE 25: LOOPBACK CODE CONTROL REGISTER - CODE 0 (LCCR0) **HEX ADDRESS: 0XN124**

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>3-2</td><td>TXLBCLEN[1:0]</td><td>R/W</td><td>00</td><td>Transmit Loopback Code Length
This bit determines transmit loopback code length. There are four lengths supported by the XRT86SH328 as presented in the table below

<table>
<tr><th>TXLBCLEN[1:0]</th><th>TRANSMIT LOOPBACK CODE ACTIVATION LENGTH</th></tr>
<tr><td>00</td><td>Selects 4-bit transmit loopback code Sequence</td></tr>
<tr><td>01</td><td>Selects 5-bit transmit loopback code Sequence</td></tr>
<tr><td>10</td><td>Selects 6-bit transmit loopback code Sequence</td></tr>
<tr><td>11</td><td>Selects 7-bit transmit loopback code Sequence</td></tr>
</table>
</td></tr>
<tr><td>1</td><td>FRAMED</td><td>R/W</td><td>0</td><td>Framed Loopback Code
This bit selects either framed or unframed loopback code generation in the transmit path.
0 = Selects an “Unframed” loopback code for transmission.
1 = Selects a “framed” loopback code for transmission.</td></tr>
<tr><td>0</td><td>AUTOENB</td><td>R/W</td><td>0</td><td>Remote Loopback Automatically
This bit configures the XRT86SH328 in remote loopback automatically upon detecting the loopback code activation code specified in the Receive Loopback Code Activation Register if Receive activation loopback code is enabled (Register address:0xN126).
The XRT86SH328 will cancel the remote loopback upon detecting the loopback code deactivation code specified in the Receive Loopback Code Deactivation register if the Receive deactivation loopback code is enabled. (Register address:0xN127)
0 = Disables automatic remote loopback upon detecting the receive activation code.
1 = Enables automatic remote loopback upon detecting the receive activation code.</td></tr>
</table>

TABLE 26: TRANSMIT LOOPBACK CODER REGISTER (TLCR) **HEX ADDRESS: 0XN125**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-1	TXLBC[6:0]	R/W	1010101	**Transmit Loopback Code** These seven bits determine the transmit loopback code. The MSB of the transmit loopback code is loaded first for transmission.
0	TXLBCENB	R/W	0	**Transmit Loopback Code Enable** This bit enables loopback code generation in the transmit path. Transmit loopback code is generated by writing the transmit loop-back code in this register and enabling it using this bit. The length and the format of the transmit loopback code is determined by the Loopback Code Control Register (Register address: 0xN124) 0 = Disables the transmit loopback code generation. 1 = Enables the transmit loopback code generation.

TABLE 27: RECEIVE LOOPBACK ACTIVATION CODE REGISTER - CODE 0 (RLACR) **HEX ADDRESS: 0XN126**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-1	RXLBAC[6:0]	R/W	1010101	**Receive activation loopback code** These seven bits determine the receive loopback activation code. The MSB of the receive activation loopback code is received first.
0	RXLBACENB	R/W	0	**Receive activation loopback code enable** This bit enables the receive loopback activation code detection. Receive loopback activation code is detected by writing the expected receive activation loopback code in this register and enabling it using this bit. The length and format of the Receive loopback activation code is determined by the Loopback Code Control Register (Register 0xN124). 0 = Disables the receive loopback code activation detection. 1 = Enables the receive loopback code activation detection.

TABLE 28: RECEIVE LOOPBACK DEACTIVATION CODE REGISTER - CODE 0 (RLDCR) **HEX ADDRESS: 0XN127**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-1	RXLBDC[6:0]	R/W	1010101	**Receive deactivation loopback code** These seven bits determine the receive loopback deactivation code. The MSB of the receive deactivation loopback code is received first.
0	RXLBDCENB	R/W	0	**Receive deactivation loopback code enable** This bit enables the receive loopback deactivation code detection. Receive loopback deactivation code is detected by writing the expected receive deactivation loopback code in this register and enabling it using this bit. The length and format of the Receive loopback deactivation code is determined by the Loopback Code Control Register (Register 0xN124). 0 = Disables the receive loopback code deactivation detection. 1 = Enables the receive loopback code deactivation detection.

TABLE 29: DEFECT DETECTION ENABLE REGISTER (DDER) **HEX ADDRESS: 0XN129**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	DEFDET	R/W	1	For defect detection per ANSI T1.231-1997 and T1.403-1999, user should leave this bit set to '1'.
6	Unused	R/O	0	Reserved
5	Transmit PDI-P (Upstream) upon LOS	R/W	0	**Transmit PDI-P (Upstream) upon LOS:** This READ/WRITE bit-field configures the Transmit SONET POH Processor block to automatically transmit the PDI-P (Path - Payload Defect Indicator) anytime the Frame Synchronizer block declares the LOS defect within the T1/E1 Ingress Path. If this configuration is implemented then the following events will occur: If the T1/E1 Frame Synchronizer block were to declare the LOS defect within the Ingress Path, then the Transmit SONET POH Processor block automatically transmits the PDI-P indicator by setting the C2 byte within the upstream STS-1 SPE to the value "0xE1-0xFC". Once the T1/E1Frame Synchronizer block clears the LOS defect, then the Transmit SONET POH Processor block automatically terminates its transmission of the PDI-P indicator by setting the C2 byte within the upstream STS-1 SPE to the value "0x02". 0 = Disables this automatic Transmit PDI-P (Upstream) upon LOS. 1 = Enable this automatic Transmit PDI-P (Upstream) upon LOS. ***NOTE:*** *C2 Auto Insert Mode on Bit-1 must be enabled on Transmit STS-1/STS-3 Path Control Register - Byte 0 on address location 0x783 to use this feature.*
4	Transmit AIS (Upstream) upon LOS	R/W	0	**Transmit AIS (Upstream) upon LOS:** This READ/WRITE bit-field configures the T1/E1 Frame Synchronizer block to automatically transmit the AIS indicator upstream, towards the Transmit SONET POH Processor block anytime that it detects and declares the LOS defect condition. 0 - Disables the "Transmit AIS (Upstream) upon LOS. 1 - Enables the "Transmit AIS (Upstream) upon LOS.

TABLE 29: DEFECT DETECTION ENABLE REGISTER (DDER) **HEX ADDRESS: 0XN129**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
3	Transmit PDI-P (Upstream) upon LOF	R/W	0	**Transmit PDI-P (Upstream) upon LOF:** This READ/WRITE bit-field configures the Transmit SONET POH Processor block to automatically transmit the PDI-P (Path - Payload Defect Indicator) anytime the Frame Synchronizer block declares the LOF defect within the T1/E1 Ingress Path. If this configuration is implemented then the following events will occur: If the T1/E1 Frame Synchronizer block were to declare the LOF defect within the Ingress Path, then the Transmit SONET POH Processor block automatically transmits the PDI-P indicator by setting the C2 byte within the upstream STS-1 SPE to the value "0xE1-0xFC". Once the T1/E1Frame Synchronizer block clears the LOF defect, then the Transmit SONET POH Processor block automatically terminates its transmission of the PDI-P indicator by setting the C2 byte within the upstream STS-1 SPE to the value "0x02". 0 = Disables this automatic Transmit PDI-P (Upstream) upon LOF. 1 = Enable this automatic Transmit PDI-P (Upstream) upon LOF. ***NOTE:*** *C2 Auto Insert Mode on Bit-1 must be enabled on Transmit STS-1/STS-3 Path Control Register - Byte 0 on address location 0x783 to use this feature.*
2	Transmit AIS-P (Upstream) upon LOF	R/W	0	**Transmit AIS (Upstream) upon LOF:** This READ/WRITE bit-field configures the T1/E1 Frame Synchronizer block to automatically transmit the AIS indicator upstream, towards the Transmit SONET POH Processor block anytime that it detects and declares the LOF defect condition. 0 - Disables the "Transmit AIS (Upstream) upon LOF. 1 - Enables the "Transmit AIS (Upstream) upon LOF.

TABLE 29: DEFECT DETECTION ENABLE REGISTER (DDER) **HEX ADDRESS: 0XN129**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	Transmit PDI-P (Upstream) upon AIS	R/W	0	**Transmit PDI-P (Upstream) upon Ingress AIS:** This READ/WRITE bit-field configures the Transmit SONET POH Processor block to automatically transmit the PDI-P (Path - Payload Defect Indicator) anytime the Frame Synchronizer block declares the AIS defect within the T1/E1 Ingress Path. If this configuration is implemented then the following events will occur: If the T1/E1 Frame Synchronizer block were to declare the AIS defect within the Ingress Path, then the Transmit SONET POH Processor block automatically transmits the PDI-P indicator by setting the C2 byte within the upstream STS-1 SPE to the value "0xE1-0xFC". Once the T1/E1Frame Synchronizer block clears the AIS defect, then the Transmit SONET POH Processor block automatically terminates its transmission of the PDI-P indicator by setting the C2 byte within the upstream STS-1 SPE to the value "0x02". 0 = Disables this automatic Transmit PDI-P (Upstream) upon AIS. 1 = Enable this automatic Transmit PDI-P (Upstream) upon AIS. ***NOTE:*** *C2 Auto Insert Mode on Bit-1 must be enabled on Transmit STS-1/STS-3 Path Control Register - Byte 0 on address location 0x783 to use this feature.*
0	Transmit AIS-P (Upstream) upon AIS	R/W	0	**Transmit AIS (Upstream) upon Ingress AIS:** This READ/WRITE bit-field configures the T1/E1 Frame Synchronizer block to automatically transmit the AIS indicator upstream, towards the Transmit SONET POH Processor block anytime that it detects and declares the AIS defect condition. 0 - Disables the "Transmit AIS (Upstream) upon AIS. 1 - Enables the "Transmit AIS (Upstream) upon AIS.

TABLE 30: LOOPBACK CODE CONTROL REGISTER - CODE 1 (LCCR1) **HEX ADDRESS: 0XN12A**

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>7-6</td><td>RXLBCALEN[1:0]</td><td>R/W</td><td>00</td><td>Receive Loopback Code Activation Length
This bit determines the receive loopback code activation length. There are four lengths supported by the XRT86SH328 as presented in the table below:

<table>
<tr><th>RXLBCALEN[1:0]</th><th>RECEIVE LOOPBACK CODE ACTIVATION LENGTH</th></tr>
<tr><td>00</td><td>Selects 4-bit receive loopback code activation Sequence</td></tr>
<tr><td>01</td><td>Selects 5-bit receive loopback code activation Sequence</td></tr>
<tr><td>10</td><td>Selects 6-bit receive loopback code activation Sequence</td></tr>
<tr><td>11</td><td>Selects 7-bit receive loopback code activation Sequence</td></tr>
</table>
</td></tr>
<tr><td>5-4</td><td>RXLBCDLEN[1:0]</td><td>R/W</td><td>00</td><td>Receive Loopback Code Deactivation Length
This bit determines the receive loopback code deactivation length. There are four lengths supported by the XRT86SH328 as presented in the table below

<table>
<tr><th>RXLBCDLEN[1:0]</th><th>RECEIVE LOOPBACK CODE DEACTIVATION LENGTH</th></tr>
<tr><td>00</td><td>Selects 4-bit receive loopback code deactivation Sequence</td></tr>
<tr><td>01</td><td>Selects 5-bit receive loopback code deactivation Sequence</td></tr>
<tr><td>10</td><td>Selects 6-bit receive loopback code deactivation Sequence</td></tr>
<tr><td>11</td><td>Selects 7-bit receive loopback code deactivation Sequence</td></tr>
</table>
</td></tr>
</table>

TABLE 30: LOOPBACK CODE CONTROL REGISTER - CODE 1 (LCCR1) **HEX ADDRESS: 0XN12A**

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>3-2</td><td>TXLBCLEN[1:0]</td><td>R/W</td><td>00</td><td>Transmit Loopback Code Length
This bit determines transmit loopback code length. There are four lengths supported by the XRT86SH328 as presented in the table below

<table>
<tr><th>TXLBCLEN[1:0]</th><th>TRANSMIT LOOPBACK CODE ACTIVATION LENGTH</th></tr>
<tr><td>00</td><td>Selects 4-bit transmit loopback code Sequence</td></tr>
<tr><td>01</td><td>Selects 5-bit transmit loopback code Sequence</td></tr>
<tr><td>10</td><td>Selects 6-bit transmit loopback code Sequence</td></tr>
<tr><td>11</td><td>Selects 7-bit transmit loopback code Sequence</td></tr>
</table>
</td></tr>
<tr><td>1</td><td>FRAMED</td><td>R/W</td><td>0</td><td>Framed Loopback Code
This bit selects either framed or unframed loopback code generation in the transmit path.
0 = Selects an “Unframed” loopback code for transmission.
1 = Selects a “framed” loopback code for transmission.</td></tr>
<tr><td>0</td><td>AUTOENB</td><td>R/W</td><td>0</td><td>Remote Loopback Automatically
This bit configures the XRT86SH328 in remote loopback automatically upon detecting the loopback code activation code specified in the Receive Loopback Code Activation Register if Receive activation loopback code is enabled (Register address:0xN126).
The XRT86SH328 will cancel the remote loopback upon detecting the loopback code deactivation code specified in the Receive Loopback Code Deactivation register if the Receive deactivation loopback code is enabled. (Register address:0xN127)
0 = Disables automatic remote loopback upon detecting the receive activation code.
1 = Enables automatic remote loopback upon detecting the receive activation code.</td></tr>
</table>

TABLE 31: RECEIVE LOOPBACK ACTIVATION CODE REGISTER - CODE 1 (RLACR1) HEX ADDRESS: 0XN12B

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-1	RXLBAC[6:0]	R/W	1010101	**Receive activation loopback code** These seven bits determine the receive loopback activation code. The MSB of the receive activation loopback code is received first.
0	RXLBACENB	R/W	0	**Receive activation loopback code enable** This bit enables the receive loopback activation code detection. Receive loopback activation code is detected by writing the expected receive activation loopback code in this register and enabling it using this bit. The length and format of the Receive loopback activation code is determined by the Loopback Code Control Register (Register 0xN124). 0 = Disables the receive loopback code activation detection. 1 = Enables the receive loopback code activation detection.

TABLE 32: RECEIVE LOOPBACK DEACTIVATION CODE REGISTER - CODE 1 (RLDCR1) HEX ADDRESS: 0XN12C

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-1	RXLBDC[6:0]	R/W	1010101	**Receive deactivation loopback code** These seven bits determine the receive loopback deactivation code. The MSB of the receive deactivation loopback code is received first.
0	RXLBDCENB	R/W	0	**Receive deactivation loopback code enable** This bit enables the receive loopback deactivation code detection. Receive loopback deactivation code is detected by writing the expected receive deactivation loopback code in this register and enabling it using this bit. The length and format of the Receive loopback deactivation code is determined by the Loopback Code Control Register (Register 0xN124). 0 = Disables the receive loopback code deactivation detection. 1 = Enables the receive loopback code deactivation detection.

TABLE 33: LOOPBACK CODE CONTROL REGISTER - CODE 2 (LCCR2) **HEX ADDRESS: 0XN12D**

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>7-6</td><td>RXLBCALEN[1:0]</td><td>R/W</td><td>00</td><td>Receive Loopback Code Activation Length
This bit determines the receive loopback code activation length. There are four lengths supported by the XRT86SH328 as presented in the table below:

<table>
<tr><th>RXLBCALEN[1:0]</th><th>RECEIVE LOOPBACK CODE ACTIVATION LENGTH</th></tr>
<tr><td>00</td><td>Selects 4-bit receive loopback code activation Sequence</td></tr>
<tr><td>01</td><td>Selects 5-bit receive loopback code activation Sequence</td></tr>
<tr><td>10</td><td>Selects 6-bit receive loopback code activation Sequence</td></tr>
<tr><td>11</td><td>Selects 7-bit receive loopback code activation Sequence</td></tr>
</table>
</td></tr>
<tr><td>5-4</td><td>RXLBCDLEN[1:0]</td><td>R/W</td><td>00</td><td>Receive Loopback Code Deactivation Length
This bit determines the receive loopback code deactivation length. There are four lengths supported by the XRT86SH328 as presented in the table below

<table>
<tr><th>RXLBCDLEN[1:0]</th><th>RECEIVE LOOPBACK CODE DEACTIVATION LENGTH</th></tr>
<tr><td>00</td><td>Selects 4-bit receive loopback code deactivation Sequence</td></tr>
<tr><td>01</td><td>Selects 5-bit receive loopback code deactivation Sequence</td></tr>
<tr><td>10</td><td>Selects 6-bit receive loopback code deactivation Sequence</td></tr>
<tr><td>11</td><td>Selects 7-bit receive loopback code deactivation Sequence</td></tr>
</table>
</td></tr>
</table>

TABLE 33: LOOPBACK CODE CONTROL REGISTER - CODE 2 (LCCR2) **HEX ADDRESS: 0XN12D**

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>3-2</td><td>TXLBCLEN[1:0]</td><td>R/W</td><td>00</td><td>Transmit Loopback Code Length
This bit determines transmit loopback code length. There are four lengths supported by the XRT86SH328 as presented in the table below
<table>
<tr><th>TXLBCLEN[1:0]</th><th>TRANSMIT LOOPBACK CODE ACTIVATION LENGTH</th></tr>
<tr><td>00</td><td>Selects 4-bit transmit loopback code Sequence</td></tr>
<tr><td>01</td><td>Selects 5-bit transmit loopback code Sequence</td></tr>
<tr><td>10</td><td>Selects 6-bit transmit loopback code Sequence</td></tr>
<tr><td>11</td><td>Selects 7-bit transmit loopback code Sequence</td></tr>
</table></td></tr>
<tr><td>1</td><td>FRAMED</td><td>R/W</td><td>0</td><td>Framed Loopback Code
This bit selects either framed or unframed loopback code generation in the transmit path.
0 = Selects an “Unframed” loopback code for transmission.
1 = Selects a “framed” loopback code for transmission.</td></tr>
<tr><td>0</td><td>AUTOENB</td><td>R/W</td><td>0</td><td>Remote Loopback Automatically
This bit configures the XRT86SH328 in remote loopback automatically upon detecting the loopback code activation code specified in the Receive Loopback Code Activation Register if Receive activation loopback code is enabled (Register address:0xN126).
The XRT86SH328 will cancel the remote loopback upon detecting the loopback code deactivation code specified in the Receive Loopback Code Deactivation register if the Receive deactivation loopback code is enabled. (Register address:0xN127)
0 = Disables automatic remote loopback upon detecting the receive activation code.
1 = Enables automatic remote loopback upon detecting the receive activation code.</td></tr>
</table>

TABLE 34: RECEIVE LOOPBACK ACTIVATION CODE REGISTER - CODE 2 (RLACR2) HEX ADDRESS: 0XN12E

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-1	RXLBAC[6:0]	R/W	1010101	**Receive activation loopback code** These seven bits determine the receive loopback activation code. The MSB of the receive activation loopback code is received first.
0	RXLBACENB	R/W	0	**Receive activation loopback code enable** This bit enables the receive loopback activation code detection. Receive loopback activation code is detected by writing the expected receive activation loopback code in this register and enabling it using this bit. The length and format of the Receive loopback activation code is determined by the Loopback Code Control Register (Register 0xN124). 0 = Disables the receive loopback code activation detection. 1 = Enables the receive loopback code activation detection.

TABLE 35: RECEIVE LOOPBACK DEACTIVATION CODE REGISTER - CODE 2 (RLDCR2) HEX ADDRESS: 0XN12F

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-1	RXLBDC[6:0]	R/W	1010101	**Receive deactivation loopback code** These seven bits determine the receive loopback deactivation code. The MSB of the receive deactivation loopback code is received first.
0	RXLBDCENB	R/W	0	**Receive deactivation loopback code enable** This bit enables the receive loopback deactivation code detection. Receive loopback deactivation code is detected by writing the expected receive deactivation loopback code in this register and enabling it using this bit. The length and format of the Receive loopback deactivation code is determined by the Loopback Code Control Register (Register 0xN124). 0 = Disables the receive loopback code deactivation detection. 1 = Enables the receive loopback code deactivation detection.

TABLE 36: TRANSMIT SPRM CONTROL REGISTER (TSPRMCR) **HEX ADDRESS: 0XN142**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	FC_Bit	R/W	0	**NPRM FC Bit** This bit is used to set the value of the FC bit field within the NPRM report.
6	PA_Bit	R/W	0	**NPRM PA Bit** This bit is used to set the value of the PA bit field within the NPRM report.
5	U1_BIT	R/W	0	**SPRM U1 Bit** This bit provides the contents of the U1 bit within the SPRM report.
4	U2_BIT	R/W	0	**SPRM U2 Bit** This bit provides the contents of the U2 bit within the SPRM report.
3-0	R_BIT	R/W	0000	**SPRM R Bit** This bit provides the contents of the R bit within the SPRM report.

TABLE 37: BERT CONTROL REGISTER (BCR) **HEX ADDRESS: 0XN163**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-4	Reserved	R/W	0	**Reserved**
3-0	BERT[3:0]	R/W	0000	**BERT Pattern Select** 0000 =PRBS X20 + X3 + 1 0011 = QRSS X20 + X17 + 1 0100 = All Ones 0101 = All Zeros 0110 = Reserved 0111 = 1 in 8 (Framed Only) 1000 = Reserved 1001 = Reserved Others = Invalid

BERT Pattern Definition

1 in 8 Framed

0000 0010 ...

TABLE 38: TRANSMIT CHANNEL CONTROL REGISTER 0-31 (TCCR 0-31) **HEX ADDRESS: 0XN300 TO 0XN31F**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-6	Reserved	-	-	Reserved (For T1 mode only)
5-4	TxZERO[1:0]	R/W	00	**Selects Type of Zero Suppression** 00 = No zero code suppression is used. 01 = AT&T bit 7 stuffing is used. 10 = GTE zero code suppression is used. If GTE zero code suppression is used, bit 8 is stuffed in non-signaling frame. Otherwise, bit 7 is stuffed in signaling frame if signaling bit is zero. 11 = DDS zero code suppression is used. The value 0x98 replaces the input data.

TABLE 38: TRANSMIT CHANNEL CONTROL REGISTER 0-31 (TCCR 0-31) **HEX ADDRESS: 0XN300 TO 0XN31F**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
3-0	TxCond(3:0)	R/W	0000	**Transmit Channel Conditioning for Timeslot 0 to 31** These bits allow the user to substitute the input PCM data (Octets 0-31) with internally generated Conditioning Codes prior to transmission to the remote terminal equipment on a per-channel basis. The table below presents the different conditioning codes based on the setting of these bits. ***NOTE:*** *Register address 0xN300 represents time slot 0, and address 0xN31F represents time slot 31.*

TXCOND[1:0]	CONDITIONING CODES
0x0 / 0xE	Contents of timeslot octet are unchanged.
0x1	All 8 bits of the selected timeslot octet are inverted (1's complement) OUTPUT = (TIME_SLOT_OCTET) XOR 0xFF
0x2	Even bits of the selected timeslot octet are inverted OUTPUT = (TIME_SLOT_OCTET) XOR 0xAA
0x3	Odd bits of the selected time slot octet are inverted OUTPUT = (TIME_SLOT_OCTET) XOR 0x55
0x4	Contents of the selected timeslot octet will be substituted with the 8 -bit value in the Transmit Programmable User Code Register (0xN320-0xN337),
0x5	Contents of the timeslot octet will be substituted with the value 0x7F (BUSY Code)
0x6	Contents of the timeslot octet will be substituted with the value 0xFF (VACANT Code)
0x7	Contents of the timeslot octet will be substituted with the BUSY time slot code (111#_####), where ##### is the Timeslot number
0x8	Contents of the timeslot octet will be substituted with the MOOF code (0x1A)
0x9	Contents of the timeslot octet will be substituted with the A-Law Digital Milliwatt pattern
0xA	Contents of the timeslot octet will be substituted with the μ-Law Digital Milliwatt pattern
0xB	The MSB (bit 1) of input data is inverted
0xC	All input data except MSB is inverted
0xD	Contents of the timeslot octet will be substituted with the BERT pattern (if enabled).
0xF	D/E time slot - The TxSIGDL[2:0] bits in the Transmit Signaling and Data Link Select Register (0xN10A) will determine the data source for D/E time slots.

TABLE 39: TRANSMIT USER CODE REGISTER 0 - 31 (TUCR 0-31) **HEX ADDRESS: 0XN320 TO 0XN33F**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	TUCR[7:0]	R/W	b00010111	**Transmit Programmable User code.** These eight bits allow users to program any code in this register to replace the input PCM data when the Transmit Channel Control Register (TCCR) is configured to replace timeslot octet with programmable user code. (i.e. if TCCR is set to '0x4') The default value of this register is an IDLE Code (b00010111).

TABLE 40: TRANSMIT SIGNALING CONTROL REGISTER 0-23 (TSCR 0-23) HEX ADDRESS: 0XN340 TO 0XN357

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	A (x)	R/W	See Note	**Transmit Signaling bit A** This bit allows user to provide signaling Bit A (Octets 0-23) if Robbed-bit signaling is enabled (Rob_Enb bit of this register set to 1) and if signalling data is inserted from TSCR (TxSIGSRC[1:0] = 01 in this register). ***NOTE:*** *Register 0xN340 represents signaling data for Time Slot 0, and 0xN357 represents signaling data for Time Slot 23.*
6	B (y)	R/W	See Note	**Transmit Signaling bit B** This bit allows user to provide signaling Bit B (Octets 0-23) if Robbed-bit signaling is enabled (Rob_Enb bit of this register set to 1) and if signalling data is inserted from TSCR (TxSIGSRC[1:0] = 01 in this register). ***NOTE:*** *Register 0xN340 represents signaling data for Time Slot 0, and 0xN357 represents signaling data for Time Slot 23.*
5	C (x)	R/W	See Note	**Transmit Signaling bit C** This bit allows user to provide signaling Bit C (Octets 0-23) if Robbed-bit signaling is enabled (Rob_Enb bit of this register set to 1) and if signalling data is inserted from TSCR (TxSIGSRC[1:0] = 01 in this register). ***NOTE:*** *Register 0xN340 represents signaling data for Time Slot 0, and 0xN357 represents signaling data for Time Slot 23.*
4	D (x)	R/W	See Note	**Transmit Signaling bit D** This bit allows user to provide signaling Bit D (Octets 0-23) if Robbed-bit signaling is enabled (Rob_Enb bit of this register set to 1) and if signalling data is inserted from TSCR (TxSIGSRC[1:0] = 01 in this register). ***NOTE:*** *Register 0xN340 represents signaling data for Time Slot 0, and 0xN357 represents signaling data for Time Slot 23.*
3	Reserved	-	See Note	**Reserved**
2	Rob_Enb	R/W	See Note	**Robbed-bit signaling enable** This bit enables or disables Robbed-bit signaling transmission. If robbed-bit signaling is enabled, signaling data is conveyed in the 8th position of each signaling channel by replacing the original LSB of the voice channel with signaling data. 0 = Disables Robbed-bit signaling. 1 = Enables Robbed-bit signaling.

TABLE 40: TRANSMIT SIGNALING CONTROL REGISTER 0-23 (TSCR 0-23) HEX ADDRESS: 0XN340 TO 0XN357

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	TxSIGSRC[1]	R/W	See Note	**Channel signaling control** These bits determine the source for signaling information, see table below.
0	TxSIGSRC[0]	R/W	See Note	

TXSIGSRC[1:0]	SIGNALING SOURCE SELECTED
00/11	Signaling data is inserted from input PCM data
01	Signaling data is inserted from this register (TSCRs).
10	Reserved

NOTE: *The default value for register address 0xN340 = 0x01, 0xN341-0xN34F = 0xD0, 0xN350 = 0xB3, 0xN351-0xN35F = 0xD0*

TABLE 41: RECEIVE CHANNEL CONTROL REGISTER X (RCCR 0-31) **HEX ADDRESS: 0XN360 TO 0XN37F**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-6	Reserved	-	-	**Reserved**
5-4	RxZERO[1:0]	R/W	00	**Selects Type of Zero Suppression** 00 = No zero code suppression is used. 01 = AT&T bit 7 stuffing is used. 10 = GTE zero code suppression is used. If GTE zero code suppression is used, bit 8 is stuffed in non-signaling frame. Otherwise, bit 7 is stuffed in signaling frame if signaling bit is zero. 11 = DDS zero code suppression is used. The value 0x98 replaces the input data.

TABLE 41: RECEIVE CHANNEL CONTROL REGISTER X (RCCR 0-31) **HEX ADDRESS: 0XN360 TO 0XN37F**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
3-0	RxCOND[3:0]	R/W	0000	**Receive Channel Conditioning for Timeslot 0 to 31** These bits allow the user to substitute the input line data (Octets 0-31) with internally generated Conditioning Codes prior to transmission to the back-plane interface on a per-channel basis. The table below presents the different conditioning codes based on the setting of these bits. ***NOTE:*** *Register address 0xN300 represents time slot 0, and address 0xN31F represents time slot 31.*

RXCOND[1:0]	CONDITIONING CODES
0x0 / 0xE	Contents of timeslot octet are unchanged.
0x1	All 8 bits of the selected timeslot octet are inverted (1's complement) OUTPUT = (TIME_SLOT_OCTET) XOR 0xFF
0x2	Even bits of the selected timeslot octet are inverted OUTPUT = (TIME_SLOT_OCTET) XOR 0xAA
0x3	Odd bits of the selected time slot octet are inverted OUTPUT = (TIME_SLOT_OCTET) XOR 0x55
0x4	Contents of the selected timeslot octet will be substituted with the 8 -bit value in the Receive Programmable User Code Register (0xN380-0xN397),
0x5	Contents of the timeslot octet will be substituted with the value 0x7F (BUSY Code)
0x6	Contents of the timeslot octet will be substituted with the value 0xFF (VACANT Code)
0x7	Contents of the timeslot octet will be substituted with the BUSY time slot code (111#_####), where ##### is the Timeslot number
0x8	Contents of the timeslot octet will be substituted with the MOOF code (0x1A)
0x9	Contents of the timeslot octet will be substituted with the A-Law Digital Milliwatt pattern
0xA	Contents of the timeslot octet will be substituted with the μ-Law Digital Milliwatt pattern
0xB	The MSB (bit 1) of input data is inverted
0xC	All input data except MSB is inverted
0xD	Contents of the timeslot octet will be substituted with the BERT pattern (if enabled).
0xF	D/E time slot - The RxSIGDL[2:0] bits in the Transmit Signaling and Data Link Select Register (0xN10C) will determine the data source for Receive D/E time slots.

TABLE 42: RECEIVE USER CODE REGISTER 0-31 (RUCR 0-31) **HEX ADDRESS: 0XN380 TO 0XN39F**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	RxUSER[7:0]	R/W	11111111	**Receive Programmable User code.** These eight bits allow users to program any code in this register to replace the received data when the Receive Channel Control Register (RCCR) is configured to replace timeslot octet with the receive programmable user code. (i.e. if RCCR is set to '0x4')

TABLE 43: RECEIVE SIGNALING CONTROL REGISTER 0-31 (RSCR 0-31) HEX ADDRESS: 0XN3A0 TO 0XN3BF

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved	R/W	0	**Reserved**
6	SIGC_ENB	R/W	0	**Signaling substitution enable** This bit enables or disables signaling substitution on the receive side on a per channel basis. Once signaling substitution is enabled, received signaling bits ABCD will be substituted with the ABCD values in the Receive Substitution Signaling Register (RSSR). Signaling substitution only occurs in the output PCM data. The Receive Signaling Array Register (RSAR - Address 0xN500-0xN51F) will not be affected. 0 = Disables signaling substitution on the receive side. 1 = Enables signaling substitution on the receive side.
5	Reserved	R/W	0	**Reserved**
4	DEB_ENB	R/W	0	**Per-channel debounce enable** This bit enables or disables the signaling debounce feature on a per channel basis. When this feature is enabled, the per-channel signaling state must be in the same state for 2 superframes before the Receive Framer updates signaling information on the Receive Signaling Array Register (RSAR). If the signaling bits for two consecutive superframes are not the same, the current state of RSAR will not change. When this feature is disabled, RSAR will be updated as soon as the receive signaling bits have changed. 0 = Disables the Signaling Debounce feature. 1 = Enables the Signaling Debounce feature.
3	RxSIGC[1]	R/W	0	**Signaling conditioning** These bits allow user to select the format of signaling substitution on a per-channel basis, as presented in the table below. **RXSIGC[1:0] — SIGNALING SUBSTITUTION SCHEMES** **00 — Substitutes all signaling bits with one.** **01 — Enables 16-code (A,B,C,D) signaling substitution.** Users must write to bits 3-0 in the Receive Signaling Substitution Register (RSSR) to provide the 16-code (A,B,C,D) signaling substitution values. **10 — Enables 4-code (A,B) signaling substitution.** Users must write to bits 4-5 in the Receive Signaling Substitution Register (RSSR) to provide the 4-code (A,B) signaling substitution values. **11 — Enables 2-code (A) signaling substitution.** Users must write to bit 6 in the Receive Signaling Substitution Register (RSSR) to provide the 2-code (A) signaling substitution values.
2	RxSIGC[0]	R/W	0	

TABLE 43: RECEIVE SIGNALING CONTROL REGISTER 0-31 (RSCR 0-31) HEX ADDRESS: 0XN3A0 TO 0XN3BF

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>1</td><td>RxSIGE[1]</td><td>R/W</td><td>0</td><td rowspan="2">Receive Signaling Extraction.
These bits control per-channel signaling extraction as presented in the table below. Signaling information can be extracted to the Receive Signaling Array Register (RSAR) if the Receive SIgnaling Interface is enabled. .

<table><tr><th>RXSIGE[1:0]</th><th>SIGNALING EXTRACTION SCHEMES</th></tr><tr><td>00</td><td>No signaling information is extracted.</td></tr><tr><td>01</td><td>Enables 16-code (A,B,C,D) signaling extraction.
All signaling bits A,B,C,D will be extracted.</td></tr><tr><td>10</td><td>Enables 4-code (A,B) signaling extraction
Only signaling bits A,B will be extracted.</td></tr><tr><td>11</td><td>Enables 2-code (A) signaling extraction
Only signaling bit A will be extracted.</td></tr></table></td></tr>
<tr><td>0</td><td>RxSIGE[0]</td><td>R/W</td><td>0</td></tr>
</table>

TABLE 44: RECEIVE SUBSTITUTION SIGNALING REGISTER 0-23 (RSSR 0-23) HEX ADDRESS: 0XN3C0 TO 0XN3D7

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-4	Reserved	-	-	**Reserved**
3	SIG16-A, 4-A, 2-A	R/W	0	**16-code/4-code/2-code Signaling Bit A** This bit provides the value of signaling bit A to substitute the receive signaling bit A on a per channel basis when 16-code or 4-code or 2-code signaling substitution is enabled.
2	SIG16-B, 4-B, 2-A	R/W	0	**16-code/4-code Signaling Bit B** This bit provides the value of signaling bit B to substitute the receive signaling bit B on a per channel basis when 16-code or 4-code signaling substitution is enabled.
1	SIG16-C, 4-A, 2-A	R/W	0	**16-code Signaling Bit C** This bit provides the value of signaling bit C to substitute the receive signaling bit C on a per channel basis when 16-code signaling substitution is enabled.
0	SIG16-D, 4-B, 2-A	R/W	0	**16-code Signaling Bit D** This bit provides the value of signaling bit D to substitute the receive signaling bit D on a per channel basis when 16-code signaling substitution is enabled.

TABLE 45: RECEIVE SIGNALING ARRAY REGISTER 0 TO 23 (RSAR 0-23) **HEX ADDRESS: 0XN500 TO 0XN517**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-4	Reserved	-	-	**Reserved**
3	A	RO	0	These READ ONLY registers reflect the most recently received signaling value (A,B,C,D) associated with timeslot 0 to 23. If signaling debounce feature is enabled, the received signaling state must be the same for 2 superframes before this register is updated. If the signaling bits for two consecutive superframes are not the same, the current value of this register will not be changed. When Bit 7 within register 0xN107 is set to '1', signaling bits in this register are updated on superframe boundary If the signaling debounce feature is disabled or if Bit 7 within register 0xN107 is set to '0', this register is updated as soon as the received signaling bits have changed. ***NOTE:*** *The content of this register only has meaning when robbed-bit signaling is enabled.*
2	B	RO	0	
1	C	RO	0	
0	D	RO	0	

TABLE 46: LAPD BUFFER 0 CONTROL REGISTER (LAPDBCR0) **HEX ADDRESS: 0XN600**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	LAPD Buffer 0	R/W	0	**LAPD Buffer 0 (65-Bytes) Auto Incrementing** This register is used to transmit and receive LAPD messages within buffer 0 of the HDLC controller. Users should determine the next available buffer by reading the BUFAVAL bit (bit 7 of the Transmit Data Link Byte Count Register address 0xN114). If buffer 0 is available, writing to buffer 0 will insert the message into the outgoing LAPD frame after the LAPD message is sent and the data from the transmit buffer cannot be retrieved. After detecting the Receive end of transfer interrupt (RxEOT), users should read the RBUFPTR bit (bit 7 of the Receive Data Link Byte Count Register address 0xN115) to determine which buffer contains the received LAPD message ready to be read. If RBUFPTR bit indicates that buffer 0 is available to be read, reading buffer 0 (Register 0xN600) continuously will retrieve the entire received LAPD message. ***NOTE:*** *When writing to or reading from Buffer 0, the register is automatically incremented such that the entire 65 Byte LAPD message can be written into or read from buffer 0 (Register 0xN600) continuously.*

TABLE 47: LAPD BUFFER 1 CONTROL REGISTER (LAPDBCR1) **HEX ADDRESS: 0XN700**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	LAPD Buffer 1	R/W	0	**LAPD Buffer 1 (65-Bytes) Auto Incrementing** This register is used to transmit and receive LAPD messages within buffer 1 of the HDLC controller. Users should determine the next available buffer by reading the BUFAVAL bit (bit 7 of the Transmit Data Link Byte Count Register address 0xN114). If buffer 1 is available, writing to buffer 1 will insert the message into the outgoing LAPD frame after the LAPD message is sent and the data from the transmit buffer 1 cannot be retrieved. After detecting the Receive end of transfer interrupt (RxEOT), users should read the RBUFPTR bit (bit 7 of the Receive Data Link Byte Count Register address 0xN115) to determine which buffer contains the received LAPD message ready to be read. If RBUFPTR bit indicates that buffer 1 is available to be read, reading buffer 1 (Register 0xN700) continuously will retrieve the entire received LAPD message. ***NOTE:*** *When writing to or reading from Buffer 0, the register is automatically incremented such that the entire 65 Byte LAPD message can be written into or read from buffer 0 (Register 0xN600) continuously.*

TABLE 48: PMON RECEIVE LINE CODE VIOLATION COUNTER MSB (RLCVCU) **HEX ADDRESS: 0XN900**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RLCVC[15]	RUR	0	**Performance Monitor "Receive Line Code Violation" 16-Bit Counter - Upper Byte:** These RESET-upon-READ bits, along with that within the PMON Receive Line Code Violation Counter Register LSB combine to reflect the cumulative number of instances that Line Code Violation has been detected by the Receive T1 Framer block since the last read of this register. This register contains the Most Significant byte of this 16-bit of the Line Code Violation counter. ***NOTE:*** *For all 16-bit wide PMON registers, user must read the MSB counter first before reading the LSB counter in order to read the accurate PMON counts and to clear the PMON count.*
6	RLCVC[14]	RUR	0	
5	RLCVC[13]	RUR	0	
4	RLCVC[12]	RUR	0	
3	RLCVC[11]	RUR	0	
2	RLCVC[10]	RUR	0	
1	RLCVC[9]	RUR	0	
0	RLCVC[8]	RUR	0	

TABLE 49: PMON RECEIVE LINE CODE VIOLATION COUNTER LSB (RLCVCL) **HEX ADDRESS: 0XN901**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RLCVC[7]	RUR	0	**Performance Monitor "Receive Line Code Violation" 16-Bit Counter - Lower Byte:** These RESET-upon-READ bits, along with that within the PMON Receive Line Code Violation Counter Register MSB combine to reflect the cumulative number of instances that Line Code Violation has been detected by the Receive T1 Framer block since the last read of this register. This register contains the Least Significant byte of this 16-bit of the Line Code Violation counter. ***NOTE:*** *For all 16-bit wide PMON registers, user must read the MSB counter first before reading the LSB counter in order to read the accurate PMON counts and to clear the PMON count.*
6	RLCVC[6]	RUR	0	
5	RLCVC[5]	RUR	0	
4	RLCVC[4]	RUR	0	
3	RLCVC[3]	RUR	0	
2	RLCVC[2]	RUR	0	
1	RLCVC[1]	RUR	0	
0	RLCVC[0]	RUR	0	

TABLE 50: PMON RECEIVE FRAMING ALIGNMENT BIT ERROR COUNTER MSB (RFAECU) HEX ADDRESS: 0XN902

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RFAEC[15]	RUR	0	**Performance Monitor "Receive Framing Alignment Error 16-Bit Counter" - Upper Byte:** These RESET-upon-READ bits, along with that within the "PMON Receive Framing Alignment Error Counter Register LSB" combine to reflect the cumulative number of instances that the Receive Framing Alignment errors has been detected by the Receive T1 Framer block since the last read of this register. This register contains the Most Significant byte of this 16-bit of the Receive Framing Alignment Error counter. ***NOTE:*** *For all 16-bit wide PMON registers, user must read the MSB counter first before reading the LSB counter in order to read the accurate PMON counts. To clear PMON count, user must read the MSB counter first before reading the LSB counter in order to clear the PMON count.*
6	RFAEC[14]	RUR	0	
5	RFAEC[13]	RUR	0	
4	RFAEC[12]	RUR	0	
3	RFAEC[11]	RUR	0	
2	RFAEC[10]	RUR	0	
1	RFAEC[9]	RUR	0	
0	RFAEC[8]	RUR	0	

TABLE 51: PMON RECEIVE FRAMING ALIGNMENT BIT ERROR COUNTER LSB (RFAECL) HEX ADDRESS: 0XN903

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RFAEC[7]	RUR	0	**Performance Monitor "Receive Framing Alignment Error 16-Bit Counter" - Lower Byte:** These RESET-upon-READ bits, along with that within the "PMON Receive Framing Alignment Error Counter Register MSB" combine to reflect the cumulative number of instances that the Receive Framing Alignment errors has been detected by the Receive T1 Framer block since the last read of this register. This register contains the Least Significant byte of this 16-bit of the Receive Framing Alignment Error counter. ***NOTE:*** *For all 16-bit wide PMON registers, user must read the MSB counter first before reading the LSB counter in order to read the accurate PMON counts. To clear PMON count, user must read the MSB counter first before reading the LSB counter in order to clear the PMON count.*
6	RFAEC[6]	RUR	0	
5	RFAEC[5]	RUR	0	
4	RFAEC[4]	RUR	0	
3	RFAEC[3]	RUR	0	
2	RFAEC[2]	RUR	0	
1	RFAEC[1]	RUR	0	
0	RFAEC[0]	RUR	0	

TABLE 52: PMON RECEIVE SEVERELY ERRORED FRAME COUNTER (RSEFC) **HEX ADDRESS: 0XN904**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RSEFC[7]	RUR	0	**Performance Monitor - Receive Severely Errored frame Counter (8-bit Counter)** These Reset-Upon-Read bit fields reflect the cumulative number of instances that Receive Severely Errored Frames have been detected by the T1 Framer since the last read of this register. Severely Errored Frame is defined as the occurrence of two consecutive errored frame alignment signals without causing loss of frame condition.
6	RSEFC[6]	RUR	0	
5	RSEFC[5]	RUR	0	
4	RSEFC[4]	RUR	0	
3	RSEFC[3]	RUR	0	
2	RSEFC[2]	RUR	0	
1	RSEFC[1]	RUR	0	
0	RSEFC[0]	RUR	0	

TABLE 53: PMON RECEIVE CRC-4 BIT ERROR COUNTER - MSB (RSBBECU) **HEX ADDRESS: 0XN905**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RSBBEC[15]	RUR	0	**Performance Monitor "Receive Synchronization Bit Error 16-Bit Counter" - Upper Byte:** These RESET-upon-READ bits, along with that within the "PMON Receive Synchronization Bit Error Counter Register LSB" combine to reflect the cumulative number of instances that the Receive Synchronization Bit errors has been detected by the Receive T1 Framer block since the last read of this register. This register contains the Most Significant byte of this 16-bit of the Receive Synchronization Bit Error counter. ***NOTE:*** *For all 16-bit wide PMON registers, user must read the MSB counter first before reading the LSB counter in order to read the accurate PMON counts. To clear PMON count, user must read the MSB counter first before reading the LSB counter in order to clear the PMON count.*
6	RSBBEC[14]	RUR	0	
5	RSBBEC[13]	RUR	0	
4	RSBBEC[12]	RUR	0	
3	RSBBEC[11]	RUR	0	
2	RSBBEC[10]	RUR	0	
1	RSBBEC[9]	RUR	0	
0	RSBBEC[8]	RUR	0	

TABLE 54: PMON RECEIVE CRC-4 BLOCK ERROR COUNTER - LSB (RSBBECL) **HEX ADDRESS: 0XN906**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RSBBEC[7]	RUR	0	**Performance Monitor "Receive Synchronization Bit Error 16-Bit Counter" - Lower Byte:** These RESET-upon-READ bits, along with that within the "PMON Receive Synchronization Bit Error Counter Register MSB" combine to reflect the cumulative number of instances that the Receive Synchronization Bit errors has been detected by the Receive T1 Framer block since the last read of this register. This register contains the Least Significant byte of this 16-bit of the Receive Synchronization Bit Error counter. ***NOTE:*** *For all 16-bit wide PMON registers, user must read the MSB counter first before reading the LSB counter in order to read the accurate PMON counts. To clear PMON count, user must read the MSB counter first before reading the LSB counter in order to clear the PMON count.*
6	RSBBEC[6]	RUR	0	
5	RSBBEC[5]	RUR	0	
4	RSBBEC[4]	RUR	0	
3	RSBBEC[3]	RUR	0	
2	RSBBEC[2]	RUR	0	
1	RSBBEC[1]	RUR	0	
0	RSBBEC[0]	RUR	0	

TABLE 55: PMON RECEIVE FAR-END BLOCK ERROR COUNTER - MSB (RFEBECU) **HEX ADDRESS: 0XN907**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RFEBEC[15]	RUR	0	**Performance Monitor - Receive Far-End Block Error 16-Bit Counter - Upper Byte:** These RESET-upon-READ bits, along with that within the "PMON Receive Far-End Block Error Counter Register LSB" combine to reflect the cumulative number of instances that the Receive Far-End Block errors has been detected by the Receive T1 Framer block since the last read of this register. This register contains the Most Significant byte of this 16-bit of the Receive Far-End Block Error counter. ***NOTE:*** *The Receive Far-End Block Error Counter will increment once each time the received E-bit is set to zero. This counter is disabled during loss of sync at either the FAS or CRC-4 level and it will continue to count if loss of multiframe sync occurs at the CAS level.* ***NOTE:*** *For all 16-bit wide PMON registers, user must read the MSB counter first before reading the LSB counter in order to read the accurate PMON counts. To clear PMON count, user must read the MSB counter first before reading the LSB counter in order to clear the PMON count.*
6	RFEBEC[14]	RUR	0	
5	RFEBEC[13]	RUR	0	
4	RFEBEC[12]	RUR	0	
3	RFEBEC[11]	RUR	0	
2	RFEBEC[10]	RUR	0	
1	RFEBEC[9]	RUR	0	
0	RFEBEC[8]	RUR	0	

TABLE 56: PMON RECEIVE FAR END BLOCK ERROR COUNTER -LSB (RFEBECL) **HEX ADDRESS: 0XN908**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RFEBEC[7]	RUR	0	**Performance Monitor - Receive Far-End Block Error 16-Bit Counter - Lower Byte:** These RESET-upon-READ bits, along with that within the "PMON Receive Far-End Block Error Counter Register MSB" combine to reflect the cumulative number of instances that the Receive Far-End Block errors has been detected by the Receive T1 Framer block since the last read of this register. This register contains the Least Significant byte of this 16-bit of the Receive Far-End Block Error counter. ***NOTE:*** *The Receive Far-End Block Error Counter will increment once each time the received E-bit is set to zero. This counter is disabled during loss of sync at either the FAS or CRC-4 level and it will continue to count if loss of multiframe sync occurs at the CAS level.* ***NOTE:*** *For all 16-bit wide PMON registers, user must read the MSB counter first before reading the LSB counter in order to read the accurate PMON counts. To clear PMON count, user must read the MSB counter first before reading the LSB counter in order to clear the PMON count.*
6	RFEBEC[6]	RUR	0	
5	RFEBEC[5]	RUR	0	
4	RFEBEC[4]	RUR	0	
3	RFEBEC[3]	RUR	0	
2	RFEBEC[2]	RUR	0	
1	RFEBEC[1]	RUR	0	
0	RFEBEC[0]	RUR	0	

TABLE 57: PMON RECEIVE SLIP COUNTER (RSC) **HEX ADDRESS: 0XN909**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RSC[7]	RUR	0	**Performance Monitor - Receive Slip Counter (8-bit Counter)** These Reset-Upon-Read bit fields reflect the cumulative number of instances that Receive Slip events have been detected by the T1 Framer since the last read of this register. ***NOTE:*** *A slip event is defined as a replication or deletion of a T1 frame by the receive slip buffer.*
6	RSC[6]	RUR	0	
5	RSC[5]	RUR	0	
4	RSC[4]	RUR	0	
3	RSC[3]	RUR	0	
2	RSC[2]	RUR	0	
1	RSC[1]	RUR	0	
0	RSC[0]	RUR	0	

TABLE 58: PMON RECEIVE LOSS OF FRAME COUNTER (RLFC) **HEX ADDRESS: 0XN90A**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RLFC[7]	RUR	0	**Performance Monitor - Receive Loss of Frame Counter (8-bit Counter)** These Reset-Upon-Read bit fields reflect the cumulative number of instances that Receive Loss of Frame condition have been detected by the T1 Framer since the last read of this register. ***NOTE:*** *This counter counts once every time the Loss of Frame condition is declared. This counter provides the capability to measure an accumulation of short failure events.*
6	RLFC[6]	RUR	0	
5	RLFC[5]	RUR	0	
4	RLFC[4]	RUR	0	
3	RLFC[3]	RUR	0	
2	RLFC[2]	RUR	0	
1	RLFC[1]	RUR	0	
0	RLFC[0]	RUR	0	

TABLE 59: PMON RECEIVE CHANGE OF FRAME ALIGNMENT COUNTER (RCFAC) **HEX ADDRESS: 0XN90B**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RCFAC[7]	RUR	0	**Performance Monitor - Receive Change of Frame Alignment Counter (8-bit Counter)** These Reset-Upon-Read bit fields reflect the cumulative number of instances that Receive Change of Framing Alignment have been detected by the T1 Framer since the last read of this register. ***NOTE:*** *Change of Framing Alignment (COFA) is declared when the newly-locked framing pattern is different from the one offered by off-line framer.*
6	RCFAC[6]	RUR	0	
5	RCFAC[5]	RUR	0	
4	RCFAC[4]	RUR	0	
3	RCFAC[3]	RUR	0	
2	RCFAC[2]	RUR	0	
1	RCFAC[1]	RUR	0	
0	RCFAC[0]	RUR	0	

TABLE 60: PMON LAPD FRAME CHECK SEQUENCE ERROR COUNTER 1 (LFCSEC1) **HEX ADDRESS: 0XN90C**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	FCSEC1[7]	RUR	0	**Performance Monitor - LAPD Frame Check Sequence Error Counter (8-bit Counter)** These Reset-Upon-Read bit fields reflect the cumulative number of instances that Frame Check Sequence Error have been detected by the LAPD Controller since the last read of this register.
6	FCSEC1[6]	RUR	0	
5	FCSEC1[5]	RUR	0	
4	FCSEC1[4]	RUR	0	
3	FCSEC1[3]	RUR	0	
2	FCSEC1[2]	RUR	0	
1	FCSEC1[1]	RUR	0	
0	FCSEC1[0]	RUR	0	

TABLE 61: PMON PRBS BIT ERROR COUNTER MSB (PBECU) **HEX ADDRESS: 0XN90D**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	PRBSE[15]	RUR	0	**Performance Monitor - T1 PRBS Bit Error 16-Bit Counter - Upper Byte:** These RESET-upon-READ bits, along with that within the "PMON T1 PRBS Bit Error Counter Register LSB" combine to reflect the cumulative number of instances that the ReceiveT1 PRBS Bit errors has been detected by the Receive T1 Framer block since the last read of this register. This register contains the Most Significant byte of this 16-bit of the Receive T1 PRBS Bit Error counter. ***NOTE:*** *For all 16-bit wide PMON registers, user must read the MSB counter first before reading the LSB counter in order to read the accurate PMON counts. To clear PMON count, user must read the MSB counter first before reading the LSB counter in order to clear the PMON count.*
6	PRBSE[14]	RUR	0	
5	PRBSE[13]	RUR	0	
4	PRBSE[12]	RUR	0	
3	PRBSE[11]	RUR	0	
2	PRBSE[10]	RUR	0	
1	PRBSE[9]	RUR	0	
0	PRBSE[8]	RUR	0	

TABLE 62: PMON PRBS BIT ERROR COUNTER LSB (PBECL) **HEX ADDRESS: 0XN90E**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	PRBSE[7]	RUR	0	**Performance Monitor - T1 PRBS Bit Error 16-Bit Counter - Lower Byte:** These RESET-upon-READ bits, along with that within the "PMON T1 PRBS Bit Error Counter Register MSB" combine to reflect the cumulative number of instances that the ReceiveT1 PRBS Bit errors has been detected by the Receive T1 Framer block since the last read of this register. This register contains the Least Significant byte of this 16-bit of the Receive T1 PRBS Bit Error counter. ***NOTE:*** *For all 16-bit wide PMON registers, user must read the MSB counter first before reading the LSB counter in order to read the accurate PMON counts. To clear PMON count, user must read the MSB counter first before reading the LSB counter in order to clear the PMON count.*
6	PRBSE[6]	RUR	0	
5	PRBSE[5]	RUR	0	
4	PRBSE[4]	RUR	0	
3	PRBSE[3]	RUR	0	
2	PRBSE[2]	RUR	0	
1	PRBSE[1]	RUR	0	
0	PRBSE[0]	RUR	0	

TABLE 63: PMON TRANSMIT SLIP COUNTER (TSC) **HEX ADDRESS: 0XN90F**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	TxSLIP[7]	RUR	0	**Performance Monitor - Transmit Slip Counter (8-bit Counter)** These Reset-Upon-Read bit fields reflect the cumulative number of instances that Transmit Slip events have been detected by the T1 Framer since the last read of this register. ***NOTE:*** *A slip event is defined as a replication or deletion of a T1 frame by the transmit slip buffer.*
6	TxSLIP[6]	RUR	0	
5	TxSLIP[5]	RUR	0	
4	TxSLIP[4]	RUR	0	
3	TxSLIP[3]	RUR	0	
2	TxSLIP[2]	RUR	0	
1	TxSLIP[1]	RUR	0	
0	TxSLIP[0]	RUR	0	

TABLE 64: PMON EXCESSIVE ZERO VIOLATION COUNTER MSB (EZVCU) **HEX ADDRESS: 0XN910**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	EZVC[15]	RUR	0	**Performance Monitor - T1 Excessive Zero Violation 16-Bit Counter - Upper Byte:** These RESET-upon-READ bits, along with that within the "PMON T1 Excessive Zero Violation Counter Register LSB" combine to reflect the cumulative number of instances that the ReceiveT1 Excessive Zero Violation has been detected by the Receive T1 Framer block since the last read of this register. This register contains the Most Significant byte of this 16-bit of the Receive T1 Excessive Zero Violation counter. ***NOTE:*** *For all 16-bit wide PMON registers, user must read the MSB counter first before reading the LSB counter in order to read the accurate PMON counts. To clear PMON count, user must read the MSB counter first before reading the LSB counter in order to clear the PMON count.*
6	EZVC[14]	RUR	0	
5	EZVC[13]	RUR	0	
4	EZVC[12]	RUR	0	
3	EZVC[11]	RUR	0	
2	EZVC[10]	RUR	0	
1	EZVC[9]	RUR	0	
0	EZVC[8]	RUR	0	

TABLE 65: PMON EXCESSIVE ZERO VIOLATION COUNTER LSB (EZVCL) **HEX ADDRESS: 0XN911**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	EZVC[7]	RUR	0	**Performance Monitor - T1 Excessive Zero Violation 16-Bit Counter - Lower Byte:** These RESET-upon-READ bits, along with that within the "PMON T1 Excessive Zero Violation Counter Register MSB" combine to reflect the cumulative number of instances that the ReceiveT1 Excessive Zero Violation has been detected by the Receive T1 Framer block since the last read of this register. This register contains the Least Significant byte of this 16-bit of the Receive T1 Excessive Zero Violation counter. ***NOTE:*** *For all 16-bit wide PMON registers, user must read the MSB counter first before reading the LSB counter in order to read the accurate PMON counts. To clear PMON count, user must read the MSB counter first before reading the LSB counter in order to clear the PMON count.*
6	EZVC[6]	RUR	0	
5	EZVC[5]	RUR	0	
4	EZVC[4]	RUR	0	
3	EZVC[3]	RUR	0	
2	EZVC[2]	RUR	0	
1	EZVC[1]	RUR	0	
0	EZVC[0]	RUR	0	

TABLE 66: BLOCK INTERRUPT STATUS REGISTER (BISR) **HEX ADDRESS: 0XNB00**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved			For E1 mode only
6	LBCODE	RO	0	**Loopback Code Block Interrupt Status** This bit indicates whether or not the Loopback Code block has an interrupt request awaiting service. 0 - Indicates no outstanding Loopback Code Block interrupt request is awaiting service 1 - Indicates the Loopback Code block has an interrupt request awaiting service. Interrupt Service routine should branch to the interrupt source and read the Loopback Code Interrupt Status register to clear the interrupt ***NOTE:*** *This bit will be reset to 0 after the microprocessor has performed a read to the Loopback Code Interrupt Status Register.*
5	Reserved	RO	0	**Reserved**
4	ONESEC	RO	0	**One Second Interrupt Status** This bit indicates whether or not the framer has experienced a One Second interrupt since the last read of this register. 0 = Indicates One Second interrupt has not occurred since the last read of this register 1 = Indicates One Second interrupt has occurred since the last read of this register
3	HDLC	RO	0	**HDLC Block Interrupt Status** This bit indicates whether or not the HDLC block has any interrupt request awaiting service. 0 = Indicates no outstanding HDLC block interrupt request is awaiting service 1 = Indicates HDLC Block has an interrupt request awaiting service. Interrupt Service routine should branch to the interrupt source and read the corresponding Data LInk Status Registers to clear the interrupt. ***NOTE:*** *This bit will be reset to 0 after the microprocessor has performed a read to the corresponding Data Link Status Registers that generated the interrupt.*
2	SLIP	RO	0	**Slip Buffer Block Interrupt Status** This bit indicates whether or not the Slip Buffer block has any outstanding interrupt request awaiting service. 0 = Indicates no outstanding Slip Buffer Block interrupt request is awaiting service 1 = Indicates Slip Buffer block has an interrupt request awaiting service. Interrupt Service routine should branch to the interrupt source and read the Slip Buffer Interrupt Status register (address 0xNB08) to clear the interrupt ***NOTE:*** *This bit will be reset to 0 after the microprocessor has performed a read to the Slip Buffer Interrupt Status Register.*

TABLE 66: BLOCK INTERRUPT STATUS REGISTER (BISR) **HEX ADDRESS: 0XNB00**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	ALARM	RO	0	**Alarm & Error Block Interrupt Status** This bit indicates whether or not the Alarm & Error Block has any outstanding interrupt request awaiting service. 0 = Indicates no outstanding interrupt request is awaiting service 1 = Indicates the Alarm & Error Block has an interrupt request awaiting service. Interrupt service routine should branch to the interrupt source and read the corresponding alarm and error status registers to clear the interrupt. ***NOTE:*** *This bit will be reset to 0 after the microprocessor has performed a read to the corresponding Alarm & Error Interrupt Status register that generated the interrupt.*
0	T1 FRAME	RO	0	**T1 Framer Block Interrupt Status** This bit indicates whether or not the T1 Framer block has any outstanding interrupt request awaiting service. 0 = Indicates no outstanding interrupt request is awaiting service. 1 = Indicates the T1 Framer Block has an interrupt request awaiting service. Interrupt service routine should branch to the interrupt source and read the T1 Framer status register (address 0xNB04) to clear the interrupt ***NOTE:*** *This bit will be reset to 0 after the microprocessor has performed a read to the T1 Framer Interrupt Status register.*

TABLE 67: BLOCK INTERRUPT ENABLE REGISTER (BIER) **HEX ADDRESS: 0XNB01**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved			**For E1 mode only**
6	LBCODE_ENB	R/W	0	**Loopback Code Block interrupt enable** This bit permits the user to either enable or disable the Loopback Code Interrupt Block for interrupt generation. Writing a “0” to this register bit will disable the Loopback Code Block for interrupt generation, all Loopback Code interrupts will be disabled for interrupt generation. If the user writes a “1” to this register bit, the Loopback Code Interrupts at the “Block Level” will be enabled. However, the individual Loopback Code interrupts at the “Source Level” still need to be enabled to in order to generate that particular interrupt to the interrupt pin. 0 - Disables all Loopback Code Interrupt Block interrupt within the device. 1 - Enables the Loopback Code interrupt at the “Block-Level”.
5	Reserved	R/W	0	**Reserved**
4	ONESEC_ENB	R/W	0	**One Second Interrupt Enable** This bit permits the user to either enable or disable the One Second Interrupt for interrupt generation. 0 - Disables the One Second Interrupt within the device. 1 - Enables the One Second interrupt at the “Source-Level”.

TABLE 67: BLOCK INTERRUPT ENABLE REGISTER (BIER) **HEX ADDRESS: 0XNB01**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
3	HDLC_ENB	R/W	0	**HDLC Block Interrupt Enable** This bit permits the user to either enable or disable the HDLC Block for interrupt generation. Writing a “0” to this register bit will disable the HDLC Block for interrupt generation, all HDLC interrupts will be disabled for interrupt generation. If the user writes a “1” to this register bit, the HDLC Block interrupt at the “Block Level” will be enabled. However, the individual HDLC interrupts at the “Source Level” still need to be enabled in order to generate that particular interrupt to the interrupt pin. 0 - Disables all SA6 Block interrupt within the device. 1 - Enables the SA6 interrupt at the “Block-Level”.
2	SLIP_ENB	R/W	0	**Slip Buffer Block Interrupt Enable** This bit permits the user to either enable or disable the Slip Buffer Block for interrupt generation. Writing a “0” to this register bit will disable the Slip Buffer Block for interrupt generation, then all Slip Buffer interrupts will be disabled for interrupt generation. If the user writes a “1” to this register bit, the Slip Buffer Block interrupt at the “Block Level” will be enabled. However, the individual Slip Buffer interrupts at the “Source Level” still need to be enabled in order to generate that particular interrupt to the interrupt pin. 0 - Disables all Slip Buffer Block interrupt within the device. 1 - Enables the Slip Buffer interrupt at the “Block-Level”.
1	ALARM_ENB	R/W	0	**Alarm & Error Block Interrupt Enable** This bit permits the user to either enable or disable the Alarm & Error Block for interrupt generation. Writing a “0” to this register bit will disable the Alarm & Error Block for interrupt generation, then all Alarm & Error interrupts will be disabled for interrupt generation. If the user writes a “1” to this register bit, the Alarm & Error Block interrupt at the “Block Level” will be enabled. However, the individual Alarm & Error interrupts at the “Source Level” still need to be enabled in order to generate that particular interrupt to the interrupt pin. 0 - Disables all Alarm & Error Block interrupt within the device. 1 - Enables the Alarm & Error interrupt at the “Block-Level”.
0	T1FRAME_ENB	R/W	0	**T1 Framer Block Enable** This bit permits the user to either enable or disable the T1 Framer Block for interrupt generation. Writing a “0” to this register bit will disable the T1 Framer Block for interrupt generation, then all T1 Framer interrupts will be disabled for interrupt generation. If the user writes a “1” to this register bit, the T1 Framer Block interrupt at the “Block Level” will be enabled. However, the individual T1 Framer interrupts at the “Source Level” still need to be enabled in order to generate that particular interrupt to the interrupt pin. 0 - Disables all T1 Framer Block interrupt within the device. 1 - Enables the T1 Framer interrupt at the “Block-Level”.

TABLE 68: ALARM & ERROR INTERRUPT STATUS REGISTER (AEISR) **HEX ADDRESS: 0XNB02**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Rx LOF State	RO	0	**Receive Loss of Frame State** This READ-ONLY bit indicates whether or not the Receive T1 Framer block is currently declaring the "Loss of Frame" condition within the incoming T1 data-stream, as described below. Loss of Frame is declared when "TOLR" out of "RANG" errors in the framing bit pattern is detected. (Register 0xN10B) 0 – The Receive T1 Framer block is NOT currently declaring the "Loss of Frame" condition. 1 – The Receive T1 Framer block is currently declaring the "Loss of Frame" condition.
6	RxAIS State	RO	0	**Receive Alarm Indication Status Defect State** This READ-ONLY bit indicates whether or not the Receive T1 Framer block is currently declaring the AIS defect condition within the incoming T1 data-stream, as described below. AIS defect is declared when AIS condition persists for 42 milliseconds. AIS defect is cleared when AIS condition is absent for 42 milliseconds. 0 – The Receive T1 Framer block is NOT currently declaring the AIS defect condition. 1 – The Receive T1 Framer block is currently declaring the AIS defect condition.
5	RxYEL_State	RO	0	**Receive Yellow Alarm State** This READ-ONLY bit indicates whether or not the Receive T1 Framer block is currently declaring the Yellow Alarm condition within the incoming T1 data-stream, as described below. Yellow alarm or Remote Alarm Indication (RAI) is declared when RAI condition persists for 900 milliseconds. Yellow alarm or RAI is cleared immediately when RAI condition is absent even if the T1 Framer is receiving T1 Idle or RAI-CI signatures in ESF mode. 0 – The Receive T1 Framer block is NOT currently declaring the Yellow Alarm condition. 1 – The Receive T1 Framer block is currently declaring the Yellow Alarm condition.
4	LOS_State	RO	0	**Framer Receive Loss of Signal (LOS) State** This READ-ONLY bit indicates whether or not the Receive T1 framer is currently declaring the Loss of Signal (LOS) condition within the incoming T1 data-stream, as described below LOS defect is declared when LOS condition persists for 175 consecutive bits. LOS defect is cleared when LOS condition is absent or when the received signal reaches a 12.5% ones density for 175 consecutive bits. 0 = The Receive T1 Framer block is NOT currently declaring the Loss of Signal (LOS) condition. 1 = The Receive T1 Framer block is currently declaring the Loss of Signal (LOS) condition.

TABLE 68: ALARM & ERROR INTERRUPT STATUS REGISTER (AEISR) **HEX ADDRESS: 0XNB02**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
3	LCV Int Status	RUR/ WC	0	**Line Code Violation Interrupt Status**. This Reset-Upon-Read bit field indicates whether or not the Receive T1 LIU block has detected a Line Code Violation interrupt since the last read of this register. 0 = Indicates no Line Code Violation have occurred since the last read of this register. 1 = Indicates one or more Line Code Violation interrupt has occurred since the last read of this register.
2	Rx LOF State Change	RUR/ WC	0	**Change in Receive Loss of Frame Condition Interrupt Status**. This Reset-Upon-Read bit field indicates whether or not the “Change in Receive Loss of Frame Condition” interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive T1 Framer block declares the Loss of Frame condition. **2.** Whenever the Receive T1 Framer block clears the Loss of Frame condition 0 = Indicates that the “Change in Receive Loss of Frame condition” interrupt has not occurred since the last read of this register 1 = Indicates that the “Change in Receive Loss of Frame condition” interrupt has occurred since the last read of this register
1	RxAIS State Change	RUR/ WC	0	**Change in Receive AIS Condition Interrupt Status**. This Reset-Upon-Read bit field indicates whether or not the “Change in Receive AIS Condition” interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive T1 Framer block declares the AIS condition. **2.** Whenever the Receive T1 Framer block clears the AIS condition 0 = Indicates that the “Change in Receive AIS condition” interrupt has not occurred since the last read of this register 1 = Indicates that the “Change in Receive AIS condition” interrupt has occurred since the last read of this register
0	RxYEL State Change	RUR/ WC	0	**Change in Receive Yellow Alarm Interrupt Status.** This Reset-Upon-Read bit field indicates whether or not the “Change in Receive Yellow Alarm Condition” interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive T1 Framer block declares the Yellow Alarm condition. **2.** Whenever the Receive T1 Framer block clears the Yellow Alarm condition 0 = Indicates that the “Change in Receive Yellow Alarm condition” interrupt has not occurred since the last read of this register 1 = Indicates that the “Change in Receive Yellow Alarm condition” interrupt has occurred since the last read of this register

TABLE 69: ALARM & ERROR INTERRUPT ENABLE REGISTER (AEIER) **HEX ADDRESS: 0XNB03**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-5	Reserved	-	-	**Reserved (E1 mode only)**
4	-	-	-	**This bit should be set to'0' for proper operation.**
3	LCV ENB	R/W	0	**Line Code violation interrupt enable** This bit permits the user to either enable or disable the "Line Code Violation" interrupt within the XRT86SH328XRT86SH328 device. If the user enables this interrupt, then the Receive T1 Framer block will generate an interrupt when Line Code Violation is detected. 0 = Disables the interrupt generation when Line Code Violation is detected. 1 = Enables the interrupt generation when Line Code Violation is detected.
2	RxLOF ENB	R/W	0	**Change in Loss of Frame Condition interrupt enable** This bit permits the user to either enable or disable the "Change in Loss of Frame Condition" Interrupt, within the XRT86SH328 device. If the user enables this interrupt, then the Receive T1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** The instant that the Receive T1 Framer block declares the Loss of Frame condition. **2.** The instant that the Receive T1 Framer block clears the Loss of Frame condition. 0 – Disables the "Change in Loss of Frame Condition" Interrupt. 1 – Enables the "Change in Loss of Frame Condition" Interrupt.
1	RxAIS ENB	R/W	0	**Change in AIS Condition interrupt enable** This bit permits the user to either enable or disable the "Change in AIS Condition" Interrupt, within the XRT86SH328 device. If the user enables this interrupt, then the Receive T1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** The instant that the Receive T1 Framer block declares the AIS condition. **2.** The instant that the Receive T1 Framer block clears the AIS condition. 0 – Disables the "Change in AIS Condition" Interrupt. 1 – Enables the "Change in AIS Condition" Interrupt.
0	RxYEL ENB	R/W	0	**Change in Yellow alarm Condition interrupt enable** This bit permits the user to either enable or disable the "Change in Yellow Alarm Condition" Interrupt, within the XRT86SH328 device. If the user enables this interrupt, then the Receive T1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** The instant that the Receive T1 Framer block declares the Yellow Alarm condition. **2.** The instant that the Receive T1 Framer block clears the Yellow Alarm condition. 0 – Disables the "Change in Yellow Alarm Condition" Interrupt. 1 – Enables the "Change in Yellow Alarm Condition" Interrupt.

TABLE 70: FRAMER INTERRUPT STATUS REGISTER (FISR) **HEX ADDRESS: 0XNB04**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-6	-	-	-	**Reserved (For E1 mode only)**
5	SIG	RUR/ WC	0	**Change in Signaling Bits Interrupt Status** This Reset-Upon-Read bit field indicates whether or not the "Change in Signaling Bits" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt whenever any one of the four signaling bits values (A,B,C,D) has changed in any one of the 24 channels within the incoming T1 frames. Users can read the signaling change registers (address 0xN10D-0xN10F) to determine which signalling channel has changed. 0 = Indicates that the "Change in Signaling Bits" interrupt has not occurred since the last read of this register. 1 = Indicates that the "Change in Signaling Bits" interrupt has occurred since the last read of this register. ***NOTE:*** *This bit only has meaning when Robbed-Bit Signaling is enabled.*
4	COFA	RUR/ WC	0	**Change of Frame Alignment (COFA) Interrupt Status** This Reset-Upon-Read bit field indicates whether or not the "Change of Framing Alignment (COFA)" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt whenever the Receive T1 Framer block detects a Change of Framing Alignment Signal (e.g., the Framing bits have appeared to move to a different location within the incoming T1 data stream). 0 = Indicates that the "Change of Framing Alignment (COFA)" interrupt has not occurred since the last read of this register. 1 = Indicates that the "Change of Framing Alignment (COFA)" interrupt has occurred since the last read of this register.
3	LOF_Status	RUR/ WC	0	**Change in Receive Loss of Frame Condition Interrupt Status**. This Reset-Upon-Read bit field indicates whether or not the "Change in Receive Loss of Frame Condition" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive T1 Framer block declares the Loss of Frame condition. **2.** Whenever the Receive T1 Framer block clears the Loss of Frame condition 0 = Indicates that the "Change in Receive Loss of Frame condition" interrupt has not occurred since the last read of this register 1 = Indicates that the "Change in Receive Loss of Frame condition" interrupt has occurred since the last read of this register

TABLE 70: FRAMER INTERRUPT STATUS REGISTER (FISR) **HEX ADDRESS: 0XNB04**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
2	FMD	RUR/ WC	0	**Frame Mimic Detection Interrupt Status** This Reset-Upon-Read bit field indicates whether or not the "Frame Mimic Detection" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt whenever the Receive T1 Framer block detects the presence of Frame Mimic bits (i.e., the Payload bits have appeared to mimic the Framing Bit pattern within the incoming T1 data stream). 0 = Indicates that the "Frame Mimic Detection" interrupt has not occurred since the last read of this register. 1 = Indicates that the "Frame Mimic Detection" interrupt has occurred since the last read of this register.
1	SE	RUR/ WC	0	**Synchronization Bit Error (CRC-6) Interrupt Status** This Reset-Upon-Read bit field indicates whether or not the "CRC-6 Error" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt whenever the Receive T1 Framer block detects a CRC-6 Error within the incoming T1 multiframe. 0 = Indicates that the "CRC-6 Error" interrupt has not occurred since the last read of this register. 1 = Indicates that the "CRC-6 Error" interrupt has occurred since the last read of this register.
0	FE	RUR/ WC	0	**Framing Error Interrupt Status** This Reset-Upon-Read bit field indicates whether or not a "Framing Error" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt whenever the Receive T1 Framer block detects one or more Framing Alignment Bit Error within the incoming T1 data stream. 0 = Indicates that the "Framing Error" interrupt has not occurred since the last read of this register. 1 = Indicates that the "Framing Error" interrupt has occurred since the last read of this register. ***NOTE:*** *This bit doesn't not necessarily indicate that synchronization has been lost.*

TABLE 71: FRAMER INTERRUPT ENABLE REGISTER (FIER) **HEX ADDRESS: 0XNB05**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
5	SIG_ENB	R/W	0	**Change in Signaling Bits Interrupt Enable** This bit permits the user to either enable or disable the "Change in Signaling Bits" Interrupt, within the XRT86SH328 device. If the user enables this interrupt, then the Receive T1 Framer block will generate an interrupt when it detects a change in the any four signaling bits (A,B,C,D) in any one of the 24 signaling channels. Users can read the signaling change registers (address 0xN10D-0xN10F) to determine which signalling channel has changed state. 0 - Disables the Change in Signaling Bits Interrupt 1 - Enables the Change in Signaling Bits Interrupt ***NOTE:*** *This bit has no meaning when Robbed-Bit Signaling is disabled.*
4	COFA_ENB	R/W	0	**Change of Framing Alignment (COFA) Interrupt Enable** This bit permits the user to either enable or disable the "Change in FAS Framing Alignment (COFA)" Interrupt, within the XRT86SH328 device. If the user enables this interrupt, then the Receive T1 Framer block will generate an interrupt when it detects a Change of Framing Alignment Signal (e.g., the Framing bits have appeared to move to a different location within the incoming T1 data stream). 0 - Disables the "Change of Framing Alignment (COFA)" Interrupt. 1 - Enables the "Change of Framing Alignment (COFA)" Interrupt.
3	LOF_ENB	R/W	0	**Change in Loss of Frame Condition interrupt enable** This bit permits the user to either enable or disable the "Change in Loss of Frame Condition" Interrupt, within the XRT86SH328 device. If the user enables this interrupt, then the Receive T1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** The instant that the Receive T1 Framer block declares the Loss of Frame condition. **2.** The instant that the Receive T1 Framer block clears the Loss of Frame condition. 0 – Disables the "Change in Loss of Frame Condition" Interrupt. 1 – Enables the "Change in Loss of Frame Condition" Interrupt.
2	FMD_ENB	R/W	0	**Frame Mimic Detection Interrupt Enable** This bit permits the user to either enable or disable the "Frame Mimic Detection" Interrupt, within the XRT86SH328 device. If the user enables this interrupt, then the Receive T1 Framer block will generate an interrupt when it detects the presence of Frame mimic bits (i.e., the payload bits have appeared to mimic the framing bit pattern within the incoming T1 data stream). 0 - Disables the "Frame Mimic Detection" Interrupt. 1 - Enables the "Frame Mimic Detection" Interrupt.

TABLE 71: FRAMER INTERRUPT ENABLE REGISTER (FIER) **HEX ADDRESS: 0XNB05**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	SE_ENB	R/W	0	**Synchronization Bit (CRC-6) Error Interrupt Enable** This bit permits the user to either enable or disable the “CRC-6 Error Detection” Interrupt, within the XRT86SH328 device. If the user enables this interrupt, then the Receive T1 Framer block will generate an interrupt when it detects a CRC-6 error within the incoming T1 multiframe. 0 - Disables the “CRC-6 Error Detection” Interrupt. 1 - Enables the “CRC-6 Error Detection” Interrupt.
0	FE_ENB	R/W	0	**Framing Bit Error Interrupt Enable** This bit permits the user to either enable or disable the “Framing Alignment Bit Error Detection” Interrupt, within the XRT86SH328 device. If the user enables this interrupt, then the Receive T1 Framer block will generate an interrupt when it detects one or more Framing Alignment Bit error within the incoming T1 data stream. 0 - Disables the “Framing Alignment Bit Error Detection” Interrupt. 1 - Enables the “Framing Alignment Bit Error Detection” Interrupt. ***NOTE:*** *Detecting Framing Alignment Bit Error doesn't not necessarily indicate that synchronization has been lost.*

TABLE 72: DATA LINK STATUS REGISTER 1 (DLSR1) **HEX ADDRESS: 0XNB06**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	MSG TYPE	RO	0	**HDLC1 Message Type Identifier** This READ ONLY bit indicates the type of data link message received by Receive HDLC 1 Controller. Two types of data link messages are supported within the XRT86SH328 device: Message Oriented Signaling (MOS) or Bit-Oriented Signalling (BOS). 0 = Indicates Bit-Oriented Signaling (BOS) type data link message is received 1 = Indicates Message Oriented Signaling (MOS) type data link message is received
6	TxSOT	RUR/ WC	0	**Transmit HDLC1 Controller Start of Transmission (TxSOT) Interrupt Status** This Reset-Upon-Read bit indicates whether or not the “Transmit HDLC1 Controller Start of Transmission (TxSOT) “Interrupt has occurred since the last read of this register. Transmit HDLC1 Controller will declare this interrupt when it has started to transmit a data link message. For sending large HDLC messages, start loading the next available buffer once this interrupt is detected. 0 = Transmit HDLC1 Controller Start of Transmission (TxSOT) interrupt has not occurred since the last read of this register 1 = Transmit HDLC1 Controller Start of Transmission interrupt (TxSOT) has occurred since the last read of this register.
5	RxSOT	RUR/ WC	0	**Receive HDLC1 Controller Start of Reception (RxSOT) Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Receive HDLC1 Controller Start of Reception (RxSOT) interrupt has occurred since the last read of this register. Receive HDLC1 Controller will declare this interrupt when it has started to receive a data link message. 0 = Receive HDLC1 Controller Start of Reception (RxSOT) interrupt has not occurred since the last read of this register 1 = Receive HDLC1 Controller Start of Reception (RxSOT) interrupt has occurred since the last read of this register
4	TxEOT	RUR/ WC	0	**Transmit HDLC1 Controller End of Transmission (TxEOT) Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Transmit HDLC1 Controller End of Transmission (TxEOT) Interrupt has occurred since the last read of this register. Transmit HDLC1 Controller will declare this interrupt when it has completed its transmission of a data link message. For sending large HDLC messages, it is critical to load the next available buffer before this interrupt occurs. 0 = Transmit HDLC1 Controller End of Transmission (TxEOT) interrupt has not occurred since the last read of this register 1 = Transmit HDLC1 Controller End of Transmission (TxEOT) interrupt has occurred since the last read of this register

TABLE 72: DATA LINK STATUS REGISTER 1 (DLSR1) **HEX ADDRESS: 0XNB06**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
3	RxEOT	RUR/ WC	0	**Receive HDLC1 Controller End of Reception (RxEOT) Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Receive HDLC1 Controller End of Reception (RxEOT) Interrupt has occurred since the last read of this register. Receive HDLC1 Controller will declare this interrupt once it has completely received a full data link message, or once the buffer is full. 0 = Receive HDLC1 Controller End of Reception (RxEOT) interrupt has not occurred since the last read of this register 1 = Receive HDLC1 Controller End of Reception (RxEOT) Interrupt has occurred since the last read of this register
2	FCS Error	RUR/ WC	0	**FCS Error Interrupt Status** This Reset-Upon-Read bit indicates whether or not the FCS Error Interrupt has occurred since the last read of this register. Receive HDLC1 Controller will declare this interrupt when it has detected the FCS error in the most recently received data link message. 0 = FCS Error interrupt has not occurred since the last read of this register 1 = FCS Error interrupt has occurred since the last read of this register
1	Rx ABORT	RUR/ WC	0	**Receipt of Abort Sequence Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Receipt of Abort Sequence interrupt has occurred since last read of this register. Receive HDLC1 Controller will declare this interrupt if it detects the Abort Sequence (i.e. a string of seven (7) consecutive 1's) in the incoming data link channel. 0 = Receipt of Abort Sequence interrupt has not occurred since last read of this register 1 = Receipt of Abort Sequence interrupt has occurred since last read of this register
0	RxIDLE	RUR/ WC	0	**Receipt of Idle Sequence Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Receipt of Idle Sequence interrupt has occurred since the last read of this register. The Receive HDLC1 Controller will declare this interrupt if it detects the flag sequence octet (0x7E) in the incoming data link channel. If RxIDLE "AND" RxEOT occur together, then the entire HDLC message has been received. 0 = Receipt of Idle Sequence interrupt has not occurred since last read of this register 1 = Receipt of Idle Sequence interrupt has occurred since last read of this register.

TABLE 73: DATA LINK INTERRUPT ENABLE REGISTER 1 (DLIER1) **HEX ADDRESS: 0XNB07**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved	-	-	**Reserved**
6	TxSOT ENB	R/W	0	**Transmit HDLC1 Controller Start of Transmission (TxSOT) Interrupt Enable** This bit enables or disables the "Transmit HDLC1 Controller Start of Transmission (TxSOT) "Interrupt within the XRT86SH328 device. Once this interrupt is enabled, the Transmit HDLC1 Controller will generate an interrupt when it has started to transmit a data link message. 0 = Disables the Transmit HDLC1 Controller Start of Transmission (TxSOT) interrupt. 1 = Enables the Transmit HDLC1 Controller Start of Transmission (TxSOT) interrupt.
5	RxSOT ENB	R/W	0	**Receive HDLC1 Controller Start of Reception (RxSOT) Interrupt Enable** This bit enables or disables the "Receive HDLC1 Controller Start of Reception (RxSOT) "Interrupt within the XRT86SH328 device. Once this interrupt is enabled, the Receive HDLC1 Controller will generate an interrupt when it has started to receive a data link message. 0 = Disables the Receive HDLC1 Controller Start of Reception (RxSOT) interrupt. 1 = Enables the Receive HDLC1 Controller Start of Reception (RxSOT) interrupt.
4	TxEOT ENB	R/W	0	**Transmit HDLC1 Controller End of Transmission (TxEOT) Interrupt Enable** This bit enables or disables the "Transmit HDLC1 Controller End of Transmission (TxEOT) "Interrupt within the XRT86SH328 device. Once this interrupt is enabled, the Transmit HDLC1 Controller will generate an interrupt when it has finished transmitting a data link message. 0 = Disables the Transmit HDLC1 Controller End of Transmission (TxEOT) interrupt. 1 = Enables the Transmit HDLC1 Controller End of Transmission (TxEOT) interrupt.
3	RxEOT ENB	R/W	0	**Receive HDLC1 Controller End of Reception (RxEOT) Interrupt Enable** This bit enables or disables the "Receive HDLC1 Controller End of Reception (RxEOT) "Interrupt within the XRT86SH328 device. Once this interrupt is enabled, the Receive HDLC1 Controller will generate an interrupt when it has finished receiving a complete data link message. 0 = Disables the Receive HDLC1 Controller End of Reception (RxEOT) interrupt. 1 = Enables the Receive HDLC1 Controller End of Reception (RxEOT) interrupt.

TABLE 73: DATA LINK INTERRUPT ENABLE REGISTER 1 (DLIER1) **HEX ADDRESS: 0XNB07**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
2	FCS ERR ENB	R/W	0	**FCS Error Interrupt Enable** This bit enables or disables the “Received FCS Error “Interrupt within the XRT86SH328 device. Once this interrupt is enabled, the Receive HDLC1 Controller will generate an interrupt when it has detected the FCS error within the incoming data link message. 0 = Disables the “Receive FCS Error” interrupt. 1 = Enables the “Receive FCS Error” interrupt.
1	RxABORT ENB	R/W	0	**Receipt of Abort Sequence Interrupt Enable** This bit enables or disables the “Receipt of Abort Sequence“ Interrupt within the XRT86SH328 device. Once this interrupt is enabled, the Receive HDLC1 Controller will generate an interrupt when it has detected the Abort Sequence (i.e. a string of seven (7) consecutive 1’s) within the incoming data link channel. 0 = Disables the “Receipt of Abort Sequence” interrupt. 1 = Enables the “Receipt of Abort Sequence” interrupt.
0	RxIDLE ENB	R/W	0	**Receipt of Idle Sequence Interrupt Enable** This bit enables or disables the “Receipt of Idle Sequence“ Interrupt within the XRT86SH328 device. Once this interrupt is enabled, the Receive HDLC1 Controller will generate an interrupt when it has detected the Idle Sequence Octet (i.e. 0x7E) within the incoming data link channel. 0 = Disables the “Receipt of Idle Sequence” interrupt. 1 = Enables the “Receipt of Idle Sequence” interrupt.

TABLE 74: SLIP BUFFER INTERRUPT STATUS REGISTER (SBISR) **HEX ADDRESS: 0XNB08**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	TxSB_FULL	RUR/ WC	0	**Transmit Slip buffer Full Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Transmit Slip Buffer Full interrupt has occurred since the last read of this register. The transmit Slip Buffer Full interrupt is declared when the transmit slip buffer is filled. If the transmit slip buffer is full and a WRITE operation occurs, then a full frame of data will be deleted, and this interrupt bit will be set to '1'. 0 = Indicates that the Transmit Slip Buffer Full interrupt has not occurred since the last read of this register. 1 = Indicates that the Transmit Slip Buffer Full interrupt has occurred since the last read of this register.
6	TxSB_EMPT	RUR/ WC	0	**Transmit Slip buffer Empty Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Transmit Slip Buffer Empty interrupt has occurred since the last read of this register. The transmit Slip Buffer Empty interrupt is declared when the transmit slip buffer is emptied. If the transmit slip buffer is emptied and a READ operation occurs, then a full frame of data will be repeated, and this interrupt bit will be set to '1'. 0 = Indicates that the Transmit Slip Buffer Empty interrupt has not occurred since the last read of this register. 1 = Indicates that the Transmit Slip Buffer Empty interrupt has occurred since the last read of this register.
5	TxSB_SLIP	RUR/ WC	0	**Transmit Slip Buffer Slips Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Transmit Slip Buffer Slips interrupt has occurred since the last read of this register. The transmit Slip Buffer Slips interrupt is declared when the transmit slip buffer is either filled or emptied. This interrupt bit will be set to '1' in either one of these two conditions: **1.** If the transmit slip buffer is emptied and a READ operation occurs, then a full frame of data will be repeated, and this interrupt bit will be set to '1'. **2.** If the transmit slip buffer is full and a WRITE operation occurs, then a full frame of data will be deleted, and this interrupt bit will be set to '1'. 0 = Indicates that the Transmit Slip Buffer Slips interrupt has not occurred since the last read of this register. 1 = Indicates that the Transmit Slip Buffer Slips interrupt has occurred since the last read of this register. ***NOTE:*** *Users still need to read the Transmit Slip Buffer Empty Interrupt (bit 6 of this register) or the Transmit Slip Buffer Full Interrupts (bit 7 of this register) to determine whether transmit slip buffer empties or fills.*

TABLE 74: SLIP BUFFER INTERRUPT STATUS REGISTER (SBISR) **HEX ADDRESS: 0XNB08**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
4	SLC®96 LOCK	RO	0	**SLC®96 is in SYNC** This READ ONLY bit field indicates whether or not frame synchronization is achieved when the XRT86SH328 is configured in SLC®96 framing mode. 0 = Indicates that frame synchronization is not achieved in SLC®96 framing mode. 1 = Indicates that frame synchronization is achieved in SLC®96 framing mode.
3	Multiframe LOCK	RO	0	**Multiframe is in SYNC** This READ ONLY bit field indicates whether or not the T1 Receive Framer Block is declaring T1 Multiframe LOCK status. 0 = Indicates that the T1 Receive Framer is currently declaring T1 multiframe LOSS OF LOCK status 0 = Indicates that the T1 Receive Framer is currently declaring T1 multiframe LOCK status
2	RxSB_FULL	RUR/ WC	0	**Receive Slip buffer Full Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Receive Slip Buffer Full interrupt has occurred since the last read of this register. The Receive Slip Buffer Full interrupt is declared when the receive slip buffer is filled. If the receive slip buffer is full and a WRITE operation occurs, then a full frame of data will be deleted, and this interrupt bit will be set to '1'. 0 = Indicates that the Receive Slip Buffer Full interrupt has not occurred since the last read of this register. 1 = Indicates that the Receive Slip Buffer Full interrupt has occurred since the last read of this register.

TABLE 74: SLIP BUFFER INTERRUPT STATUS REGISTER (SBISR) **HEX ADDRESS: 0XNB08**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	RxSB_EMPT	RUR/ WC	0	**Receive Slip buffer Empty Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Receive Slip Buffer Empty interrupt has occurred since the last read of this register. The Receive Slip Buffer Empty interrupt is declared when the receive slip buffer is emptied. If the receive slip buffer is emptied and a READ operation occurs, then a full frame of data will be repeated, and this interrupt bit will be set to '1'. 0 = Indicates that the Receive Slip Buffer Empty interrupt has not occurred since the last read of this register. 1 = Indicates that the Receive Slip Buffer Empty interrupt has occurred since the last read of this register.
0	RxSB_SLIP	RUR/ WC	0	**Receive Slip Buffer Slips Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Receive Slip Buffer Slips interrupt has occurred since the last read of this register. The Receive Slip Buffer Slips interrupt is declared when the receive slip buffer is either filled or emptied. This interrupt bit will be set to '1' in either one of these two conditions: **1.** If the receive slip buffer is emptied and a READ operation occurs, then a full frame of data will be repeated, and this interrupt bit will be set to '1'. **2.** If the receive slip buffer is full and a WRITE operation occurs, then a full frame of data will be deleted, and this interrupt bit will be set to '1'. 0 = Indicates that the Receive Slip Buffer Slips interrupt has not occurred since the last read of this register. 1 = Indicates that the Receive Slip Buffer Slips interrupt has occurred since the last read of this register. ***NOTE:*** *Users still need to read the Receive Slip Buffer Empty Interrupt (bit 1 of this register) or the Receive Slip Buffer Full Interrupts (bit 2 of this register) to determine whether transmit slip buffer empties or fills.*

TABLE 75: SLIP BUFFER INTERRUPT ENABLE REGISTER (SBIER) **HEX ADDRESS: 0XNB09**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	TxFULL_ENB	R/W	0	**Transmit Slip Buffer Full Interrupt Enable** This bit enables or disables the Transmit Slip Buffer Full interrupt within the XRT86SH328 device. Once this interrupt is enabled, the transmit Slip Buffer Full interrupt is declared when the transmit slip buffer is filled. If the transmit slip buffer is full and a WRITE operation occurs, then a full frame of data will be deleted, and the interrupt status bit will be set to '1'. 0 - Disables the Transmit Slip Buffer Full interrupt when the Transmit Slip Buffer fills 1 - Enables the Transmit Slip Buffer Full interrupt when the Transmit Slip Buffer fills.
6	TxEMPT_ENB	R/W	0	**Transmit Slip Buffer Empty Interrupt Enable** This bit enables or disables the Transmit Slip Buffer Empty interrupt within the XRT86SH328 device. Once this interrupt is enabled, the transmit Slip Buffer Empty interrupt is declared when the transmit slip buffer is emptied. If the transmit slip buffer is emptied and a READ operation occurs, then a full frame of data will be repeated, and the interrupt status bit will be set to '1'. 0 - Disables the Transmit Slip Buffer Empty interrupt when the Transmit Slip Buffer empties 1 - Enables the Transmit Slip Buffer Empty interrupt when the Transmit Slip Buffer empties.
5	TxSLIP_ENB	R/W	0	**Transmit Slip Buffer Slips Interrupt Enable** This bit enables or disables the Transmit Slip Buffer Slips interrupt within the XRT86SH328 device. Once this interrupt is enabled, the transmit Slip Buffer Slips interrupt is declared when either the transmit slip buffer is filled or emptied. If the transmit slip buffer is emptied and a READ operation occurs, then a full frame of data will be repeated, and the interrupt status bit will be set to '1'. The interrupt status bit will be set to '1' in either one of these two conditions: **1.** If the transmit slip buffer is emptied and a READ operation occurs, then a full frame of data will be repeated, and this interrupt bit will be set to '1'. **2.** If the transmit slip buffer is full and a WRITE operation occurs, then a full frame of data will be deleted, and this interrupt bit will be set to '1'. 0 - Disables the Transmit Slip Buffer Slips interrupt when the Transmit Slip Buffer empties or fills 1 - Enables the Transmit Slip Buffer Slips interrupt when the Transmit Slip Buffer empties or fills.
4-3	Reserved	-	-	**Reserved**

TABLE 75: SLIP BUFFER INTERRUPT ENABLE REGISTER (SBIER) **HEX ADDRESS: 0XNB09**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
2	RxFULL_ENB	R/W	0	**Receive Slip Buffer Full Interrupt Enable** This bit enables or disables the Receive Slip Buffer Full interrupt within the XRT86SH328 device. Once this interrupt is enabled, the Receive Slip Buffer Full interrupt is declared when the receive slip buffer is filled. If the Receive slip buffer is full and a WRITE operation occurs, then a full frame of data will be deleted, and the interrupt status bit will be set to '1'. 0 - Disables the Receive Slip Buffer Full interrupt when the Transmit Slip Buffer fills 1 - Enables the Receive Slip Buffer Full interrupt when the Transmit Slip Buffer fills.
1	RxEMPT_ENB	R/W	0	**Receive Slip buffer Empty Interrupt Enable** This bit enables or disables the Receives Slip Buffer Empty interrupt within the XRT86SH328 device. Once this interrupt is enabled, the Receive Slip Buffer Empty interrupt is declared when the Receive slip buffer is emptied. If the Receive slip buffer is emptied and a READ operation occurs, then a full frame of data will be repeated, and the interrupt status bit will be set to '1'. 0 - Disables the Receive Slip Buffer Empty interrupt when the Transmit Slip Buffer empties 1 - Enables the Receive Slip Buffer Empty interrupt when the Transmit Slip Buffer empties.
0	RxSLIP_ENB	R/W	0	**Receive Slip buffer Slips Interrupt Enable** This bit enables or disables the Receive Slip Buffer Slips interrupt within the XRT86SH328 device. Once this interrupt is enabled, the Receive Slip Buffer Slips interrupt is declared when either the Receive slip buffer is filled or emptied. If the Receive slip buffer is emptied and a READ operation occurs, then a full frame of data will be repeated, and the interrupt status bit will be set to '1'. The interrupt status bit will be set to '1' in either one of these two conditions: **1.** If the Receive slip buffer is emptied and a READ operation occurs, then a full frame of data will be repeated, and this interrupt bit will be set to '1'. **2.** If the Receive slip buffer is full and a WRITE operation occurs, then a full frame of data will be deleted, and this interrupt bit will be set to '1'. 0 - Disables the Receive Slip Buffer Slips interrupt when the Transmit Slip Buffer empties or fills 1 - Enables the Receive Slip Buffer Slips interrupt when the Transmit Slip Buffer empties or fills.

RECEIVE LOOPBACK CODE INTERRUPT AND STATUS REGISTER - CODE 0 (RLCISR0) HEX ADDRESS: 0XNB0A

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-4	-	-	-	**Reserved (For E1 mode only)**
3	RXASTAT	RO	0	**Receive Loopback Activation Code State** This READ ONLY bit indicates whether or not the Receive T1 Framer Block is currently detecting the Receive Loopback Activation Code, as specified in the Receive Loopback Activation Code Register (RLACR - address 0xN126) if Receive Loopback Activation Code Detection is enabled. 0 = Indicates that the Receive T1 Framer Block is NOT currently detecting the Receive Loopback Activation Code. 1 = Indicates that the Receive T1 Framer Block is currently detecting the Receive Loopback Activation Code.
2	RXDSTAT	RO	0	**Receive Loopback Deactivation Code State** This READ ONLY bit indicates whether or not the Receive T1 Framer Block is currently detecting the Receive Loopback Deactivation Code, as specified in the Receive Loopback Deactivation Code Register (RLDCR - address 0xN127) if Receive Loopback Deactivation Code Detection is enabled. 0 = Indicates that the Receive T1 Framer Block is NOT currently detecting the Receive Loopback Deactivation Code. 1 = Indicates that the Receive T1 Framer Block is currently detecting the Receive Loopback Deactivation Code.
1	RXAINT	RUR/ WC	0	**Change in Receive Loopback Activation Code interrupt Status** This Reset-Upon-Read bit field indicates whether or not the “Change in Receive Loopback Activation Code” interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive T1 Framer block detects the Receive Loopback Activation Code. **2.** Whenever the Receive T1 Framer block no longer detects the Receive Loopback Activation Code. 0 = Indicates that the “Change in Receive Loopback Activation Code” interrupt has not occurred since the last read of this register 1 = Indicates that the “Change in Receive Loopback Activation Code” interrupt has occurred since the last read of this register
0	RXDINT	RUR/ WC	0	**Change in Receive Loopback Deactivation Code interrupt Status** This Reset-Upon-Read bit field indicates whether or not the “Change in Receive Loopback Deactivation Code” interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive T1 Framer block detects the Receive Loopback Deactivation Code. **2.** Whenever the Receive T1 Framer block no longer detects the Receive Loopback Deactivation Code. 0 = Indicates that the “Change in Receive Loopback Deactivation Code” interrupt has not occurred since the last read of this register 1 = Indicates that the “Change in Receive Loopback Deactivation Code” interrupt has occurred since the last read of this register

TABLE 76: RECEIVE LOOPBACK CODE INTERRUPT ENABLE REGISTER-CODE 0 (RLCIER0)HEX ADDRESS: 0XNB0B

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-2	Reserved	-	-	**Reserved**
1	RXAENB	R/W	0	**Receive Loopback Activation Code Interrupt Enable** This bit enables or disables the “Change in Receive Loopback Activation Code” interrupt within the T1 Receive Framer. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive T1 Framer block detects the Receive Loopback Activation Code. **2.** Whenever the Receive T1 Framer block no longer detects the Receive Loopback Activation Code. 0 - Disables the “Change in Receive Loopback Activation Code” interrupt within the T1 Receive Framer. 1 - Enables the “Change in Receive Loopback Activation Code” interrupt within the T1 Receive Framer.
0	RXDENB	R/W	0	**Receive Loopback Deactivation Code Interrupt Enable** This bit enables or disables the “Change in Receive Loopback Deactivation Code” interrupt within the T1 Receive Framer. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive T1 Framer block detects the Receive Loopback Deactivation Code. **2.** Whenever the Receive T1 Framer block no longer detects the Receive Loopback Deactivation Code. 0 - Disables the “Change in Receive Loopback Deactivation Code” interrupt within the T1 Receive Framer. 1 - Enables the “Change in Receive Loopback Deactivation Code” interrupt within the T1 Receive Framer.

TABLE 77: EXCESSIVE ZERO STATUS REGISTER (EXZSR) **HEX ADDRESS: 0XNB0E**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-1	Reserved	-	-	**Reserved**
0	EXZ_STATUS	RUR/ WC	0	**Change in Excessive Zero Condition Interrupt Status** This Reset-Upon-Read bit field indicates whether or not the "Change in Excessive Zero Condition" interrupt within the T1 Receive Framer Block has occurred since the last read of this register. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive T1 Framer block detects the Excessive Zero Condition. **2.** Whenever the Receive T1 Framer block clears the Excessive Zero Condition 0 = Indicates the "Change in Excessive Zero Condition" interrupt has NOT occurred since the last read of this register 1 = Indicates the "Change in Excessive Zero Condition" interrupt has occurred since the last read of this register

TABLE 78: EXCESSIVE ZERO ENABLE REGISTER (EXZER) **HEX ADDRESS: 0XNB0F**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-1	-	-	-	**Reserved**
0	EXZ_ENB	R/W	0	**Change in Excessive Zero Condition Interrupt Enable** This bit enables or disables the "Change in Excessive Zero Condition" interrupt within the T1 Receive Framer. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive T1 Framer block detects the Excessive Zero Condition. **2.** Whenever the Receive T1 Framer block clears the Excessive Zero Condition 0 - Disables the "Change in Excessive Zero Condition" interrupt within the Receive T1 Framer Block 1 - Enables the "Change in Excessive Zero Condition" interrupt within the Receive T1 Framer Block

TABLE 79: SS7 STATUS REGISTER FOR LAPD (SS7SR) **HEX ADDRESS: 0XNB10**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
0	SS7_STATUS	RUR/ WC	0	**SS7 Interrupt Status for LAPD Controller** This Reset-Upon-Read bit field indicates whether or not the “SS7” interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt when the Received LAPD message is more than 276 Bytes in length. 0 = Indicates that the “SS7” interrupt has not occurred since the last read of this register 1 = Indicates that the “SS7” interrupt has occurred since the last read of this register

TABLE 80: SS7 ENABLE REGISTER FOR LAPD (SS7ER) **HEX ADDRESS: 0XNB11**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
0	SS7_ENB	R/W	0	**SS7 Interrupt Enable for LAPD Controller** This bit enables or disables the “SS7” interrupt within the LAPD Controller. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt when the Received LAPD message is more than 276 Bytes in length. 0 - Disables the “SS7” interrupt within the LAPD Controller. 1 - Enables the “SS7” interrupt within the LAPD Controller.

TABLE 81: RXLOS/CRC INTERRUPT STATUS REGISTER (RLCISR) **HEX ADDRESS: 0XNB12**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-4	-	-	-	Reserved
3	RxLOSINT	RUR/ WC	0	**Change in Receive LOS condition Interrupt Status** This bit indicates whether or not the “Change in Receive LOS condition” interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive T1 Framer block declares the Receive LOS condition. **2.** Whenever the Receive T1 Framer block clears the Receive LOS condition. 0 = Indicates that the “Change in Receive LOS Condition” interrupt has not occurred since the last read of this register. 1 = Indicates that the “Change in Receive LOS Condition” interrupt has occurred since the last read of this register.
2-0	Reserved	-	-	

TABLE 82: RXLOS/CRC INTERRUPT ENABLE REGISTER (RLCIER) **HEX ADDRESS: 0XNB13**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
3	RxLOS_ENB	R/W	0	**Change in Receive LOS Condition Interrupt Enable** This bit enables the “Change in Receive LOS Condition” interrupt. 0 = Enables “Change in Receive LOS Condition” Interrupt. 1 = Disables “Change in Receive LOS Condition” Interrupt.
2-0	-	-	-	Reserved

RECEIVE LOOPBACK CODE INTERRUPT AND STATUS REGISTER - CODE 1 (RLCISR1) HEX ADDRESS: 0XNB14

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-4	-	-	-	**Reserved (For E1 mode only)**
3	RXASTAT	RO	0	**Receive Loopback Activation Code State** This READ ONLY bit indicates whether or not the Receive T1 Framer Block is currently detecting the Receive Loopback Activation Code, as specified in the Receive Loopback Activation Code Register (RLACR - address 0xN126) if Receive Loopback Activation Code Detection is enabled. 0 = Indicates that the Receive T1 Framer Block is NOT currently detecting the Receive Loopback Activation Code. 1 = Indicates that the Receive T1 Framer Block is currently detecting the Receive Loopback Activation Code.
2	RXDSTAT	RO	0	**Receive Loopback Deactivation Code State** This READ ONLY bit indicates whether or not the Receive T1 Framer Block is currently detecting the Receive Loopback Deactivation Code, as specified in the Receive Loopback Deactivation Code Register (RLDCR - address 0xN127) if Receive Loopback Deactivation Code Detection is enabled. 0 = Indicates that the Receive T1 Framer Block is NOT currently detecting the Receive Loopback Deactivation Code. 1 = Indicates that the Receive T1 Framer Block is currently detecting the Receive Loopback Deactivation Code.
1	RXAINT	RUR/ WC	0	**Change in Receive Loopback Activation Code interrupt Status** This Reset-Upon-Read bit field indicates whether or not the “Change in Receive Loopback Activation Code” interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive T1 Framer block detects the Receive Loopback Activation Code. **2.** Whenever the Receive T1 Framer block no longer detects the Receive Loopback Activation Code. 0 = Indicates that the “Change in Receive Loopback Activation Code” interrupt has not occurred since the last read of this register 1 = Indicates that the “Change in Receive Loopback Activation Code” interrupt has occurred since the last read of this register
0	RXDINT	RUR/ WC	0	**Change in Receive Loopback Deactivation Code interrupt Status** This Reset-Upon-Read bit field indicates whether or not the “Change in Receive Loopback Deactivation Code” interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive T1 Framer block detects the Receive Loopback Deactivation Code. **2.** Whenever the Receive T1 Framer block no longer detects the Receive Loopback Deactivation Code. 0 = Indicates that the “Change in Receive Loopback Deactivation Code” interrupt has not occurred since the last read of this register 1 = Indicates that the “Change in Receive Loopback Deactivation Code” interrupt has occurred since the last read of this register

TABLE 83: RECEIVE LOOPBACK CODE INTERRUPT ENABLE REGISTER-CODE 1 (RLCIER1)HEX ADDRESS: 0XNB15

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-2	Reserved	-	-	**Reserved**
1	RXAENB	R/W	0	**Receive Loopback Activation Code Interrupt Enable** This bit enables or disables the “Change in Receive Loopback Activation Code” interrupt within the T1 Receive Framer. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive T1 Framer block detects the Receive Loopback Activation Code. **2.** Whenever the Receive T1 Framer block no longer detects the Receive Loopback Activation Code. 0 - Disables the “Change in Receive Loopback Activation Code” interrupt within the T1 Receive Framer. 1 - Enables the “Change in Receive Loopback Activation Code” interrupt within the T1 Receive Framer.
0	RXDENB	R/W	0	**Receive Loopback Deactivation Code Interrupt Enable** This bit enables or disables the “Change in Receive Loopback Deactivation Code” interrupt within the T1 Receive Framer. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive T1 Framer block detects the Receive Loopback Deactivation Code. **2.** Whenever the Receive T1 Framer block no longer detects the Receive Loopback Deactivation Code. 0 - Disables the “Change in Receive Loopback Deactivation Code” interrupt within the T1 Receive Framer. 1 - Enables the “Change in Receive Loopback Deactivation Code” interrupt within the T1 Receive Framer.

RECEIVE LOOPBACK CODE INTERRUPT AND STATUS REGISTER - CODE 2 (RLCISR2) HEX ADDRESS: 0XNB1A

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-4	-	-	-	**Reserved (For E1 mode only)**
3	RXASTAT	RO	0	**Receive Loopback Activation Code State** This READ ONLY bit indicates whether or not the Receive T1 Framer Block is currently detecting the Receive Loopback Activation Code, as specified in the Receive Loopback Activation Code Register (RLACR - address 0xN126) if Receive Loopback Activation Code Detection is enabled. 0 = Indicates that the Receive T1 Framer Block is NOT currently detecting the Receive Loopback Activation Code. 1 = Indicates that the Receive T1 Framer Block is currently detecting the Receive Loopback Activation Code.
2	RXDSTAT	RO	0	**Receive Loopback Deactivation Code State** This READ ONLY bit indicates whether or not the Receive T1 Framer Block is currently detecting the Receive Loopback Deactivation Code, as specified in the Receive Loopback Deactivation Code Register (RLDCR - address 0xN127) if Receive Loopback Deactivation Code Detection is enabled. 0 = Indicates that the Receive T1 Framer Block is NOT currently detecting the Receive Loopback Deactivation Code. 1 = Indicates that the Receive T1 Framer Block is currently detecting the Receive Loopback Deactivation Code.
1	RXAINT	RUR/ WC	0	**Change in Receive Loopback Activation Code interrupt Status** This Reset-Upon-Read bit field indicates whether or not the “Change in Receive Loopback Activation Code” interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive T1 Framer block detects the Receive Loopback Activation Code. **2.** Whenever the Receive T1 Framer block no longer detects the Receive Loopback Activation Code. 0 = Indicates that the “Change in Receive Loopback Activation Code” interrupt has not occurred since the last read of this register 1 = Indicates that the “Change in Receive Loopback Activation Code” interrupt has occurred since the last read of this register
0	RXDINT	RUR/ WC	0	**Change in Receive Loopback Deactivation Code interrupt Status** This Reset-Upon-Read bit field indicates whether or not the “Change in Receive Loopback Deactivation Code” interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive T1 Framer block detects the Receive Loopback Deactivation Code. **2.** Whenever the Receive T1 Framer block no longer detects the Receive Loopback Deactivation Code. 0 = Indicates that the “Change in Receive Loopback Deactivation Code” interrupt has not occurred since the last read of this register 1 = Indicates that the “Change in Receive Loopback Deactivation Code” interrupt has occurred since the last read of this register

TABLE 84: RECEIVE LOOPBACK CODE INTERRUPT ENABLE REGISTER-CODE 2 (RLCIER2)HEX ADDRESS: 0XNB1B

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-2	Reserved	-	-	**Reserved**
1	RXAENB	R/W	0	**Receive Loopback Activation Code Interrupt Enable** This bit enables or disables the "Change in Receive Loopback Activation Code" interrupt within the T1 Receive Framer. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive T1 Framer block detects the Receive Loopback Activation Code. **2.** Whenever the Receive T1 Framer block no longer detects the Receive Loopback Activation Code. 0 - Disables the "Change in Receive Loopback Activation Code" interrupt within the T1 Receive Framer. 1 - Enables the "Change in Receive Loopback Activation Code" interrupt within the T1 Receive Framer.
0	RXDENB	R/W	0	**Receive Loopback Deactivation Code Interrupt Enable** This bit enables or disables the "Change in Receive Loopback Deactivation Code" interrupt within the T1 Receive Framer. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive T1 Framer block detects the Receive Loopback Deactivation Code. **2.** Whenever the Receive T1 Framer block no longer detects the Receive Loopback Deactivation Code. 0 - Disables the "Change in Receive Loopback Deactivation Code" interrupt within the T1 Receive Framer. 1 - Enables the "Change in Receive Loopback Deactivation Code" interrupt within the T1 Receive Framer.

TABLE 85: CUSTOMER INSTALLATION ALARM STATUS REGISTER (CIASR) **HEX ADDRESS: 0XNB40**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
[7:6]	Reserved	-	-	**Reserved**
5	RxAIS-CI_state	RO	0	**Receive Alarm Indication Signal-Customer Installation (AIS-CI) State** This READ ONLY bit field indicates whether or not the Receive T1 Framer is currently detecting the Alarm Indication Signal-Customer Installation (AIS-CI) condition. Alarm Indication Signal-Customer Installation (AIS-CI) is intended for use in a network to differentiate between an issue within the network or the Customer Installation (CI). AIS-CI is an all ones signal with an embedded signature of 01111100 11111111 (right-to left) which recurs at 386 bit intervals in-the DS-1 signal. 0 = Indicates the Receive T1 Framer is currently NOT detecting the AIS-CI condition 1 = Indicates the Receive T1 Framer is currently detecting the AIS-CI condition ***NOTE:*** *This bit only works if AIS-CI detection is enabled (Register 0xN11C)*
4	RxRAI-CI_state	RO	0	**Rx RAI-CI State** This READ ONLY bit field indicates whether or not the Receive T1 Framer is currently declaring the Remote Alarm Indication - Customer Installation (RAI-CI) condition. (This is for T1 ESF framing mode only) Remote Alarm Indication - Customer Installation (RAI-CI) is intended for use in a network to differentiate between an issue within the network or the Customer Installation (CI). RAI-CI is a repetitive pattern with a period of 1.08 seconds. It is comprised of 0.99 seconds of RAI message (00000000 11111111 Right-to-left) and a 90 ms of RAI-CI signature (00111110 11111111 Right to left) to form a RAI-CI signal. 0 = Indicates the Receive T1 Framer is currently NOT detecting the RAI-CI condition 1 = Indicates the Receive T1 Framer is currently detecting the RAI-CI condition ***NOTE:*** *This bit only works if RAI-CI detection is enabled (Register 0xN11C)*
[3:2]	Reserved	-	-	**Reserved**

TABLE 85: CUSTOMER INSTALLATION ALARM STATUS REGISTER (CIASR) **HEX ADDRESS: 0XNB40**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	RxAIS-CI	RUR/ WC	0	**Change in Receive AIS-CI Condition Interrupt Status** This Reset-Upon-Read bit field indicates whether or not the "Change in AIS-CI Condition" interrupt within the T1 Receive Framer Block has occurred since the last read of this register. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive T1 Framer block detects the AIS-CI Condition. **2.** Whenever the Receive T1 Framer block clears the AIS-CI Condition 0 = Indicates the "Change in AIS-CI Condition" interrupt has NOT occurred since the last read of this register 1 = Indicates the "Change in AIS-CI Condition" interrupt has occurred since the last read of this register
0	RxRAI-CI	RUR/ WC	0	**Change in Receive RAI-CI Condition Interrupt Status** This Reset-Upon-Read bit field indicates whether or not the "Change in RAI-CI Condition" interrupt within the T1 Receive Framer Block has occurred since the last read of this register. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive T1 Framer block detects the RAI-CI Condition. **2.** Whenever the Receive T1 Framer block clears the RAI-CI Condition 0 = Indicates the "Change in RAI-CI Condition" interrupt has NOT occurred since the last read of this register 1 = Indicates the "Change in RAI-CI Condition" interrupt has occurred since the last read of this register

TABLE 86: CUSTOMER INSTALLATION ALARM STATUS REGISTER (CIAIER) **HEX ADDRESS: 0XNB41**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	RxAIS-CI_ENB	R/W	0	**Change in Receive AIS-CI Condition Interrupt Enable** This bit enables or disables the "Change in AIS-CI Condition" interrupt within the T1 Receive Framer Block. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive T1 Framer block detects the AIS-CI Condition. **2.** Whenever the Receive T1 Framer block clears the AIS-CI Condition 0 - Disables the "Change in AIS-CI Condition" interrupt. 1 - Enables the "Change in AIS-CI Condition" interrupt.
0	RxRAI-CI_ENB	R/W	0	**Change in Receive RAI-CI Condition Interrupt Enable** This bit enables or disables the "Change in RAI-CI Condition" interrupt within the T1 Receive Framer Block. If this interrupt is enabled, then the Receive T1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive T1 Framer block detects the RAI-CI Condition. **2.** Whenever the Receive T1 Framer block clears the AIS-CI Condition 0 - Disables the "Change in RAI-CI Condition" interrupt. 1 - Enables the "Change in RAI-CI Condition" interrupt.

2.0 LIU GLOBAL CONTROL REGISTERS

TABLE 87: LIU GLOBAL CONTROL REGISTER 0 (ADDRESS = 0X0100)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	ATAOS	Reserved				TCLKCNTL	LIU Software RESET
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - Reserved:

BIT 6 - ATAOS: Automatic Transmit All Ones Upon RLOS Condition

If ATAOS is selected, an all ones pattern will be transmitted on any channel that experiences an RLOS condition. If an RLOS condition does not occur, TAOS will remain inactive.

0 = Disabled

1 = Enabled

Bits [5:2] - Reserved:

BIT 1 - TCLKCNTL

If TCLKCNTL is selected, and if the transmit clock to the DS-1 framer is missing, Low, or High, then the transmitter outputs to the line interface will send an All Ones Signal.

0 = Disabled

1 = Enabled

BIT 0 - LIU Software RESET:

Writing a 1 to this bit for more than 10µS initiates a device reset for all internal circuits except the microprocessor register bits. To reset the registers to their default setting, use the Hardware Reset pin (See the pin description for more details)

0 = Disabled

1 = Enabled

TABLE 88: LIU GLOBAL CONTROL REGISTER 1 (ADDRESS = 0X0101)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LCVB_OF	PLL19_Dis	Reserved	Slicer Level Select [1:0]		RXMUTE	EXLOS	ICT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - Line Code Violation / Counter Overflow Monitor Select

This bit is used to select the monitoring activity between the LCV and the counter overflow status. When the 16-bit LCV counter saturates, the counter overflow condition is activated. By default, the LCV activity is monitored by bit D4 in register 0xN005, where N is equal to the channel number.

} 0 - Monitoring LCV

} 1 - Monitoring the counter overflow status

BIT 6 - PLL 19.44MHz Disable

This bit is used in conjunction with the DS-1/E1 recovered clock to synchronize to a 19.44MHz clock source. If this bit is set High, one of the 28 channel recovered line clocks, or an external line clock and be used to provide this synchronization.

} 0 - Disabled

} 1 - Enabled

BIT 5 - Reserved

BIT [4:3] - Slicer Level Select [1:0]

These bits are to used to select the amplitude level that is used by the receive line interface to determine whether the input data is High or Low.

00 - 50%

01 - 45%

10 - 55%

11 - 68%

BIT 2 - RxMUTE

This bit is used to force the receive DS-1/E1 signals Low to prevent chattering any time that the DS-1/E1 receiver inputs at Rtip/Rring experience an RLOS condition.

} 0 - Disabled

} 1 - Enabled

BIT 1 - EXLOS

The number of zeros required to declare a Digital Loss of Signal is extended to 4,096.

} 0 - Normal RLOS operation

} 1 - EXLOS enabled

BIT 0 - In Circuit Testing

For Internal use only. This bit should be set to Low.

This bit forces all Ingress and Egress signals to be High-Z.

} 0 - Disabled

} 1 - Enabled (Force High-Z)

TABLE 89: LIU GLOBAL CONTROL REGISTER 2 (ADDRESS = 0X0102)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved				CLKSEL[3:0]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:4] - Reserved

BIT [3:0] - Input Clock Selection

These bits are used to select the frequency of the input clock source to the PLL. Any state not listed is reserved.

0000 = 2.048 MHz

0001 = 1.544 MHz

1000 = 4.096 MHz

1001 = 3.088 MHz

1010 = 8.192 MHz

1011 = 6.176 MHz

1100 = 16.384 MHz

1101 = 12.352 MHz

1110 = 2.048 MHz

1111 = 1.544 MHz

TABLE 90: LIU GLOBAL CONTROL REGISTER 3 (ADDRESS = 0X0103)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	DS1/E1 LIU Global Interrupt Status Channel 6	DS1/E1 LIU Global Interrupt Status Channel 5	DS1/E1 LIU Global Interrupt Status Channel 4	DS1/E1 LIU Global Interrupt Status Channel 3	DS1/E1 LIU Global Interrupt Status Channel 2	DS1/E1 LIU Global Interrupt Status Channel 1	DS1/E1 LIU Global Interrupt Status Channel 0
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT 7 - Reserved

BIT [6:0] - Global Channel Interrupt Status - Channels 0 to 6

These RUR bit fields are used to indicate which channel experienced a change in status relative to alarm indications. If a channel experiences a change in alarm status, the associated bit for that channel will be set High. Once this register is read back, these bit fields will automatically return Low.

TABLE 91: LIU GLOBAL CONTROL REGISTER 4 (ADDRESS = 0X0104)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	DS1/E1 LIU Global nterrupt Status Channel 13	DS1/E1 LIU Global nterrupt Status Channel 12	DS1/E1 LIU Global nterrupt Status Channel 11	DS1/E1 LIU Global nterrupt Status Channel 10	DS1/E1 LIU Global nterrupt Status Channel 9	DS1/E1 LIU Global nterrupt Status Channel 8	DS1/E1 LIU Global nterrupt Status Channel 7
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT 7 - Reserved

BIT [6:0] - Global Channel Interrupt Status - Channels 7 to 13

These RUR bit fields are used to indicate which channel experienced a change in status relative to alarm indications. If a channel experiences a change in alarm status, the associated bit for that channel will be set High. Once this register is read back, these bit fields will automatically return Low.

TABLE 92: LIU GLOBAL CONTROL REGISTER 5 (ADDRESS = 0X0105)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	DS1/E1 LIU Global nterrupt Status Channel 20	DS1/E1 LIU Global nterrupt Status Channel 19	DS1/E1 LIU Global nterrupt Status Channel 18	DS1/E1 LIU Global nterrupt Status Channel 17	DS1/E1 LIU Global nterrupt Status Channel 16	DS1/E1 LIU Global nterrupt Status Channel 15	DS1/E1 LIU Global nterrupt Status Channel 14
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT 7 - Reserved

BIT [6:0] - Global Channel Interrupt Status - Channels 14 to 20

These RUR bit fields are used to indicate which channel experienced a change in status relative to alarm indications. If a channel experiences a change in alarm status, the associated bit for that channel will be set High. Once this register is read back, these bit fields will automatically return Low.

TABLE 93: LIU GLOBAL CONTROL REGISTER 6 (ADDRESS = 0X0106)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	DS1/E1 LIU Global Interrupt Status Channel 27	DS1/E1 LIU Global Interrupt Status Channel 26	DS1/E1 LIU Global Interrupt Status Channel 25	DS1/E1 LIU Global Interrupt Status Channel 24	DS1/E1 LIU Global Interrupt Status Channel 23	DS1/E1 LIU Global Interrupt Status Channel 22	DS1/E1 LIU Global Interrupt Status Channel 21
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT 7 - Reserved

BIT [6:0] - Global Channel Interrupt Status - Channels 21 to 27

These RUR bit fields are used to indicate which channel experienced a change in status relative to alarm indications. If a channel experiences a change in alarm status, the associated bit for that channel will be set High. Once this register is read back, these bit fields will automatically return Low.

3.0 T1/E1 LIU CHANNEL CONTROL REGISTERS

- **(N ranges from 0x01 to 0x1C)**

TABLE 94: LIU CHANNEL CONTROL REGISTER 0 (ADDRESS = 0XN000)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PRBS/QRSS	PRBS_Rx_Tx	RXON	EQC[4:0]				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - PRBS/QRSS:

These bits are used to select between QRSS and PRBS. To send the a QRSS or PRBS pattern, the TxTEST[2:0] bits in register 0xN002h must be programmed.

} 0 = QRSS

} 1 = PRBS

BIT6 - PRBS/QRSS Direction Select Rx/Tx:

This bit is used to select which direction is used to send the PRBS/QRSS pattern if enabled within the TxTEST[2:0] bits in register 0xN002h.

} 0 = Line Interface (Ttip/Tring)

} 1 = System Side Interface (Clock/Data)

BIT 5 - RXON Receiver Enable:

This bit is used enable the receiver line interface. By default, the receivers are turned off to support redundancy.

} 0 = Disabled.

} 1 = Enabled.

BIT [4:0] - Equalizer Control and Line Build Out:

These bits are used to select the equalizer control and line build out.

Selection Chart for Equalizer Control and Line Build-Out

EQC[4:0]	T1/E1 MODE RECEIVE SENSITIVITY	TRANSMIT LBO	CABLE	CODING
01000	T1 Short Haul	0 - 133 Ft (0.6dB)	100Ω TP	B8ZS
01001	T1 Short Haul	133 - 266 Ft (1.2dB)	100Ω TP	B8ZS
01010	T1 Short Haul	266 - 399 Ft (1.8dB)	100Ω TP	B8ZS
01011	T1 Short Haul	399 - 533 Ft (2.4dB)	100Ω TP	B8ZS
01100	T1 Short Haul	533 - 655 Ft (3.0dB)	100Ω TP	B8ZS
01101	T1 Short Haul	Arbitrary Pulse	100Ω TP	B8ZS
10000	T1 Short Haul	0dB	100Ω TP	B8ZS
10001	T1 Short Haul	-7.5dB	100Ω TP	B8ZS
10010	T1 Short Haul	-15dB	100Ω TP	B8ZS
10011	T1 Short Haul	-22dB	100Ω TP	B8ZS
11100	E1 Short Haul	ITU G.703	75Ω Coax	HDB3
11101	E1 Short Haul	ITU G.703	120Ω TP	HDB3

TABLE 95: LIU CHANNEL CONTROL REGISTER 1 (ADDRESS = 0XN001)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTSEL	TxTSEL	TERSEL[1:0]		JASEL[1:0]		JABW	FIFOSEL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - RxTSEL:

This bit is used for the receive line interface to select between Internal (automatic line impedance) and External (high impedance) modes.

} 0 = External Impedance

} 1 = Internal Impedance

BIT6 - TxTSEL:

This bit is used for the transmit line interface to select between Internal (automatic line impedance) and External (high impedance) modes.

} 0 = External Impedance

} 1 = Internal Impedance

BIT [5:4] - TERSEL[1:0]:

These bits are used to select the line impedance for internal termination control.

} 00 = 100Ω

} 01 = 110Ω

} 10 = 75Ω

} 11 = 120Ω

BIT [3:2] - JASEL[1:0]:

These bits are used to select which path the Jitter Attenuator is placed.

} 00 = Disabled.

} 01 = Transmit Line Interface Path

} 10 = Receive Line Interface Path

} 11 = Receive Line Interface Path

BIT 1 - Jitter Attenuator Bandwidth:

The jitter bandwidth is a global setting that is applied in both transmit and receive directions.

} 0 = 10 Hz

} 1 = 1.5 Hz

BIT 0 - FIFO Depth Select:

This bit is used to select the depth of the FIFO within both the Receive and Transmit Jitter Attenuators.

} 0 = 32-Bit FIFO

} 1 = 64-Bit FIFO

TABLE 96: LIU CHANNEL CONTROL REGISTER 2 (ADDRESS = 0XN002)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
INVQRSS	TxTEST[2:0]			TXON	LOOP[2:0]		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - Invert QRSS:

INVQRSS is used to invert the transmit QRSS pattern set by the TxTEST[2:0] bits. By default, INVQRSS is disabled and the QRSS will be transmitted with normal polarity.

} 0 = Standard QRSS pattern

} 1 = Inverted QRSS pattern

BIT [6:4] - Tx Test Pattern [2:0]:

These bits are used to select a Test Pattern to be sent to the transmit line interface. If bit 6 in register 0xN000h is set High, then the Test Pattern will be sent out on the receive DS-1/E1 system side.

} 0XX = No Test Pattern

} 100 = Tx QRSS

} 101 = Tx TAOS

} 110 = Reserved

} 111 = Reserved

BIT 3 - TXON Transmitter Enable:

This bit is used enable the transmitter line interface. By default, the transmitters are turned off to support redundancy.

} 0 = Disabled.

} 1 = Enabled.

BIT [2:0] - Loop Back Mode Select [2:0]:

These bits are used to select a loop back mode for diagnostic testing. These bits only represent the loop back modes supported in the LIU section of Voyager. For other loop back mode options, see the register map in other modes of operation.

} 0XX = No Loop Back

} 100 = Dual Loop Back

} 101 = Analog Loop Back

} 110 = Remote Loop Back

} 111 = Digital Loop Back

TABLE 97: LIU CHANNEL CONTROL REGISTER 3 (ADDRESS = 0XN003)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxRES[1:0]		CODES	Reserved	E1ARBIT	INSBPV	INSBER	Reserved
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:6] - Receiver Fixed External Termination:

RxRES[1:0] are used to select the value for a high precision external resistor to improve return loss.

} 00 = None

} 01 = 240Ω

} 10 = 210Ω

} 11 = 150Ω

BIT 5 - CODES Encoding / Decoding Select:

This bit is used to select the type of encoding/decoding the transmitter and receiver will generate/process.

} 0 = HDB3 (E1), B8ZS (T1)

} 1 = AMI Coding

BIT 4 - Reserved:

BIT 3 - E1Arbitrary Pulse Select:

This bit is used to enable the Arbitrary Pulse Generator for shaping the transmit pulse when E1 mode is selected.

} 0 = Disabled (Normal E1 Pulse Shape ITU G.703)

} 1 = Arbitrary Pulse Enabled

BIT 2 - Insert Bipolar Violation:

When this bit transitions from Low to High, a bipolar violation will be inserted in the transmitted data from TPOS, QRSS/ PRBS pattern. The state of this bit will be sampled on the rising edge of TCLK. To ensure proper operation, it is recommended to write a 0 to this bit before writing a 1.

} 0 to 1 Transition = Insert one bipolar violation

BIT 1 - Insert Bit Error:

When this bit transitions from Low to High, a bit error will be inserted in the transmitted QRSS/PRBS pattern. The state of this bit will be sampled on the rising edge of TCLK. To ensure proper operation, it is recommended to write a 0 to this bit before writing a 1.

} 0 to 1 Transition = Insert one bit error

BIT 0 - Reserved:

TABLE 98: LIU CHANNEL CONTROL REGISTER 4 (ADDRESS = 0XN004)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	DMOIE	FLSIE	LCVIE	Reserved	AISDIE	RLOSIE	QRPDIE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - Reserved:

BIT6 - Digital Monitor Output Interrupt Enable:

} 0 = Masks the DMO function

} 1 = Enables interrupt generation for DMO

BIT 5 - FIFO Limit Status Interrupt Enable:

} 0 = Masks the FLS function

} 1 = Enables interrupt generation for FLS

BIT 4 - Line Code Violation Interrupt Enable:

} 0 = Masks the LCV function

} 1 = Enables interrupt generation for LCV

BIT 3 - Reserved:

BIT 2 - Alarm Indication Signal Interrupt Enable:

} 0 = Masks the AIS function

} 1 = Enables interrupt generation for AIS

BIT 1 - Receive Loss of Signal Interrupt Enable:

} 0 = Masks the RLOS function

} 1 = Enables interrupt generation for RLOS

BIT 0 - Quasi Random Pattern Detection Interrupt Enable:

} 0 = Masks the QRPD function

} 1 = Enables interrupt generation for QRPD

TABLE 99: LIU CHANNEL CONTROL REGISTER 5 (ADDRESS = 0XN005)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	DMO	FLS	LCV	Reserved	AISD	RLOS	QRPD
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

BIT6 - Digital Monitor Output:

This bit indicates the DMO activity. An interrupt will not occur unless the DMOIE is set High in register 0xN004h and the global interrupt enable has been set.

} 0 = No Alarm

} 1 = Transmit output driver has failures

BIT 5 - FIFO Limit Status:

This bit indicates whether the RD/WR pointers are within 3-Bits. An interrupt will not occur unless the FLSIE is set High in register 0xN004h and the global interrupt enable has been set.

} 0 = No Alarm

} 1 = RD/WR FIFO pointers are within ±3-Bits

BIT 4 - Line Code Violation:

This bit serves a dual purpose. By default, this bit monitors the line code violation activity. However, if bit 7 in register 0x0101h is set High, this bit monitors the overflow status of the internal LCV counter. An interrupt will not occur unless the LCV/OFIE is set High in register 0xN004h and the global interrupt enable has been set.

} 0 = No Alarm

} 1 = A line code violation, bipolar violation, or excessive zeros has occurred

BIT 3 - Reserved:

BIT 2 - Alarm Indication Signal:

This bit indicates the AIS activity. An interrupt will not occur unless the AISIE is set High in register 0xN004h and the global interrupt enable has been set.

} 0 = No Alarm

} 1 = An all ones signal is detected

BIT 1 - Receive Loss of Signal:

This bit indicates the RLOS activity. An interrupt will not occur unless the RLOSIE is set High in register 0xN004h and the global interrupt enable has been set.

} 0 = No Alarm

} 1 = An RLOS condition is present

BIT 0 - Quasi Random Pattern Detection:

This bit indicates that a QRPD has been detected. An interrupt will not occur unless the QRPDIE is set High in register 0xN004h and the global interrupt enable has been set.

} 0 = No Alarm

} 1 = A QRP is detected

TABLE 100: LIU CHANNEL CONTROL REGISTER 6 (ADDRESS = 0XN006)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	DMOIS	FLSIS	LCVIS	Reserved	AISDIS	RLOSIS	QRPDIS
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

NOTE: *These register bits are Reset Upon Read. They will be set High anytime a change in status occurs. Once these bits are read back, they will automatically be set Low.*

BIT7 - Reserved:

BIT6 - Digital Monitor Output Interrupt Enable:

} 0 = No change

} 1 = Change in status occurred

BIT 5 - FIFO Limit Status Interrupt Enable:

} 0 = No change

} 1 = Change in status occurred

BIT 4 - Line Code Violation Interrupt Enable:

} 0 = No change

} 1 = Change in status occurred

BIT 3 - Reserved:

BIT 2 - Alarm Indication Signal Interrupt Enable:

} 0 = No change

} 1 = Change in status occurred

BIT 1 - Receive Loss of Signal Interrupt Enable:

} 0 = No change

} 1 = Change in status occurred

BIT 0 - Quasi Random Pattern Detection Interrupt Enable:

} 0 = No change

} 1 = Change in status occurred

TABLE 101: LIU CHANNEL CONTROL REGISTER 7 (ADDRESS = 0XN007)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ENROM	Reserved	Reserved	RSTALL	UPDATEALL	HI/LO	UPDATE	RST
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - Enable ROM for LCV Counter:

This bit is used to enable data from an internal LCV counter to be read back.

} 0 = Disabled.

} 1 = Enabled.

BIT [6:5] - Reserved:

BIT 4 - Reset Internal LCV Counters:

This bit is used to reset the Internal LCV counters for this channel to its default state 0000h. This bit must be set High for a minimum of 1mS.

} 0 = Normal Operation

} 1 = Resets LCV Counters

BIT 3 - Update All LCV Counters:

This bit is used to latch the contents of the internal LCV counters for this channel so that the values can be read. When the HI/LO bit is set Low, initiating this update bit places the lower 8 bits of the 16-bit word in register 0xN011h. When the HI/LO bit is set High, initiating this update bit places the upper 8 bits of the 16-bit word in register 0xN010h.

} 0 = Normal Operation

} 1 = Updates LCV Counters

BIT 2 - High Byte / Low Byte Select:

This bit is used to select which byte of the 16-bit LCV value will be placed in the read back registers.

} 0 = Lower Byte LCV[7:0]

} 1 = Upper Byte LCV[15:8]

BIT 1 - Update LCV Counter:

This bit is used to latch the contents of the internal LCV counter for this channel so that the value can be read. When the HI/LO bit is set Low, initiating this update bit places the lower 8 bits of the 16-bit word in register 0xN011h. When the HI/LO bit is set High, initiating this update bit places the upper 8 bits of the 16-bit word in register 0xN010h.

} 0 = Normal Operation

} 1 = Update LCV Counter

BIT 0 - Reset Internal LCV Counter:

This bit is used to reset the Internal LCV for this channel to its default state 0000h. This bit must be set High for a minimum of 1mS.

} 0 = Normal Operation

} 1 = Reset LCV Counter

TABLE 102: LIU CHANNEL CONTROL REGISTER 8 (ADDRESS = 0XN008)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	B6S1	B5S1	B4S1	B3S1	B2S1	B1S1	B0S1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - Reserved:

BIT [6:0] - Arbitrary Pulse Generation Segment 1:

The transmit output pulse is divided into 8 individual segments. This register is used to program the first segment which corresponds to the overshoot of the pulse amplitude. There are four segments for the top portion of the pulse and four segments for the bottom portion of the pulse. Segment number 5 corresponds to the undershoot of the pulse. The MSB of each segment is the sign bit.

- **If Sign Bit (BIT6) =:**

} 0 - Negative Direction

} 1 - Positive Direction

TABLE 103: LIU CHANNEL CONTROL REGISTER 9 (ADDRESS = 0XN009)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	B6S2	B5S2	B4S2	B3S2	B2S2	B1S2	B0S2
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - Reserved:

BIT [6:0] - Arbitrary Pulse Generation Segment 2:

The transmit output pulse is divided into 8 individual segments. This register is used to program the second segment of the pulse amplitude. The MSB of each segment is the sign bit.

- **If Sign Bit (BIT6) =:**

} 0 - Negative Direction

} 1 - Positive Direction

TABLE 104: LIU CHANNEL CONTROL REGISTER 10 (ADDRESS = 0XN00A)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	B6S3	B5S3	B4S3	B3S3	B2S3	B1S3	B0S3
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - Reserved:

BIT [6:0] - Arbitrary Pulse Generation Segment 3:

The transmit output pulse is divided into 8 individual segments. This register is used to program the Third segment of the pulse amplitude. The MSB of each segment is the sign bit.

- **If Sign Bit (BIT6) =:**

} 0 - Negative Direction

} 1 - Positive Direction

TABLE 105: LIU CHANNEL CONTROL REGISTER 11 (ADDRESS = 0XN00B)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	B6S4	B5S4	B4S4	B3S4	B2S4	B1S4	B0S4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - Reserved:

BIT [6:0] - Arbitrary Pulse Generation Segment 4:

The transmit output pulse is divided into 8 individual segments. This register is used to program the Fourth segment of the pulse amplitude. The MSB of each segment is the sign bit.

- **If Sign Bit (BIT6) =:**

} 0 - Negative Direction

} 1 - Positive Direction

TABLE 106: LIU CHANNEL CONTROL REGISTER 12 (ADDRESS = 0XN00C)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	B6S5	B5S5	B4S5	B3S5	B2S5	B1S5	B0S5
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - Reserved:

BIT [6:0] - Arbitrary Pulse Generation Segment 5:

The transmit output pulse is divided into 8 individual segments. This register is used to program the Fifth segment of the pulse amplitude. The MSB of each segment is the sign bit.

- **If Sign Bit (BIT6) =:**

} 0 - Negative Direction

} 1 - Positive Direction

TABLE 107: LIU CHANNEL CONTROL REGISTER 13 (ADDRESS = 0XN00D)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	B6S6	B5S6	B4S6	B3S6	B2S6	B1S6	B0S6
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - Reserved:

BIT [6:0] - Arbitrary Pulse Generation Segment 6:

The transmit output pulse is divided into 8 individual segments. This register is used to program the Sixth segment of the pulse amplitude. The MSB of each segment is the sign bit.

- **If Sign Bit (BIT6) =:**

} 0 - Negative Direction

} 1 - Positive Direction

TABLE 108: LIU CHANNEL CONTROL REGISTER 14 (ADDRESS = 0XN00E)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	B6S7	B5S7	B4S7	B3S7	B2S7	B1S7	B0S7
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - Reserved:

BIT [6:0] - Arbitrary Pulse Generation Segment 7:

The transmit output pulse is divided into 8 individual segments. This register is used to program the Seventh segment of the pulse amplitude. The MSB of each segment is the sign bit.

- **If Sign Bit (BIT6) =:**

} 0 - Negative Direction

} 1 - Positive Direction

TABLE 109: LIU CHANNEL CONTROL REGISTER 15 (ADDRESS = 0XN00F)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	B6S8	B5S8	B4S8	B3S8	B2S8	B1S8	B0S8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - Reserved:

BIT [6:0] - Arbitrary Pulse Generation Segment 8:

The transmit output pulse is divided into 8 individual segments. This register is used to program the Eighth segment of the pulse amplitude. The MSB of each segment is the sign bit.

- **If Sign Bit (BIT6) =:**

} 0 - Negative Direction

} 1 - Positive Direction

TABLE 110: LIU CHANNEL CONTROL REGISTER 16 (ADDRESS = 0XN010)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LCVHI7	LCVHI6	LCVHI5	LCVHI4	LCVHI3	LCVHI2	LCVHI1	LCVHI0
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

BIT [7:0] - Internal LCV Counter High Byte:

Once the internal LCV counter has been enabled and updated, these bits contain the upper byte of the 16-bit LCV counter word.

TABLE 111: LIU CHANNEL CONTROL REGISTER 17 (ADDRESS = 0XN011)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LCVLO7	LCVLO6	LCVLO5	LCVLO4	LCVLO3	LCVLO2	LCVLO1	LCVLO0
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

BIT [7:0] - Internal LCV Counter Low Byte:

Once the internal LCV counter has been enabled and updated, these bits contain the lower byte of the 16-bit LCV counter word.

REVISION HISTORY

REVISION #	DATE	DESCRIPTION
1.0.0	May 2008	Final release datasheet of the XRT86SH328 T1 Framer + LIU Register Description
1.0.1	August 2008	Updated bit register description 0x0101, 0xN001, 0xN003, 0xN129.