

# Accutek Microcircuit Corporation

## AK594096AS / AK594096AG 4,194,304 Word x 9 Bit CMOS Dynamic Random Access Memory

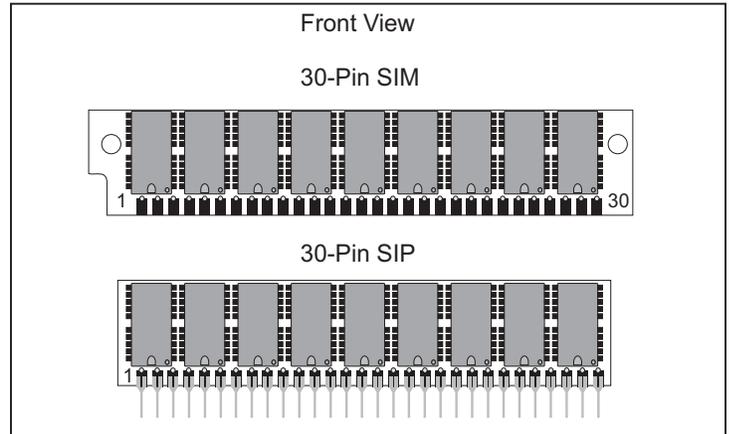
### DESCRIPTION

The Accutek AK594096A high density memory module is a CMOS random access memory organized in 4 Meg x 9 bit words. The assembly consists of nine standard 4 Meg x 1 DRAMs in plastic leaded chip carriers (SOJ) mounted on the front side of a printed circuit board. The module can be configured as a leadless 30 pad SIM or a leaded 30 pin SIP. The module is only 0.800 inches high (same height as a standard 1 Meg module), making it ideally suited for applications with low height restrictions.

The operation of the AK594096A is identical to nine 4 Meg x 1 DRAMs. For the lower eight bits data input is tied to the data output and brought out separately for each device, with common  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$  control. This common I/O feature dictates the use of early-write cycles to prevent contention of D and Q. Since the Write-Enable ( $\overline{\text{WE}}$ ) signal must always go low before  $\overline{\text{CAS}}$  in a write cycle, Read-Write and Read-Modify-Write operation is not possible. For the ninth bit, the data input ( $\text{D}_9$ ) and the data output ( $\text{Q}_9$ ) pins are brought out separately and controlled by a separate  $\overline{\text{PCAS}}$  for that bit. Bit nine is generally used for parity.

### FEATURES

- 4,194,304 x 9 bit organization
- Optional 30 Pad leadless SIM (Single In-Line Module) or 30 Pin leaded SIP (Single In-Line Package)
- JEDEC standard pinout
- Common  $\overline{\text{CAS}}$  and  $\overline{\text{RAS}}$  control for the lower eight bits
- Separate  $\overline{\text{PCAS}}$  for control for  $\text{D}_9$  and  $\text{Q}_9$
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh
- Power
  - 4.45 Watt Max Active (80 nSEC)
  - 3.96 Watt Max Active (100 nSEC)
  - 49.5 mW Max Standby
- Operating free air temperature  $0^\circ\text{C}$  to  $70^\circ\text{C}$
- Upward compatible with AK5916384
- Downward compatible with AK591024, AK59256



### PIN NOMENCLATURE

DQ <sub>1</sub> - DQ <sub>8</sub>	Data In / Data Out
D <sub>9</sub>	Data In 9
Q <sub>9</sub>	Data Out 9
A <sub>0</sub> - A <sub>10</sub>	Address Inputs
$\overline{\text{CAS}}$ , $\overline{\text{PCAS}}$	Column Address Strobe
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{WE}}$	Write Enable
V <sub>cc</sub>	5v Supply
V <sub>ss</sub>	Ground
NC	No Connect

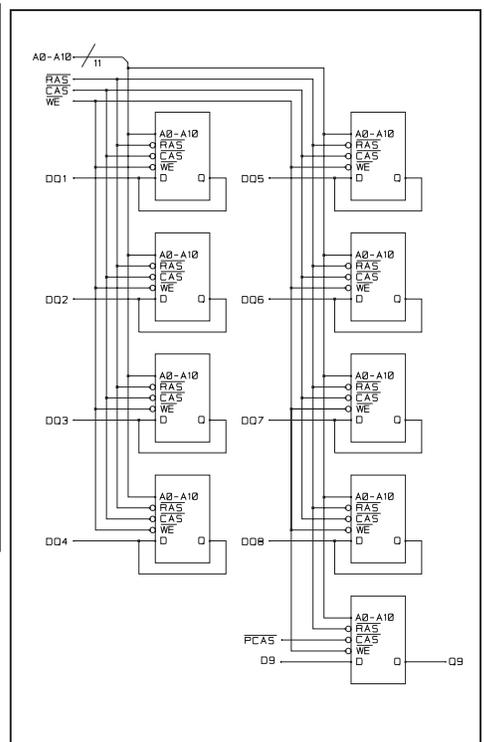
### MODULE OPTIONS

Leadless SIM: AK594096AS
Leaded SIP: AK594096AG

### PIN ASSIGNMENT

PIN #	SYMBOL	PIN #	SYMBOL
1	V <sub>cc</sub>	16	DQ <sub>5</sub>
2	$\overline{\text{CAS}}$	17	A <sub>8</sub>
3	DQ <sub>1</sub>	18	A <sub>9</sub>
4	A <sub>0</sub>	19	A <sub>10</sub>
5	A <sub>1</sub>	20	DQ <sub>6</sub>
6	DQ <sub>2</sub>	21	$\overline{\text{WE}}$
7	A <sub>2</sub>	22	V <sub>ss</sub>
8	A <sub>3</sub>	23	DQ <sub>7</sub>
9	V <sub>ss</sub>	24	NC
10	DQ <sub>3</sub>	25	DQ <sub>8</sub>
11	A <sub>4</sub>	26	Q <sub>9</sub>
12	A <sub>5</sub>	27	$\overline{\text{RAS}}$
13	DQ <sub>4</sub>	28	$\overline{\text{PCAS}}$
14	A <sub>6</sub>	29	D <sub>9</sub>
15	A <sub>7</sub>	30	V <sub>cc</sub>

### FUNCTIONAL DIAGRAM



## ORDERING INFORMATION

### PART NUMBER CODING INTERPRETATION

Position	1	2	3	4	5	6	7	8
<b>1 Product</b>								
	<b>AK = Accuthek Memory</b>							
<b>2 Type</b>								
	4 = Dynamic RAM 5 = CMOS Dynamic RAM 6 = Static RAM							
<b>3 Organization/Word Width</b>								
	1 = by 1    16 = by 16 4 = by 4    32 = by 32 8 = by 8    36 = by 36 9 = by 9							
<b>4 Size/Bits Depth</b>								
	64 = 64K    4096 = 4 MEG 256 = 256K    8192 = 8 MEG 1024 = 1 MEG    16384 = 16 MEG							
<b>5 Package Type</b>								
	G = Single In-Line Package (SIP) S = Single In-Line Module (SIM) D = Dual In-Line Package (DIP) W = .050 inch Pitch Edge Connect Z = Zig-Zag In-Line Package (ZIP)							
<b>6 Special Designation</b>								
	P = Page Mode N = Nibble Mode K = Static Column Mode W = Write Per Bit Mode V = Video Ram							
<b>7 Separator</b>								
	- = Commercial 0°C to +70°C M = Military Equivalent Screened (-55°C to +125°C) I = Industrial Temperature Tested (-45°C to +85°C) X = Burned In							
<b>8 Speed (first two significant digits)</b>								
	DRAMS				SRAMS			
	50 = 50 nS				8 = 8 nS			
	60 = 60 nS				10 = 10 nS			
	70 = 70 nS				12 = 12 nS			
	80 = 80 nS				15 = 15 nS			

The numbers and coding on this page do not include all variations available but are show as examples of the most widely used variations. Contact Accuthek if other information is required.

### EXAMPLES:

#### AK594096ASP-80

4 Meg x 9, 80 nSEC DRAM 30 pin SIM Configuration, Page Mode

#### AK594096AGP-70

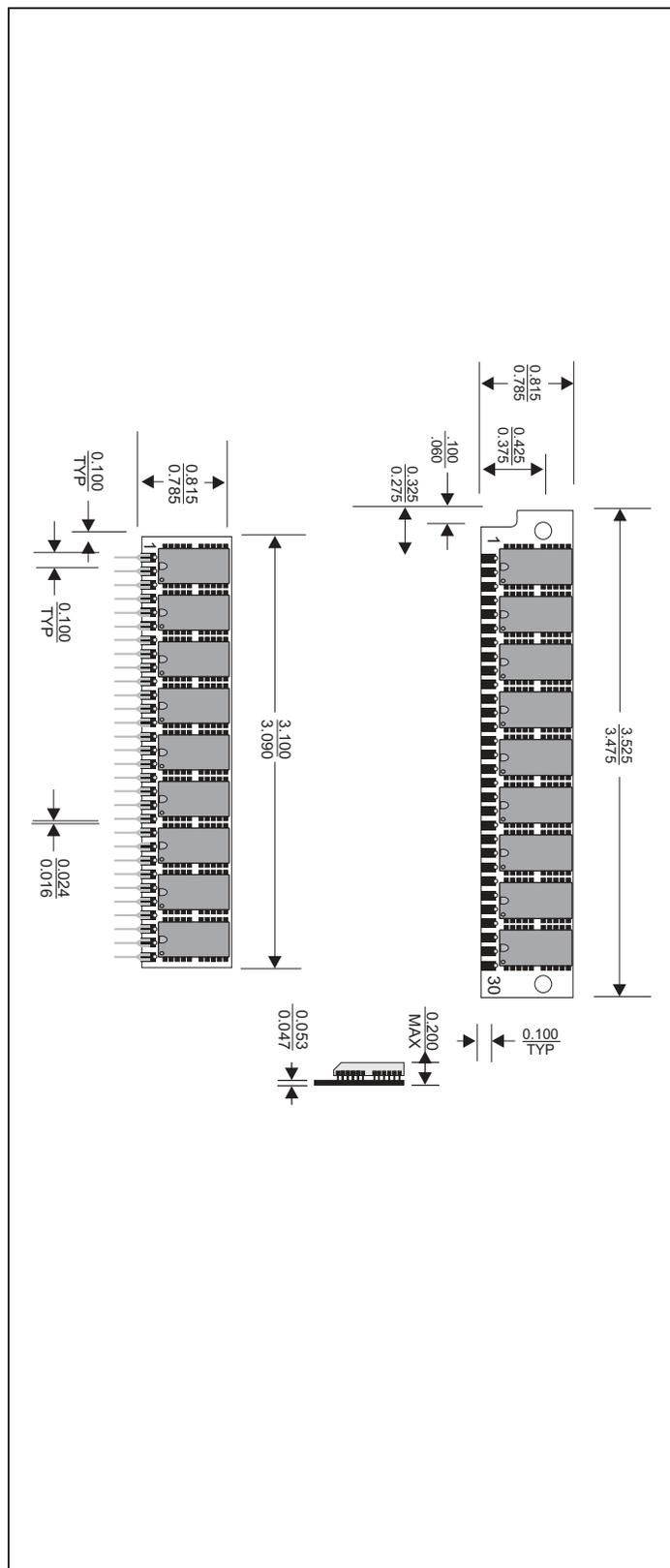
4 Meg x 9, 70 nSEC Dram 30 pin SIP Configuration, Page Mode



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## MECHANICAL DIMENSIONS

Inches



Accuthek reserves the right to make changes in specifications at any time and without notice. Accuthek does not assume any responsibility for the use of any circuitry described; no circuit patent licenses are implied. Preliminary data sheets contain minimum and maximum limits based upon design objectives, which are subject to change upon full characterization over the specific operating conditions.