



# 4-/6-/8-Channel, 16-Bit, Simultaneous-Sampling ADCs

## General Description

The MAX11047/MAX11048/MAX11049 16-bit ADCs offer 4, 6, or 8 independent input channels. Featuring independent track and hold (T/H) and SAR circuitry, these parts provide simultaneous sampling at 250ksps for each channel.

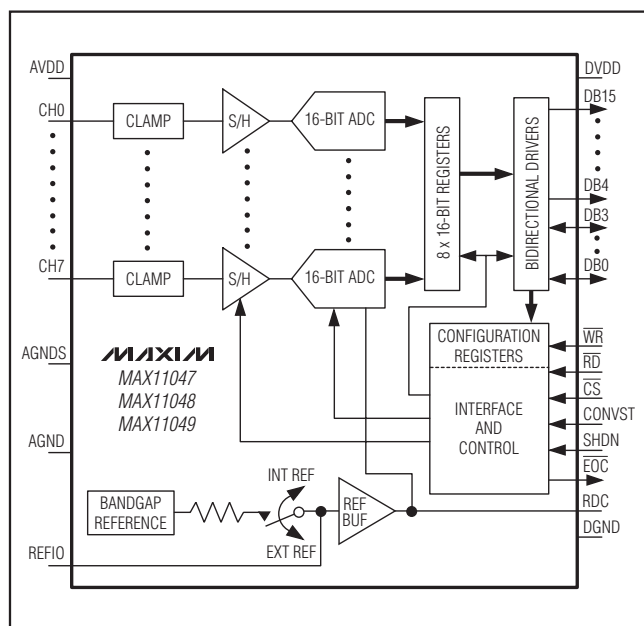
The MAX11047/MAX11048/MAX11049 accept a 0 to +5V input. All inputs are overrange protected with internal  $\pm 20\text{mA}$  input clamps providing overrange protection with a simple external resistor. Other features include a 4MHz T/H input bandwidth, internal clock, and internal or external reference. A 20MHz, 16-bit, bidirectional, parallel interface provides the conversion results and accepts digital configuration inputs.

The MAX11047/MAX11048/MAX11049 operate with a 4.75V to 5.25V analog supply and a separate flexible 2.7V to 5.25V digital supply for interfacing with the host without a level shifter. The MAX11047/MAX11048/MAX11049 are available in a 56-pin TQFN package and operate over the extended  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$  temperature range.

## Applications

- Automatic Test Equipment
- Power-Factor Monitoring and Correction
- Power-Grid Protection
- Multiphase Motor Control
- Vibration and Waveform Analysis

## Functional Diagram



## Features

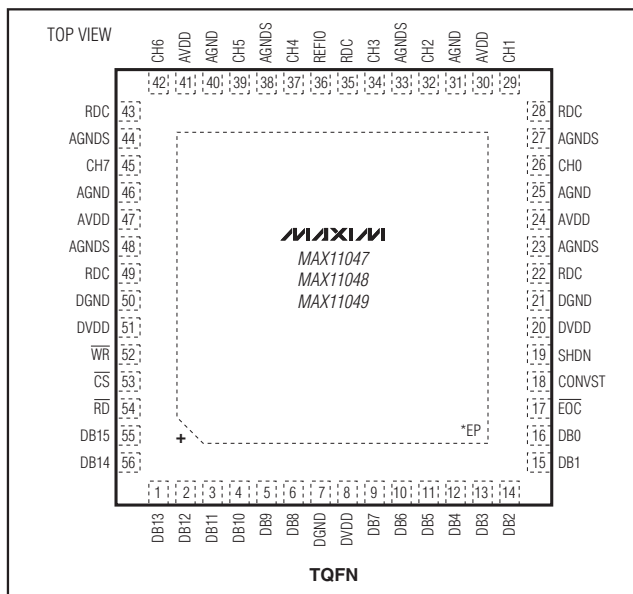
- ◆ 4-/6-/8-Channel 16-Bit ADC
- ◆ Single Analog and Digital Supply
- ◆ High-Impedance Inputs Up to  $1\text{G}\Omega$
- ◆ On-Chip T/H Circuit for Each Channel
- ◆ Fast  $3\mu\text{s}$  Conversion Time
- ◆ High Throughput: 250ksps for All 8 Channels
- ◆ 16-Bit, High-Speed, Parallel Interface
- ◆ Internal Clocked Conversions
- ◆ 10ns Aperture Delay
- ◆ 100ps Channel-to-Channel T/H Matching
- ◆ Low Drift, Accurate 4.096V Internal Reference Providing an Input Range of 0 to 5V
- ◆ External Reference Range of 3.0V to 4.25V, Allowing Full-Scale Input Ranges of  $+3.7\text{V}$  to  $+5.2\text{V}$
- ◆ 56-Pin TQFN Package (8mm x 8mm)
- ◆ Evaluation Kit Available

## Ordering Information

PART	PIN-PACKAGE	CHANNELS
MAX11047ETN+	56 TQFN-EP*	4
MAX11048ETN+	56 TQFN-EP*	6
MAX11049ETN+	56 TQFN-EP*	8

**Note:** All devices are specified over the  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$  operating temperature range.  
 +Denotes a lead(Pb)-free/RoHS-compliant package.  
 \*EP = Exposed pad.

## Pin Configuration



MAX11047/MAX11048/MAX11049



# 4-/6-/8-Channel, 16-Bit, Simultaneous-Sampling ADCs

## ABSOLUTE MAXIMUM RATINGS

AVDD to AGND .....	-0.3V to +6V
DVDD to AGND and DGND .....	-0.3V to +6V
DGND to AGND.....	-0.3V to +0.3V
AGNDS to AGND.....	-0.3V to +0.3V
CH0-CH7 to AGND .....	-2.5V to +7.5V
REFIO, RDC to AGND .....	-0.3V to the lower of (AVDD + 0.3V) and +6V
$\overline{EOC}$ , $\overline{WR}$ , $\overline{RD}$ , $\overline{CS}$ , CONVST to AGND.....	-0.3V to the lower of (DVDD + 0.3V) and +6V

DB0-DB15 to AGND .....	-0.3V to the lower of (DVDD + 0.3V) and +6V
Maximum Current into Any Pin Except AVDD, DVDD, AGND, DGND .....	±50mA
Continuous Power Dissipation ( $T_A = +70^\circ\text{C}$ )	
56-Pin TQFN (derated 36mW/°C above +70°C) .....	2222mW
Operating Temperature Range .....	-40°C to +85°C
Junction Temperature .....	+150°C
Storage Temperature Range .....	-65°C to +150°C
Lead Temperature (soldering, 10s) .....	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(AVDD = 4.75V to 5.25V, DVDD = +2.7V to 5.25V,  $V_{AGNDS} = V_{AGND} = V_{DGND} = 0\text{V}$ ,  $V_{REFIO}$  = internal reference,  $C_{RDC} = 4 \times 33\mu\text{F}$ ,  $C_{REFIO} = 0.1\mu\text{F}$ ,  $C_{AVDD} = 4 \times 0.1\mu\text{F} \parallel 10\mu\text{F}$ ,  $C_{DVDD} = 3 \times 0.1\mu\text{F} \parallel 10\mu\text{F}$ ; all digital inputs at DVDD or DGND, unless otherwise noted.  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ\text{C}$ .)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>STATIC PERFORMANCE (Note 1)</b>						
Resolution	N		16			Bits
Integral Nonlinearity	INL	(Note 2)	-2	±0.6	+2	LSB
Integral Nonlinearity	INL	(Note 3)		±0.8		LSB
Differential Nonlinearity	DNL	(Note 2)	> -1	±0.6	< +1.3	LSB
Differential Nonlinearity	DNL	(Note 3)		±0.7		LSB
No Missing Codes			16			Bits
Offset Error				±0.002	±0.01	%FSR
Offset Temperature Coefficient				±2.4		μV/°C
Channel Offset Matching					±0.01	%FSR
Gain Error					±0.03	%FSR
Positive Full-Scale Error					±0.02	%FSR
Positive Full-Scale Error Matching					±0.02	%FSR
Channel Gain-Error Matching		Between all channels			±0.03	%FSR
Gain Temperature Coefficient				±0.8		ppm/°C
<b>DYNAMIC PERFORMANCE (Note 4)</b>						
Signal-to-Noise Ratio	SNR	$f_{IN} = 10\text{kHz}$ , full-scale input	91	92.3		dB
Signal-to-Noise and Distortion Ratio	SINAD	$f_{IN} = 10\text{kHz}$ , full-scale input	90.5	92		dB
Spurious-Free Dynamic Range	SFDR	$f_{IN} = 10\text{kHz}$ , full-scale input	95	106		dB
Total Harmonic Distortion	THD	$f_{IN} = 10\text{kHz}$ , full-scale input		-105	-95	dB
Channel-to-Channel Crosstalk		$f_{IN} = 60\text{Hz}$ , full scale and ground on adjacent channel (Note 5)		-126	-100	dB
<b>ANALOG INPUTS (CH0-CH7)</b>						
Input Voltage Range		(Note 6)	0		1.22 x $V_{REFIO}$	V
Input Leakage Current			-1		+1	μA

# 4-/6-/8-Channel, 16-Bit, Simultaneous-Sampling ADCs

MAX11047/MAX11048/MAX11049

## ELECTRICAL CHARACTERISTICS (continued)

(AVDD = 4.75V to 5.25V, DVDD = +2.7V to 5.25V, VAGNDS = VAGND = VDGND = 0V, VREFIO = internal reference, CRDC = 4 x 33μF, CREFIO = 0.1μF, CAVDD = 4 x 0.1μF || 10μF, CDVDD = 3 x 0.1μF || 10μF; all digital inputs at DVDD or DGND, unless otherwise noted. TA = -40°C to +85°C, unless otherwise noted. Typical values are at TA = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance				15		pF
Input-Clamp Protection Current		Each input simultaneously	-20		+20	mA
<b>TRACK AND HOLD</b>						
Throughput Rate		Per channel, 8 channels in 4μs			250	ksps
Acquisition Time	tACQ		1			μs
Full-Power Bandwidth		-3dB point		4		MHz
		-0.1dB point		> 0.2		
Aperture Delay				10		ns
Aperture-Delay Matching				100		ps
Aperture Jitter				50		psRMS
<b>INTERNAL REFERENCE</b>						
REFIO Voltage	VREF		4.073	4.096	4.119	V
REFIO Temperature Coefficient				±5		ppm/°C
<b>EXTERNAL REFERENCE</b>						
Input Current			-10		+10	μA
REF Voltage Input Range	VREF		3.00		4.25	V
REF Input Capacitance				15		pF
<b>DIGITAL INPUTS (DB0–DB15, RD, WR, CS, CONVST)</b>						
Input-Voltage High	VIH	VDVDD = 2.7V to 5.25V	2			V
Input-Voltage Low	VIL	VDVDD = 2.7V to 5.25V			0.8	V
Input Capacitance	CIN			10		pF
Input Current	IIN	VIN = 0 or VDVDD			±10	μA
<b>DIGITAL OUTPUTS (DB0–DB15, EOC)</b>						
Output-Voltage High	VOH	ISOURCE = 1.2mA			VDVDD - 0.4	V
Output-Voltage Low	VOL	ISINK = 1mA			0.4	V
Three-State Leakage Current		DB0–DB15, VRD ≥ VIH or VCS ≥ VIH			10	μA
Three-State Output Capacitance		DB0–DB15, VRD ≥ VIH or VCS ≥ VIH		15		pF
<b>POWER SUPPLIES (MAX11047)</b>						
Analog Supply Voltage	AVDD		4.75		5.25	V
Digital Supply Voltage	DVDD		2.70		5.25	V
Analog Supply Current	I <sub>AVDD</sub>				32	mA
Digital Supply Current	I <sub>DVDD</sub>	VDVDD = 3.3V (Note 7)			5.7	mA
Shutdown Current		For DVDD			10	μA
Shutdown Current		For AVDD			12	μA
Power-Supply Rejection Ratio	PSRR	V <sub>AVDD</sub> = 4.9V to 5.1V (Note 8)		±0.5		LSB

# 4-/6-/8-Channel, 16-Bit, Simultaneous-Sampling ADCs

## ELECTRICAL CHARACTERISTICS (continued)

(AVDD = 4.75V to 5.25V, DVDD = +2.7V to 5.25V, V<sub>AGNDS</sub> = V<sub>AGND</sub> = V<sub>DGND</sub> = 0V, V<sub>REFIO</sub> = internal reference, C<sub>RDC</sub> = 4 x 33μF, C<sub>REFIO</sub> = 0.1μF, C<sub>AVDD</sub> = 4 x 0.1μF || 10μF, C<sub>DVDD</sub> = 3 x 0.1μF || 10μF; all digital inputs at DVDD or DGND, unless otherwise noted. T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>POWER SUPPLIES (MAX11048)</b>						
Analog Supply Voltage	AVDD		4.75		5.25	V
Digital Supply Voltage	DVDD		2.70		5.25	V
Analog Supply Current	I <sub>AVDD</sub>				36	mA
Digital Supply Current	I <sub>DVDD</sub>	V <sub>DVDD</sub> = 3.3V (Note 7)			6.5	mA
Shutdown Current		For DVDD			10	μA
Shutdown Current		For AVDD			12	μA
Power-Supply Rejection Ratio	PSRR	V <sub>AVDD</sub> = 4.9V to 5.1V (Note 8)		±0.5		LSB
<b>POWER SUPPLIES (MAX11049)</b>						
Analog Supply Voltage	AVDD		4.75		5.25	V
Digital Supply Voltage	DVDD		2.70		5.25	V
Analog Supply Current	I <sub>AVDD</sub>				40	mA
Digital Supply Current	I <sub>DVDD</sub>	V <sub>DVDD</sub> = 3.3V (Note 7)			7.3	mA
Shutdown Current		For DVDD			10	μA
Shutdown Current		For AVDD			12	μA
Power-Supply Rejection Ratio	PSRR	V <sub>AVDD</sub> = 4.9V to 5.1V (Note 8)		±0.5		LSB
<b>TIMING CHARACTERISTICS (Note 7)</b>						
CONVST Rise to $\overline{\text{EOC}}$ Fall	t <sub>CON</sub>	Conversion time (Note 9)			3	μs
Acquisition Time	t <sub>ACQ</sub>		1			μs
$\overline{\text{CS}}$ Rise to CONVST Rise	t <sub>Q</sub>	Sample quiet time (Note 9)	500			ns
CONVST Rise to $\overline{\text{EOC}}$ Rise	t <sub>0</sub>			65	140	ns
$\overline{\text{EOC}}$ Fall to CONVST Fall	t <sub>1</sub>	CONVST mode B0 = 0 only (Note 10)	0			ns
CONVST Low Time	t <sub>2</sub>	CONVST mode B0 = 1 only	20			ns
$\overline{\text{CS}}$ Fall to $\overline{\text{WR}}$ Fall	t <sub>3</sub>		0			ns
$\overline{\text{WR}}$ Low Time	t <sub>4</sub>		20			ns
$\overline{\text{CS}}$ Rise to $\overline{\text{WR}}$ Rise	t <sub>5</sub>		0			ns
Input Data Setup Time	t <sub>6</sub>		10			ns
Input Data Hold Time	t <sub>7</sub>		0			ns
$\overline{\text{CS}}$ Fall to $\overline{\text{RD}}$ Fall	t <sub>8</sub>		0			ns
$\overline{\text{RD}}$ Low Time	t <sub>9</sub>		30			ns
$\overline{\text{RD}}$ Rise to $\overline{\text{CS}}$ Rise	t <sub>10</sub>		0			ns
$\overline{\text{RD}}$ High Time	t <sub>11</sub>		10			ns
$\overline{\text{RD}}$ Fall to Data Valid	t <sub>12</sub>				35	ns
$\overline{\text{RD}}$ Rise to Data Hold Time	t <sub>13</sub>	(Note 10)	5			ns

# 4-/6-/8-Channel, 16-Bit, Simultaneous-Sampling ADCs

## ELECTRICAL CHARACTERISTICS (continued)

(AVDD = 4.75V to 5.25V, DVDD = +2.7V to 5.25V, VAGNDS = VAGND = VDGND = 0V, VREFIO = internal reference, CRDC = 4 x 33μF, CREFIO = 0.1μF, CAVDD = 4 x 0.1μF || 10μF, CDVDD = 3 x 0.1μF || 10μF; all digital inputs at DVDD or DGND, unless otherwise noted. TA = -40°C to +85°C, unless otherwise noted. Typical values are at TA = +25°C.)

**Note 1:** See the *Definitions* section at the end of the data sheet.

**Note 2:** Guaranteed at 5V ≤ AVDD ≤ 5.25V for +25°C ≤ TA ≤ +85°C. See the *Input Range and Protection* section and *Typical Operating Characteristics*.

**Note 3:** TA = -40°C.

**Note 4:** Dynamic performance is guaranteed at AVDD = 5.0V to 5.25V. See the *Input Range and Protection* section and the *Typical Operating Characteristics*.

**Note 5:** Tested with alternating channels modulated at full scale and ground.

**Note 6:** See the *Input Range and Protection* section.

**Note 7:** CLOAD = 30pF on DB0–DB15 and  $\overline{EOC}$ . Inputs (CH0–CH7) alternate between full scale and zero scale. fCONV = 250kps. All data is read out.

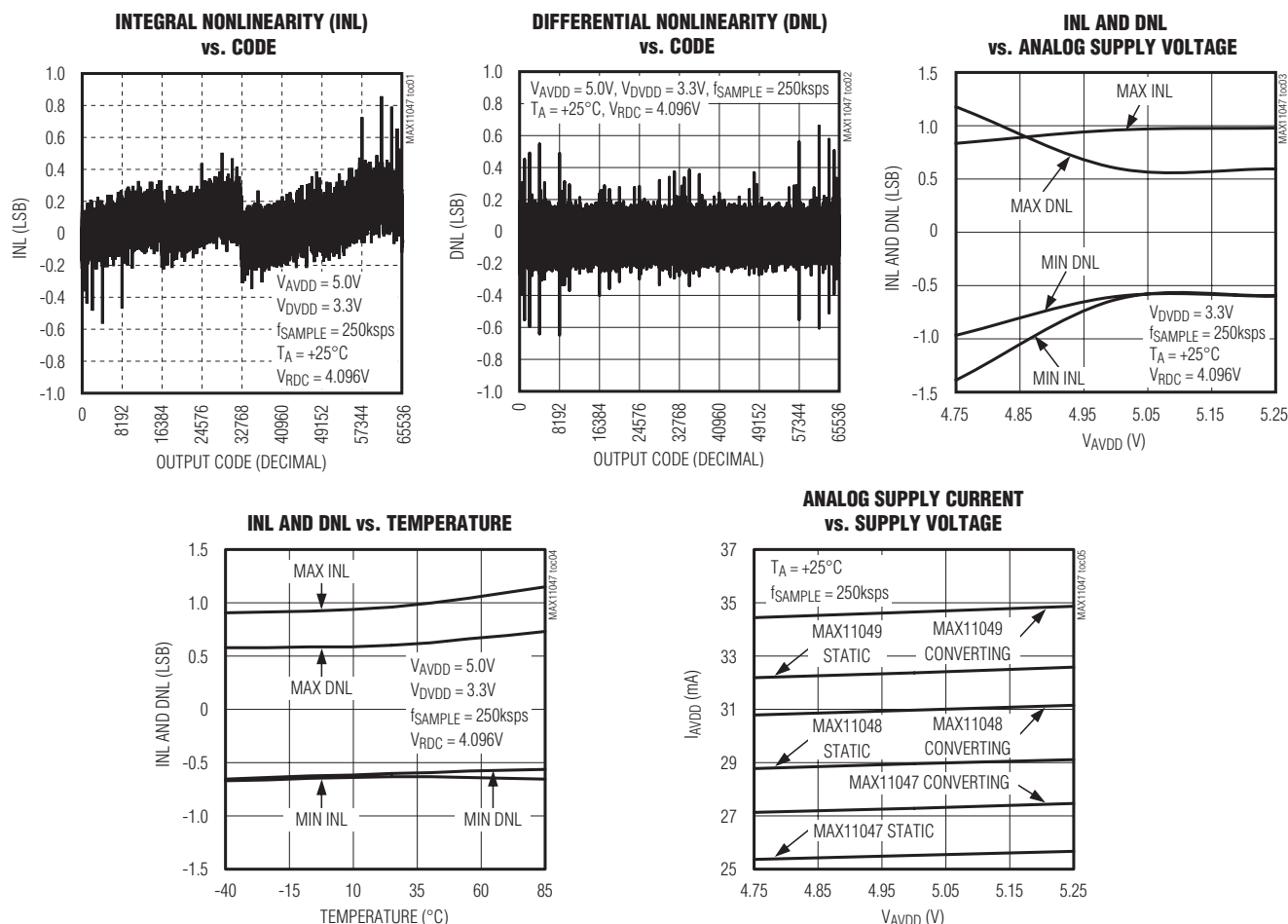
**Note 8:** Defined as the change in positive full scale caused by a ±2% variation in the nominal supply voltage.

**Note 9:** It is recommended that  $\overline{RD}$ ,  $\overline{WR}$ , and  $\overline{CS}$  are kept high for the quiet time (tQ) and conversion time (tCON).

**Note 10:** Guaranteed by design.

## Typical Operating Characteristics

(AVDD = 5V, DVDD = 3.3V, TA = +25°C, fSAMPLE = 250kps, internal reference, unless otherwise noted.)

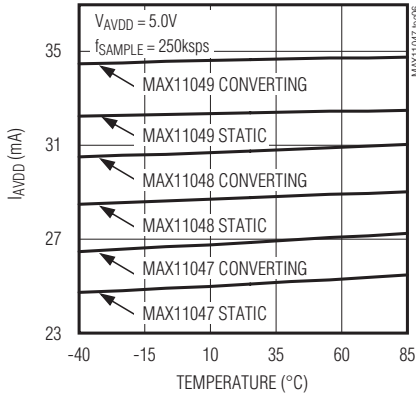


# 4-/6-/8-Channel, 16-Bit, Simultaneous-Sampling ADCs

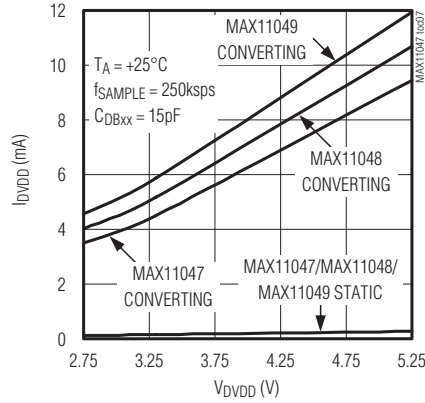
## Typical Operating Characteristics (continued)

(AVDD = 5V, DVDD = 3.3V, TA = +25°C, fSAMPLE = 250ksp/s, internal reference, unless otherwise noted.)

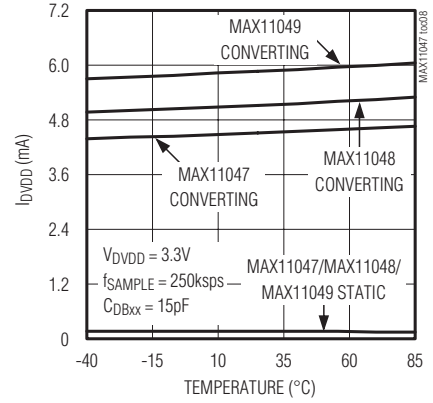
**ANALOG SUPPLY CURRENT vs. TEMPERATURE**



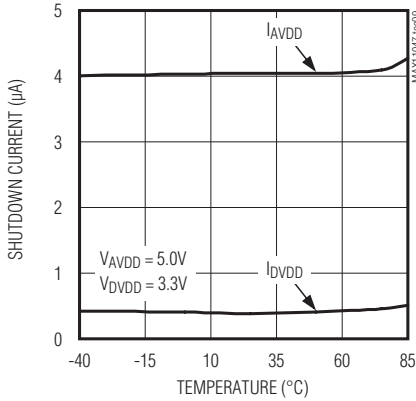
**DIGITAL SUPPLY CURRENT vs. SUPPLY VOLTAGE**



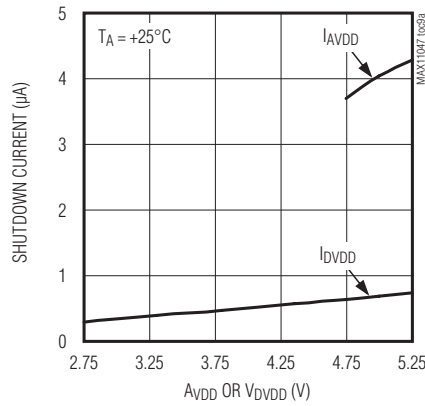
**DIGITAL SUPPLY CURRENT vs. TEMPERATURE**



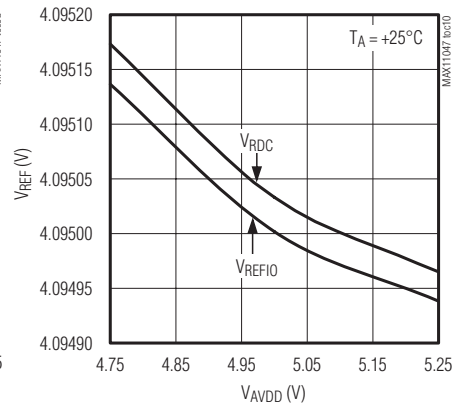
**ANALOG AND DIGITAL SHUTDOWN CURRENT vs. TEMPERATURE**



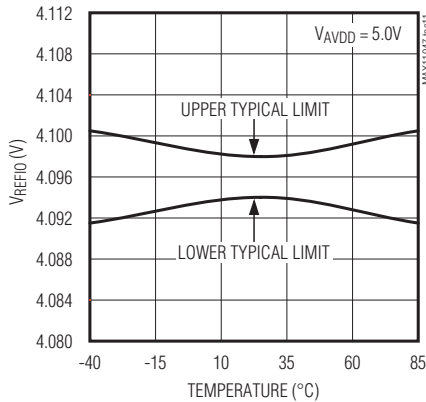
**ANALOG AND DIGITAL SHUTDOWN CURRENT vs. SUPPLY VOLTAGE**



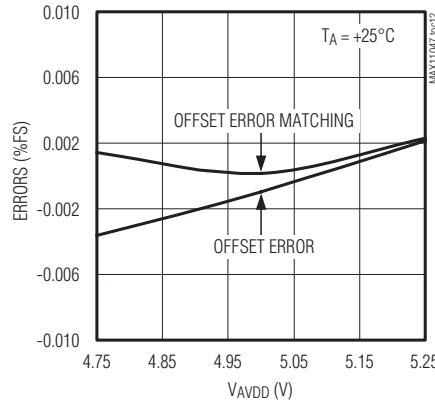
**INTERNAL REFERENCE VOLTAGES vs. SUPPLY VOLTAGE**



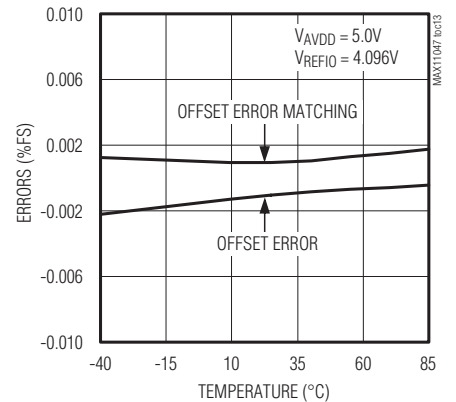
**INTERNAL REFERENCE VOLTAGE vs. TEMPERATURE**



**OFFSET ERROR AND OFFSET ERROR MATCHING vs. SUPPLY VOLTAGE**



**OFFSET ERROR AND OFFSET ERROR MATCHING vs. TEMPERATURE**



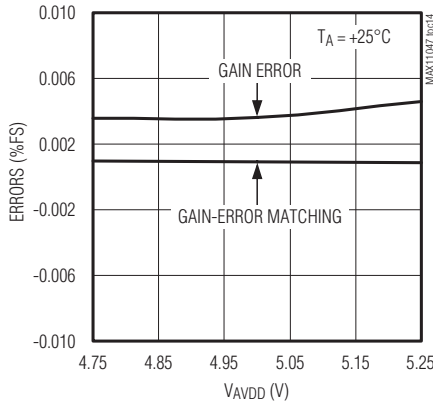
# 4-/6-/8-Channel, 16-Bit, Simultaneous-Sampling ADCs

## Typical Operating Characteristics (continued)

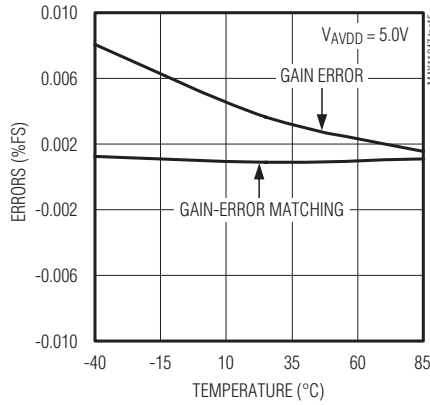
(AVDD = 5V, DVDD = 3.3V, TA = +25°C, fSAMPLE = 250ksps, internal reference, unless otherwise noted.)

MAX11047/MAX11048/MAX11049

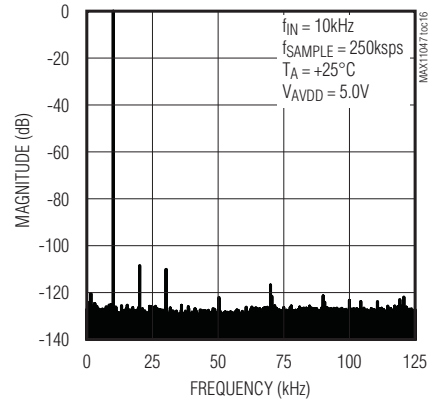
**GAIN ERROR AND GAIN ERROR MATCHING vs. SUPPLY VOLTAGE**



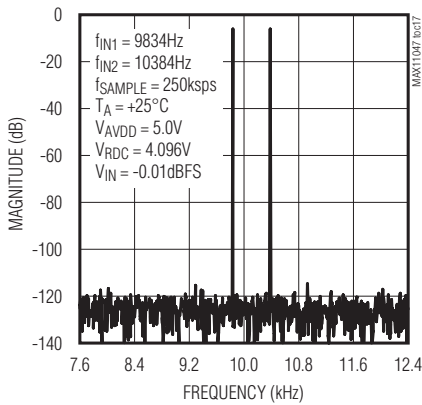
**GAIN ERROR AND GAIN ERROR MATCHING vs. TEMPERATURE**



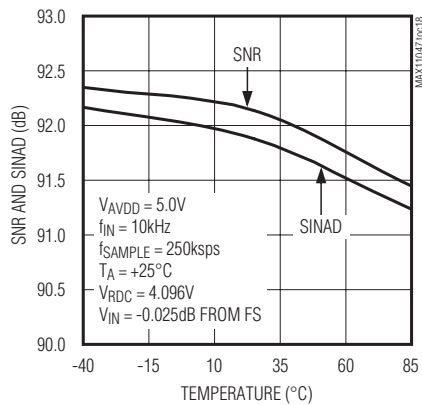
**FFT PLOT**



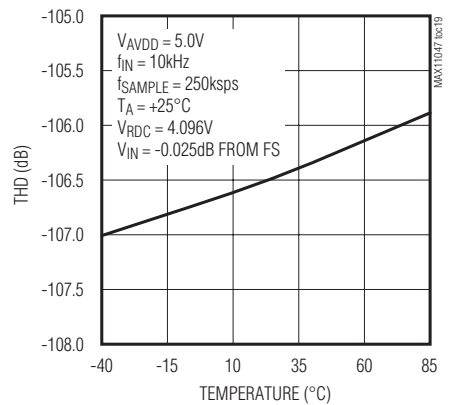
**TWO-TONE IMD PLOT**



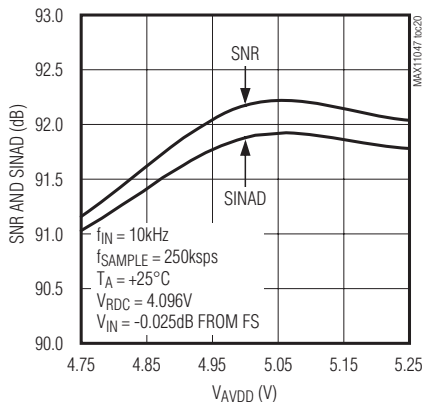
**SIGNAL-TO-NOISE RATIO (SNR) AND SIGNAL-TO-NOISE AND DISTORTION RATIO (SINAD) vs. TEMPERATURE**



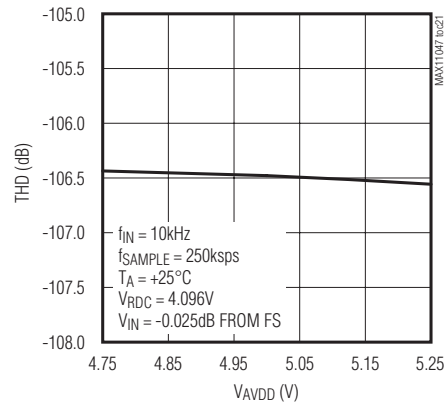
**TOTAL HARMONIC DISTORTION vs. TEMPERATURE**



**SNR AND SINAD vs. ANALOG SUPPLY VOLTAGE**



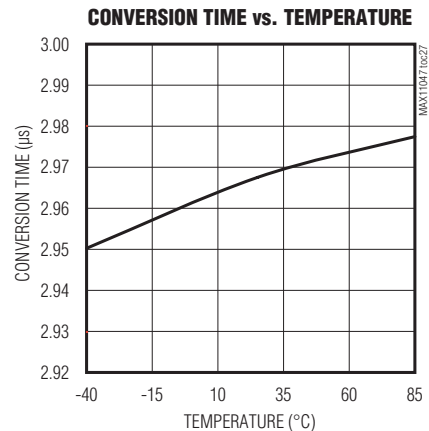
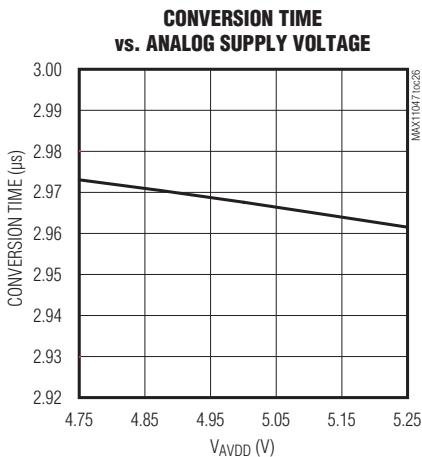
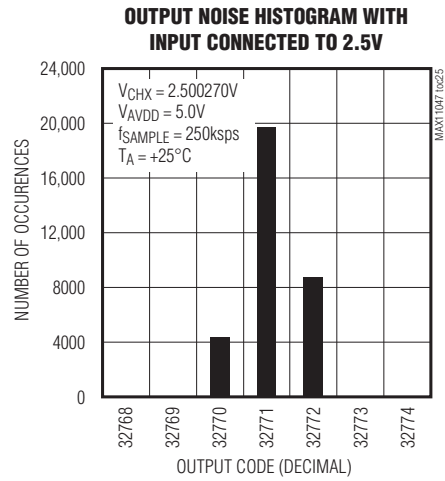
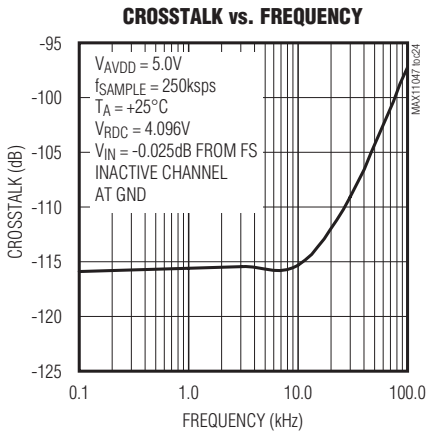
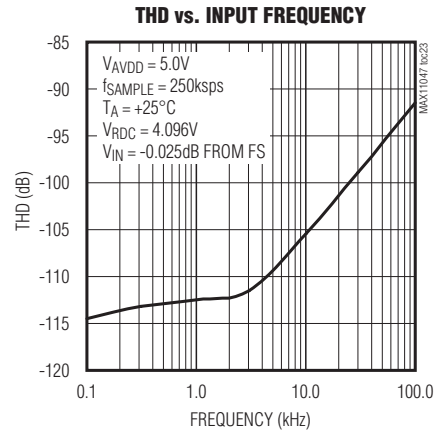
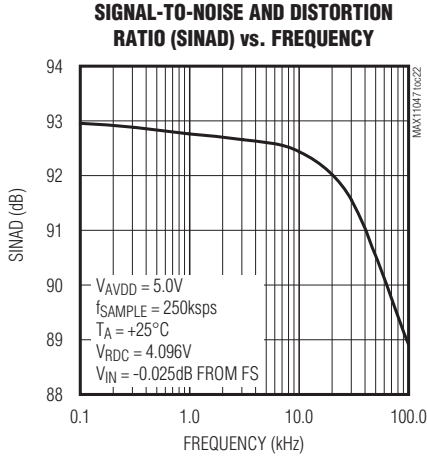
**THD vs. ANALOG SUPPLY VOLTAGE**



# 4-/6-/8-Channel, 16-Bit, Simultaneous-Sampling ADCs

## Typical Operating Characteristics (continued)

(AVDD = 5V, DVDD = 3.3V, TA = +25°C, fSAMPLE = 250kps, internal reference, unless otherwise noted.)





# 4-/6-/8-Channel, 16-Bit, Simultaneous-Sampling ADCs

## Pin Description

MAX11047/MAX11048/MAX11049

PIN	NAME	FUNCTION
1	DB13	16-Bit Parallel Data Bus Digital Output Bit 13
2	DB12	16-Bit Parallel Data Bus Digital Output Bit 12
3	DB11	16-Bit Parallel Data Bus Digital Output Bit 11
4	DB10	16-Bit Parallel Data Bus Digital Output Bit 10
5	DB9	16-Bit Parallel Data Bus Digital Output Bit 9
6	DB8	16-Bit Parallel Data Bus Digital Output Bit 8
7, 21, 50	DGND	Digital Ground
8, 20, 51	DVDD	Digital Supply. Bypass to DGND with a 0.1µF capacitor at each DVDD input.
9	DB7	16-Bit Parallel Data Bus Digital Output Bit 7
10	DB6	16-Bit Parallel Data Bus Digital Output Bit 6
11	DB5	16-Bit Parallel Data Bus Digital Output Bit 5
12	DB4	16-Bit Parallel Data Bus Digital Output Bit 4
13	DB3	16-Bit Parallel Data Bus Digital I/O Bit 3
14	DB2	16-Bit Parallel Data Bus Digital I/O Bit 2
15	DB1	16-Bit Parallel Data Bus Digital I/O Bit 1
16	DB0	16-Bit Parallel Data Bus Digital I/O Bit 0
17	$\overline{\text{EOC}}$	Active-Low, End-of-Conversion Output. $\overline{\text{EOC}}$ goes low when a conversion is completed. $\overline{\text{EOC}}$ goes high when a conversion is initiated.
18	CONVST	Convert Start Input. The rising edge of CONVST ends sample and starts a conversion on the captured sample. The ADC is in acquisition mode when CONVST is low and CONVST mode is zero.
19	SHDN	Active-High Shutdown Input. Drive the SHDN high to place the device into a low-current state. In shutdown mode, the contents of the configuration register are not lost.
22, 28, 35, 43, 49	RDC	Reference Buffer Decoupling. Bypass to AGND with at least a 22µF capacitor each at pins 22, 28, 43, and 49. Connect all RDC outputs together and bypass with 80µF total capacitance. See the <i>Layout, Grounding, and Bypassing</i> section.
23, 27, 33, 38, 44, 48	AGNDS	Signal Ground. Connect all AGND and AGNDS inputs together.
24, 30, 41, 47	AVDD	Analog Supply Input. Bypass AVDD to AGND with a 0.1µF capacitor at each AVDD input.
25, 31, 40, 46	AGND	Analog Ground. Connect all AGND inputs together.
26	CH0	Channel 0 Analog Input for the MAX11049
29	CH1	Channel 1 Analog Input for the MAX11049. Channel 0 for the MAX11048.
32	CH2	Channel 2 Analog Input for MAX11049. Channel 1 for the MAX11048, Channel 0 for the MAX11047.
34	CH3	Channel 3 Analog Input for MAX11049. Channel 2 for the MAX11048, Channel 1 for the MAX11047.
36	REFIO	External Reference Input/Internal Reference Output. Place a 0.1µF capacitor from REFIO to AGND.
37	CH4	Channel 4 Analog Input for the MAX11049. Channel 3 for the MAX11048, Channel 2 for the MAX11047.
39	CH5	Channel 5 Analog Input for the MAX11049. Channel 4 for the MAX11048, Channel 3 for the MAX11047.

# 4-/6-/8-Channel, 16-Bit, Simultaneous-Sampling ADCs

## Pin Description (continued)

PIN	NAME	FUNCTION
42	CH6	Channel 6 Analog Input for MAX11049. Channel 5 for MAX11048.
45	CH7	Channel 7 Analog Input for MAX11049
52	$\overline{WR}$	Active-Low Write Input. Drive $\overline{WR}$ low to write to the ADC. Configuration registers are loaded on the rising edge of $\overline{WR}$ .
53	$\overline{CS}$	Active-Low Chip-Select Input. Drive $\overline{CS}$ low when reading from or writing to the ADC.
54	$\overline{RD}$	Active-Low Read Input. Drive $\overline{RD}$ low to read from the ADC. Each rising edge of $\overline{RD}$ advances the channel output on the data bus.
55	DB15	16-Bit Parallel Data Bus Digital Out Bit 15
56	DB14	16-Bit Parallel Data Bus Digital Out Bit 14
—	EP	Exposed Pad. Internally connected to AGND. Connect to a large ground plane to maximize thermal performance. Not intended as an electrical connection point.

### Detailed Description

The MAX11047/MAX11048/MAX11049 are fast, low-power ADCs that combine 4, 6, or 8 independent ADC channels in a single IC. Each channel includes simultaneously sampling independent T/H circuitry that preserves relative phase information between inputs making the MAX11047/MAX11048/MAX11049 ideal for motor control and power monitoring. The MAX11047/MAX11048/MAX11049 are available with a 0 to 5V input range that features  $\pm 20\text{mA}$  overrange, fault-tolerant inputs. The MAX11047/MAX11048/MAX11049 operate with a single 4.75V to 5.25V supply. A separate 2.7V to 5.25V supply for digital circuitry makes the devices compatible with low-voltage processors.

The MAX11047/MAX11048/MAX11049 perform conversions for all channels in parallel by activating independent ADCs. Results are available through a high-speed, 20MHz, parallel data bus after a conversion time of  $3\mu\text{s}$  following the end of a sample. The data bus is bidirectional and allows for easy programming of the configuration register. The MAX11047/MAX11048/MAX11049 feature a reference buffer, which is driven by an internal bandgap reference circuit ( $V_{\text{REFIO}} = 4.096\text{V}$ ). Drive  $V_{\text{REFIO}}$  with an external reference or bypass with a  $0.1\mu\text{F}$  capacitor to ground when using the internal reference.

#### Analog Inputs

##### Track and Hold (T/H)

To preserve phase information across all channels, each input includes a dedicated T/H circuitry. The input tracking circuitry provides a 4MHz small-signal bandwidth, enabling the device to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by

using undersampling techniques. Use anti-alias filtering to avoid high-frequency signals being aliased into the frequency band of interest.

#### Input Range and Protection

The full-scale analog input voltage is a product of the reference voltage. For MAX11047/MAX11048/MAX11049, the input is unipolar in the range of:

$$0 \text{ to } +V_{\text{REFIO}} \times \frac{5.0}{4.096}$$

In external reference mode, drive  $V_{\text{REFIO}}$  with a 3.0V to 4.25V source, resulting in a full-scale input range of 3.662V to 5.188V, respectively.

All analog inputs are fault-protected up to  $\pm 20\text{mA}$ . The MAX11047/MAX11048/MAX11049 include an input clamping circuit that activates when the input voltage at the analog input is above ( $V_{\text{AVDD}} + 300\text{mV}$ ) or below  $-300\text{mV}$ . The clamp circuit remains high impedance while the input signal is within the range of 0V to  $+V_{\text{AVDD}}$  and draws little to no current. However, when the input signal exceeds the range of 0V to  $+V_{\text{AVDD}}$ , the clamps begin to turn on. Consequently, to obtain the highest accuracy, ensure that the input voltage does not exceed the range of 0V to  $+V_{\text{AVDD}}$ .

To make use of the input clamps, connect a resistor ( $R_S$ ) between the analog input and the voltage source to limit the voltage at the analog input so that the fault current into the MAX11047/MAX11048/MAX11049 does not exceed  $\pm 20\text{mA}$ . Note that the voltage at the analog input pin limits to approximately 7V during a fault condition so the following equation can be used to calculate the value of  $R_S$ :

# 4-/6-/8-Channel, 16-Bit, Simultaneous-Sampling ADCs

## Applications Information

### Digital Interface

The bidirectional, parallel, digital interface, DB0–DB3, sets the 4-bit configuration register. This interface configures the following control signals: chip select ( $\overline{CS}$ ), read ( $\overline{RD}$ ), write ( $\overline{WR}$ ), end of conversion ( $\overline{EOC}$ ), and convert start ( $\overline{CONVST}$ ). Figures 6 and 7 and the Timing Characteristics in the *Electrical Characteristics* table show the operation of the interface. DB0–DB3, together with the output-only DB4–DB15, also output the 16-bit conversion result. All bits are high impedance when  $\overline{RD} = 1$  or  $\overline{CS} = 1$ .

$$R_S = \frac{V_{\text{FAULT\_MAX}} - 7V}{20\text{mA}}$$

where  $V_{\text{FAULT\_MAX}}$  is the maximum voltage that the source produces during a fault condition.

Figures 2 and 3 illustrate the clamp circuit voltage-current characteristics for a source impedance  $R_S = 1280\Omega$ . While the input voltage is within the range of  $-300\text{mV}$  to  $+(V_{\text{AVDD}} + 300\text{mV})$ , no current flows in the input clamps. Once the input voltage goes beyond this voltage range, the clamps turn on and limit the voltage at the input pin.

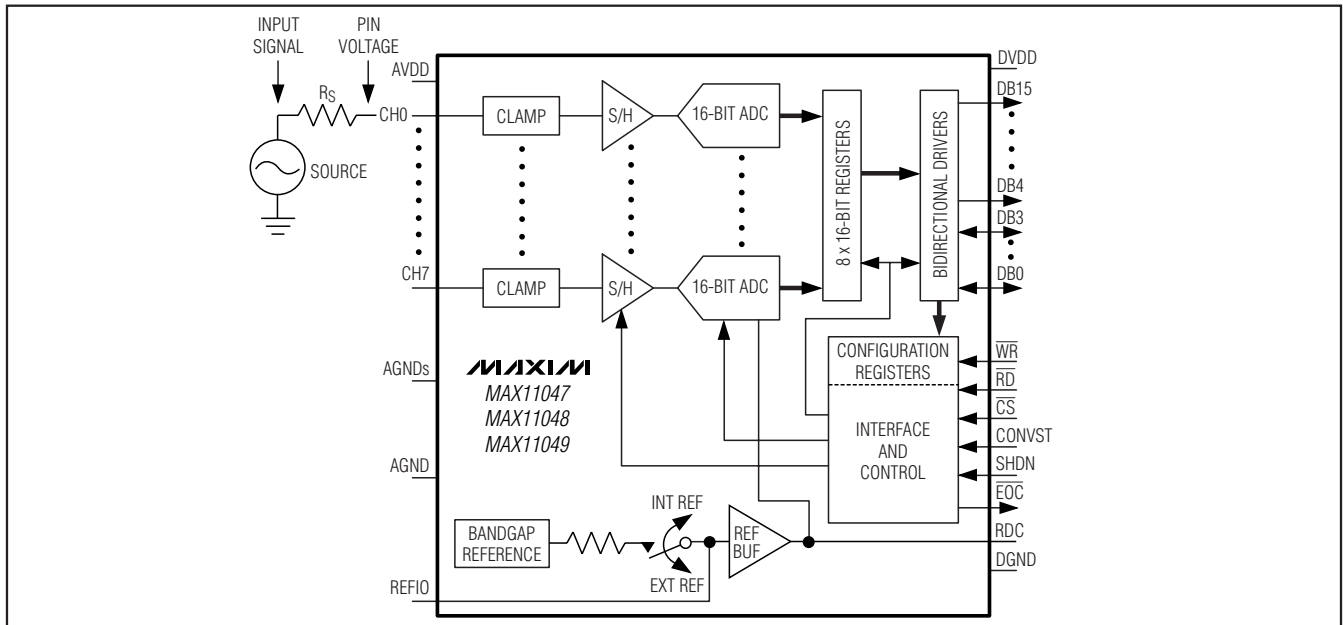


Figure 1. Required Setup for Clamp Circuit

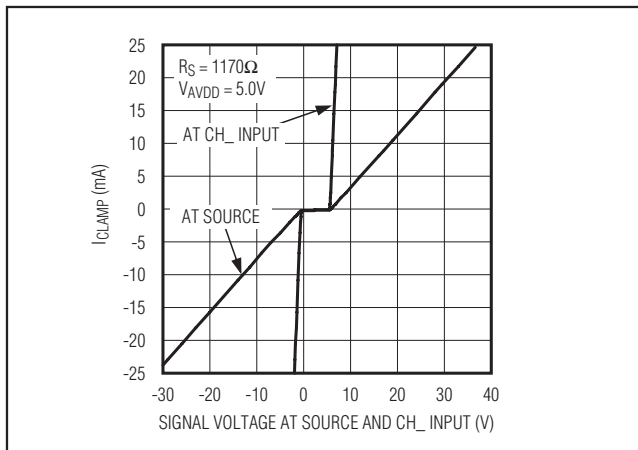


Figure 2. Input Clamp Characteristics

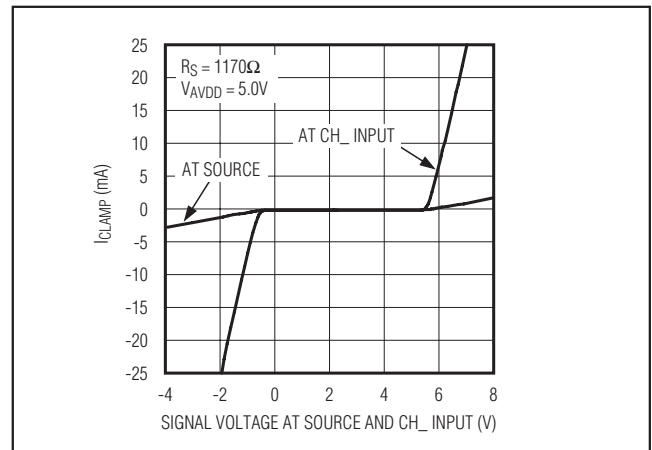


Figure 3. Input Clamp Characteristics (Zoom In)

MAX11047/MAX11048/MAX11049

# 4-/6-/8-Channel, 16-Bit, Simultaneous-Sampling ADCs

## DB3 (Int/Ext Reference)

DB3 selects the internal or external reference. The POR default = 0.

0 = internal reference, REFIO internally driven through a 10k $\Omega$  resistor, bypass with 0.1 $\mu$ F capacitor to AGND.

1 = external reference, drive REFIO with a high quality reference.

## DB2 (Output Data Format)

DB2 selects the output data format. The POR default = 0.

0 = offset binary.

1 = two's complement.

## DB1 (Reserved)

Set to 0 for normal operation.

0 = normal operation.

1 = reserved; do not use.

## DB0 (CONVST Mode)

DB0 selects the acquisition mode. The POR default = 0.

0 = CONVST controls the acquisition and conversion. Drive CONVST low to start acquisition. The rising edge of CONVST begins the conversion.

1 = acquisition mode starts as soon as previous conversion is complete. The rising edge of CONVST begins the conversion.

## Programming the Configuration Register

To program the configuration register, bring the  $\overline{CS}$  and  $\overline{WR}$  low and apply the required configuration data on DB3–DB0 of the bus and then raise  $\overline{WR}$  once to save changes.

## Starting a Conversion

CONVST initiates conversions. The MAX11047/MAX11048/MAX11049 provide two acquisition modes set through the configuration register. Allow a quiet time ( $t_Q$ ) of 500ns prior to the start of conversion to avoid any noise interference during readout or write operations from corrupting a sample.

In default mode (DB0 = 0), drive CONVST low to place the MAX11047/MAX11048/MAX11049 into acquisition mode. All the input switches are closed and the internal T/H circuits track the respective input voltage. Keep the CONVST signal low for at least 1 $\mu$ s ( $t_{ACQ}$ ) to enable proper settling of the sampled voltages. On the rising edge of CONVST, the switches are opened and the MAX11047/MAX11048/MAX11049 begin the conversion on all the samples in parallel.  $\overline{EOC}$  remains high until the conversion is completed.

Table 1. Configuration Register

DB3	DB2	DB1	DB0
Int/Ext Reference	Output Data Format	Reserved	CONVST Mode

In the second mode (DB0 = 1), the MAX11047/MAX11048/MAX11049 enter acquisition mode as soon as the previous conversion is completed. CONVST rising edge initiates the next sample and conversion sequence. Drive CONVST low for at least 20ns to be valid.

Provide adequate time for acquisition and the requisite quiet time in both modes to achieve accurate sampling and maximum performance of the MAX11047/MAX11048/MAX11049.

## Reading Conversion Results

The  $\overline{CS}$  and  $\overline{RD}$  are active-low, digital inputs that control the readout through the 16-bit, parallel, 20MHz data bus (D0–D15). After  $\overline{EOC}$  transitions low, read the conversion data by driving  $\overline{CS}$  and  $\overline{RD}$  low. Each low period of  $\overline{RD}$  presents the next channel's result. When  $\overline{CS}$  and  $\overline{RD}$  are high, the data bus is high impedance.  $\overline{CS}$  may be driven high between individual channel readouts or left low during the entire 8-channel readout.

## Reference

### Internal Reference

The MAX11047/MAX11048/MAX11049 feature a precision, low-drift, internal bandgap reference. Bypass REFIO with a 0.1 $\mu$ F capacitor to AGND to reduce noise. The REFIO output voltage may be used as a reference for other circuits. The output impedance of REFIO is 10k $\Omega$ . Drive only high-impedance circuits or buffer externally when using REFIO to drive external circuitry.

### External Reference

Set the configuration register to disable the internal reference and drive REFIO with a high-quality external reference. To avoid signal degradation, ensure that the integrated reference noise applied to REFIO is less than 10 $\mu$ V in the bandwidth of up to 50kHz.

### Reference Buffer

The MAX11047/MAX11048/MAX11049 have a built-in reference buffer to provide a low-impedance reference source to the SAR converters. This buffer is used in both internal and external reference modes. The internal reference buffer output feeds five RDC outputs. Connect all RDC outputs together. The reference buffer is externally compensated and requires at least 10 $\mu$ F on the RDC node for stability. For best performance, provide a total of at least 80 $\mu$ F on the RDC outputs.

## 4-/6-/8-Channel, 16-Bit, Simultaneous-Sampling ADCs

### Transfer Functions

Figures 8 and 9 show the transfer functions for all the formats and devices. Code transitions occur halfway between successive-integer LSB values.

### Layout, Grounding, and Bypassing

For best performance, use PCBs with ground planes. Ensure that digital and analog signal lines are separated from each other. Do not run analog and digital lines parallel to one another (especially clock lines), and avoid running digital lines underneath the ADC package. A single solid GND plane configuration with digital signals routed from one direction and analog signals from the other provides the best performance. Connect DGND, AGND, and AGNDS pins on the MAX11047/MAX11048/MAX11049 to this ground plane. Keep the ground return to the power supply for this ground low impedance and as short as possible for noise-free operation.

To achieve the highest performance, connect all the RDC outputs to a local RDC plane on the PCB. Bypass the RDC outputs with a total of at least 80 $\mu$ F of capacitance. For example, if two capacitors are used, place two 47 $\mu$ F, 10V X5R capacitors in 1210 case size as close as possible to pins 22 and 49. Alternatively, if four capacitors are used, place four 22 $\mu$ F, 10V X5R capacitors in 1210 case size as close as possible to pins 22, 28, 43, and 49. Ensure that each capacitor is connected directly into the GND plane with an independent via.

In cases where Y5U or Z5U ceramics are used, select higher voltage rating capacitors to compensate for the high-voltage coefficient of these ceramic capacitors, thus ensuring that at least 80 $\mu$ F of capacitance is on the RDC plane when the plane is driven to 4.096V by the internal reference buffer. For example, at 4.096V, a 22 $\mu$ F X5R ceramic capacitor with a 10V rating diminishes to only 20 $\mu$ F, whereas the same capacitor in Y5U ceramic at 4.096V decreases to about 13 $\mu$ F. However, a 22 $\mu$ F Y5U ceramic capacitor with a 25V rating capacitor is approximately 20 $\mu$ F at 4.096V.

Bypass AVDD and DVDD to the ground plane with 0.1 $\mu$ F ceramic chip capacitors on each pin as close as possible to the device to minimize parasitic inductance. Add at least one bulk 10 $\mu$ F decoupling capacitor to AVDD and DVDD per PCB. Interconnect all of the AVDD inputs and DVDD inputs using two solid power planes. For best performance, bring the AVDD power plane in on the analog interface side of the MAX11047/MAX11048/MAX11049 and the DVDD power plane from the digital interface side of the device.

For sampling periods near minimum (1 $\mu$ s) use a 1nF C0G ceramic chip capacitor between each of the channel inputs to the ground plane as close as possible to the MAX11047/MAX11048/MAX11049. This capacitor reduces the inductance seen by the sampling circuitry and reduces the voltage transient seen by the input source circuit.

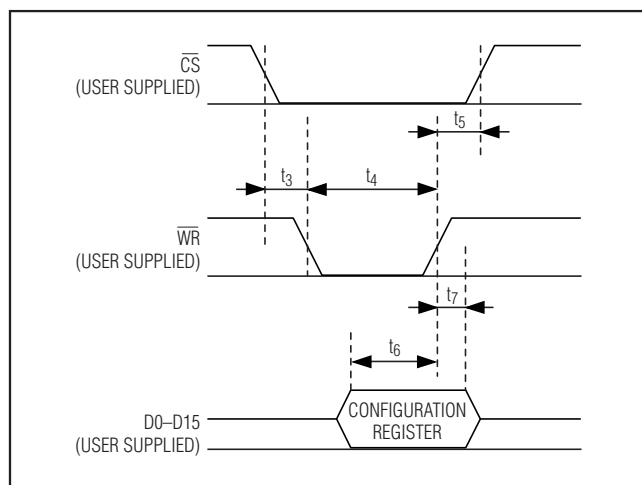


Figure 4. Programming Configuration-Register Timing Requirements

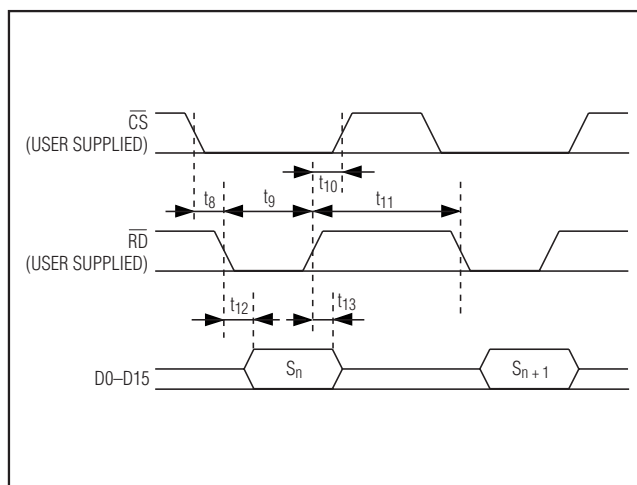


Figure 5. Readout Timing Requirements

# 4-/6-/8-Channel, 16-Bit, Simultaneous-Sampling ADCs

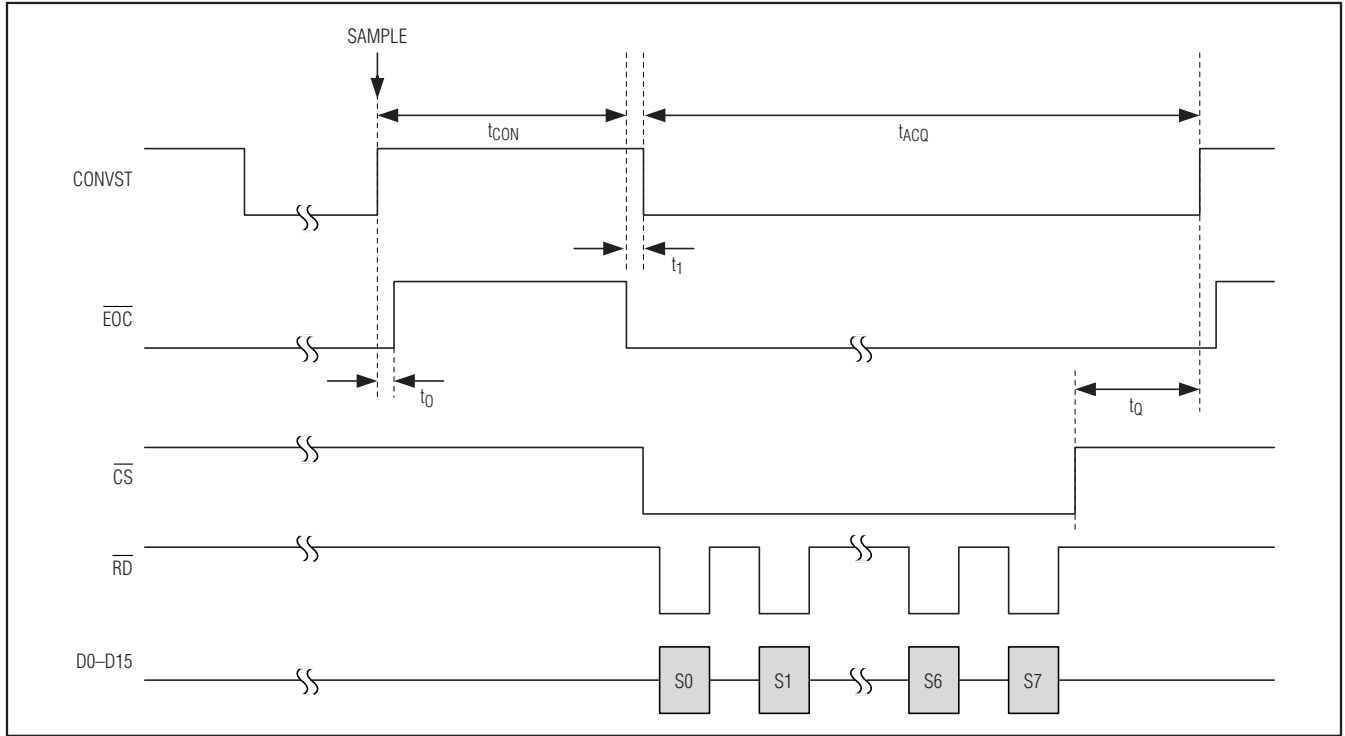


Figure 6. Conversion Timing Diagram (DB0 = 0)

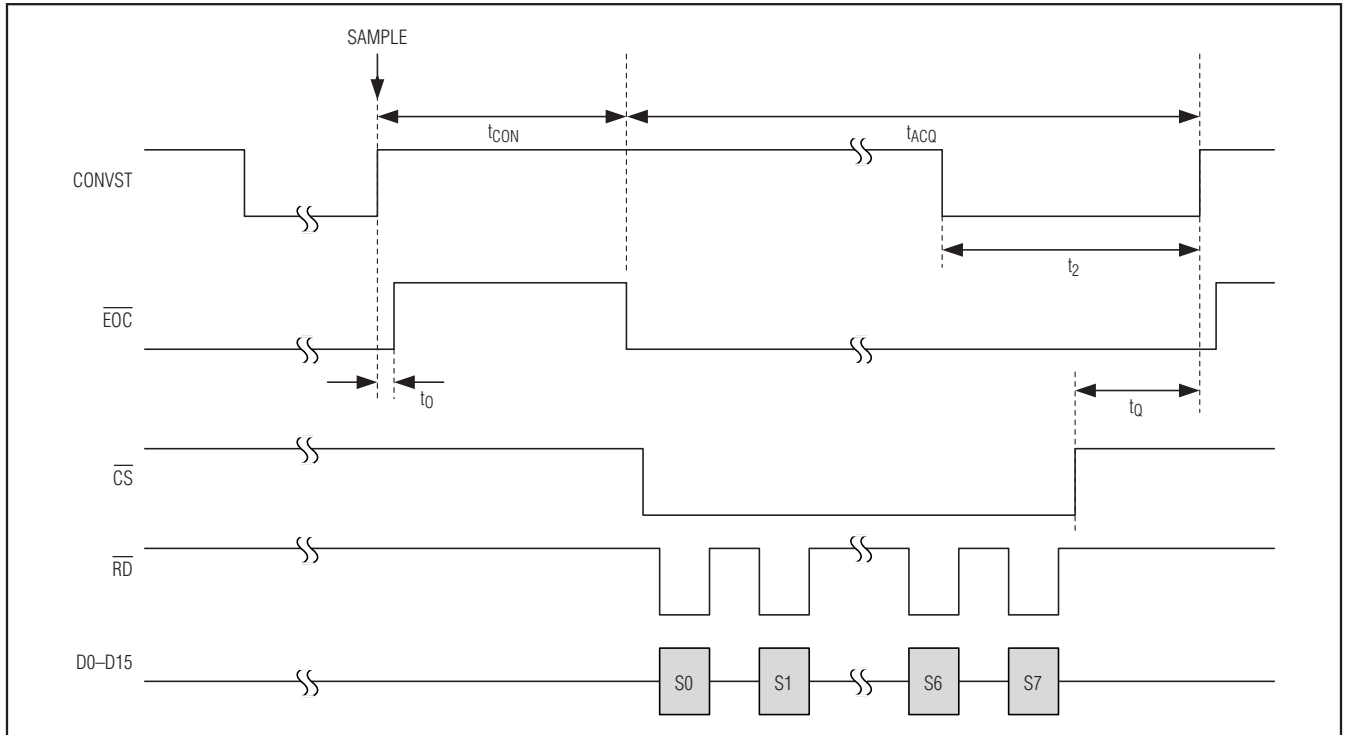


Figure 7. Conversion Timing Diagram (DB0 = 1)



## 4-/6-/8-Channel, 16-Bit, Simultaneous-Sampling ADCs

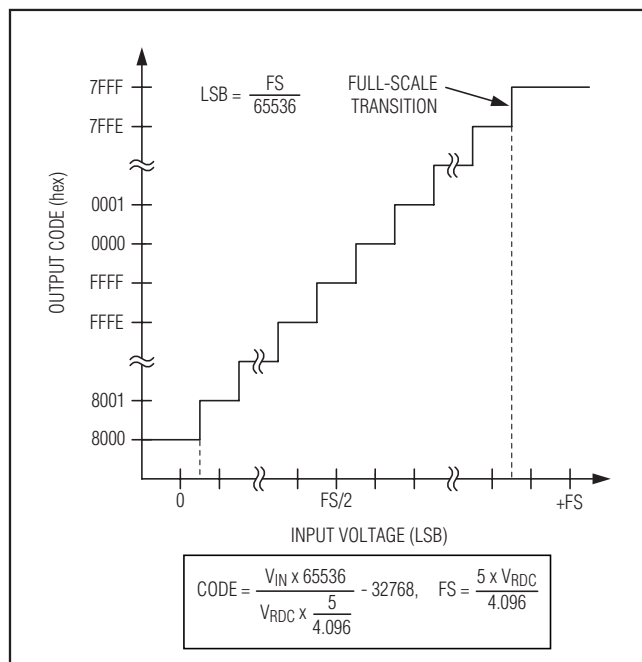


Figure 8. Two's Complement Transfer Function

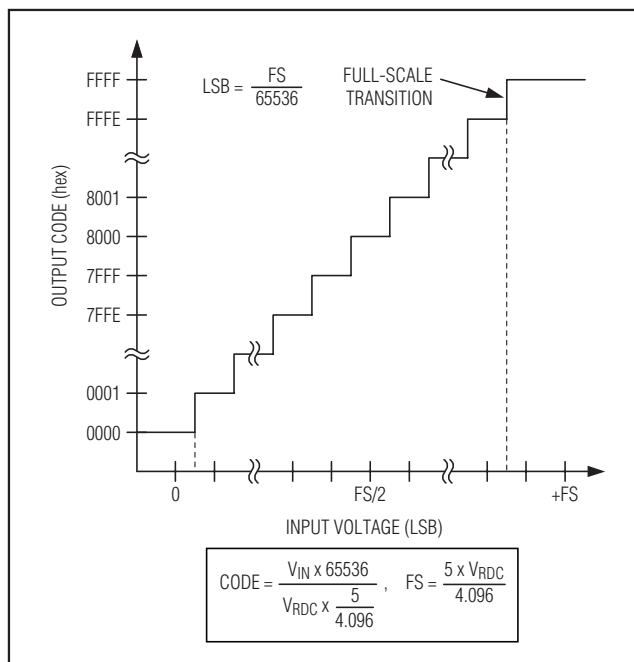


Figure 9. Offset-Binary Transfer Function

### Typical Application Circuits

#### Power-Grid Protection

Figure 10 shows a typical power-grid protection application.

#### DSP Motor Control

Figure 11 shows a typical DSP motor control application.

### Definitions

#### Integral Nonlinearity (INL)

INL is the deviation of the values on an actual transfer function from a straight line. For these devices, this straight line is a line drawn between the end points of the transfer function, once offset and gain errors have been nullified.

#### Differential Nonlinearity (DNL)

DNL is the difference between an actual step width and the ideal value of 1 LSB. For these devices, the DNL of each digital output code is measured and the worst-case value is reported in the *Electrical Characteristics* table. A DNL error specification of greater than -1 LSB guarantees no missing codes and a monotonic transfer function for an SAR ADC. For example, -0.9 LSB guarantees no missing code while -1.1 LSB results in missing code.

#### Offset Error

For the MAX11047/MAX11048/MAX11049, the offset error is defined at code transition 0x0000 to 0x0001 in offset binary encoding and 0x8000 to 0x8001 for two's complement encoding. The offset code transitions should occur with an analog input voltage of exactly  $0.5 \times (5/4.096) \times V_{REF}/65,536$  above GND. The offset error is defined as the deviation between the actual analog input voltage required to produce the offset code transition and the ideal analog input of  $0.5 \times (5/4.096) \times V_{REF}/65,536$  above GND, expressed in LSBs.

#### Gain Error

Gain error is defined as the difference between the change in analog input voltage required to produce a top code transition minus a bottom code transition, subtracted from the ideal change in analog input voltage on  $(5/4.096) \times V_{REF} \times (65,534/65,536)$ . For the MAX11047/MAX11048/MAX11049, top code transition is 0x7FFE to 0x7FFF in two's complement mode and 0xFFFE to 0xFFFF in offset binary mode. The bottom code transition is 0x8000 and 0x8001 in two's complement mode and 0x0000 and 0x0001 in offset binary mode. For the MAX11047/MAX11048/MAX11049, the analog input voltage to produce these code transitions is measured and the gain error is computed by subtracting  $(5/4.096) \times V_{REF} \times (65,534/65,536)$  from this measurement.

# 4-/6-/8-Channel, 16-Bit, Simultaneous-Sampling ADCs

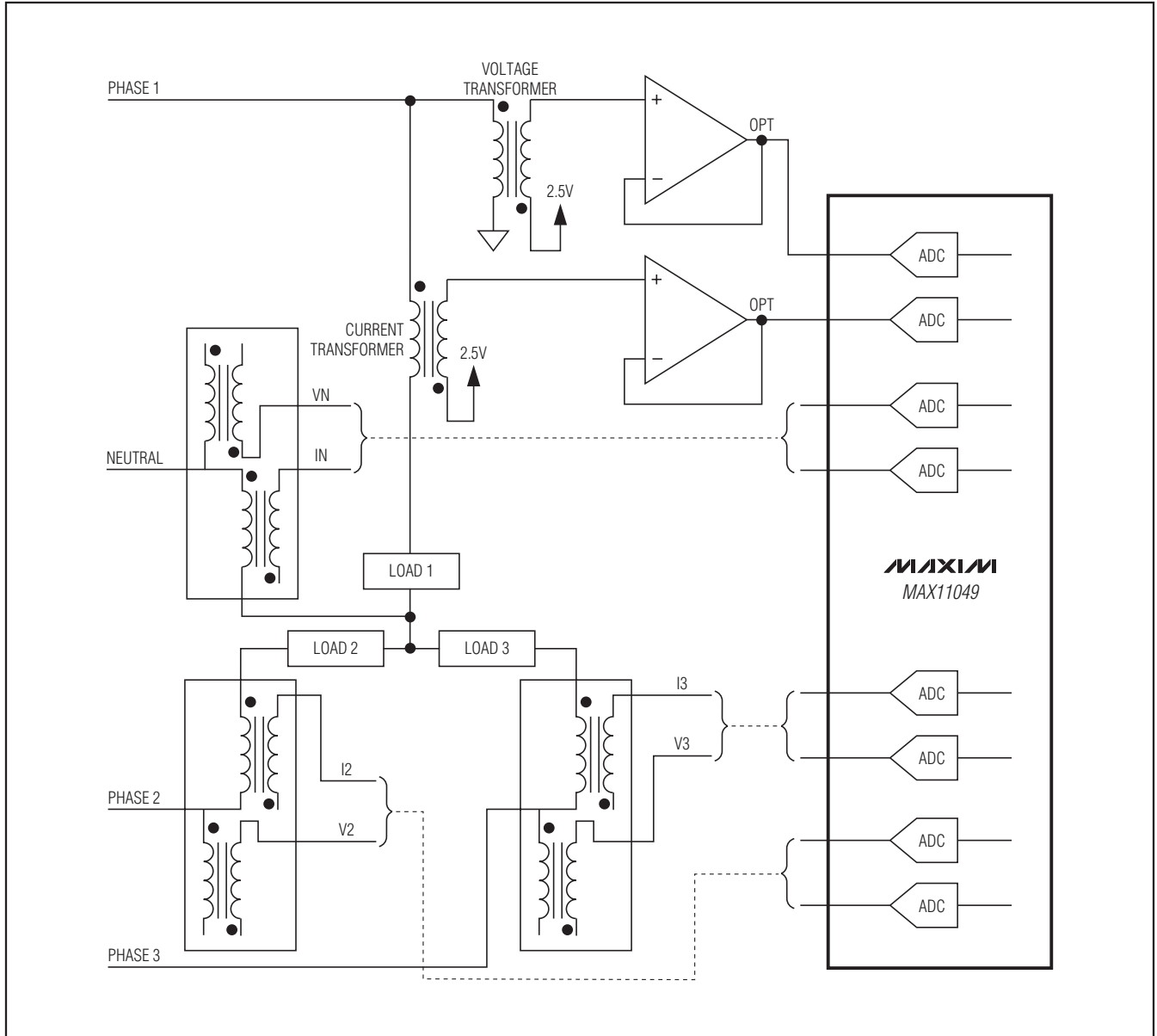


Figure 10. Power-Grid Protection



# 4-/6-/8-Channel, 16-Bit, Simultaneous-Sampling ADCs

MAX11047/MAX11048/MAX11049

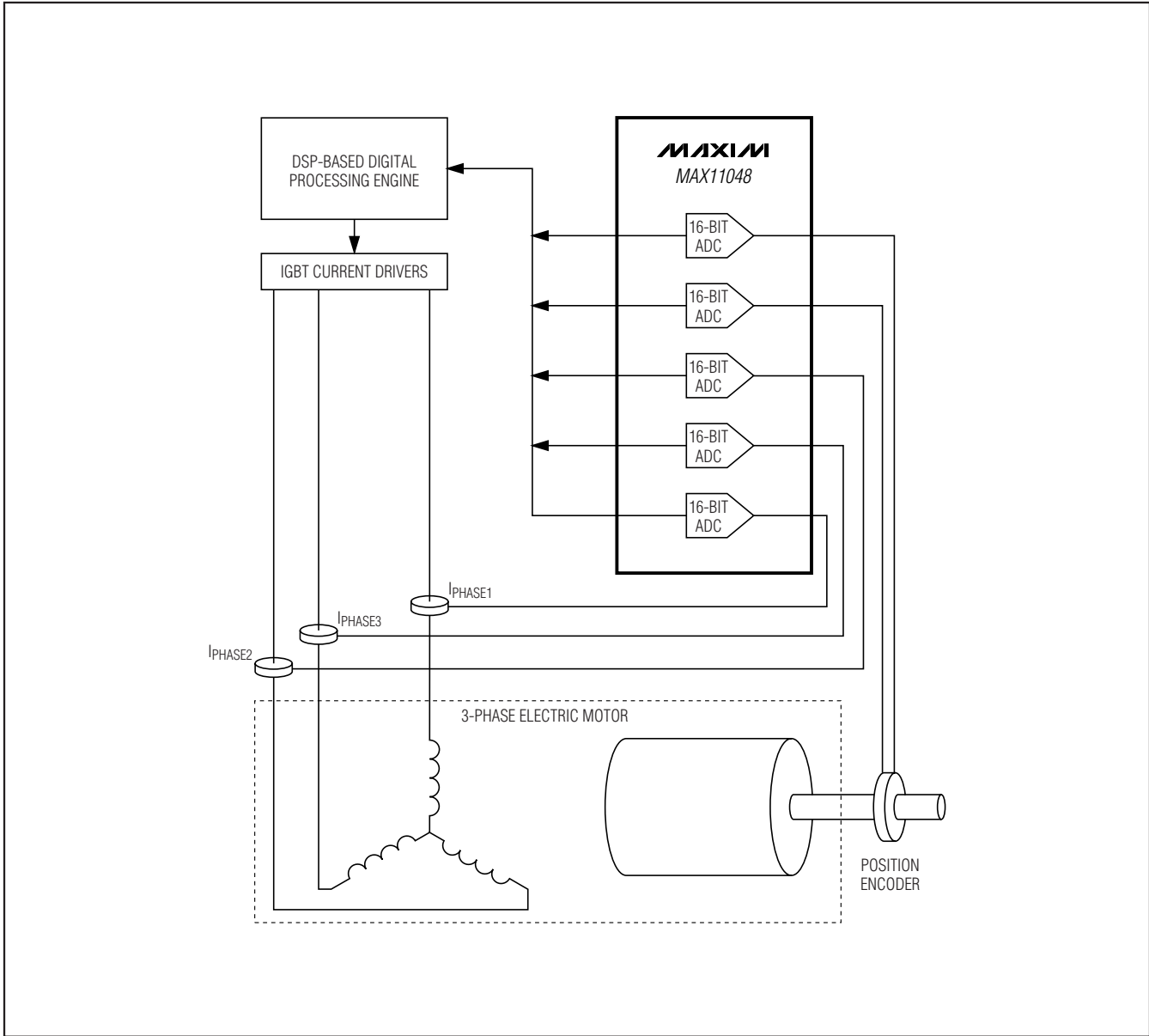


Figure 11. DSP Motor Control

# 4-/6-/8-Channel, 16-Bit, Simultaneous-Sampling ADCs

## Signal-to-Noise Ratio (SNR)

For a waveform perfectly reconstructed from digital samples, SNR is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization noise error only and results directly from the ADC's resolution (N bits):

$$\text{SNR} = (6.02 \times N + 1.76)\text{dB}$$

where N = 16 bits. In reality, there are other noise sources besides quantization noise: thermal noise, reference noise, clock jitter, etc. SNR is computed by taking the ratio of the RMS signal to the RMS noise, which includes all spectral components not including the fundamental, the first five harmonics, and the DC offset.

## Signal-to-Noise Plus Distortion (SINAD)

SINAD is the ratio of the fundamental input frequency's RMS amplitude to the RMS equivalent of all the other ADC output signals:

$$\text{SINAD(dB)} = 10 \times \log \left[ \frac{\text{Signal}_{\text{RMS}}}{(\text{Noise} + \text{Distortion})_{\text{RMS}}} \right]$$

## Effective Number of Bits (ENOB)

The ENOB indicates the global accuracy of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. With an input range equal to the full-scale range of the ADC, calculate the ENOB as follows:

$$\text{ENOB} = \frac{\text{SINAD} - 1.76}{6.02}$$

## Total Harmonic Distortion (THD)

THD is the ratio of the RMS of the first five harmonics of the input signal to the fundamental itself. This is expressed as:

$$\text{THD} = 20 \times \log \left[ \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2}}{V_1} \right]$$

where V<sub>1</sub> is the fundamental amplitude and V<sub>2</sub> through V<sub>5</sub> are the 2nd- through 5th-order harmonics.

## Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio of the RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next-largest frequency component.

## Aperture Delay

Aperture delay (t<sub>AD</sub>) is the time delay from the sampling clock edge to the instant when an actual sample is taken.

## Aperture Jitter

Aperture Jitter (t<sub>AJ</sub>) is the sample-to-sample variation in aperture delay.

## Channel-to-Channel Isolation

Channel-to-channel isolation indicates how well each analog input is isolated from the other channels. Channel-to-channel isolation is measured by applying DC to channels 1 to 7, while a -0.4dBFS sine wave at 60Hz is applied to channel 0. A 10kps FFT is taken for channel 0 and channel 1. Channel-to-channel isolation is expressed in dB as the power ratio of the two 60Hz magnitudes.

## Small-Signal Bandwidth

A small -20dBFS analog input signal is applied to an ADC in a manner that ensures that the signal's slew rate does not limit the ADC's performance. The input frequency is then swept up to the point where the amplitude of the digitized conversion result has decreased 3dB.

## Full-Power Bandwidth

A large -0.5dBFS analog input signal is applied to an ADC, and the input frequency is swept up to the point where the amplitude of the digitized conversion result has decreased by 3dB. This point is defined as full-power input bandwidth frequency.

## Chip Information

PROCESS: BiCMOS

## Package Information

For the latest package outline information and land patterns, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
56 TQFN-EP	T5688+2	<a href="#">21-0135</a>

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

18 **Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600**