

RQJ0305EQDQA

Silicon P Channel MOS FET
Power Switching

REJ03G1718-0100

Rev.1.00

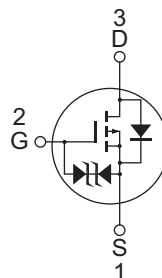
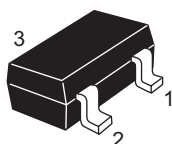
Jul 28, 2008

Features

- Low gate drive
 V_{DSS} : -30 V and 2.5 V gate drive
- Low drive current
- High speed switching
- Small traditional package (MPAK)

Outline

RENESAS Package code: PLSP0003ZB-A
(Package name: MPAK)



1. Source
2. Gate
3. Drain

Notes: Marking is "EQ".

Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	-30	V
Gate to source voltage	V_{GSS}	+8 / -12	V
Drain current	I_D	-2.4	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	-10	A
Body - drain diode reverse drain current	I_{DR}	2.4	A
Channel dissipation	P_{ch} ^{Note2}	0.8	W
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Notes: 1. $PW \leq 10 \mu\text{s}$, Duty cycle $\leq 1\%$

2. When using the glass epoxy board (FR-4 40 × 40 × 1 mm)

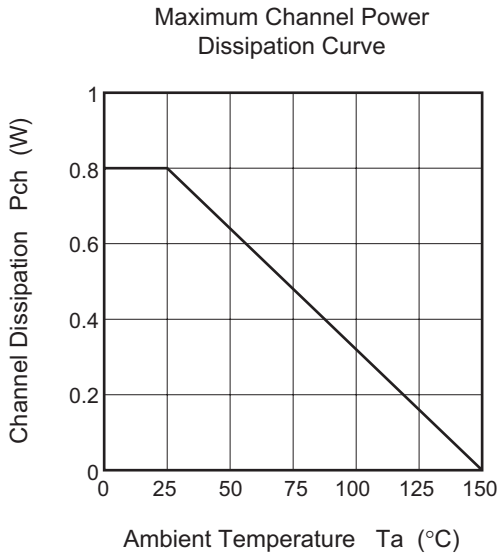
Electrical Characteristics

(Ta = 25°C)

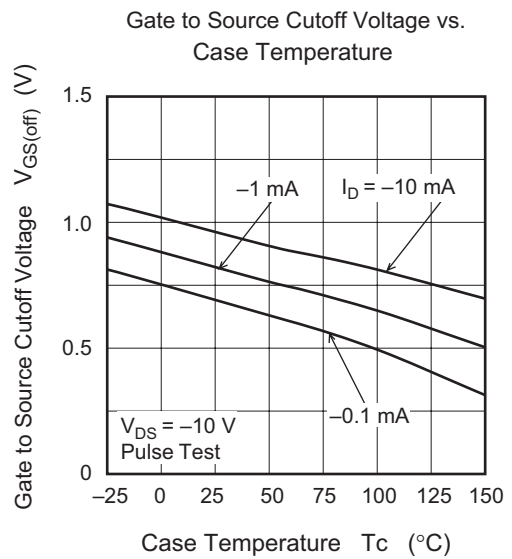
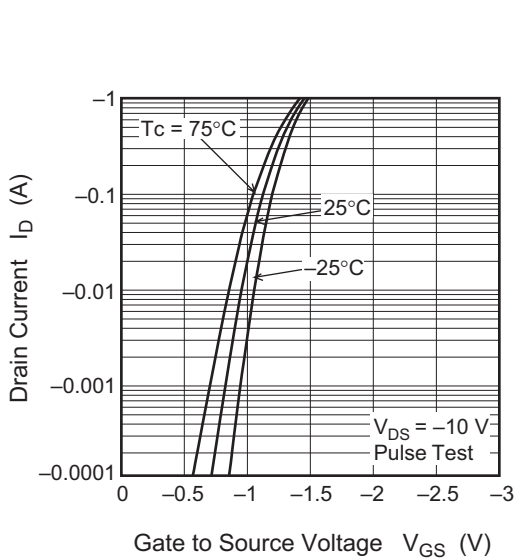
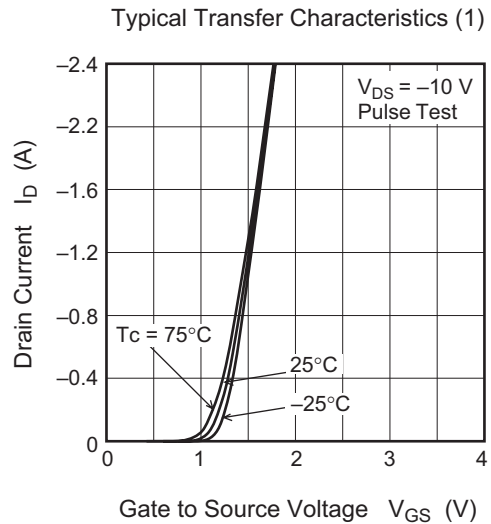
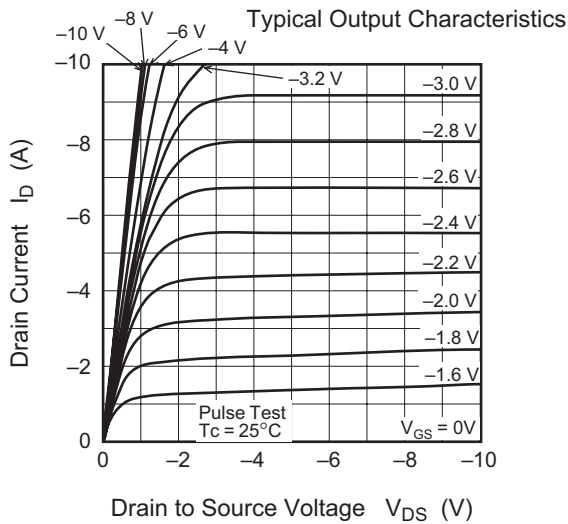
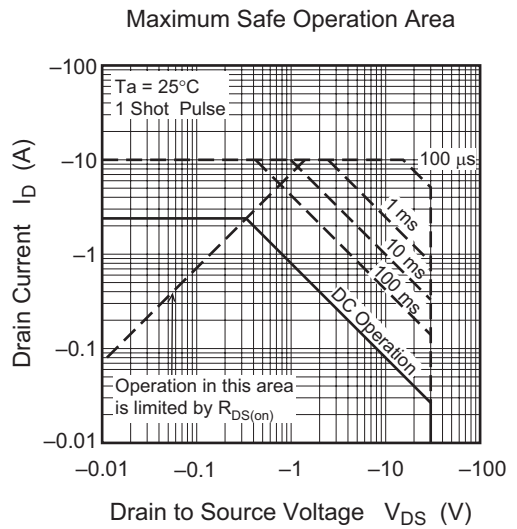
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-30	—	—	V	$I_D = -10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	+8	—	—	V	$I_G = +100 \text{ }\mu\text{A}$, $V_{DS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	-12	—	—	V	$I_G = -100 \text{ }\mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	+10	μA	$V_{GS} = +6 \text{ V}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	-10	μA	$V_{GS} = -10 \text{ V}$, $V_{DS} = 0$
Drain to source leak current	I_{DSS}	—	—	-1	μA	$V_{DS} = -30 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-0.4	—	-1.4	V	$V_{DS} = -10 \text{ V}$, $I_D = -1 \text{ mA}$
Drain to source on state resistance	$R_{DS(on)}$	—	110	140	$\text{m}\Omega$	$I_D = -1.3 \text{ A}$, $V_{GS} = -4.5 \text{ V}$ ^{Note3}
Drain to source on state resistance	$R_{DS(on)}$	—	165	230	$\text{m}\Omega$	$I_D = -1.3 \text{ A}$, $V_{GS} = -2.5 \text{ V}$ ^{Note3}
Forward transfer admittance	$ y_{fs} $	2.6	3.9	—	S	$I_D = -1.3 \text{ A}$, $V_{DS} = -10 \text{ V}$ ^{Note3}
Input capacitance	C_{iss}	—	330	—	pF	$V_{DS} = -10 \text{ V}$, $V_{GS} = 0$, $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	70	—	pF	
Reverse transfer capacitance	C_{rss}	—	40	—	pF	
Turn - on delay time	$t_{d(on)}$	—	17	—	ns	$I_D = -1.3 \text{ A}$ $V_{GS} = -4.5 \text{ V}$ $R_L = 7.7 \text{ }\Omega$ $R_g = 4.7 \text{ }\Omega$
Rise time	t_r	—	37	—	ns	
Turn - off delay time	$t_{d(off)}$	—	39	—	ns	
Fall time	t_f	—	10	—	ns	
Total gate charge	Q_g	—	3.0	—	nC	$V_{DD} = -10 \text{ V}$
Gate to Source charge	Q_{gs}	—	0.6	—	nC	$V_{GS} = -4.5 \text{ V}$
Gate to drain charge	Q_{gd}	—	1.3	—	nC	$I_D = -2.4 \text{ A}$
Body - drain diode forward voltage	V_{DF}	—	-0.85	-1.2	V	$I_F = -2.4 \text{ A}$, $V_{GS} = 0$ ^{Note3}

Notes: 3. Pulse test

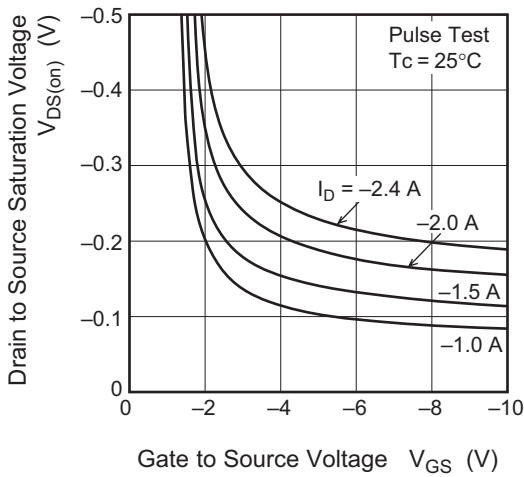
Main Characteristics



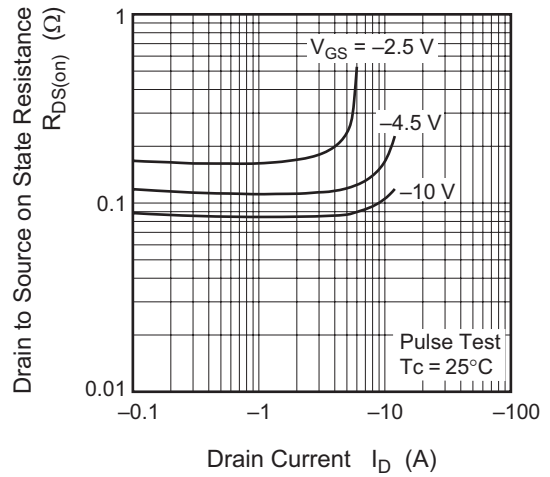
*When using the glass epoxy board (FR-4 40 x 40 x 1 mm)



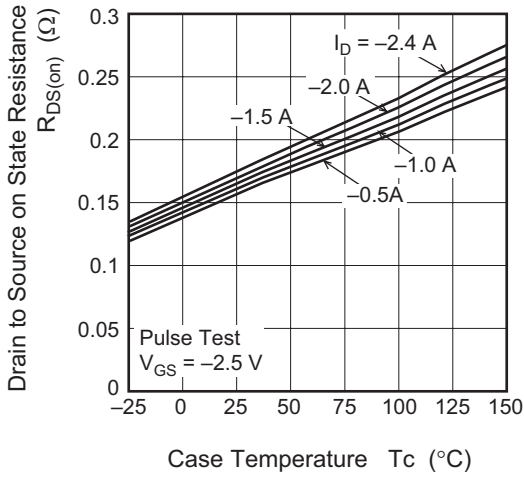
Drain to Source Saturation Voltage vs. Gate to Source Voltage



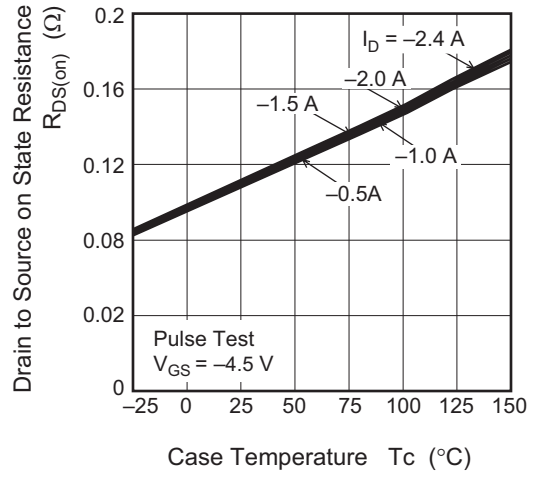
Static Drain to Source on State Resistance vs. Drain Current



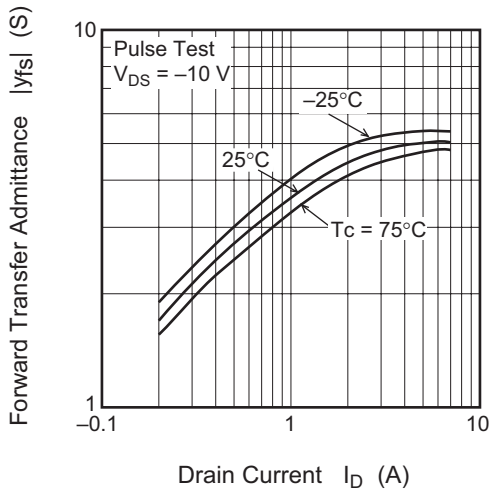
Static Drain to Source on State Resistance vs. Case Temperature (1)



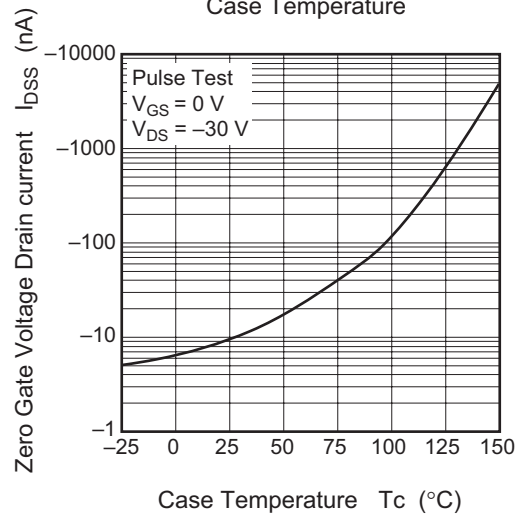
Static Drain to Source on State Resistance vs. Case Temperature (2)



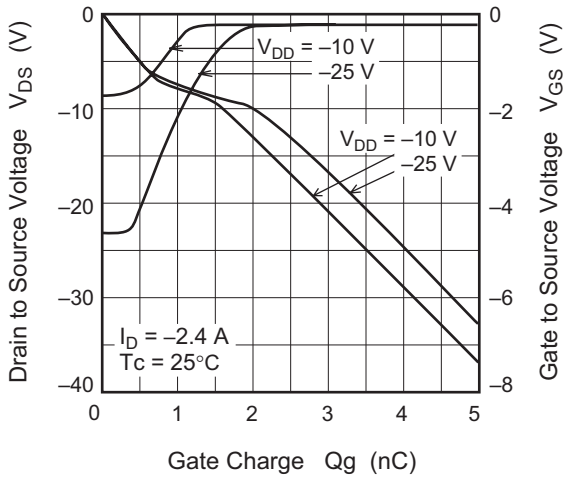
Forward Transfer Admittance vs. Drain Current



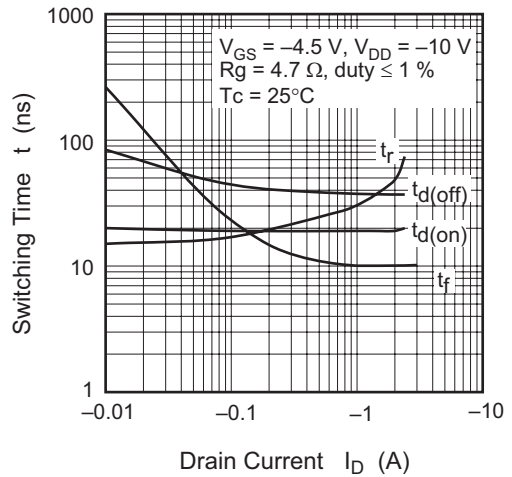
Zero Gate Voltage Drain current vs. Case Temperature



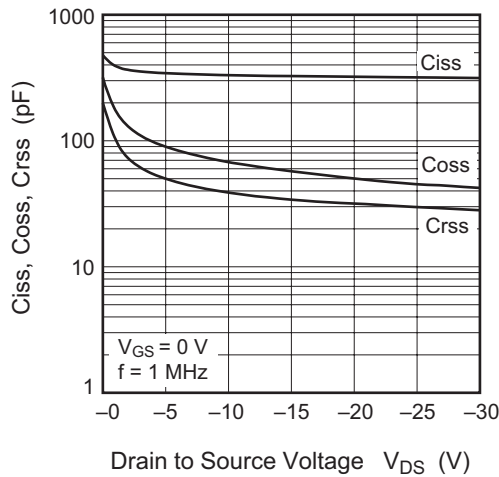
Dynamic Input Characteristics



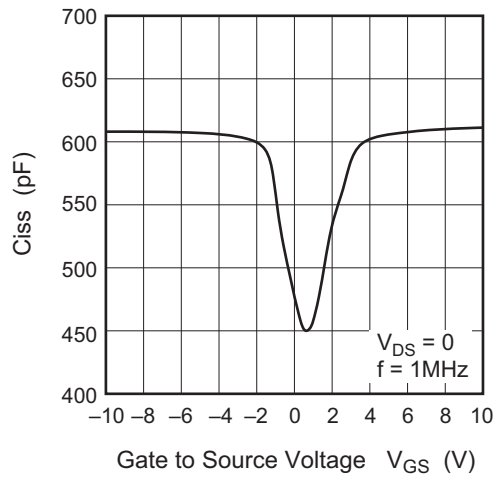
Switching Characteristics



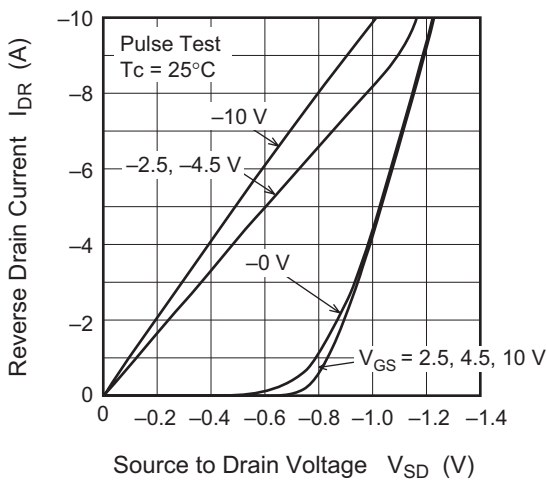
Typical Capacitance vs. Drain to Source Voltage



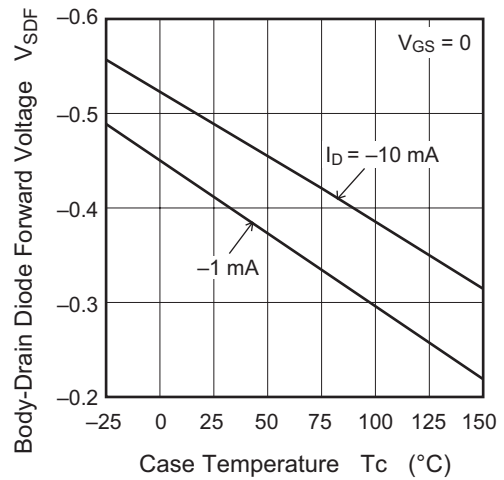
Input Capacitance vs. Gate to Source Voltage

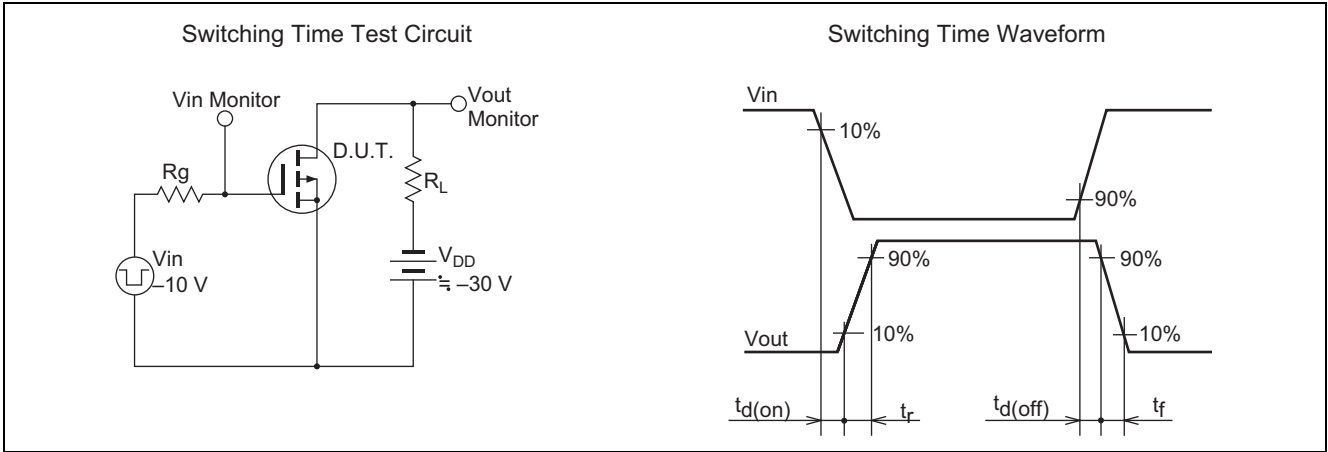


Reverse Drain Current vs. Source to Drain Voltage

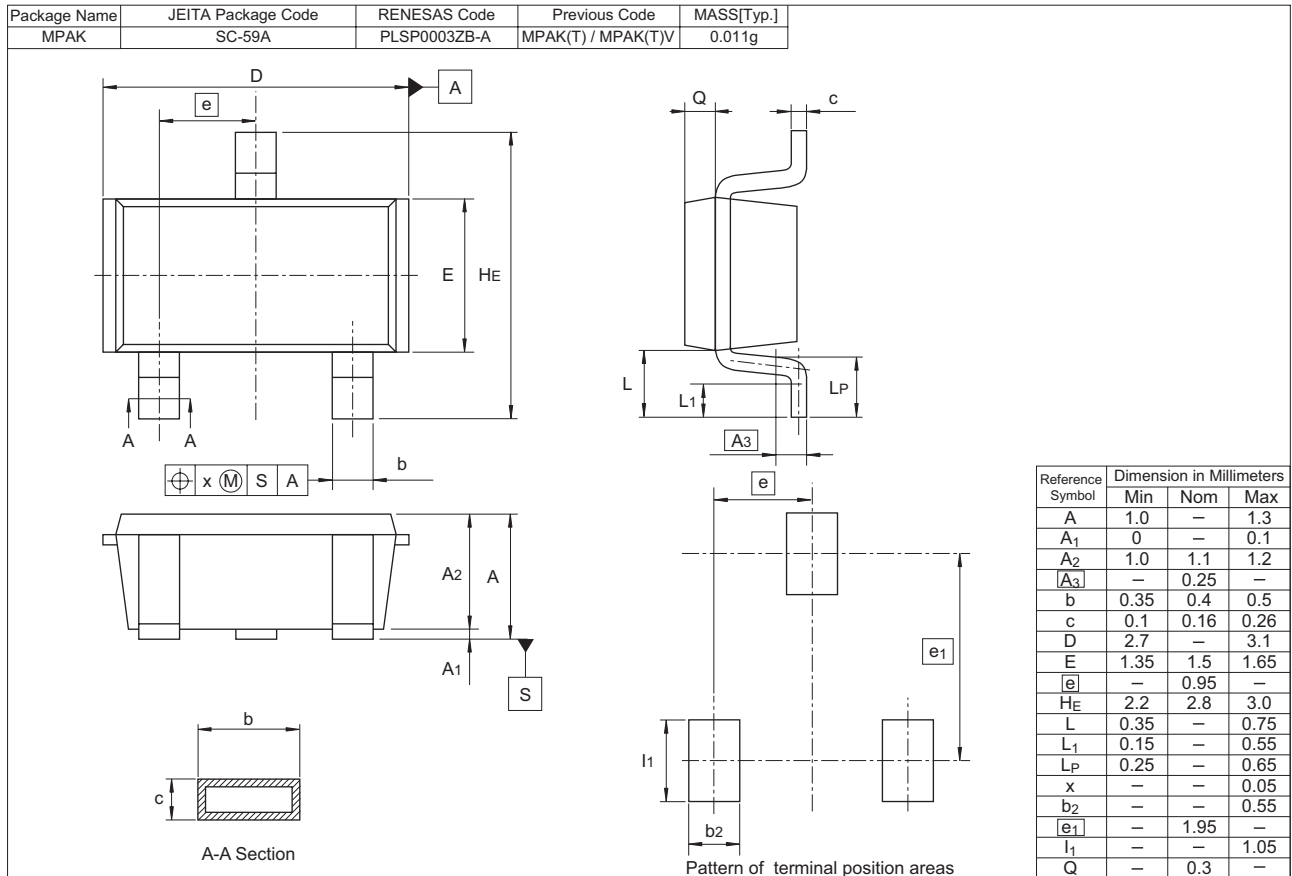


Body-Drain Diode Forward Voltage vs. Case Temperature





Package Dimensions



Ordering Information

Part No.	Quantity	Shipping Container
RQJ0305EQDQATL-E	3000 pcs.	φ178 mm reel, 8 mm Emboss taping

Notes:

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450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology (Shanghai) Co., Ltd.
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Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7858/7898

Renesas Technology Hong Kong Ltd.
7th Floor, North Tower, World Finance Centre, Harbour City, Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2377-3473

Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 3518-3399

Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.
Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510