10G 850nm XFP Transceiver

(Up to 300m transmission)

Members of Flexon™ Family

Features

- Support 10GE application at the data-rate of 9.953Gbps and 10.3125Gbps
- Up to 300m transmission distance on 50μm MMF (2000MHz.km)
- 850nm VCSEL and PIN receiver
- XFI electrical interface
- 2-wire interface for integrated Digital Diagnostic monitoring
- XFP MSA package with duplex LC connector
- Hot pluggable
- Very low EMI and excellent ESD protection
- +5V, +3.3V power supply
- Power consumption less than 1.5 W
- Operating case temperature: 0~+70°C

Applications

- 10GBASE-SR at 10.3125Gbps
- 10GBASE-SW at 9.953Gbps
- Other optical links

Standard

- Compatible with XFP MSA
- Compatible with IEEE 802.3ae-2002
- Compatible with FCC 47 CFR Part 15, Class B
- Compatible with FDA 21 CFR 1040.10 and 1040.11, Class I
- RoHS compliance

Description

FTM-83X0C-X03G is a high performance, cost effective module, which is optimized for 10G Ethernet, supporting data-rate of 10.3125Gbps (10GBASE-SR) or 9.953Gbps (10GBASE-SW), and transmission distance up to 300m on 50μm MMF (2000MHz.km).

The transceiver consists of two sections: The transmitter section incorporates an 850nm VCSEL, driver and re-timer. The receiver section consists of a PIN photodiode integrated with a transimpedance preamplifier (TIA) and CDR.

The module is hot pluggable into the 30-pin XFI connector. The high-speed electrical interface is base on low voltage logic, with nominal 100 Ohms differential impedance and AC coupled in the module. The optical output can be disabled by LVTTL logic high-level input of TX_DIS. Loss of signal (RX_LOS) output is provided to indicate the loss of an input optical signal of receiver.

The user can access transceiver monitoring and configuration data via the 2-wire XFP Management Interface. This interface uses a single address, A0h, with a memory map divided into a lower and upper area. Basic digital diagnostic (DD) data is held in the lower area while specific data is held in a series of tables in the high memory area.

Regulatory Compliance

The transceivers are tested according to American and European product safety and electromagnetic compatibility regulations (See Table 1). For further information regarding regulatory certification, please refer to Fiberxon regulatory specification and safety guidelines, or contact with Fiberxon, Inc. America sales office listed at the end of the documentation.

Table 1- Regulatory Compliance

Feature	Standard	Performance
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883E Method 3015.7	Class 1(>500 V)
Electrostatic Discharge (ESD) to the Duplex LC Receptacle	IEC 61000-4-2 GR-1089-CORE	Compatible with standards
Electromagnetic Interference (EMI)	FCC Part 15 Class B EN55022 Class B (CISPR 22B) VCCI Class B	Compatible with standards
Immunity	IEC 61000-4-3	Compatible with standards
Laser Eye Safety	FDA 21CFR 1040.10 and 1040.11 EN60950, EN (IEC) 60825-1,2	Compatible with Class 1 laser product.
Component Recognition	UL and CSA	UL file E223705

Absolute Maximum Ratings

Stress in excess of the maximum absolute ratings can cause permanent damage to the module.

Table 2 - Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	T_S	-40	+85	°C
Supply Voltage	V_{CC5}	-0.5	6.0	V
	V_{CC3}	-0.5	4.0	V
Operating Relative Humidity	RH		85	%

Recommended Operating Conditions

Table 3 - Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Operating Case Temperature	T_C	0		+70	°C	
Power Supply Voltage	V_{CC5}	4.75	5.0	5.25	V	
	V_{CC3}	3.13	3.3	3.47		
Power Supply Current	I_{CC5}			20	mA	
	I_{CC3}			400	mA	
Power Dissipation	P_D			1.5	W	
Data Rate			9.953/10.3125		Gbps	
Transmission Distance		2		300	m	1
Note 1: The transmission distance depends on the fiber type. PLS see “Table 52-6” in IEEE 802.3ae.						

Optical Characteristics

Table 4 - Optical Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Transmitter						
Operating Data Rate			9.953/ 10.3125		Gbps	
Centre Wavelength	λ_C	840		860	nm	
Average Output Power	P_{0UT}	-7.3		-1.0	dBm	1
Extinction Ratio	ER	3.0			dB	2
Optical Modulation Amplitude	OMA	See Note 3			dBm	3
Spectral Width	Δλ	See Note 3			nm	3
Dispersion Penalty	DP			3.9	dB	
Optical Eye Mask	Compatible with IEEE 802.3ae					
Receiver						
Operating Data Rate			9.953/ 10.3125		Gbps	
Centre Wavelength	λ_C	840		860	nm	
Receiver Sensitivity	P_{IN}			-9.9	dBm	4
Receiver Sensitivity in OMA	P_{IN}			-11.1	dBm	4
Receiver Overload	P_{IN}	-1.0			dBm	4
LOS Assert	LOS_A	-25	-15		dBm	
LOS Deassert	LOS_D			-12	dBm	
LOS Hysteresis		1		4	dB	
Receiver Reflectance				-12	dB	

Notes:

1. The optical power is launched into MMF.
2. Measured with a PRBS 2^{31}-1 test pattern @10.3125Gbps.
3. Reference to Table 52-8 of IEEE P802.3ae.
4. Measured with a PRBS 2^{31}-1 test pattern @10.3125Gbps, BER$\leqslant 10^{-12}$.

Electrical Characteristics

Table 5 - Electrical Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
High-speed Signal (CML) Interface Specification						
Input Data Rate			9.953/ 10.3125		Gbps	
Differential Data Input Amplitude		120		1200	mVpp	1
Input Differential Impedance			100		Ω	
Output Data Rate			9.953/ 10.3125		Gbps	
Differential Date Output Amplitude		500		800	mVpp	1
Output Differential Impedance			100		Ω	
Low-speed Signal (LVTTL) Interface Specification						
Input High Voltage		2.0		Vdd1=3.3	V	
Input Low Voltage		GND		0.8	V	
Output High Voltage		2.4		Vdd1=3.3	V	
Output Low Voltage		GND		0.4	V	
2 Wire Serial Interface (LVTTL) Specification						
Clock Frequency	f_{SCL}			400	kHz	
Reference Clock (PECL) Interface Specification						
No reference clock needed						

Notes:

1. Internally AC coupled

Management Interface

The structure of the memory map is shown in Figure 1, which is accessible over a 2 wire serial interface at the 8-bit address 1010000X (A0h). The normal 256 Byte I2C address space is divided into lower and upper blocks of 128 Bytes. The lower block of 128 Bytes is always directly available and is used for the diagnostics and control function. The monitoring specification is shown in Table 6. Multiple blocks of memories are available in the upper 128 Bytes of the address space. These are individually addressed through a table select Byte which the user enters into a location in the lower address space. Thus, there is a total available address space of 128 * 256 = 32Kbytes in this upper memory space. The contents of Table 01h are list in table 7 below. PLS refer INF-8077i (Revision 4.0) for detailed information.

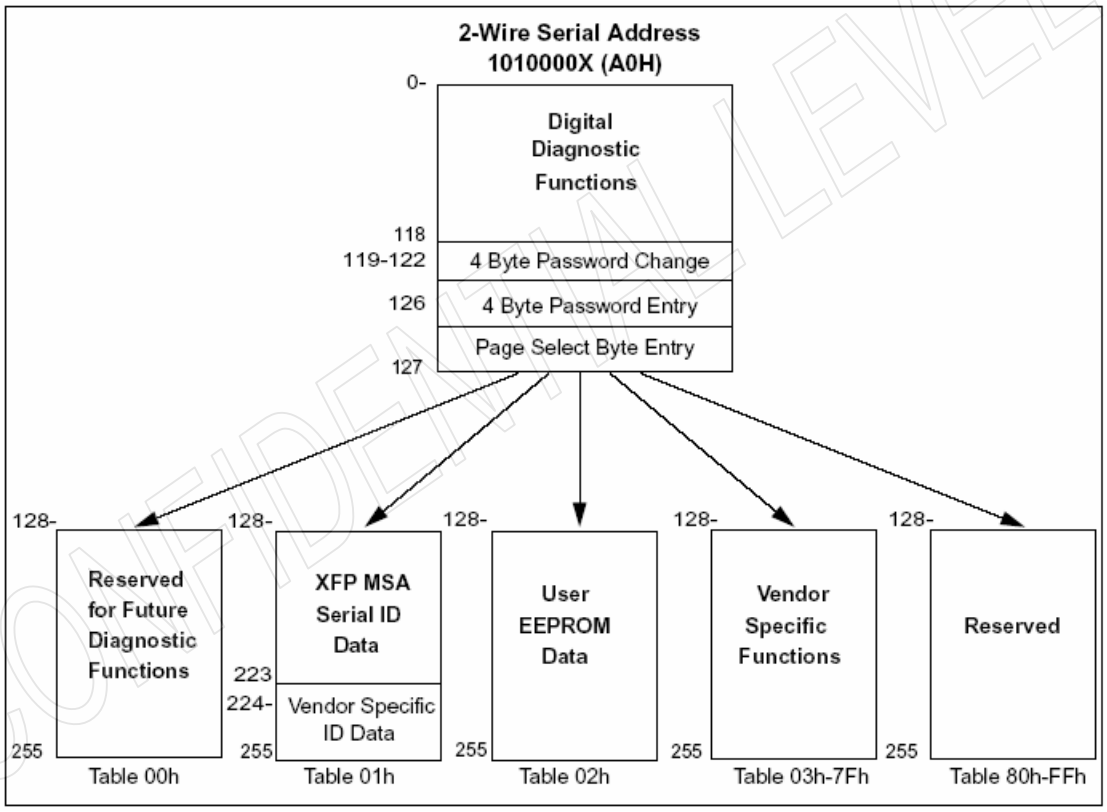


Figure 1, 2-wire Serial Digital Diagnostic Memory Map

Table 6 - Monitoring Specification

Data Address	Parameter	Range	Accuracy
96-97	Temperature	-10 to +80°C	±3°C
100-101	Bias Current	0 to 15mA	±10%
102-103	TX Power	-9 to 0dBm	±2dB
104-105	RX Power	-15 to 0dBm	±2dB
106-107	V_{CC5} Voltage	+4.5V to +5.5V	±3%
108-109	V_{CC3} Voltage	+3.0V to +3.7V	±3%

Table 7 - Serial ID Memory Contents (Table 01h)

Addr.	Field Size (Bytes)	Name of Field	Hex	Description
128	1	Identifier	06	XFP
129	1	Ext. Identifier	10	TX Ref Clock Input not Required
130	1	Connector	07	LC Connector
131-138	8	Transceiver	88 00 00 00 00 00 00 00	10GBASE-SR/SW
139	1	Encoding	10	NRZ
140	1	BR-Min	63	9.953Gbps
141	1	BR-Max	6F	11.1Gbps
142	1	Length (9um)-km	00	
143	1	Length (E-50um)	96	300m
144	1	Length (50um)	52	82m
145	1	Length (62.5um)	21	33m
146	1	Length (copper)	00	
147	1	Device Tech	00	850nm VCSEL, PIN Detector
148-163	16	Vendor name	46 49 42 45 52 58 4F 4E 20 49 4E 43 2E 20 20 20	“FIBERXON INC. “(ASCⅡ)
164	1	CDR Support	F8	CDR supports 9.953Gbps~11.1Gbps
165-167	3	Vendor OUI	00 00 00	
168-183	16	Vendor PN	46 54 4D 2D 38 33 58 30 43 2D 58 30 33 47 20 20	“FTM-83X0C-X03G” (ASCⅡ)
184-185	2	Vendor rev	xx xx	ASCⅡ(“32 61” means 2a revision)
186-187	2	Wavelength	42 68	850nm
188-189	2	Wavelength Tolerance	07 D0	+/- 10nm
190	1	Max Case Temp	46	70degC
191	1	CC_BASE		Check sum of bytes 128 - 190
192-195	4	Power Supply	4B 96 14 00	1.5W (max), 1.5W (max, power down mode), 20mA(max, +5.0V), 400mA (max, +3.3V)
196-211	16	Vendor SN	xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx	ASCⅡ.
212-219	8	Vendor date code	xx xx xx xx xx xx 20 20	Year (2 bytes), Month (2 bytes), Day (2 bytes)
220	1	Diagnostic type	08	No BER Support, Average Power
221	1	Enhanced option	60	Optional Soft Tx_Disable and P_Down
222	1	Aux Monitoring	67	+5.0V and +3.3V Supply Voltage
223	1	CC EXT	xx	Check sum of bytes 192 - 222
224-255	32	Vendor specific		Reserved By Vendor

Recommended Host Board Power Supply Circuit

Figure 2 shows the recommended host board power supply circuit.

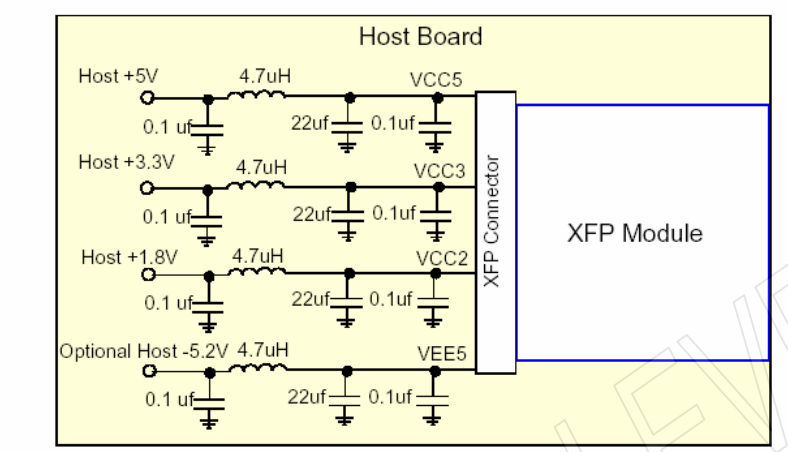


Figure 2, Recommended Host Board Power Supply Circuit

Recommended Interface Circuit

Figure 3 shows the recommended interface circuit.

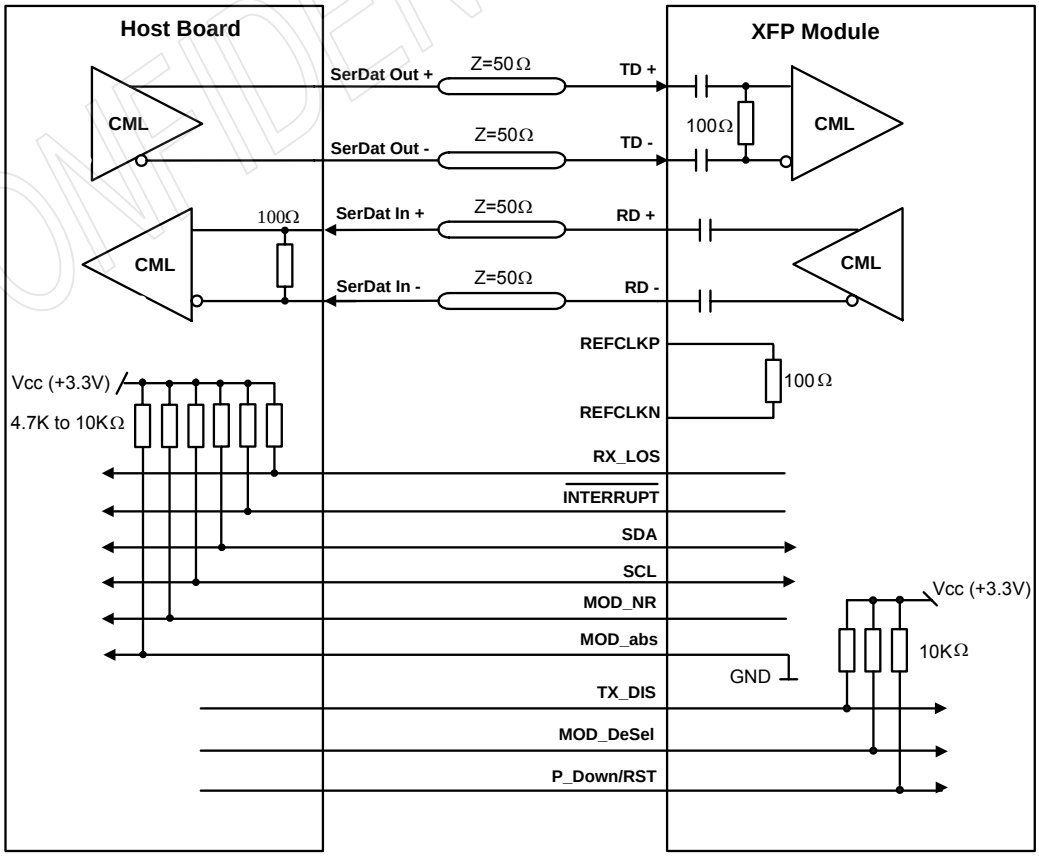


Figure 3, Recommended Interface Circuit

Pin Definitions

Figure 4 below shows the pin numbering of XFP electrical interface. The pin functions are described in Table 5 with some accompanying notes.

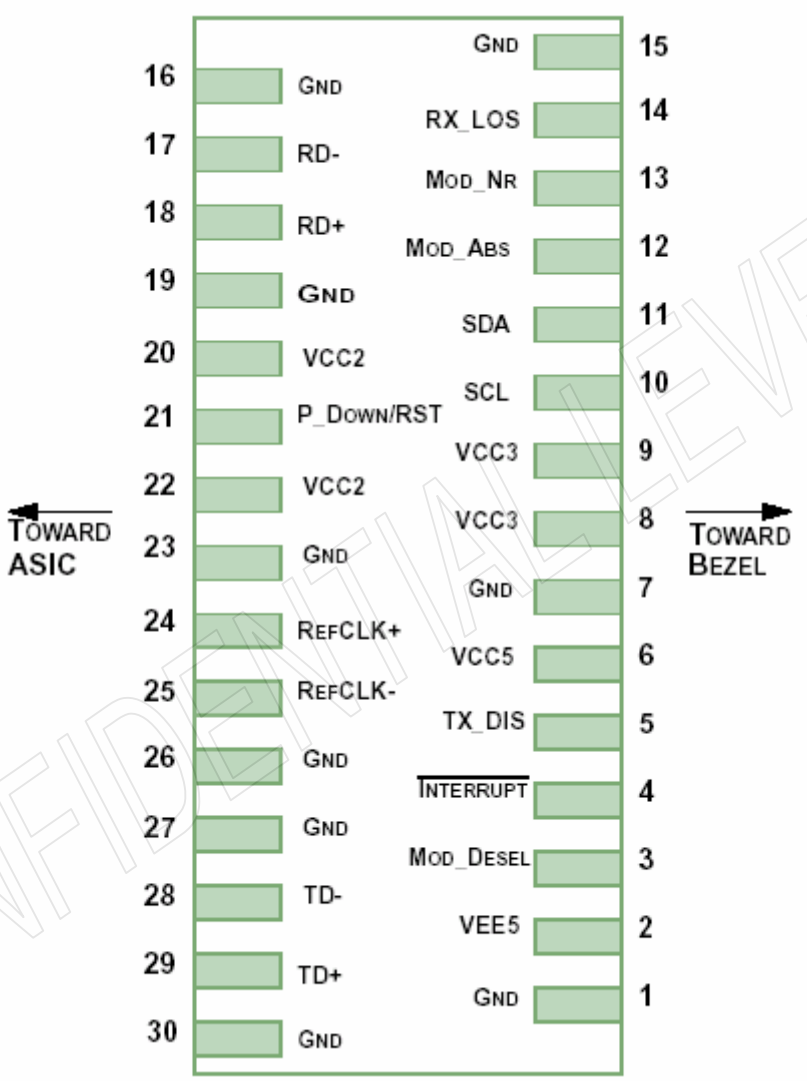


Figure 4, Pin View

Table 8 – Pin Function Definitions

Pin	Logic	Symbol	Name/Description	Note
1		GND	Module Ground	1
2		V_{EE5}	Optional -5.2V Power Supply (Not implemented)	
3	LVTTL-I	Mod_Desel	Module De-select; When held low allows the module to respond to 2-wire serial interface	
4	LVTTL-O	$\overline{\text{Interrupt}}$	$\overline{\text{Interrupt}}$; Indicates presence of an important condition which can be read over the 2-wire serial interface	2
5	LVTTL-I	TX_DIS	Transmitter Disable; Turns off transmitter laser output	
6		V_{CC5}	+5V Power Supply	

7		GND	Module Ground	1
8		V_{CC3}	+3.3V Power Supply	
9		V_{CC3}	+3.3V Power Supply	
10	LVTTL-I/O	SCL	2-Wire Serial Interface Clock	2
11	LVTTL-I/O	SDA	2-Wire Serial Interface Data Line	2
12	LVTTL-O	Mod_Abs	Indicates Module is not present. Grounded in the Module	2
13	LVTTL-O	Mod_NR	Module Not Ready; Indicating Module Operational Fault	2
14	LVTTL-O	RX_LOS	Receiver Loss Of Signal Indicator	2
15		GND	Module Ground	1
16		GND	Module Ground	1
17	CML-O	RD-	Receiver Inverted Data Output	
18	CML-O	RD+	Receiver Non-Inverted Data Output	
19		GND	Module Ground	1
20		V_{CC2}	+1.8V Power Supply (Not implemented).	3
21	LVTTL-I	P_Down/RST	Power down; When high, requires the module to limit power consumption to 1.5W or below. 2-Wire serial interface must be functional in the low power mode.	
			Reset; The falling edge initiates a complete reset of the module including the2-wire serial interface, equivalent to a power cycle.	
22		V_{CC2}	+1.8V Power Supply (Not implemented)	3
23		GND	Module Ground	1
24	PECL-I	RefCLK+	Not used, internally terminated to 50ohm (100ohm diff).	4
25	PECL-I	RefCLK-	Not used, internally terminated to 50ohm (100ohm diff).	4
26		GND	Module Ground	1
27		GND	Module Ground	1
28	CML-I	TD-	Transmitter Inverted Data Input	
29	CML-I	TD+	Transmitter Non-Inverted Data Input	
30		GND	Module Ground	1

1. Module ground pins GND are isolated from the module case and chassis ground within the module.
2. Shall be pulled up with 4.7K-10Kohms to a voltage between 3.15V and 3.45V on the host board.
3. The pins are open within module.
4. Reference Clock is not required.

Mechanical Design Diagram

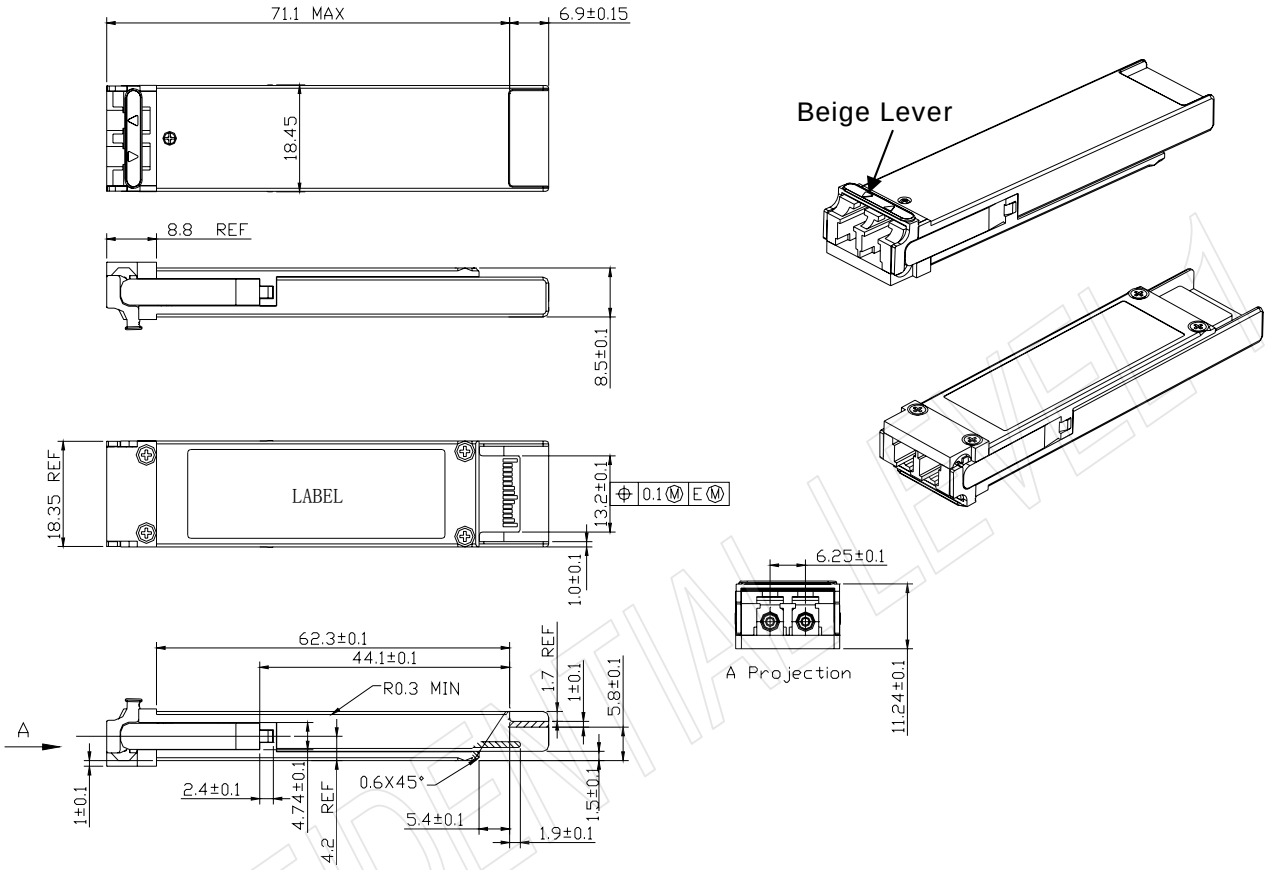
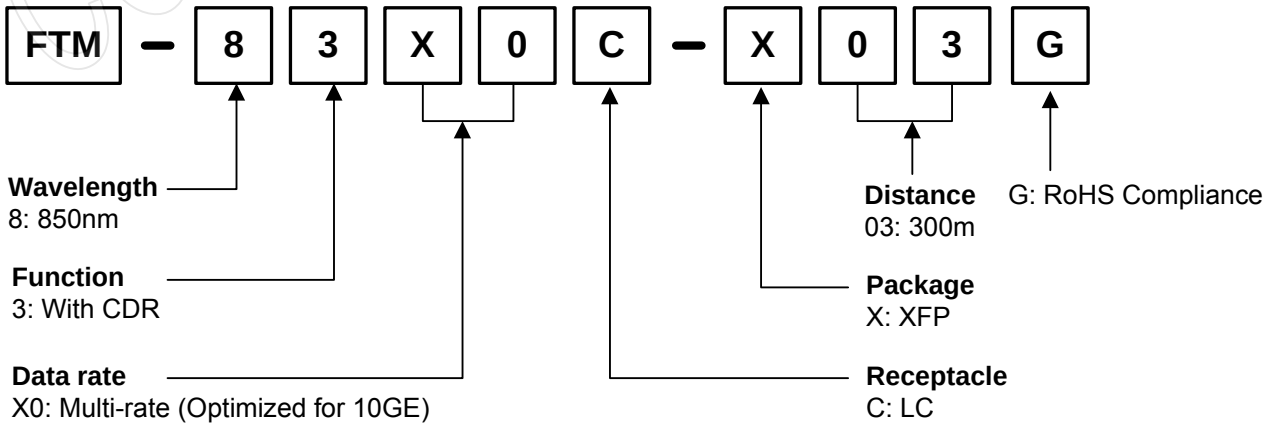


Figure 5, Mechanical Design Diagram of XFP

Ordering information



Part No.	Product Description
FTM-83X0C-X03G	850nm VCSEL, multi-rate for 10GE, 300m, XFP, RoHS compliance

Related Documents

- *INF-8077i (10 Gigabit Small Form Factor Pluggable Module), Revision 4.0*

Obtaining Document

You can visit our website:
http://www.fiberxon.com

Or contact with Fiberxon, Inc. America Sales Office listed at the end of documentation to get the latest documents.

Revision History

Revision	Initiate	Review	Approve	Subject	Release Date
Rev. 1a	Andy.Xiao	Tonny Yin	Alain.Shang	Initial datasheet	Mar. 28, 2006
Rev. 1b	Andy.Xiao	Tonny Yin	Alain.Shang	1. Update the LOS Assert / De-assert spec 2. Remove the minimum transmission, and add a note.	Nov.27, 2006

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